MCU Based Dual Port USB Type-C EPR PD Controller

1 General Description

The RT7889D/RT7889DB is a highly integrated dual port USB type-C EPR PD controller featuring a 3:1 SBU MUX, MCU, VCONN load switches, and dual-port PD control circuitry. The IC incorporates an ARM Cortex – M0 MCU controller, which handles various functions of protocol communication, smart control of external DC-DC power, firmware-based protections, and customized functions. The RT7889D/RT7889DB provides robust protections for VCONN and SBU1/2. The IC is available in a compact WQFN 7x7 package.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Ordering Information

RT7889D/DB □-□□

Packing
A: Standard

Customized Firmware Code AABBX(1)
AA: Firmware Application Code
BB: Hardware Model Code
X: Firmware Version Code

Package Type(2)
N: WQFN-68L 7x7 (W-Type)

Dead Battery Rd Type
RT7889DB: With Dead Battery Rd
RT7889D: Without Dead Battery Rd

Note 1.

- Marked with (1) indicates that if the firmware code is empty, this field will be removed.
- Marked with (2) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

3 Applications

- Docking Stations
- Monitors
- Notebook Computers

4 Features

- **Integrated USB Type-C Power Delivery (PD) Controller**
  - **Support 28V Extended Power Range (EPR) for Both Sink and Source Devices**
  - **Compliant with USB PD 3.2 Specification**
  - **Fast Role Swap**
  - **2 Slave I^2C Interfaces (I^2C1, I^2C2)**
  - **2 Master/Slave I^2C Interfaces (I^2C3, I^2C4)**
- **Featured Function**
  - **RT7889D: Without Dead Battery Rd**
  - **RT7889DB: With Dead Battery Rd**
- **CC1/2 and SBU1/2 Withstand Voltage to 28V**
- **Integrated VCONN Switch for CC1/2, Supply Power up to 1.5W**
- **Port Protection for VCONN and SBU1/2**
  - **Support VCONN RVP, OCP, OVP, and OTP Detection**
  - **Support SBU1/2 OVP Detection**
- **256kB Flash Memory with Dual-Bank Operation**
- **3:1 SBU MUX with Level Shift for Alternate Mode and Debug Mode Operation**
- **Support USB Full-Speed Device**
- **Support SHA-256 and ECDSA**
- **Support Firmware Update via USB PD (CC1/2), DP/DM, and I^2C Interface**
- **36 Configurable GPIOs**
- **Programmable PWM LED Controller**

5 Marking Information

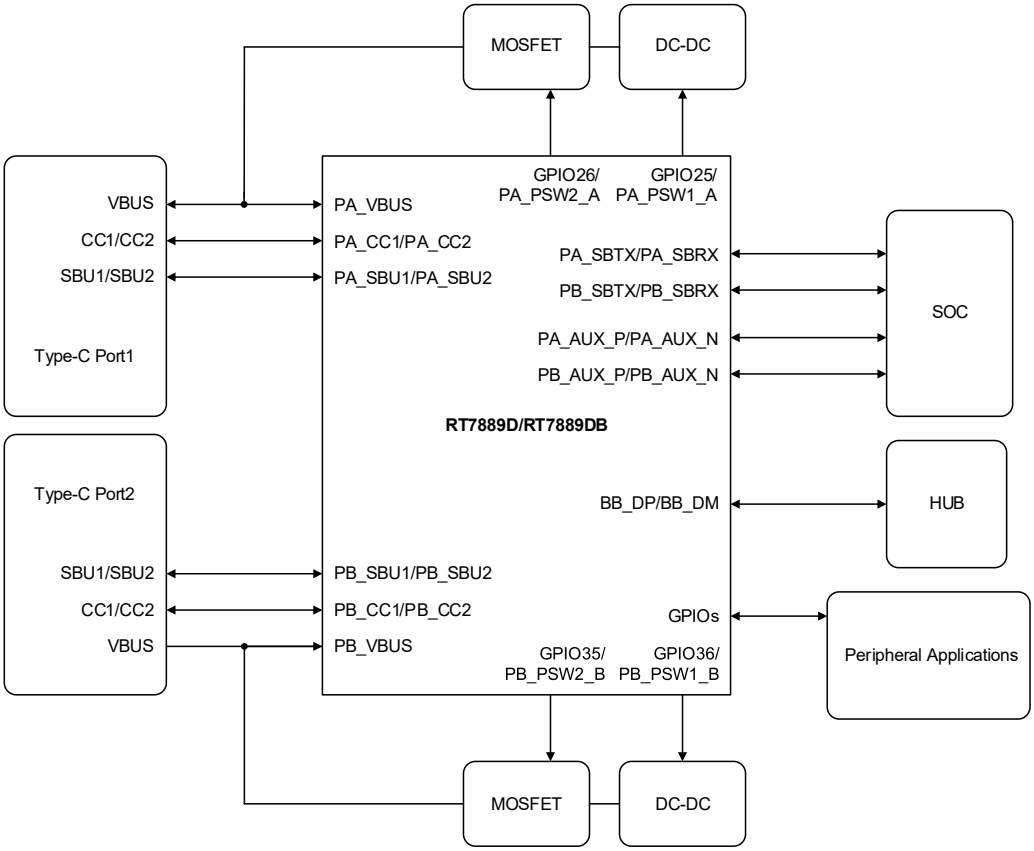
RT7889DN-A

RT7889DN: Product Code
YMDAN: Date Code

RT7889DBN-A

RT7889DBN: Product Code
YMDAN: Date Code

6 Simplified Application Circuit



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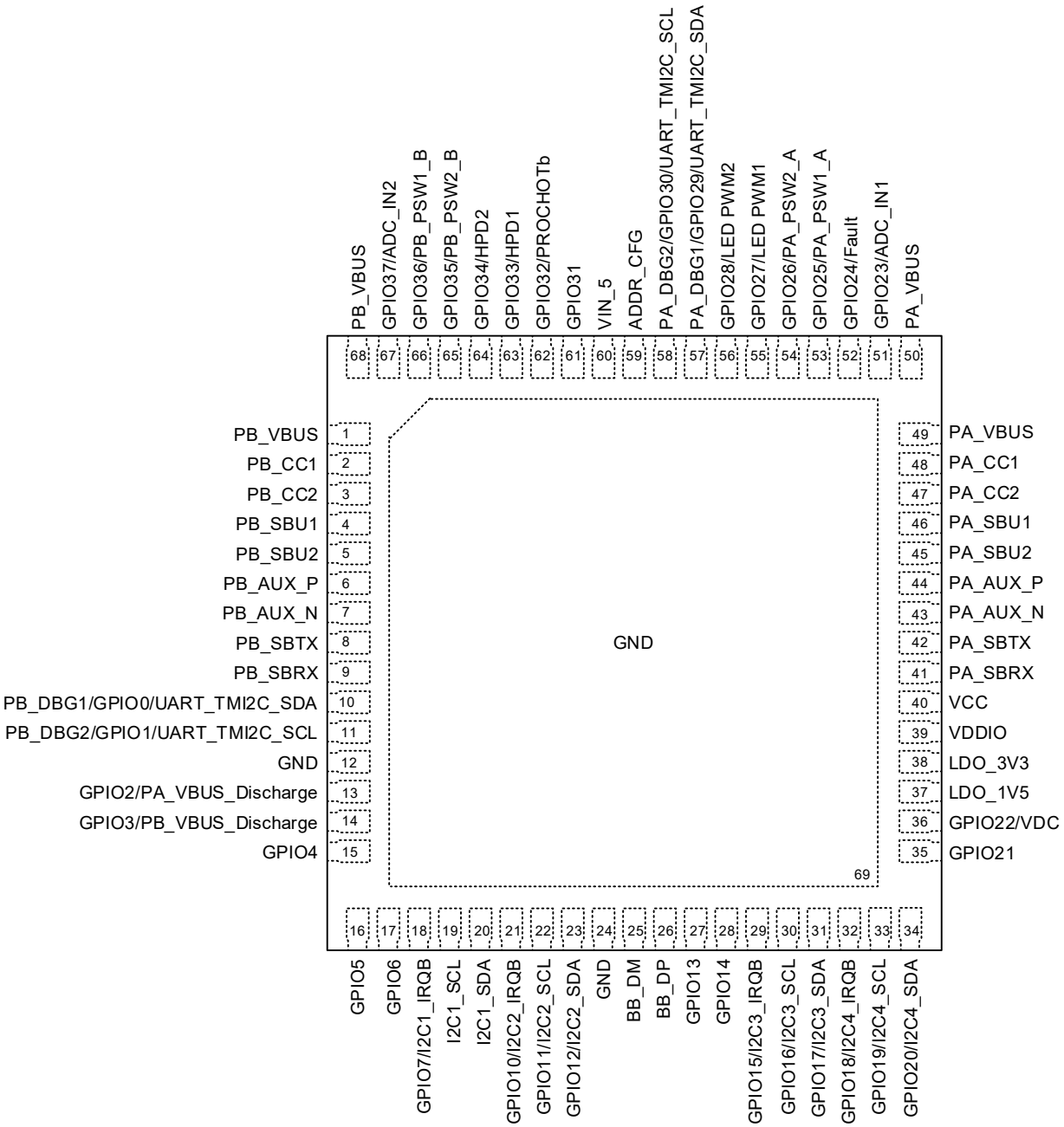
7 Pin Configuration

(TOP VIEW)



WQFN-68L 7x7

8 Functional Pin Description

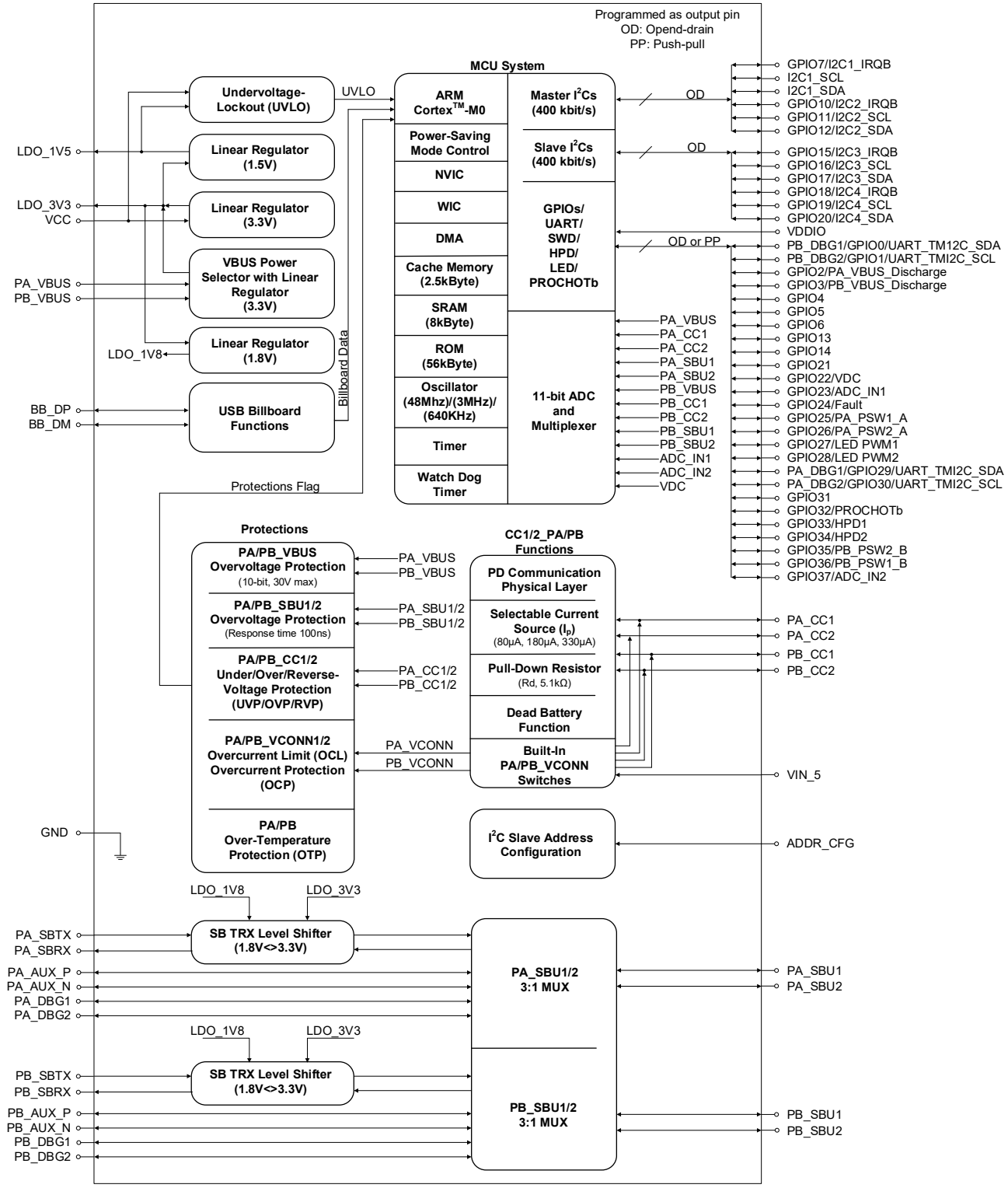
Pin No.	Pin Name	Application	Pin Function
1, 68	PB_VBUS	PD	One of power input for the RT7889D/RT7889DB. Connect this pin to port-B Type-C connector VBUS terminal.
2	PB_CC1	PD	Type-C connector configuration channel 1. Connect this pin to port-B Type-C connector CC1 terminal.
3	PB_CC2	PD	Type-C connector configuration channel 2. Connect this pin to port-B Type-C connector CC2 terminal.
4	PB_SBU1	SBU	SBU1 signal for SBU mux. Connect this pin to port-B Type-C connector SBU1 terminal.
5	PB_SBU2	SBU	SBU2 signal for SBU mux. Connect this pin to port-B Type-C connector SBU2 terminal.
6	PB_AUX_P	SBU	Port-B AUX_P signal from SBU mux.
7	PB_AUX_N	SBU	Port-B AUX_N signal from SBU mux.
8	PB_SBTX	SBU	Port-B SBTX signal from SBU mux. Connect this pin to SBTX of AP.
9	PB_SBRX	SBU	Port-B SBRX signal from SBU mux. Connect this pin to SBRX of AP.
10	PB_DBG1/GPIO0/ UART_TMI2C_SDA	SBU	General-purpose input/output. Port-B SBU mux output connected to PB_SBU1 during debug mode.
11	PB_DBG2/GPIO1/ UART_TMI2C_SCL	SBU	General-purpose input/output. Port-B SBU mux output connected to PB_SBU2 during debug mode.
12, 24, 69 (Exposed Pad)	GND	Power	Analog ground. The exposed pad must be connected to GND and be well soldered to a large copper PCB for maximum power dissipation.
13	GPIO2/PA_VBUS_ Discharge	GPIO	Push-pull general-purpose input/output. External VBUS discharge for port-A.
14	GPIO3/PB_VBUS_ Discharge	GPIO	Push-pull general-purpose input/output. External VBUS discharge for port-B.
15	GPIO4	GPIO	Push-pull general-purpose input/output.
16	GPIO5	GPIO	Push-pull general-purpose input/output.
17	GPIO6	GPIO	Push-pull general-purpose input/output.
18	GPIO7/I2C1_IRQB	I^2C	Open-drain general-purpose input/output. IRQB signal of slave I^2C1 interface.
19	I2C1_SCL	I^2C	SCL signal of slave I^2C1 interface. If unused, connect to 1.8V or 3.3V with 1kΩ resister. Support FW update.
20	I2C1_SDA	I^2C	SDA signal of slave I^2C1 interface. If unused, connect to 1.8V or 3.3V with 1kΩ resister. Support FW update.
21	GPIO10/I2C2_IRQB	I^2C	Open-drain general-purpose input/output. IRQB signal of slave I^2C2 interface.
22	GPIO11/I2C2_SCL	I^2C	Open-drain general-purpose input/output. SCL signal of slave I^2C2 interface.

Pin No.	Pin Name	Application	Pin Function
23	GPIO12/I2C2_SDA	I^2C	Open-drain general-purpose input/output. SDA signal of slave I^2C2 interface.
25	BB_DM	USB	USB 2.0 full speed PHY DM.
26	BB_DP	USB	USB 2.0 full speed PHY DP.
27	GPIO13	GPIO	Push-pull general-purpose input/output.
28	GPIO14	GPIO	Push-pull general-purpose input/output.
29	GPIO15/I2C3_IRQB	I^2C	Open-drain general-purpose input/output. IRQB signal of master/slave I^2C3 interface.
30	GPIO16/I2C3_SCL	I^2C	Open-drain general-purpose input/output. SCL signal of master/slave I^2C3 interface.
31	GPIO17/I2C3_SDA	I^2C	Open-drain general-purpose input/output. SDA signal of master/slave I^2C3 interface.
32	GPIO18/I2C4_IRQB	I^2C	Open-drain general-purpose input/output. IRQB signal of master/slave I^2C4 interface.
33	GPIO19/I2C4_SCL	I^2C	Open-drain general-purpose input/output. SCL signal of master/slave I^2C4 interface.
34	GPIO20/I2C4_SDA	I^2C	Open-drain general-purpose input/output. SDA signal of master/slave I^2C4 interface.
35	GPIO21	GPIO	Push-pull general-purpose input/output.
36	GPIO22/VDC	GPIO	Push-pull general-purpose input/output. DC power input detection pin.
37	LDO_1V5	Power	1.5V LDO output. Connect 1μF capacitor at LDO_1V5.
38	LDO_3V3	Power	3.3V LDO output. Connect 10μF capacitor at LDO_3V3. The 10μF bypass capacitor must be placed close to the IC pins in the PCB layout.
39	VDDIO	Power	Power input for GPIO. Connect 1μF capacitor at VDDIO.
40	VCC	Power	Power input for chip. Place a 1Ω series resistor and a 4.7μF bypass capacitor at the VCC pin. VCC must be supplied with 5V.
41	PA_SBRX	SBU	Port-A SBRX signal from SBU mux. Connect this pin to SBRX of AP.
42	PA_SBTX	SBU	Port-A SBTX signal from SBU mux. Connect this pin to SBTX of AP.
43	PA_AUX_N	SBU	Port-A AUX_N output signal from SBU mux.
44	PA_AUX_P	SBU	Port-A AUX_P output signal from SBU mux.
45	PA_SBU2	SBU	SBU2 signal for SBU mux. Connect this pin to port-A Type-C connector SBU2 terminal.
46	PA_SBU1	SBU	SBU1 signal for SBU mux. Connect this pin to port-A Type-C connector SBU1 terminal.
47	PA_CC2	PD	Type-C connector configuration channel 2. Connect this pin to port-A Type-C connector CC2 terminal.
48	PA_CC1	PD	Type-C connector configuration channel 1. Connect this pin to port-A Type-C connector CC1 terminal.
49, 50	PA_VBUS	PD	One of power input for the RT7889D/RT7889DB. Connect this pin to port-A Type-C connector VBUS terminal.

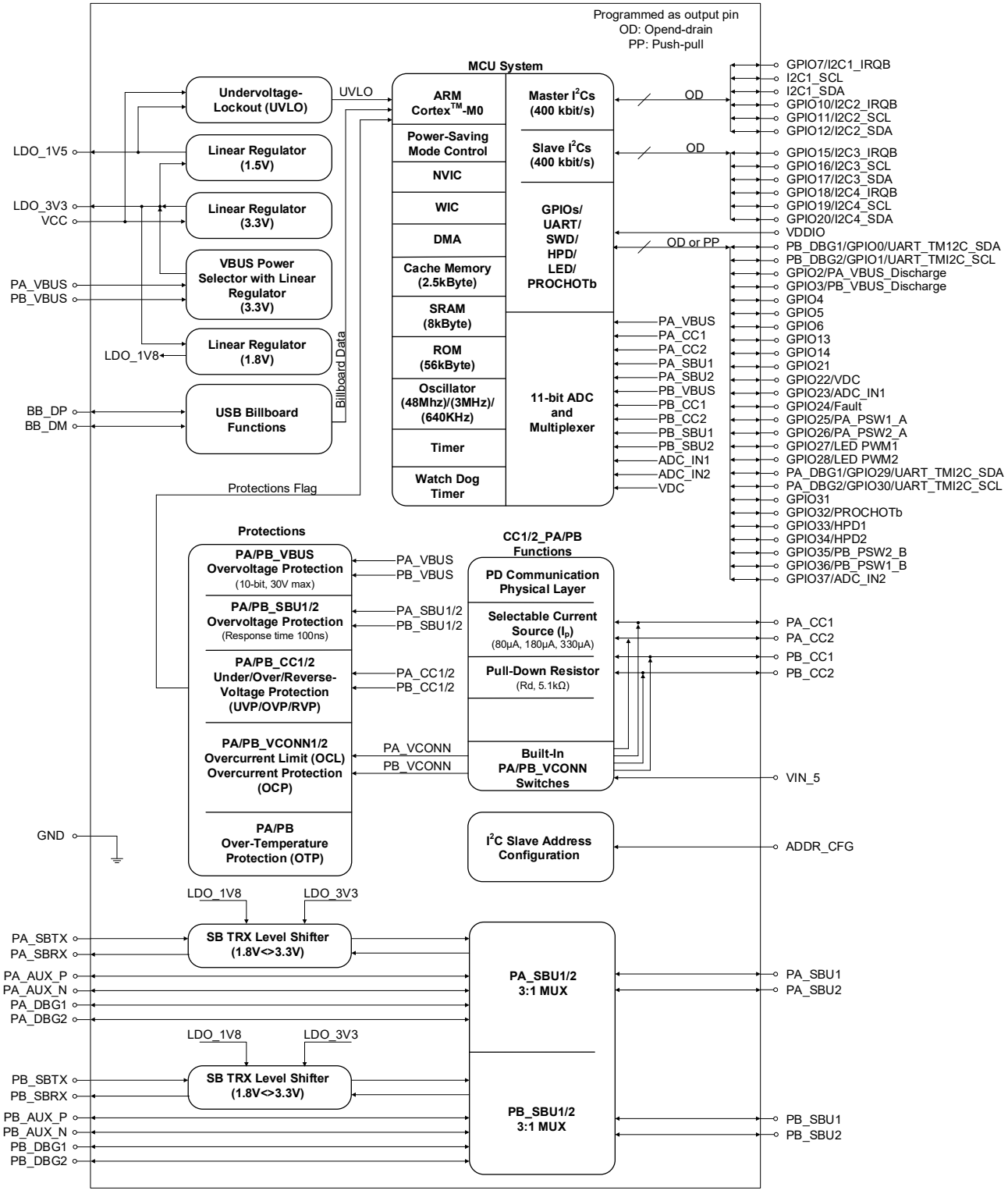
Pin No.	Pin Name	Application	Pin Function
51	GPIO23/ADC_IN1	GPIO	Open-drain general-purpose input/output. ADC measurement pin (up to 6V.)
52	GPIO24/Fault	I^2C	Open-drain general-purpose input/output. Input for interrupt signal.
53	GPIO25/PA_PSW1_A	PD	Push-pull general-purpose input/output. External DC-DC enable control for port A.
54	GPIO26/PA_PSW2_A	PD	Push-pull general-purpose input/output. External DC-DC enable control for port A.
55	GPIO27/LED PWM1	GPIO	Push-pull general-purpose input/output. Programmable PWM LED controller.
56	GPIO28/LED PWM2	GPIO	Push-pull general-purpose input/output. Programmable PWM LED controller.
57	PA_DBG1/GPIO29/ UART_TMI2C_SDA	SBU	General-purpose input/output. Port-A SBU mux output connected to PA_SBU1 during debug mode.
58	PA_DBG2/GPIO30/ UART_TMI2C_SCL	SBU	General-purpose input/output. Port-A SBU mux output connected to PA_SBU2 during debug mode.
59	ADDR_CFG	GPIO	Slave address configure.
60	VIN_5	Power	Power input for VCONN. Connect 10μF capacitor at VIN_5.
61	GPIO31	GPIO	Push-pull general-purpose input/output.
62	GPIO32/PROCHOTb	GPIO	Push-pull general-purpose input/output. Control mux power.
63	GPIO33/HPD1	GPIO	Open-drain general-purpose input/output. HPD for port A.
64	GPIO34/HPD2	GPIO	Open-drain general-purpose input/output. HPD for port B.
65	GPIO35/PB_PSW2_B	PD	Push-pull general-purpose input/output. External DC-DC enable control for port B.
66	GPIO36/PB_PSW1_B	PD	Push-pull general-purpose input/output. External DC-DC enable control for port B.
67	GPIO37/ADC_IN2	GPIO	Open-drain general-purpose input/output. ADC measurement pin (up to 6V.)

9 Functional Block Diagram

9.1 RT7889DB (With Dead Battery Rd)



9.2 RT7889D (Without Dead Battery Rd)



10 Absolute Maximum Ratings

(Note 2)

- VCC to GND ---------- –0.3V to 6V
- LDO_3V3 to GND ---------- –0.3V to 3.6V
- LDO_1V5 to GND ---------- –0.3V to 1.65V
- VDDIO to GND ---------- –0.3V to 6V
- PA_VBUS, PB_VBUS to GND ---------- –0.3V to 36V
- PA_CC1, PA_CC2, PB_CC1, PB_CC2 to GND ---------- –0.3V to 36V
- PA_SBU1, PA_SBU2, PB_SBU1, PB_SBU2 to GND ---------- –0.3V to 36V
- BB_DP, BB_DM to GND ---------- –0.3V to LDO_3V3 + 0.5V
- VIN_5 to GND ---------- –0.3V to 6V
- PA_AUX_P, PA_AUX_N, PB_AUX_P, PB_AUX_N to GND ---------- –0.3V to 6V
- PA_SBTX, PA_SBRX, PB_SBTX, PB_SBRX to GND ---------- –0.3V to LDO_3V3 + 0.5V
- PA_DBG1/GPIO29/ UART_TMI2C_SDA, PA_DBG2/GPIO30/UART_TMI2C_SCL, PB_DBG1/GPIO0/UART_TMI2C_SDA, PB_DBG2/GPIO1/ UART_TMI2C_SCL to GND ---------- –0.3V to 6V
- Others ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-68L 7x7 ---------- 3.92W
- Package Thermal Resistance (Note 3)
- WQFN-68L 7x7, θ_{JA} ---------- 25.52°C/W
  WQFN-68L 7x7, θ_{JC} ---------- 0.69°C/W
- Lead Temperature ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- VBUS Power Supply, V_{BUS} ---------- 4V to 30V
- System Power Supply, V_{CC} ---------- 3.3V to 5.5V
- IO Power Supply, V_{DDIO} ---------- 1.8V to 5.5V
- VCONN Power Supply, V_{IN_5} ---------- 4V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Consumption						
VCC Power-On, Shutdown Current	I_{VCC_SHDN}	VCC = 3.3V, PA_VBUS = 0V/PB_VBUS = 0V, measure the input current of VCC	43	61	79	μA
VCC Power-On, Two Port in Low Power Mode	$I_{VCC\_2P\_UATTACH\_DRP\_Toggle\_RP\_LP}$	VCC = 3.3V, PA_VBUS = 0V/PB_VBUS = 0V, measure the input current of VCC	55	79	103	μA
VCC Power-On, Two Port are Sink in Idle Mode	$I_{VCC\_2P\_ATTACH\_IDE}$	VCC = 3.3V, PA_VBUS = 0V/PB_VBUS = 0V, measure the input current of VCC	116	166	216	μA
VCC Power-On, Two Port are Sink in Idle Mode. VCONN Output Voltage and All Vconn Function Enabled	$I_{VCC\_2P\_ATTACH\_VCONN\_ON\_IDE}$	VCC = 3.3V, PA_VBUS = 0V/PB_VBUS = 0V, measure the input current of VCC	177	253	329	μA
VCC Power-On, Two Port are Sink in Normal Mode	$I_{VCC\_2P\_ATTACH\_NOR}$	VCC = 3.3V, PA_VBUS = 0V/PB_VBUS = 0V, measure the input current of VCC	1453	2075	2698	μA
VCC Power-On, Two Port are Sink in Normal Mode. Billboard Enabled	$I_{VCC\_2P\_ATTACH\_BILLBOARD\_ON\_NOR}$	VCC = 3.3V, PA_VBUS = 0V/PB_VBUS = 0V, measure the input current of VCC	2068	2954	3840	μA
VCC Power-On, Two Port are Sink in Normal Mode. VCONN Output Voltage and All Vconn Function Enabled	$I_{VCC\_2P\_ATTACH\_VCONN\_ON\_NOR}$	VCC = 3.3V, PA_VBUS = 0V/PB_VBUS = 0V, measure the input current of VCC	1531	2187	2843	μA
VCC Power-On, Two Port are Sink in Normal Mode. VCONN Output Voltage and All Vconn Function Enabled. CC Enable TX for Communication	$I_{VCC\_2P\_ATTACH\_VCONN\&TX\_ON\_NOR}$	VCC = 3.3V, PA_VBUS = 0V/PB_VBUS = 0V, measure the input current of VCC	4693	6704	8715	μA
VBUS Power Selector						
Px_VBUS Power-Good High Voltage Threshold	$V_{VBUS\_PG\_Px}$		3.4	3.55	3.7	V
Px_VBUS Power-Good High Voltage Hysteresis	$V_{VBUS\_PG\_Px\_HYS}$		0.1	0.2	0.3	V
VCC Power-Good High Voltage Threshold	V_{VCC_PG}		3	3.1	3.2	V
VCC Power-Good High Voltage Hysteresis	$V_{VCC\_PG\_HYS}$		0.28	0.33	0.38	V
VBUS LDO Output Voltage	$V_{VBUS\_LDO\_OUT}$	VBUS = 4.6V, Ilead = 30mA	3.06	3.4	3.74	V
VBUS LDO Output Current Limit	$I_{VBUS\_LDO\_LIM}$		40	--	65	mA
VCC LDO Output Voltage	$V_{VCC\_LDO\_OUT}$		2.97	3.3	3.63	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LDO1V5 Output Voltage	$V_{1V5\_LDO\_OUT}$		1.5	1.575	1.65	V
Type-C Port Control and CC Detection						
DFP 80μA CC Current	$I_{Rp80\mu\_NOR}$	VCC = 3.3 to 5.5V	64	80	96	μA
DFP 180μA CC Current	$I_{Rp180\mu\_NOR}$	VCC = 3.3 to 5.5V	166	180	194	μA
DFP 330μA CC Current	$I_{Rp330\mu\_NOR}$	VCC = 3.3 to 5.5V	304	330	356	μA
UFP Ra	R_a	VCC = 3.3 to 5.5V	0.8	1	1.2	kΩ
UFP Rd	R_d	VCC = 3.3 to 5.5V	4.59	5.1	5.61	kΩ
UFP Pull-Down Voltage in Dead Battery under DFP 80μA	$V_{80\mu A\_DB}$	VCC = 0V, apply a current source of 80μA (RT7889DB)	0.25	--	1.5	V
UFP Pull-Down Voltage in Dead Battery under DFP 180μA	$V_{180\mu A\_DB}$	VCC = 0V, apply a current source of 180μA (RT7889DB)	0.45	--	1.5	V
UFP Pull-Down Voltage in Dead Battery under DFP 330μA	$V_{330\mu A\_DB}$	VCC = 0V, apply a current source of 330μA (RT7889DB)	0.85	--	2.45	V
CC Fast Role Swap Tx	$R_{FRSSwapTx}$		0	--	5	Ω
PD CC TRX Communication						
Bit Rate	$f_{BitRate\_PD}$	VCC = 3.3 to 5.5V	270	300	330	Kbps
Maximum Difference between the Bit-Rate during the Part of the Packet following the Preamble and the Reference Bit-Rate	$p_{BitRate}$	VCC = 3.3 to 5.5V	--	--	0.25	%
Fall Time	t_{Fall}	VCC = 3.3 to 5.5V	300	--	--	ns
Rise Time	t_{Rise}	VCC = 3.3 to 5.5V	300	--	--	ns
Voltage Swing	V_{Swing}	VCC = 3.3 to 5.5V	1.05	1.125	1.2	V
Transmitter Output Impedance	Z_{Driver}	VCC = 3.3 to 5.5V	33	50	75	Ω
Receiver Input Impedance	Z_{BmcRx}	VCC = 3.3 to 5.5V	1	--	--	MΩ
VCONN Switch						
VCONN OVP	V_{VCONN_OVP}		5.6	5.75	5.9	V
Hysteresis on VCONN OVP	$V_{VCONN\_OVP\_HYS}$		50	75	100	mV
OVP Response Time on the CC Pins. Time from OVP Asserted until OVP FETs Turn Off	$t_{VCONN\_OVP\_Response}$		--	100	--	ns
VCONN Present	$V_{VCONN\_Present}$	VCC = 3.3 to 5.5V	2.28	2.4	2.52	V
VCONN Invalid	$V_{VCONN\_Invalid}$	VCC = 3.3 to 5.5V	2.565	2.7	2.835	V
VCONN Safe0V	V_{VCONN_Safe0v}	VCC = 3.3 to 5.5V	--	0.4	0.8	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Hysteresis of VCONN Present	$V_{VCONN\_Present\_HYS}$	VCC = 3.3 to 5.5V	50	100	150	mV
Hysteresis of VCONN Invalid	$V_{VCONN\_Invalid\_HYS}$	VCC = 3.3 to 5.5V	50	100	150	mV
Hysteresis of VCONN Safe0v	$V_{VCONN\_Safe0v\_HYS}$	VCC = 3.3 to 5.5V	50	100	150	mV
VCONN RVP	V_{VCONN_RVP}		0.115	0.3	0.5	V
Release of VCONN RVP	$V_{VCONN\_RVP\_HYS}$		0	50	115	mV
RVP response time on the CC Pins. Time from OVP Asserted until OVP FETs Turn Off	$t_{VCONN\_RVP\_Response}$		--	300	--	ns
VCONN OCP Range (Shutdown)	$I_{VCONN\_OCP\_1}$		180	200	220	mA
VCONN OCP Range (Shutdown)	$I_{VCONN\_OCP\_2}$		270	300	330	mA
VCONN OCP Range (Shutdown)	$I_{VCONN\_OCP\_3}$		360	400	440	mA
VCONN OCP Range (Shutdown)	$I_{VCONN\_OCP\_4}$		450	500	550	mA
VCONN OCP Range (Shutdown)	$I_{VCONN\_OCP\_5}$		540	600	660	mA
VCONN OCP Range (Shutdown)	$I_{VCONN\_OCP\_6}$		630	700	770	mA
VCONN OCL Range (Limit)	$I_{VCONN\_OCL\_1}$		140	200	260	mA
VCONN OCL Range (Limit)	$I_{VCONN\_OCL\_2}$		240	300	360	mA
VCONN OCL Range (Limit)	$I_{VCONN\_OCL\_3}$		320	400	480	mA
VCONN OCL Range (Limit)	$I_{VCONN\_OCL\_4}$		400	500	600	mA
VCONN OCL Range (Limit)	$I_{VCONN\_OCL\_5}$		480	600	720	mA
VCONN OCL Range (Limit)	$I_{VCONN\_OCL\_6}$		560	700	840	mA
Ron for VCONN Switch	R_{ON_VCONN}	VIN_5 = 5V, VCC = 3.3 to 5.5V PA_CC1/PA_CC2/PB_CC1/PB_CC2 sink a 600mA loading	--	1	1.3	Ω
Power−Off Leakage Current of VCONN	$I_{OFF\_VCONN\_5.5V}$	VIN_5 = 5.5V, VCC = 3.3V	−1	--	1	μA
Off Leakage Current of VCONN	$I_{OZ\_VCONN\_5.5V}$	VIN_5 = 5.5V, VCC = 0V	−1	--	1	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBUS Detection						
VREF_VBUS_FRS	$V_{VBUS\_FRS\_0}$		4.512	4.8	5.088	V
	$V_{VBUS\_FRS\_1}$		4.5872	4.88	5.1728	V
	$V_{VBUS\_FRS\_2}$		4.7376	5.04	5.3424	V
	$V_{VBUS\_FRS\_3}$		4.8128	5.12	5.4272	V
	$V_{VBUS\_FRS\_4}$		4.888	5.2	5.512	V
	$V_{VBUS\_FRS\_5}$		4.9632	5.28	5.5968	V
	$V_{VBUS\_FRS\_6}$		5.1136	5.44	5.7664	V
	$V_{VBUS\_FRS\_7}$		5.1888	5.52	5.8512	V
VREF_VBUS_FRS HYS	$V_{VBUS\_FRS\_HYS}$		0.3	0.43	0.56	V
VBUS Force Discharge	R_{VBUS_FDIS}		0.28	0.4	0.52	kΩ
VBUS Bleed Discharge	R_{VBUS_BDIS}		2.8	4	5.2	kΩ
SBU OVP Switch Mux						
On Leakage Current of SBU Switch	$I_{ON\_SBU\_CON\_AUX\_3.6V}$	VCC = 3.3 to 5.5V, SBUX = 3.6 V, AUXP/AUXN/DBG1/DBG2 is floating	–3.6	--	3.6	μA
On Leakage Current of SBU Switch	$I_{ON\_SBU\_CON\_SBTRX\_3.3V}$	VCC = 3.3 to 5.5V, SBUX = 3.3 V, SBTX/SBRX is floating and at level shifter = 3.3V setting	–3.3	--	3.3	μA
Off Leakage Current of SBU Connector Side	$I_{OZ\_SBU\_CON\_3.6V}$	VCC = 3.3 to 5.5V, SBUX = 3.6 V	–3.6	--	3.6	μA
Off Leakage Current of SBU Connector Side	$I_{OZ\_SBU\_CON\_28V}$	VCC = 3.3 to 5.5V, SBUX = 28V	--	--	150	μA
Power-Off Leakage Current SBU Connector Side	$I_{OFF\_SBU\_CON\_3.6V}$	VCC = 0V, SBUX = 3.6V	–3	--	3	μA
On Leakage Current of SBU Host Side	$I_{ON\_SBU\_HOST\_3.6V}$	VCC = 3.3 to 5.5V, SBUX = floating, AUXP/AUXN/ DBG1/DBG2 is 3.6V	–3	--	3	μA
Off Leakage of SBU Host Side	$I_{OZ\_SBU\_HOST\_3.6V}$	VCC = 3.3 to 5.5V, SBUX = floating, AUXP/AUXN/ DBG1/DBG2 is 3.6V	–3	--	3	μA
Power-Off Leakage Current of SBU Host Side	$I_{OFF\_SBU\_HOST\_3.6V}$	VCC = 0V, SBUX = floating, AUXP/AUXN/ DBG1/DBG2 is 3.6V	–1	--	1	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Off Leakage Current of SBU_CON to SBU Host Side	$I_{OFF\_SBU\_CON\_28V\ to\ SBU\_HOST}$	VCC = 3.3 to 5.5V, SBUX = 28V, AUXP/AUXN/ DBG1/DBG2 are set to 0V, measure leakage out of AUXP/AUXN/ DBG1/DBG2 pins	–1	--	1	μA
SBU Input OVP Lockout	V_{SBU_OVP}		4.25	4.5	4.75	V
SBU Input OVP Hysteresis	$V_{SBU\_OVP\_HYS}$		35	60	85	mV
SBU Pins OVP Response Time	t_{SBU_OVP}		30	60	120	ns
SBUx to AUXP/N Switch On-Resistance	$R_{ON\_SBU\_AUX}$	V_{SW} = 0V to 3.6V, I_{SW} = 10mA	--	3.5	6	Ω
SBUx to AUXP/N Switch On-Resistance Flatness	$R_{ON\_SBU\_FLAT}$		--	--	500	mΩ
SBUx to DBGx Switch On-Resistance	$R_{ON\_SBU\_DBUG}$	V_{SW} = 0V to 3.6V, I_{SW} = 10mA	--	8	16	Ω
SBU MUX Switch Turn-On Time	t_{SBU_ON}	SBUx = 2.5 V, R_L = 1kΩ	150	250	400	μs
SBU MUX Switch Turn-Off Time	t_{SBU_OFF}	SBUx = 2.5 V, R_L = 1kΩ	0	--	1	μs
AUX Channel –3dB Bandwidth	BW_{SBU}		175	--	--	MHz
Crosstalk for SBU	X_{talk_SBU}		--	–40	--	dB
Off Isolation for SBU	$OIRR_{SBU}$		--	–40	--	dB
Pull-Down Resistance of 100kΩ on AUXP	R_{AUXP_PD100k}		60	80	100	kΩ
Pull-Up Resistance of 100kΩ on AUXN	R_{AUXN_PU100k}		60	80	100	kΩ
Pull-Up Resistance of 1MΩ on AUXP	R_{AUXP_PU1M}		0.9	1.1	1.3	MΩ
Pull-Down Resistance of 1MΩ on AUXN	R_{AUXN_PD1M}		0.9	1.1	1.3	MΩ
Pull-Down Resistance of 0.47MΩ on AUXP	$R_{AUXP\_PD0.47M}$		0.25	0.47	0.75	MΩ
Pull-Down Resistance of 4.7MΩ on AUXN	$R_{AUXN\_PD4.7M}$		2.5	4.7	7.5	MΩ
SBTX Level Shifter Output High Voltage	V_{SBTX_OH}		2.4	--	3.47	V
SBTX Level Shifter Output Low Voltage	V_{SBTX_OL}		–0.05	--	0.4	V
SBTX Level Shifter Output Impedance	R_{SBTX_OUT}		25	--	90	Ω
SBTX Output Pull-Up Resistor	R_{SBTX_PU}		7	8.75	10.5	kΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SBTX Level Shifter Input High Voltage for 1.8V Mode	$V_{SBTX\_IH\_1.8V}$		1.26	--	1.98	V
SBTX Level Shifter Input Low Voltage for 1.8V Mode	$V_{SBTX\_IL\_1.8V}$		–0.3	--	0.54	V
SBTX Level Shifter Input High Voltage for 3.3V Mode	$V_{SBTX\_IH\_3.3V}$		2.31	--	3.6	V
SBTX Level Shifter Input Low Voltage for 3.3V Mode	$V_{SBTX\_IL\_3.3V}$		–0.3	--	0.99	V
SBTX Level Shifter Input High Leakage	$I_{SBTX\_LK\_INH}$	VDD3V3 = 3.3V, SBTX = 3.3V	–1	--	1	µA
SBTX Level Shifter Input Low Leakage	$I_{SBTX\_LK\_INL}$	VDD3V3 = 3.3V, SBTX = 0V	–1	--	1	µA
SBTX Input Pull-Up Resistor	R_{SBTX_PD}		7	8.75	10.5	kΩ
SBRX Level Shifter Output Impedance	R_{SBRX_OUT}		25	--	90	Ω
SBRX Level Shifter Output High Voltage for 1.8V Mode	$V_{SBRX\_OH\_1.8V}$	I_{OH} = 2mA at 1.8V VDD with output impedance of RX	1.44	--	3.6	V
SBRX Level Shifter Output Low Voltage for 1.8V Mode	$V_{SBRX\_OL\_1.8V}$	I_{OL} = 2mA at 1.8V VDD with output impedance of RX	–0.3	--	0.36	V
SBRX Level Shifter Output High Voltage for 3.3V Mode	$V_{SBRX\_OH\_3.3V}$	I_{OH} = 3mA at 3.3V VDD with output impedance of RX	2.64	--	3.6	V
SBRX Level Shifter Output Low Voltage for 3.3V Mode	$V_{SBRX\_OL\_3.3V}$	I_{OL} = 3mA at 3.3V VDD with output impedance of RX	–0.3	--	0.66	V
SBRX Level Shifter Input High Voltage	V_{SBRX_IH}		2	--	3.72	V
SBRX Level Shifter Input Low Voltage	V_{SBRX_IL}		–0.3	--	0.65	V
SBRX Level Shifter Input High Leakage	$I_{SBRX\_LK\_INH}$	VDD3V3=3.3V, SBU_CON = 3.3V	–3.3	--	3.3	µA
SBRX Level Shifter Input Low Leakage	$I_{SBRX\_LK\_INL}$	VDD3V3 = 3.3V, SBU_CON = 0V	–1	--	1	µA
SBRX Input Pull-Down Resistor	R_{SBRX_PD}		0.7	0.875	1.05	MΩ
ADC						
ADC Resolution	R_{ES_ADC}	VCC = 3.3 to 5.5V	--	11	--	bit
PA_VBUS/PB_VBUS Measurement Range	$V_{VBUS\_ADC\_RANGE}$	VCC = 3.3 to 5.5V	0	--	34	V

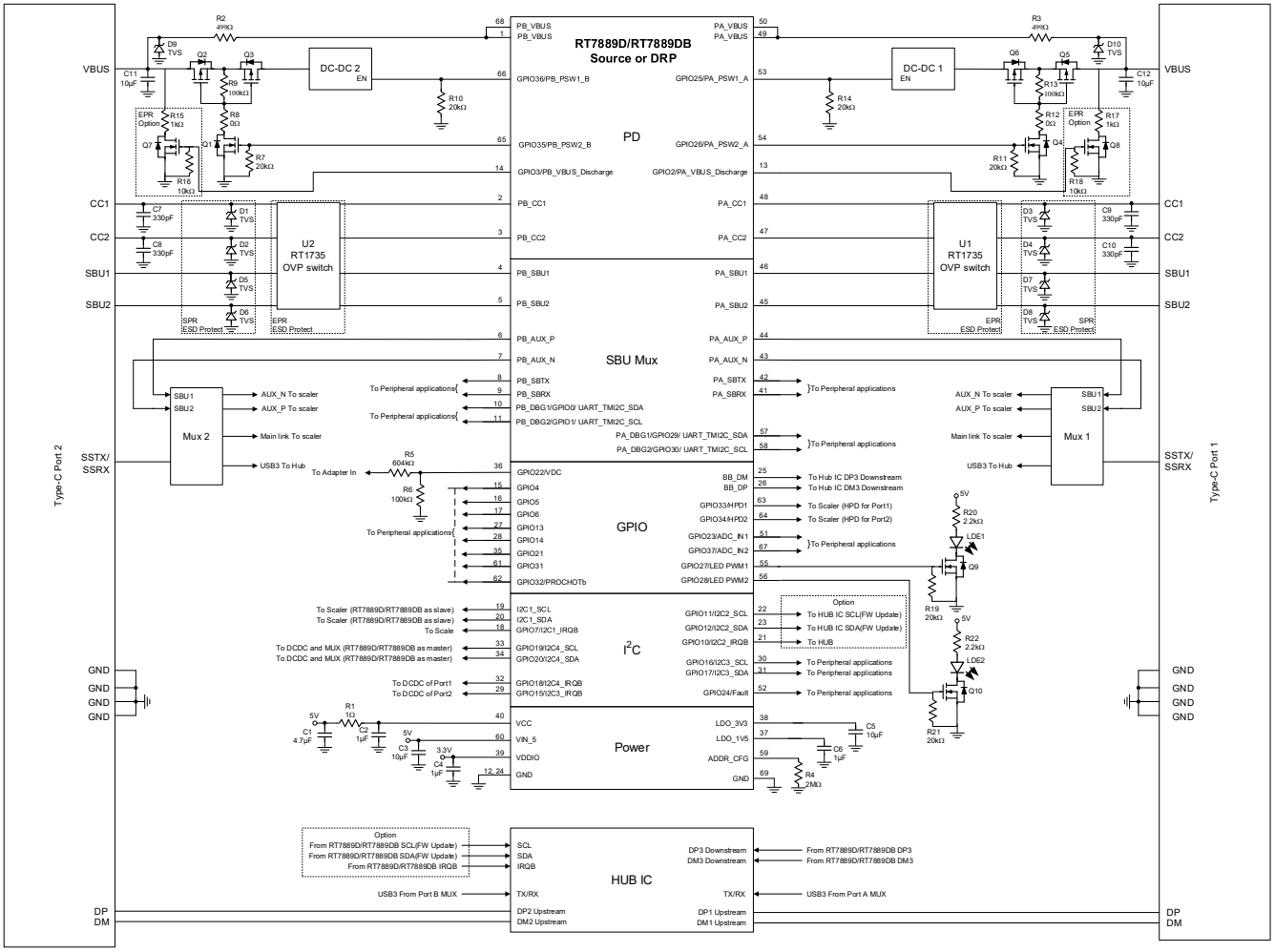
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PA_VBUS/PB_VBUS Resolution	$V_{VBUS\_ADC\_RES}$	VCC = 3.3 to 5.5V	--	17.2	--	mV
PA_VBUS/PB_VBUS Accuracy	$V_{VBUS\_ADC\_ACC}$	VCC = 3.3 to 5.5V	–175	--	175	mV
PA_CCx/PB_CCx Measurement Range	$V_{CCx\_ADC\_RANGE}$	VCC = 3.3 to 5.5V	0	--	6	V
PA_CCx/PB_CCx Resolution	$V_{CCx\_ADC\_RES}$	VCC = 3.3 to 5.5V	--	4	--	mV
PA_CCx/PB_CCx Accuracy	$V_{CCx\_ADC\_ACC}$	VCC = 3.3 to 5.5V	–40	--	40	mV
PA_SBUx/PB_SBUx Measurement Range	$V_{SBUx\_ADC\_RANGE}$	VCC = 3.3 to 5.5V	0	--	6	V
PA_SBUx/PB_SBUx Resolution	$V_{SBUx\_ADC\_RES}$	VCC = 3.3 to 5.5V	--	4	--	mV
PA_SBUx/PB_SBUx Accuracy	$V_{SBUx\_ADC\_ACC}$	VCC = 3.3 to 5.5V	–40	--	40	mV
VDC Measurement Range	$V_{SBUx\_ADC\_RANGE}$	VCC = 3.3 to 5.5V	0	--	6	V
VDC Resolution	$V_{SBUx\_ADC\_RES}$	VCC = 3.3 to 5.5V	--	4	--	mV
VDC Accuracy	$V_{SBUx\_ADC\_ACC}$	VCC = 3.3 to 5.5V	–40	--	40	mV
ADC_IN Measurement Range	$V_{ADCx\_ADC\_RANGE}$	VCC = 3.3 to 5.5V	0	--	6	V
ADC_IN Resolution	$V_{ADCx\_ADC\_RES}$	VCC = 3.3 to 5.5V	--	4	--	mV
ADC_IN Accuracy	$V_{ADCx\_ADC\_ACC}$	VCC = 3.3 to 5.5V	–40	--	40	mV
ADDR						
ADDR Threshold Address = 00 Resistor	R_{ADDR1}	VCC = 3.3 to 5.5V	--	--	110	kΩ
ADDR Threshold Address = 01 Resistor	R_{ADDR2}	VCC = 3.3 to 5.5V	180	--	320	kΩ
ADDR Threshold Address = 10 Resistor	R_{ADDR3}	VCC = 3.3 to 5.5V	460	--	1020	kΩ
ADDR Threshold Address = 11 Resistor	R_{ADDR4}	VCC = 3.3 to 5.5V	1420	--	--	kΩ
IRQB						
Output Low Threshold	V_{IRQB_OL}	I_{OL} = 4mA at VCC = 3.5V to 5.5V	--	--	0.4	V
Input Voltage High Level	V_{IRQB_IH}	VCC = 3.3V to 5.5V	1.26	--	--	V
Input Voltage Low Level	V_{IRQB_IL}	VCC = 3.3V to 5.5V	--	--	0.54	V
Input Leakage Current	I_{IRQB_LK}	VIO = 0 to 0.4V,1 to 5.5V	–1	--	1	μA
GPIO						
Input Voltage High Level	V_{GPIO_IH}	VCC = 3.3V to 5.5V	1.26	--	--	V
Input Voltage Low Level	V_{GPIO_IL}	VCC = 3.3V to 5.5V	--	--	0.54	V
Output Voltage High Level	V_{GPIO_OH}	I_{OH} = –2mA at VCC = 3.3V to 5.5V	VDDIO – 0.4	--	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Low Level	V_{GPIO_OL}	I_{OL} = 4mA at VCC = 3.3V to 5.5V	--	--	0.4	V
Input Pull-Up Resistor	R_{GPIO_PU}		50	80	120	kΩ
Input Pull-Low Resistor	R_{GPIO_PD}		50	80	120	kΩ
Input Leakage Current	I_{GPIO_LK}	VIO = 0 to 0.4V,1 to 5.5V	−1	--	1	μA
HPD						
Output Voltage Low Level	V_{HPD_OL}	I_{OL} = 4mA at VCC = 3.3V to 5.5V	--	--	0.4	V
Hot Plug Detect Threshold	V_{HPD_R}		2	--	--	V
Hot Unplug Detect Threshold	V_{HPD_F}		--	--	0.8	V
HPD Pull-Up to LDO_3V3 Resistor	R_{HPD_PU}		--	10	20	kΩ
HPD Pull-Low to GND Resistor	R_{HPD_PD}		100	150	200	kΩ
Input Leakage Current	I_{HPD_LK}	VCC = 3.3 to 5.5V, VIO = 0 to 5.5V	−1	--	1	μA
I^2C						
I^2C Pull-High			1.8	--	5.5	V
Low-Level Input Voltage	V_{IL_I2C}	VCC = 3.3 to 5.5V	--	--	0.54	V
High-Level Input Voltage	V_{IH_I2C}	VCC = 3.3 to 5.5V	1.26	--	--	V
Low-Level Output Voltage	V_{OL_I2C}	I_{OL} = 4mA at VCC = 2.5V to 5.5V	--	--	0.4	V
Input Current Each IO Pin	I_{IL_I2C}	VIO = 0 to 0.4V, 1 to 5.5V	−10	--	10	μA
SCL Clock Frequency	f_{SCL}	VCC = 3.3 to 5.5V CB ≤ 100pF	400	--	1000	kHz
Rise Time of both SDA and SCL Signals	t_R	VCC = 3.3 to 5.5V CB ≤ 100pF	--	--	120	ns
Fall Time of Both SDA and SCL Signals	t_F	VCC = 3.3 to 5.5V CB ≤ 100pF	4	--	120	ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter (400k)	t_{SP}	VCC = 3.3 to 5.5V	--	--	50	ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter (1M)	t_{SP}	VCC = 3.3 to 5.5V	--	--	15	ns
Data Hold Time	$t_{HD;DAT}$	VCC = 3.3 to 5.5V	30	--	--	ns
Data Setup Time	$t_{SU;DAT}$	VCC = 3.3 to 5.5V	50	--	--	ns
VDC						
VDC 2V Low Voltage Detection Threshold	V_{VDC_2V}	VCC = 3.3 to 5.5V	1.8	2	2.2	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDC 2V Low Voltage Detection Threshold Hysteresis	$V_{VDC\_HYS\_2V}$	VCC = 3.3 to 5.5V	--	40	--	mV
VDC 1.5V Low Voltage Detection Threshold	$V_{VDC\_1.5V}$	VCC = 3.3 to 5.5V	1.35	1.5	1.65	V
VDC 1.5V Low Voltage Detection Threshold Hysteresis	$V_{VDC\_HYS\_1.5V}$	VCC = 3.3 to 5.5V	--	40	--	mV
VDC 0.9V Low Voltage Detection Threshold	$V_{VDC\_0.9V}$	VCC = 3.3 to 5.5V	0.81	0.9	0.99	V
VDC 0.9V Low Voltage Detection Threshold Hysteresis	$V_{VDC\_HYS\_0.9V}$	VCC = 3.3 to 5.5V	--	40	--	mV
VDC 0.52V Low Voltage Detection Threshold	$V_{VDC\_0.52V}$	VCC = 3.3 to 5.5V	0.468	0.52	0.572	V
VDC 0.52V Low Voltage Detection Threshold Hysteresis	$V_{VDC\_HYS\_0.52V}$	VCC = 3.3 to 5.5V	--	40	--	mV
Over-Temperature Protection						
Over-Temperature Protection Shutdown Threshold Rising	T_{OTP_150}	VCC = 3.3 to 5.5V	140	150	160	°C
Over-Temperature Protection Shutdown Threshold Falling	$T_{OTP\_150\_F}$	VCC = 3.3 to 5.5V	95	110	125	°C
Over-Temperature Protection Shutdown Threshold Rising	T_{OTP_120}	VCC = 3.3 to 5.5V	110	120	130	°C
Over-Temperature Protection Shutdown Threshold Falling	$T_{OTP\_120\_F}$	VCC = 3.3 to 5.5V	80	90	100	°C
BASE						
OSC48M Output Frequency	f_{OSC48M}	VCC = 3.3 to 5.5V	47.04	48	48.96	MHz
OSC48M Output RMS Jitter	f_{OSC48M_Jitter}	VCC = 3.3 to 5.5V	--	145	--	ps
OSC48M Output Start-Up Time	f_{OSC48M_Jitter}	VCC = 3.3 to 5.5V	--	--	7	µs

13 Typical Application Circuit

13.1 The RT7889D/RT7889DB Used in Source or DRP Application Circuits



13.2 The RT7889D/RT7889DB Used in Sink Application Circuits

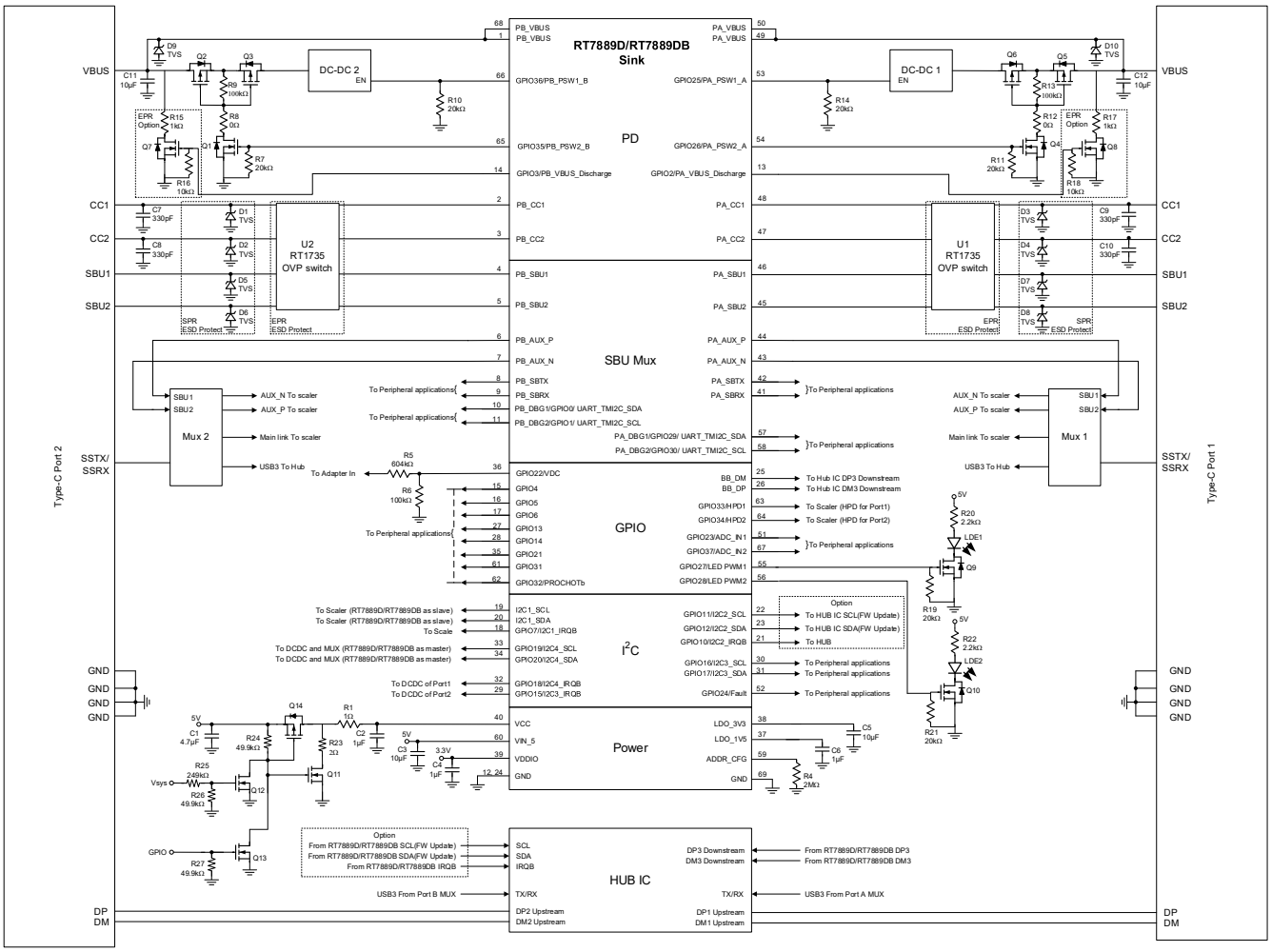


Table 1. Recommended Component Information

Pin	Part Number	Description	Package	Manufacturer	Power Range
VCC (C1)	GRM21BR61E475KA12K	4.7μF/25V/X5R (Note 6)	0805	muRata	-
VCC (C2)	GRM185R61A105KE26D	1μF/10V/X5R	0603	muRata	-
VCC (R1)	WR06W1R00FTL	1Ω (Note 6)	0603	Walsin	-
VIN_5 (C3)	GRM21BR71A106KA73L	10μF/10V/X7R	0805	muRata	-
VDDIO (C4)	0603X105K250CT	1μF/25V/X5R	0603	Walsin	-
LDO_3V3 (C5)	GRM21BR71A106KA73L	10μF/10V/X7R	0805	muRata	-
LDO_1V5 (C6)	0603X105K250CT	1μF/25V/X5R	0603	Walsin	-
PA_CC1 (C9) PA_CC2 (C10) PB_CC1 (C7) PB_CC2 (C8)	0603N331J500CT	330pF/50V/NP0	0603	Walsin	-
PA_CC1 (D3) PA_CC2 (D4) PB_CC1 (D1) PB_CC2 (D2)	AZ4520-01F	TVS Diodes (Note 7)	DFN1610P2E	Amazing	SPR
PA_SBU1 (D7) PA_SBU2 (D8) PB_SBU1 (D5) PB_SBU2 (D6)	AZ4520-01F	TVS Diodes (Note 7)	DFN1610P2E	Amazing	SPR
PA_CC1 (U1) PA_CC2 (U1) PA_SBU1 (U1) PA_SBU2 (U1) PB_CC1 (U2) PB_CC2 (U2) PB_SBU1 (U2) PB_SBU2 (U2)	RT1735	OVP switch (Note 7)	WQFN-20L 3x3	Richtek	EPR
PA_VBUS (D13) PB_VBUS (D14)	ESD5401N	TVS Diodes	DFN1006-2	Will SEMI	-
PA_VBUS (R3) PB_VBUS (R2)	WR06X4990FTL	499Ω	0603	Walsin	-
VCC (Q11) VCC (Q12) VCC (Q13)	2N7002	N-Channel MOSFET	SOT23	AOS	-
VCC (Q14)	AO3415	P-Channel MOSFET	SOT23	Onsemi	-
VCC (R23)	WR06W2R00FTL	2Ω	0603	Walsin	-
VCC (R24) VCC (R26) VCC (R27)	WR06X4992FTL	49.9kΩ	0603	Walsin	-
VCC (R25)	WR06X2493FTL	249kΩ	0603	Walsin	-

Note 6. A 1Ω series resistor and a 4.7μF bypass capacitor must be placed at the VCC pin.

Note 7. When the device power range is SPR, use the TVS AZ4520-01F; when the device power range is EPR, use the protection IC RT1735, so that PA_CC1, PA_CC2, PA_SBU1, PA_SBU2, PB_CC1, PB_CC2, PB_SBU1, and PB_SBU2 will pass IEC 61000-4-2: ±8kV contact discharge and ±15kV air discharge.

14 Application Information

(Note 9)

14.1 CPU and Memory

14.1.1 MCU

The RT7889D/RT7889DB integrates a 32-bit ARM Cortex – M0+ microcontroller, optimized for low-power operation through extensive clock gating. The core primarily utilizes 16-bit instructions and executes a subset of the Thumb-2 instruction set.

It includes a Nested Vectored Interrupt Controller (NVIC) with 32 interrupt inputs and a Wakeup Interrupt Controller (WIC), which enables the processor to wake from deep sleep mode, allowing power to be switched off to the main processor during low-power states.

The CPU subsystem also includes a 16-channel DMA/Datawire block and a Serial Wire Debug (SWD) interface, a two-wire alternative to JTAG. The debug configuration for the RT7889D/RT7889DB supports four breakpoint comparators and two watchpoint comparators.

14.1.2 Flash

The RT7889D/RT7889DB has a 256kB flash module.

14.1.3 ROM

The device includes 64kB of supervisory ROM, which contains boot and configuration routines.

14.1.4 Cryptographic Accelerator

The integrated cryptographic accelerator supports the following requirements:

- SHA2 (256-bit)
- ECDSA
- CRC32

14.1.5 Power Mode

The RT7889D/RT7889DB supports three power modes: Active Mode, Idle Mode, and Deep Green Mode. Mode transitions are controlled by the system controller. The functions available in each mode are summarized in the table below.

Mode	48MHz	MCU	Function
Active	On	On	All functions
Idle	On	Off	More functions than in deep green mode: USB 2.0 Full Speed Billboard

Mode	48MHz	MCU	Function
Deep Green	Off	Off	I²C1 to 4 IRQB1 to 4, FAULT (GPIO24) GPIO4/5/6 as input (can wake up MCU) GPIO as output HPD1 (GPIO33), HPD2 (GPIO34) VDC (GPIO22) USB PD USB 2.0 Full Speed Billboard Suspended SBU MUX ADC Alarm interrupt (at PA_VBUS, PB_VBUS, ADC_IN1, ADC_IN2) Water Detection interrupt

In different power modes, the PD power-saving modes and USB 2.0 PHY functions are listed in the table below.

MCU	Port A, Port B	USB 2.0 Full Speed Billboard	Port A TCPC	Port B TCPC
Deep Green Mode	Port A and Port B no attached	Off	Auto low power	Auto low power
Deep Green Mode	Port A or Port B attached	Off	Attached: Auto idle No attached: Auto low power	Attached: Auto idle No attached: Auto low power
Idle Mode	Port A or Port B attached	On	Attached: Auto idle No attached: Auto low power	Attached: Auto idle No attached: Auto low power
Deep Green Mode	Port A or Port B attached	Suspended command received	Attached: Auto idle No attached: Auto low power	Attached: Auto idle No attached: Auto low power

14.2 Wake-Up Interrupt Controller

The RT7889D/RT7889DB integrates a Wake-Up Interrupt Controller (WIC) to enable wake from state-retention power-gating and from clock-gated states. The WIC is responsible for monitoring for assertion of interrupts when the processor is powered down in the idle or deep green operating mode. In these modes, the entire power domain is power-gated, and as such, the processor and NVIC are not available to check for interrupts. The WIC retains a copy of which peripheral interrupt sources to the NVIC were enabled when the processor entered idle or deep green mode. If an enabled interrupt detected while the CPU is powered down, the WIC asserts a wake request and performs a handshake with the system power controller to exit idle or deep green mode so the CPU can service the interrupt. The WIC latches the event and presents a pending interrupt to the NVIC when CPU clocks are restored, ensuring the CPU observes the interrupt even if the peripheral's raw status de-asserts before the CPU is fully powered.

Function	Pin Name	
I²C Interrupt	I2C1_SCL	GPIO16/I2C3_SCL
	GPIO11/I2C2_SCL	GPIO19/I2C4_SCL
GPIO	GPIO7/I2C1_IRQB	GPIO15/I2C3_IRQB
	GPIO10/I2C2_IRQB	GPIO18/I2C4_IRQB

Function	Pin Name	
	GPIO4	GPIO5
	GPIO6	GPIO24/Fault
DisplayPort Hot-Plug Detect	GPIO33/HPD1	GPIO34/HPD2
Voltage Comparator	GPIO22/VDC	
USB PD	PA_CC1	PB_CC1
	PA_CC2	PB_CC2
USB 2.0 Full Speed Billboard	BB_DP	BB_DM
ADC Alarm Interrupt	PA_VBUS	PB_VBUS
	GPIO23/ADC_IN1	GPIO37/ADC_IN2
Water Detection Interrupt	PA_SBU1	PB_SBU1
	PA_SBU2	PB_SBU2

14.3 Power-On System

The RT7889D/RT7889DB can be powered from one of three possible external supply sources: PA_VBUS, PB_VBUS (4.0V to 30V), or VCC (4V to 5.5V). The VBUS supply is regulated inside the chip with a HV low-dropout regulator (LDO) down to 3.3V and 1.5V level. The chip's internal LDO_3V3 and LDO_1V5 rails seamlessly switch from the VBUS regulator to VCC. However, when the internal power supply switches from VCC to the VBUS regulator, it causes the IC to reset, which limits the application.

The 5V VCC power supply in the product system is estimated to require 30mA to ensure that the RT7889D/RT7889DB can operate normally. VIN_5V must be capable of sourcing300mA to support a 1.5 W VCONN load.

When additional power for the product system is required, the RT7889D/RT7889DBis powered by an external AC adapter. The system needs to supply power to VCC and VDDIO first, after which the RT7889D/RT7889DB can operate normally. Subsequently, when Type-C is connected, VIN_5 needs to be powered to enable the PD CC to output VCONN. Additionally, it can control peripheral circuits to enable PA_VBUS and PB_VBUS, allowing them to provide power output as a PD source.

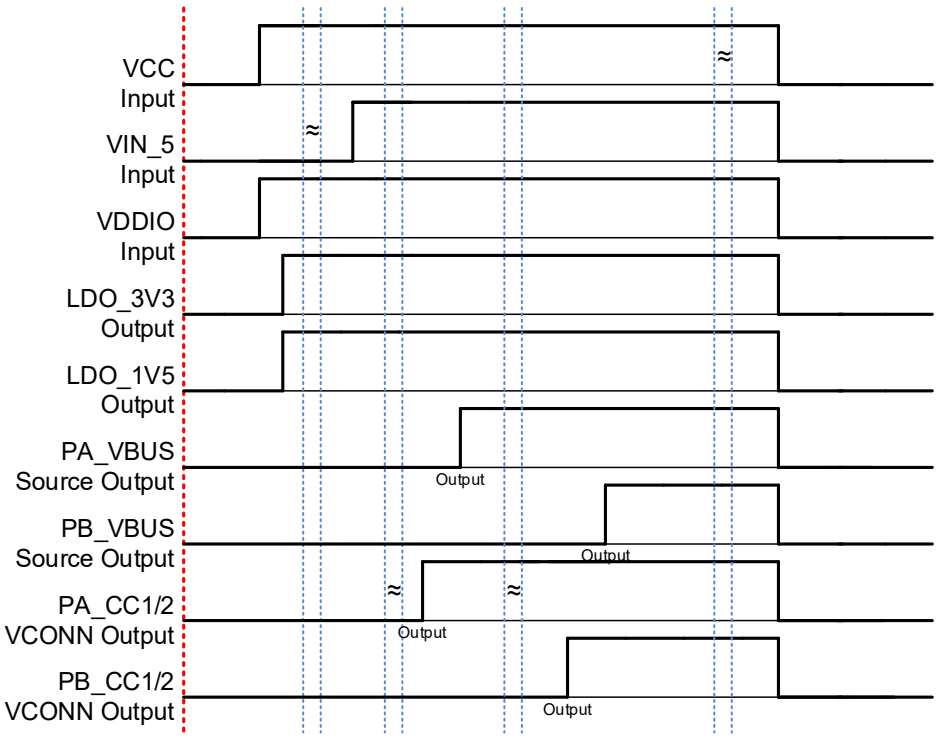


Figure 1. RT7889D/RT7889DB External Power Supply Timing Diagram

When the RT7889D/RT7889DB is in a dead battery condition, or in a system that requires power from the Type-C port, the device will begin normal operation after the Type-C port is connected, the CC line is attached, and power is supplied via PA_VBUS or PB_VBUS. The system must supply power to VCC and VDDIO. Additionally, when the PD CC outputs VCONN, VIN_5 must be powered.

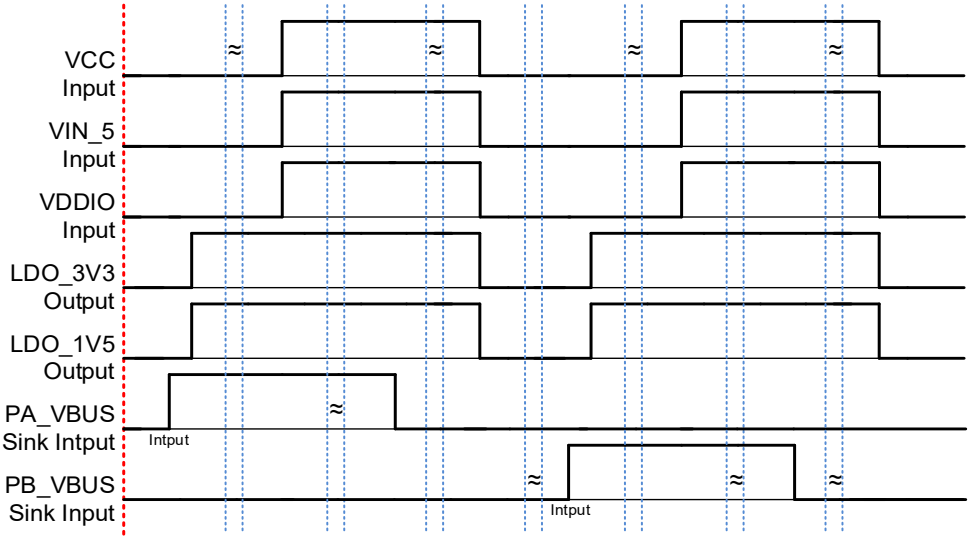


Figure 2. RT7889D/RT7889DB Requires Power from the Type-C Timing Diagram

14.4 USB-PD Physical Layer

The USB-PD subsystem includes the USB-PD physical layer block and its supporting circuits. The physical layer consists of a transmitter and receiver that communicate BMC-encoded data over the CC in accordance with the

PD 3.2 standard. All communication is conducted in a half-duplex manner. The physical layer (PHY) employs collision avoidance techniques to minimize communication errors on the channel.

14.5 VCONN Switch

The RT7889D/RT7889DB integrates two VCONN switches to power either the CC1 or CC2 pins. A dedicated VIN_5 power supply input pin provides power to E-marker cables through these VCONN switches. Each switch can deliver up to 1.5W per port over a valid VCONN voltage range of 4.85V to 5.5V on the CC1/2 pins for E-marker cables. The VCONN switches feature integrated protection circuits, including OVP, OCP, RVP, UVP, and short-to-GND protection, ensuring both normal operation and robust protection.

14.6 SBU MUX

The device features a 1:3 multiplexer (mux) for the SBU pins, allowing them to connect to different points within the system. Each RT7889D/RT7889DB provides outputs for the SBTX/RX (USB4/TBT) channel, AUX (DP) channel, and a debug channel. The SBTX/RX channel passes through an integrated level shifter, while the AUX and debug channels are passive pass-through connections.

An SBU OVP switch is connected to both the SBU-to-AUX and SBU-to-DBG paths. The ON resistance of this switch is included in the total resistance of each SBU channel (RON_SBU_AUX and RON_SBU_DBUG). The SBTX/RX channel includes an integrated level shifter.

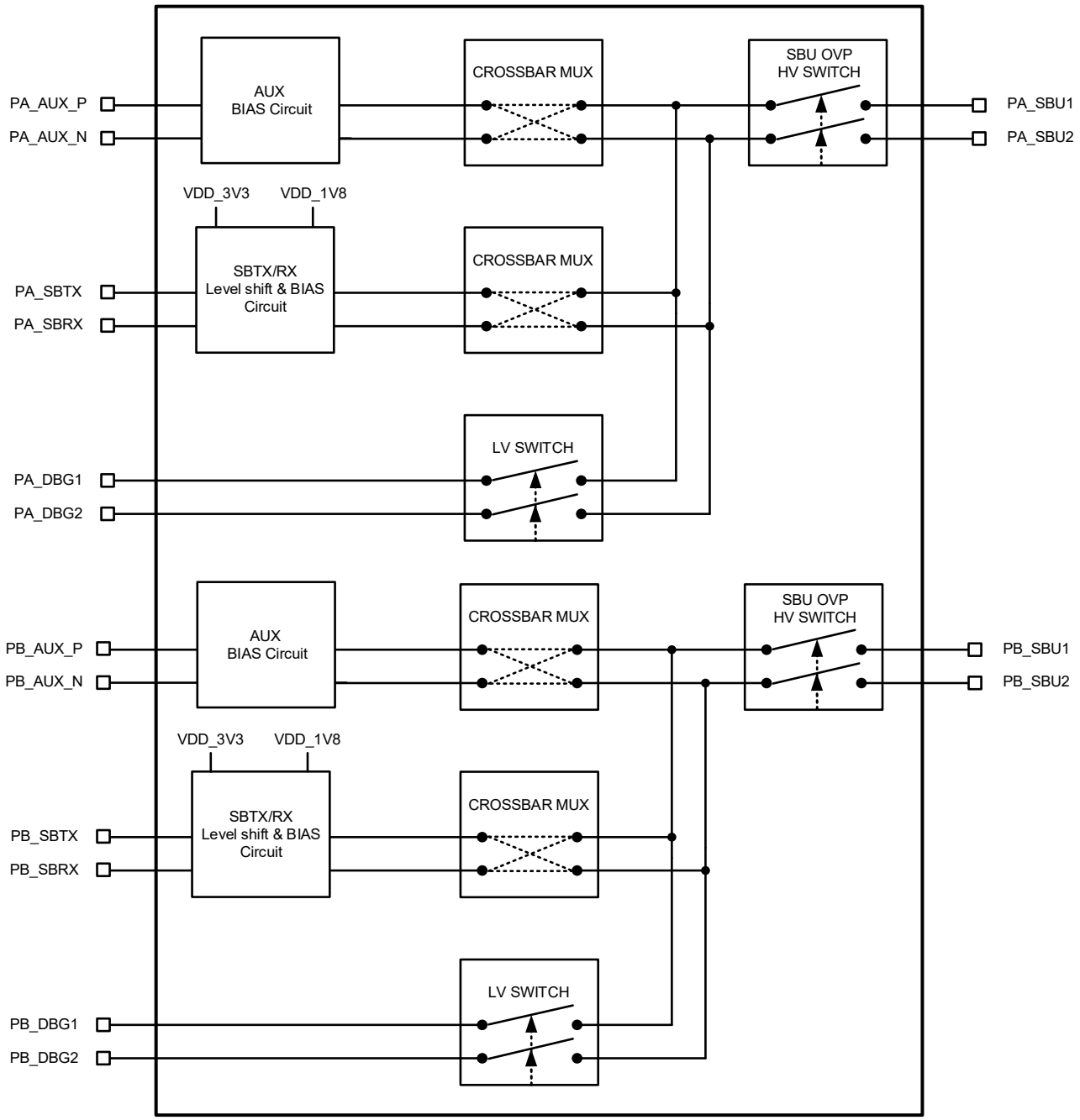


Figure 3. Diagram of SBU MUX and OVP Switch

14.6.1 SBU OVP

Each SBU pin includes an OVP comparator that disables the switch when an overvoltage condition is detected. If the SBU voltage exceeds 4.5V, the SBU OVP HV switch is disabled.

14.6.2 AUX Channel

The output from the SBU OVP module can be connected to either the AUX_P or AUX_N output through a crossbar multiplexer. Each output features bias circuits with configurable pull-down and pull-up resistors. When the SBU MUX is set to the AUX channel application, SBU1 is connected to AUX_P and SBU2 is connected to AUX_N by default.

14.6.3 SBTX/SBRX Channel

The USB4/TBT output from the SBU MUX passes through a level shifter, converting from SBU to SBTX/RX at VDD_3V3/VDD_1V8. Each output also includes a biasing resistor. When the SBU MUX is set to the SBTX/SBRX channel application, SBU1 is connected to SBTX and SBU2 is connected to SBRX by default.

14.6.4 Debug Channel

This passive mux channel can be used to pass signals such as I^2C or UART, typically for system debugging purposes.

14.7 USB 2.0 Full-Speed PHY

The RT7889D/RT7889DB includes one USB 2.0 full-speed (12Mbps) device to support billboard class and HID class applications, such as firmware downloads. The device can utilize these widely available USB interfaces to transmit and receive data with USB hosts, typically PCs or laptops.

14.8 11-Bit SAR ADC

The RT7889D/RT7889DB features an 11-bit SAR (Successive Approximation Register) ADC, as shown in Figure 4. The ADC uses an analog input multiplexer to support multiple inputs from various voltages and currents within the device. The ADC output can be read via I^2C for customized requirements and also serves as an input for the automatic ADC monitor circuits. Additionally, the PA_VBUS, PB_VBUS, ADC_IN1, and ADC_IN2 pins support the ADC Alarm interrupt function.

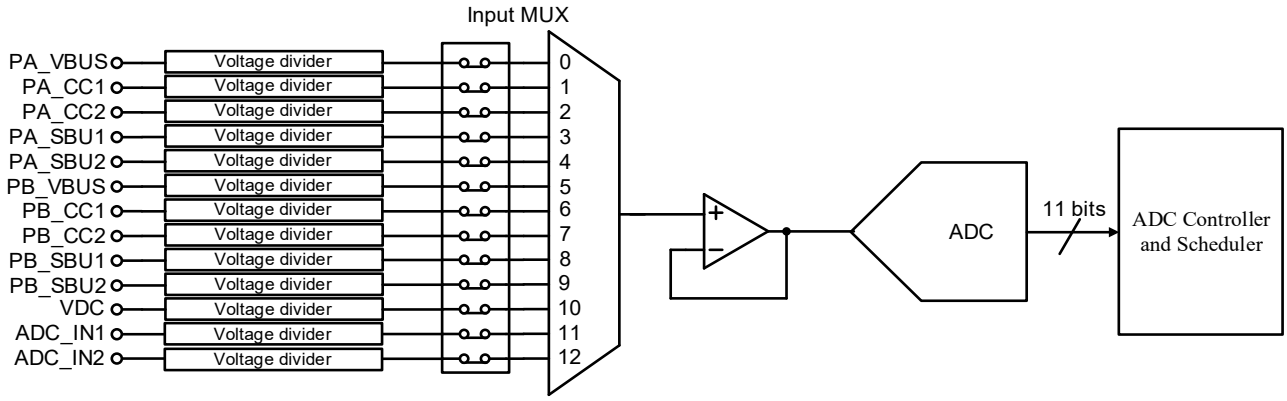


Figure 4. Diagram of ADC input

14.9 Water Detection

The RT7889D/RT7889DB integrates a water detection circuit on the PA_SBU1, PA_SBU2, PB_SBU1, and PB_SBU2 pins to perform anomaly detection prior to device attachment.

14.10 DisplayPort Hot-Plug Detect (HPD)

The RT7889D/RT7889DB supports DisplayPort Alternate Mode as both a DP source and DP sink. It provides HPD converter functionality on the GPIO33/HPD1 and GPIO34/HPD2 pins, which can operate as either HPD TX or RX. The PD messaging events are translated to the corresponding HPD pin based on the selected the DP mode.

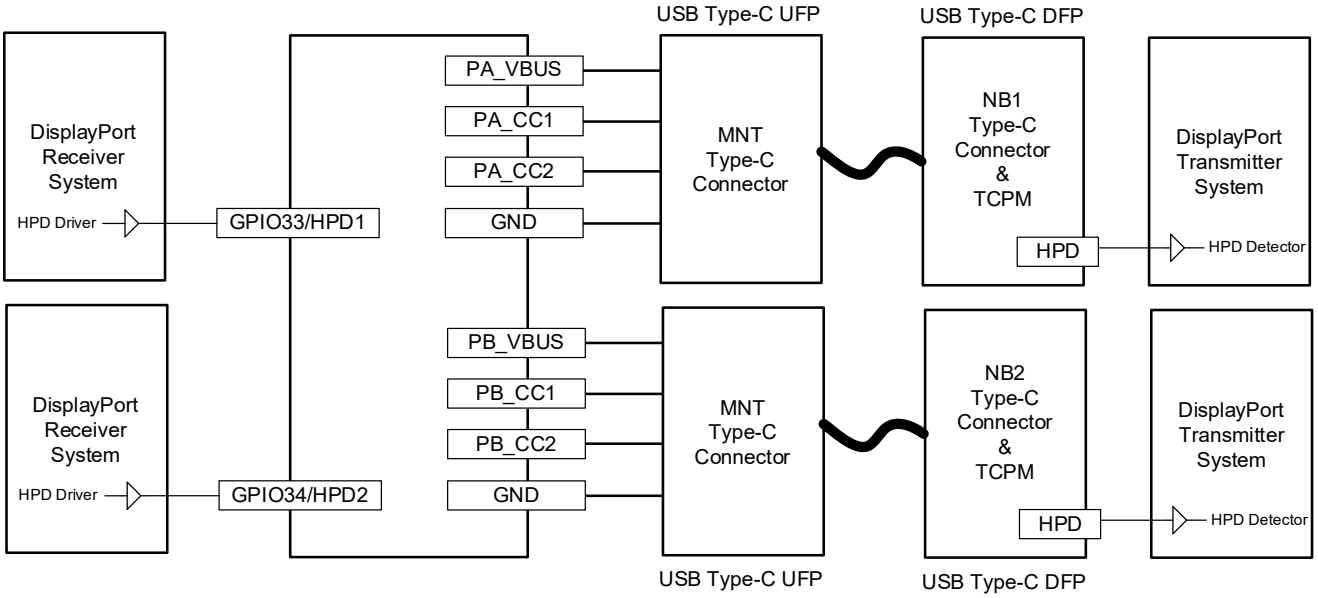


Figure 5. PD-to-HPD Converter: Passing HPD Signal in a DisplayPort System

14.11 Over-Temperature Protection

The RT7889D/RT7889DB monitors its internal temperature to prevent thermal failures. When the junction temperature reaches 120°C or 150°C, the chip disables the VCONN and SBU switches. The IC resumes normal operation once the junction temperature has decreased by 30°C or 40°C. Each port features a dedicated thermal shutdown monitor for its VCONN paths. If a port's VCONN path temperature exceeds 120°C or 150°C, the VCONN and SBU switches for that port are disabled. When the temperature drops below the threshold and the hysteresis is cleared, the VCONN paths resume normal operation.

14.12 GPIO Application

The following table lists the GPIO power domains and the describes the input/output types for various applications.

Pin Number	Pin Name	Power Domain	Output Stage	Input form
10	PB_DBG1/GPIO0/UART_TMI2C_SDA	VDDIO	Push-pull	Polling
11	PB_DBG2/GPIO1/UART_TMI2C_SCL	VDDIO	Push-pull	Polling
13	GPIO2/PA_VBUS_Discharge	VDDIO	Push-pull	Polling
14	GPIO3/PB_VBUS_Discharge	VDDIO	Push-pull	Polling
15	GPIO4	VDDIO	Push-pull	Interrupt
16	GPIO5	VDDIO	Push-pull	Interrupt
17	GPIO6	VDDIO	Push-pull	Polling
18	GPIO7/I2C1_IRQB	LDO_3V3	Open-drain	Interrupt
21	GPIO10/I2C2_IRQB	LDO_3V3	Open-drain	Interrupt
22	GPIO11/I2C2_SCL	LDO_3V3	Open-drain	Polling
23	GPIO12/I2C2_SDA	LDO_3V3	Open-drain	Polling
27	GPIO13	VDDIO	Push-pull	Polling
28	GPIO14	VDDIO	Push-pull	Polling
29	GPIO15/I2C3_IRQB	LDO_3V3	Open-drain	Interrupt

Pin Number	Pin Name	Power Domain	Output Stage	Input form
30	GPIO16/I2C3_SCL	LDO_3V3	Open-drain	Polling
31	GPIO17/I2C3_SDA	LDO_3V3	Open-drain	Polling
32	GPIO18/I2C4_IRQB	LDO_3V3	Open-drain	Interrupt
33	GPIO19/I2C4_SCL	LDO_3V3	Open-drain	Polling
34	GPIO20/I2C4_SDA	LDO_3V3	Open-drain	Polling
35	GPIO21	VDDIO	Push-pull	Polling
36	GPIO22/VDC	VDDIO	Push-pull	Polling
51	GPIO23/ADC_IN_1	LDO_3V3	Open-drain	Polling
52	GPIO24/Fault	LDO_3V3	Open-drain	Interrupt
53	GPIO25/PA_PSW1_A	VDDIO	Push-pull	Polling
54	GPIO26/PA_PSW2_A	VDDIO	Push-pull	Polling
55	GPIO27/LED PWM1	VDDIO	Push-pull	Polling
56	GPIO28/LED PWM2	VDDIO	Push-pull	Polling
57	PA_DBG1/GPIO29/UART_TMI2C_SDA	VDDIO	Push-pull	Polling
58	PA_DBG2/GPIO30/UART_TMI2C_SCL	VDDIO	Push-pull	Polling
61	GPIO31	VDDIO	Push-pull	Polling
62	GPIO32/PROCHOTb	VDDIO	Push-pull	Polling
63	GPIO33/HPD1	LDO_3V3	Open-drain	Interrupt
64	GPIO34/HPD2	LDO_3V3	Open-drain	Interrupt
65	GPIO35/PB_PSW2_B	VDDIO	Push-pull	Polling
66	GPIO36/PB_PSW1_B	VDDIO	Push-pull	Polling
67	GPIO37/ADC_IN_2	LDO_3V3	Open-drain	Polling

14.13 I²C Interface

The RT7889D/RT7889DB supports four channels of slave I²C. The I²C interface can be configured for up to 128 slave addresses by adjusting the resistance between the ADDR (pin 59) to GND, as well as through MCU register settings.

Table 2. I²C1, I²C2, I²C3, and I²C4 Slave Address (Note 8)

Address	MSB						LSB	R/W bit	R/W
ADDR Bit	7	6	5	4	3	2	1	1/0	--
How to Config	Fix	Fix	Fix	Fix	Fix	By ADDR	By ADDR	1/0	--
ADDR 10kΩ	0	1	0	0	1	0	0	1/0	49/48
ADDR 270kΩ	0	1	0	0	1	0	1	1/0	4B/4A
ADDR 750kΩ	0	1	0	0	1	1	0	1/0	4D/4C
ADDR 2MΩ	0	1	0	0	1	1	1	1/0	4F/4E

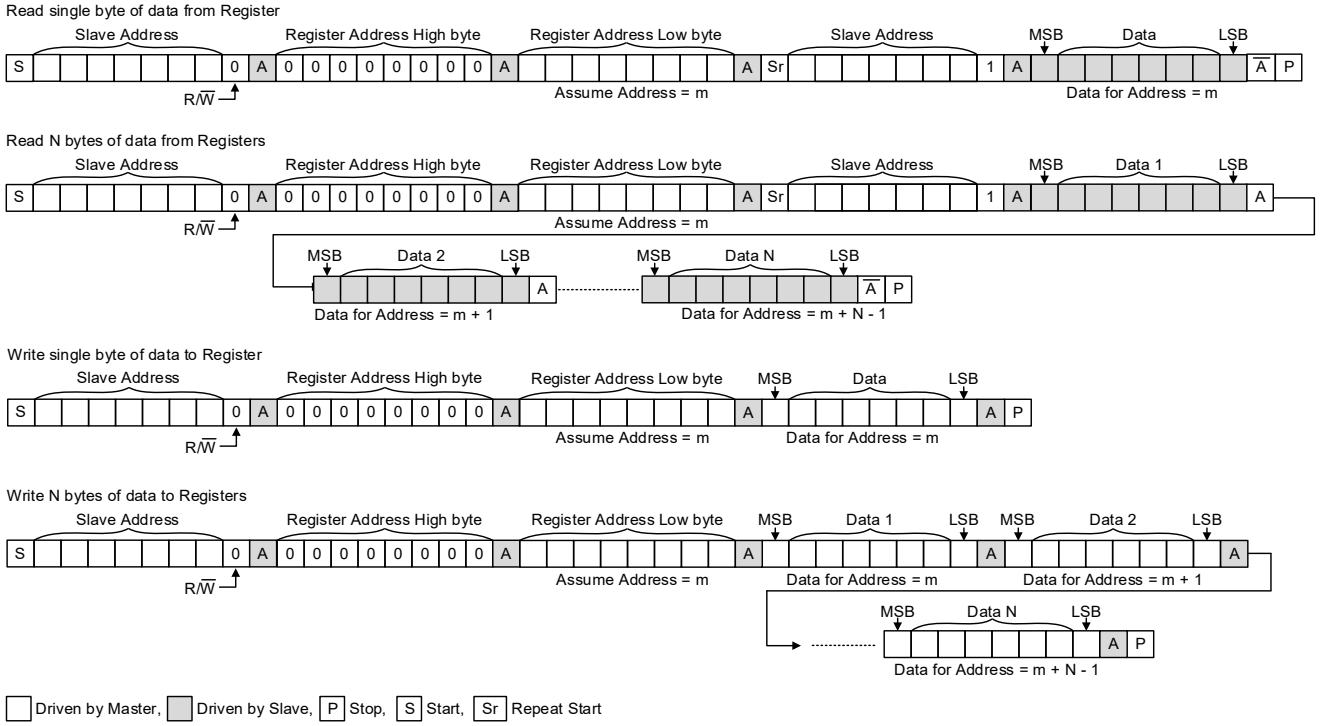
Note 8. The R/W field example is 0b'01001 with the MSB shown as an example.

When the RT7889D/RT7889DB operates with 4 slave I²C channels simultaneously, each channel supports a maximum speed of 400kHz. However, when only 2 slave I²C channels are used, one channel can operate at up to 1MHz, while the other supports up to 400kHz.

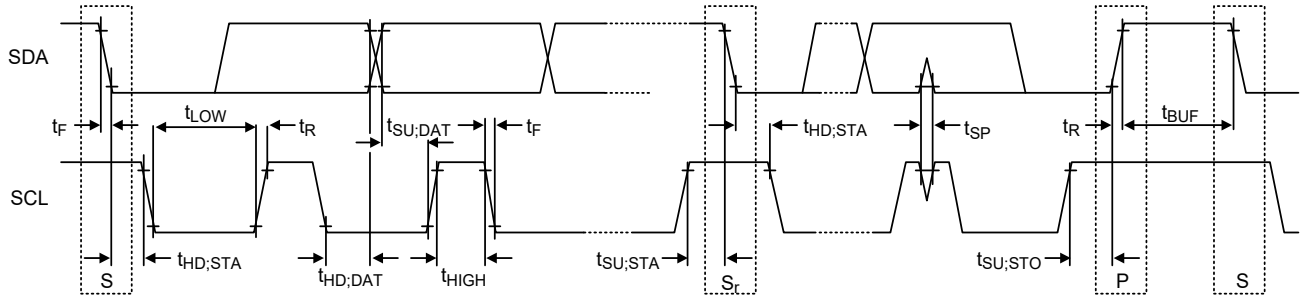
Each I²C bus interface must be connected to the power node through a 1kΩ pull-up resistor, with independent connections to the processor for each channel.

The I²C timing diagrams are provided below.

14.13.1 Read and Write Function



14.13.2 I²C Waveform Information



14.14 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is normally 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-68L 7x7 package, the thermal resistance, θ_{JA}, is 25.52°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (125°C – 25°C) / (25.52°C/W) = 3.92W for a WQFN-68L 7x7 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 6 allows the user to see the effect of rising ambient temperature on the maximum power dissipation.

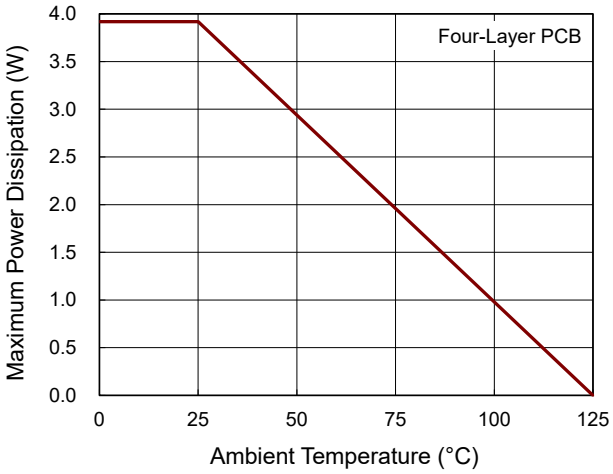


Figure 6. Derating Curve of Maximum Power Dissipation

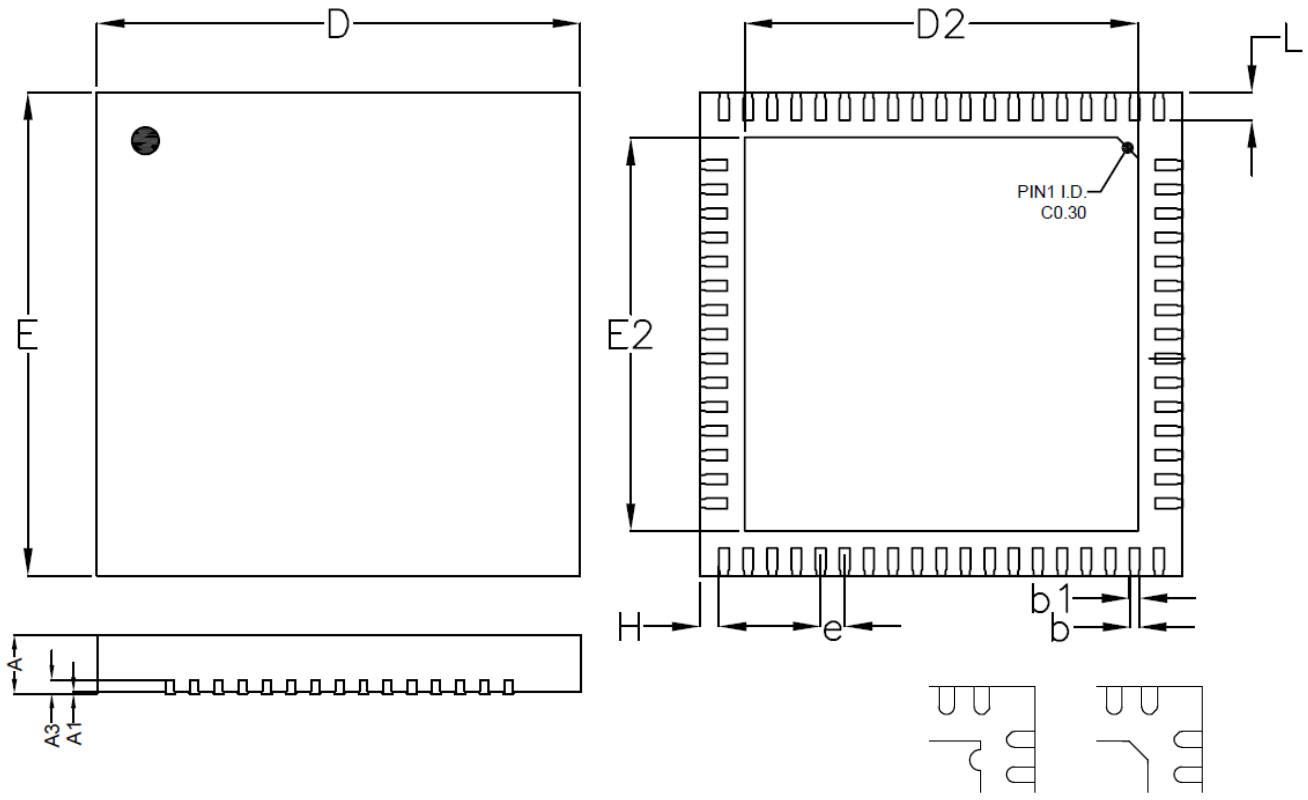
14.15 Layout Considerations

Appropriate routing and component placement are essential to maintain the signal integrity of the USB2.0, SBU, and CC signals. The following guidelines apply to the RT7889D/RT7889DB:

- Place bypass capacitors as close as possible to the VCC, VDDIO, LDO_3V3, LDO_1V5 and VIN_5 pins. Connect them to a solid ground plane using short, wide traces and multiple vias.
- Route USB 2.0 and SBU traces straight and short; minimize sharp bends and avoid stubs.
- To improve ESD immunity, place TVS diodes and MLCCs for PA_CC1/CC2, PB_CC1/2, PA_SBU1/2, PB_SBU1/2, and BB_DP/DM as close as possible to the USB Type-C connector, with low-impedance paths to GND.

Note 9. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

15 Outline Dimension

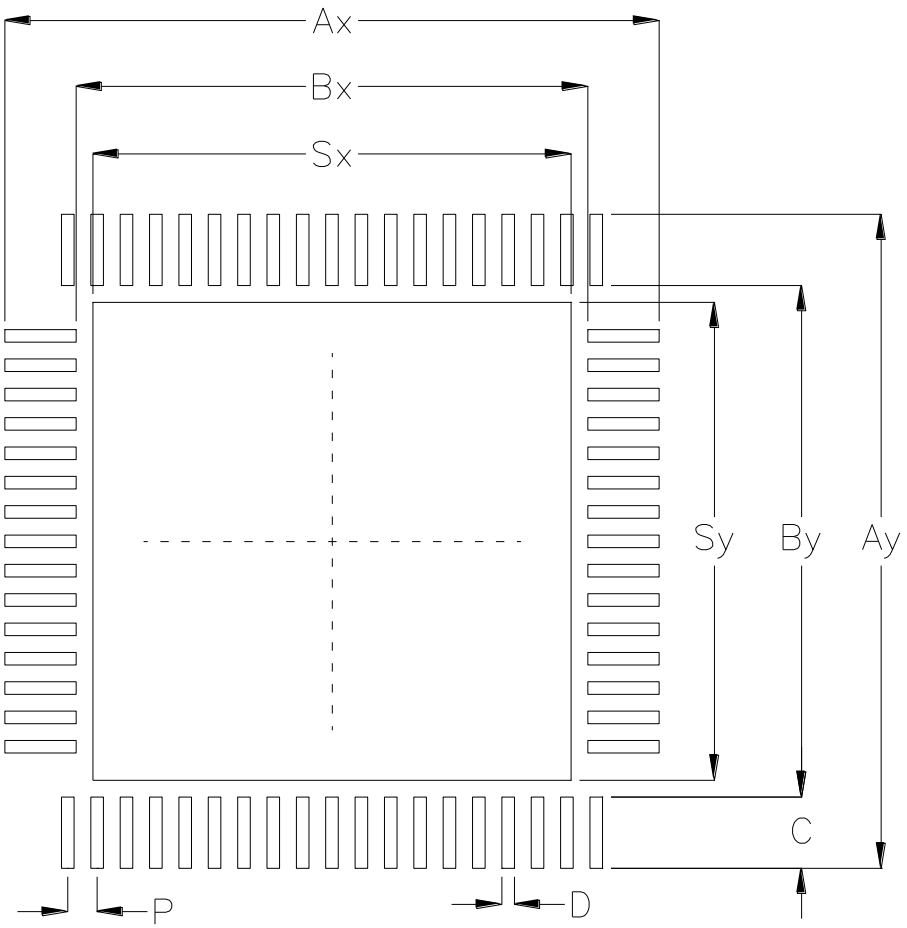


Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.100	0.200	0.004	0.008
b1	0.070	0.170	0.003	0.007
D	6.950	7.050	0.274	0.278
D2	5.650	5.750	0.222	0.226
E	6.950	7.050	0.274	0.278
E2	5.650	5.750	0.222	0.226
e	0.350		0.014	
L	0.350	0.450	0.014	0.018
H	0.225	0.325	0.009	0.013

W-Type 68L QFN 7x7 Package

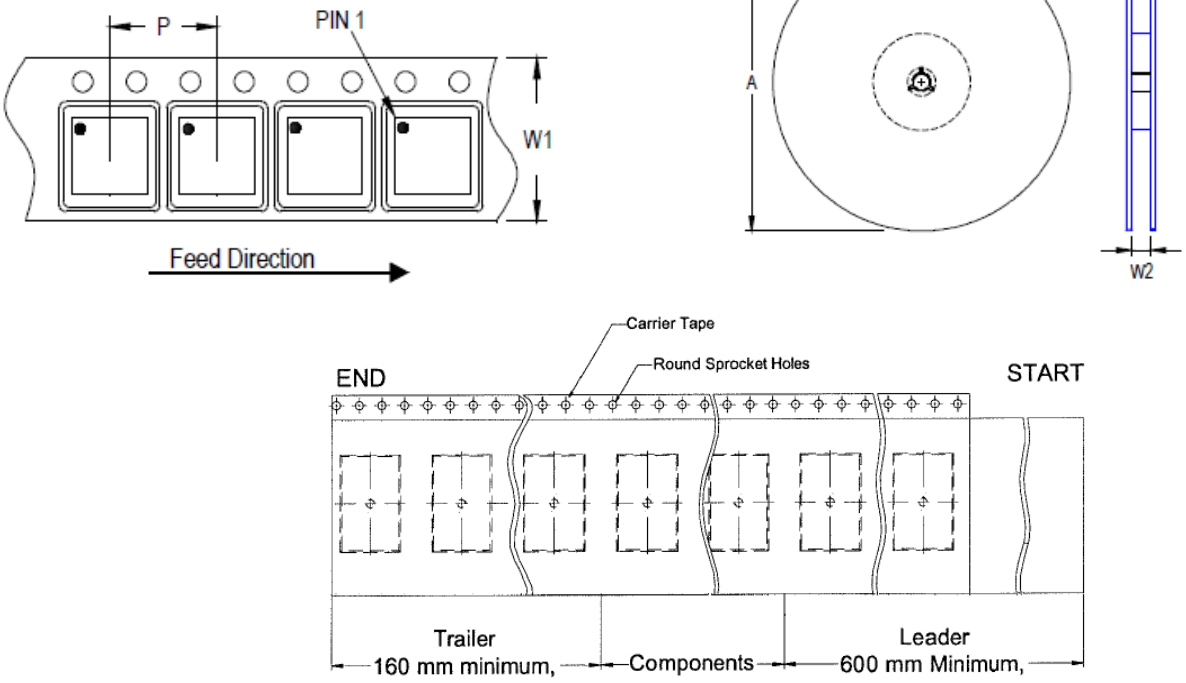
16 Footprint Information



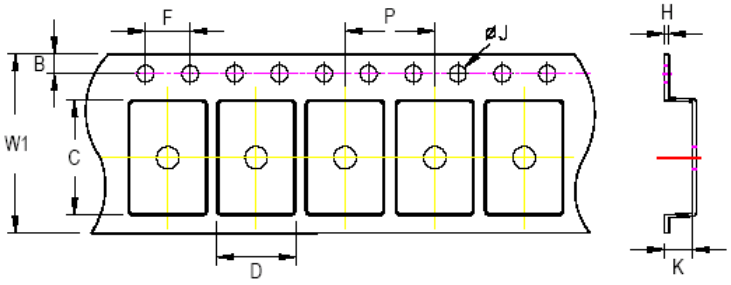
Package	Number of Pins	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN7x7-68	68	0.35	7.80	7.80	6.10	6.10	0.85	0.15	5.70	5.70	±0.05

17 Packing Information

17.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 7x7	16	12	330	13	2,500	160	600	16.4/18.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 16mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
16mm	16.3mm	11.9mm	12.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

17.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
(V, W) QFN and DFN 7x7	13”	2,500	Box G	1	2,500	Carton A	6	15,000

17.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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18 Datasheet Revision History

Version	Date	Description
00	2025/9/12	First Edition
01	2026/3/5	Ordering Information - Updated firmware code description and added notes Marking Information - Added Typical Application Circuit - Updated circuit diagrams to be used in Source or DRP applications and in Sink applications - Updated Table 1. Recommended Component Information