RICHTEK®

RT8068A

3A, 1MHz, Synchronous Buck Converter

1 General Description

The RT8068A is a high efficiency synchronous, buck converter. It features an input voltage range from 2.7V to 5.5V that provides an adjustable regulated output voltage from 0.6V to VIN while delivering up to 3A of output current. The internal synchronous low on-resistance power switches increase efficiency and eliminate the need for an external Schottky diode. The switching frequency is fixed internally at 1MHz. The 100% duty cycle provides low dropout operation, hence extending battery life in portable systems. Current mode operation with internal compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

The RT8068A is available in WDFN-10L 3x3 and SOP-8 (Exposed Pad) packages. The recommended junction temperature range is –10°C to 105°C.

2 Ordering Information

RT8068A □□

Package Type(1)
QW: WDFN-10L 3x3 (W-Type)
SP: SOP-8 (Exposed Pad)
(Exposed Pad-Option 2)

Lead Plating System
Z: ECO (Ecological Element with Halogen Free and Pb free)(2)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

3 Features

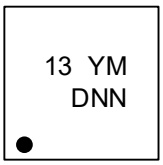
- **High Efficiency: Up to 95%**
- **Low $R_{DS(ON)}$ Internal Switches: 69mΩ/49mΩ at V_{IN} = 5V**
- **Fixed Frequency: 1MHz**
- **No Schottky Diode Required**
- **Internal Compensation**
- **0.6V Reference Allows Low Output Voltage**
- **Low Dropout Operation: 100% Duty Cycle**
- **OCP, UVP, OVP, OTP**

4 Applications

- Portable Instruments
- Battery Powered Equipment
- Notebook Computers
- Distributed Power Systems
- IP Phones
- Digital Cameras

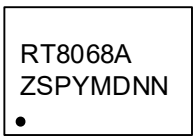
5 Marking Information

RT8068AZQW



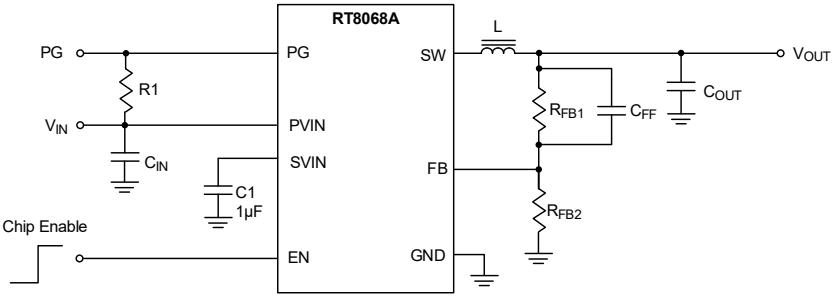
13 : Product Code
YMDNN : Date Code

RT8068AZSP



RT8068AZSP : ProductCode
YMDNN : Date Code

6 Simplified Application Circuit



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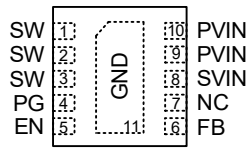
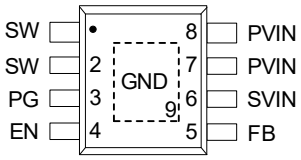
7 Pin Configuration

(TOP VIEW)



WDFN-10L 3x3

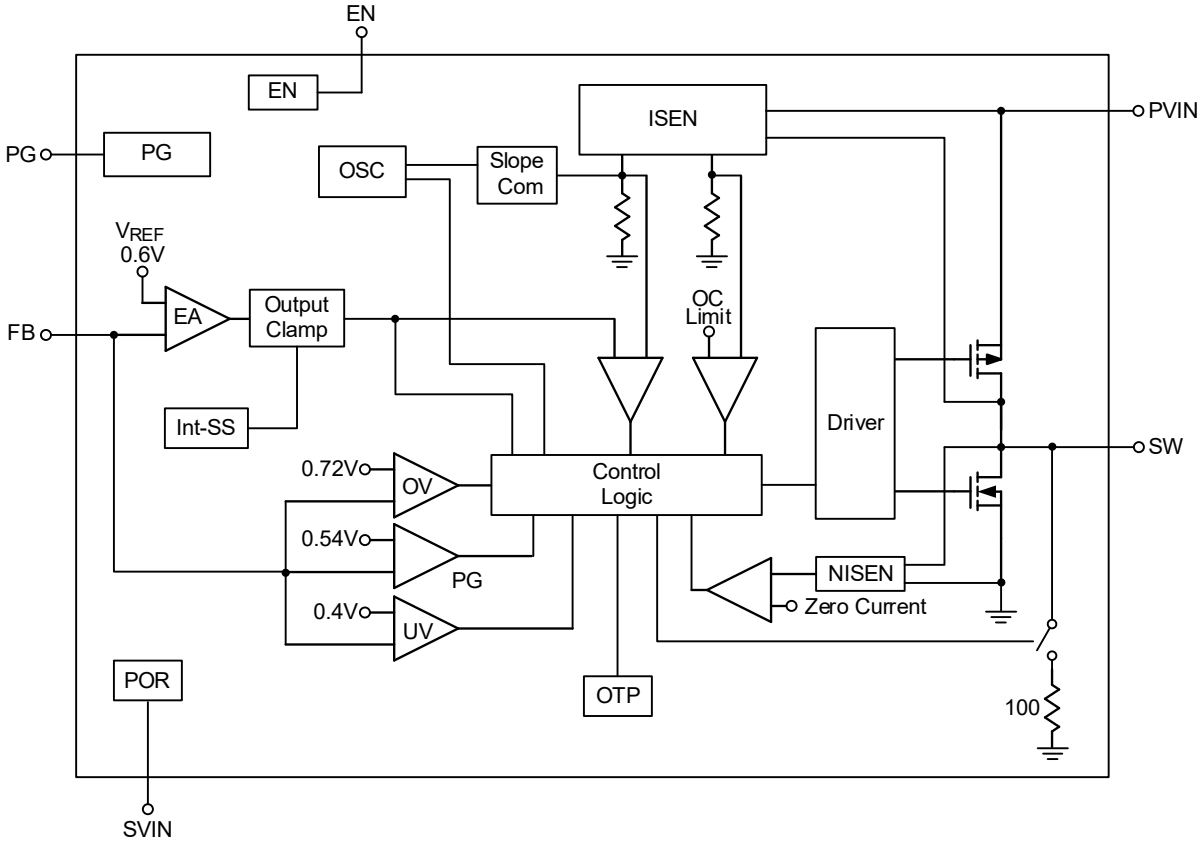


SOP-8 (Exposed Pad)

8 Functional Pin Description

Pin No.		Pin Name	Pin Function
WDFN-10L	SOP8 (Exposed Pad)		
1, 2, 3	1, 2	SW	Switch node. Connect this pin to the inductor.
4	3	PG	Power-good indicator. This pin is an open drain logic output that is pulled to ground when the output voltage is less than 90% of the target output voltage. Hysteresis = 5%.
5	4	EN	Enable control. Pull high to turn on. Do not float.
6	5	FB	Feedback pin. This pin receives the feedback voltage from a resistive voltage divider connected across the output.
7	--	NC	No internal connection.
8	6	SVIN	Signal input pin. Decouple this pin to GND with at least 1μF ceramic cap.
9, 10	7, 8	PVIN	Power input pin. Decouple this pin to GND with at least 4.7μF ceramic cap.
11 (Exposed Pad)	9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, PVIN, SVIN ---------- –0.3V to 6.5V
- Switch Node Voltage, SW ---------- –0.3V to 6.5V
- Switch Node Voltage, SW (<100ns) ---------- –2.5V to (V_{PVIN} + 0.3V)
- PVIN/SVIN to SW Voltage ---------- –0.3V to 6.5V
- PVIN/SVIN to SW Voltage (<100ns) ---------- –2.5V to (V_{IN}+ 0.3V)
- Other I/O Pin Voltage ---------- –0.3V to 6.5V
- Power Dissipation, PD @ TA = 25°C

  WDFN-10L 3x3 ---------- 1.429W

  SOP-8 (Exposed Pad) ---------- 1.333W
- Package Thermal Resistance (Note 3)

  WDFN-10L 3x3, θ_{JA} ---------- 70°C/W

  WDFN-10L 3x3, θ_{JC} ---------- 8.2°C/W

  SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W
- SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- −65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

  MM (Machine Model) ---------- 200V

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, PVIN, SVIN ---------- 2.7V to 5.5V
- Junction Temperature Range ---------- −10°C to 105°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{IN} = 5.5V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Voltage	V_{REF}		0.594	0.6	0.606	V
FB Pin Current	I_{FB}		--	0.1	0.4	μA
Quiescent Current	I_{Q_SW}	Active, V_{FB} = 0.7V, not switching	--	110	140	μA
Shutdown Current	I_{SHDN}		--	--	1	μA
Line Regulation	V_{LINE_REG}	V_{IN} = 2.7V to 5.5V, I_{OUT} = 0A	--	0.3	--	%/V
Load Regulation	V_{LOAD_REG}	(Note 6)	-1	--	1	%
Switch Leakage Current	I_{LEAK_SW}		--	--	1	μA
Switching Frequency	f_{SW}		0.8	1	1.2	MHz
On-Resistance of High-Side MOSFET	R_{DSON_H}		--	69	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}		--	49	--	mΩ
High-Side Switch (Peak) Current Limit	I_{LIM_H}		4	--	--	A
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}		2.2	2.4	2.6	V
Undervoltage-Lockout Falling Threshold	V_{UVLO_F}		2	2.2	2.4	V
EN Input Voltage Rising Threshold	V_{EN_R}		1.6	--	--	V
EN Input Voltage Falling Threshold	V_{EN_F}		--	--	0.4	V
EN Pull Low Resistance	R_{PD_EN}		--	500	--	kΩ
Over-Temperature Protection Threshold	T_{OTP}		--	150	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C
Soft-Start Time	t_{SS}		500	--	--	μs
Discharge Resistor	R_{DISCHG}		--	100	--	Ω
Output Overvoltage Rising Threshold	V_{OVP_R}	Latch-Off, Delay Time = 10μs	115	120	130	%
Output Undervoltage Falling Threshold	V_{UVP_F}	Latch-Off	57	66	75	%
Power-Good Voltage Threshold	V_{PG}	Measured FB pin, with respect to V_{REF}	85	90	--	%
Power-Good Voltage Hysteresis	V_{PG_HYS}		--	5	--	%

Note 6. Guaranteed by design.

13 Typical Application Circuit

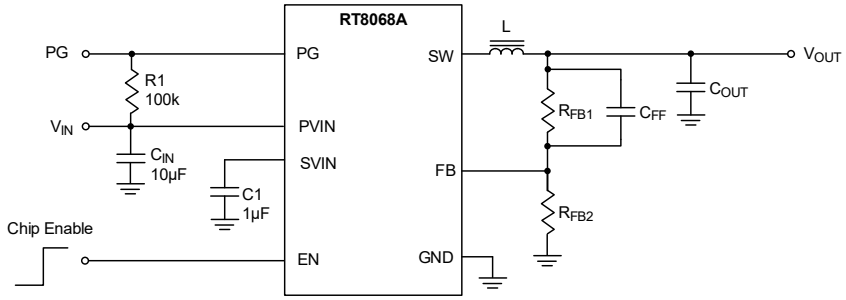


Figure 1. The Typical Application Circuit of the RT8068A

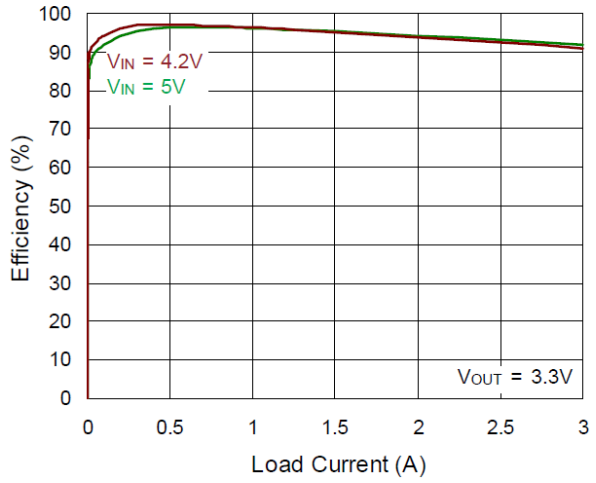
Table 1. Suggested Component Values

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	C_{FF} (pF)	L (µH)	C_{OUT} (µF)
3.3	229.5	51	22	2	22 x 2
2.5	161.5	51	22	2	22 x 2
1.8	1.05	51	22	1.5	22 x 2
1.5	76.5	51	22	1.5	22 x 2
1.2	51	51	22	1.5	22 x 2
1.0	34	51	22	1.5	22 x 2

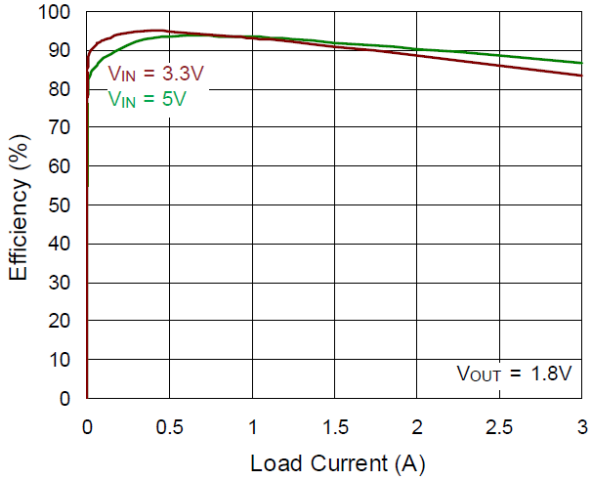
Note 7. All input and output capacitors are the suggested values, referring to the effective capacitances, which may be subject to any de-rating effect, like a DC bias.

14 Typical Operating Characteristics

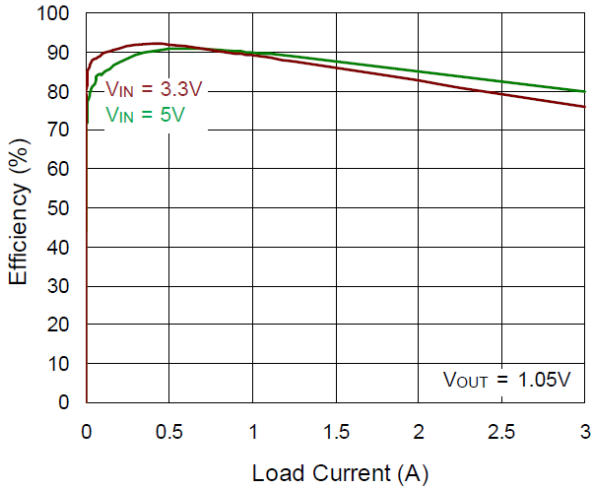
Efficiency vs. Load Current



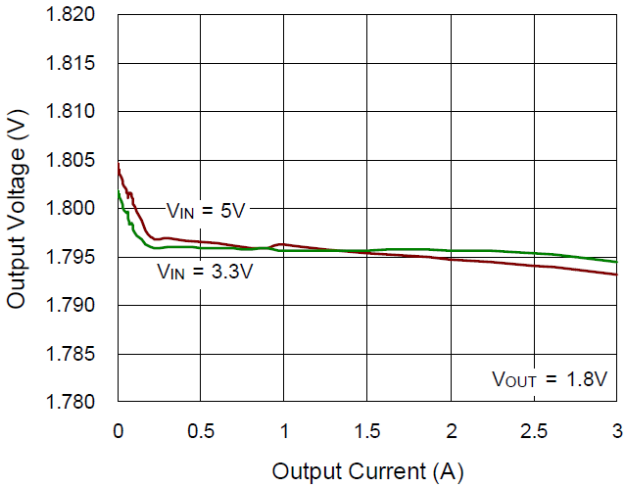
Efficiency vs. Load Current



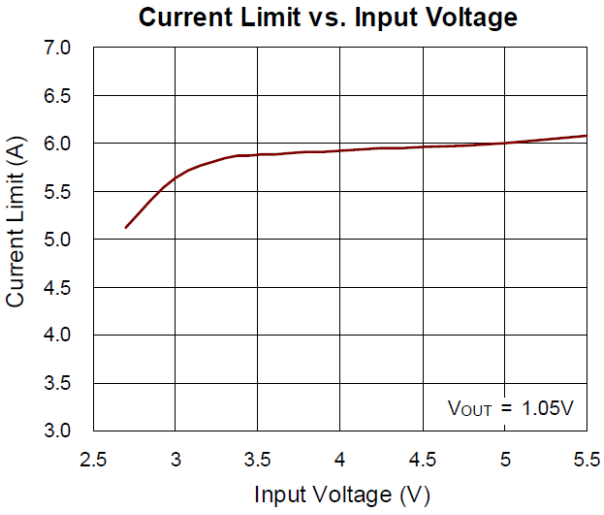
Efficiency vs. Load Current



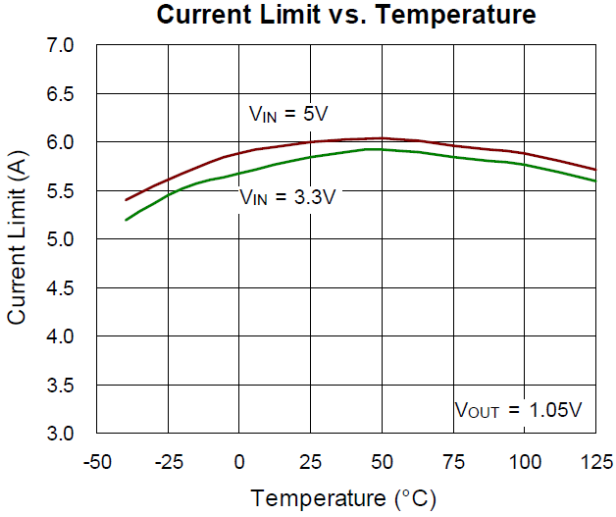
Output Voltage vs. Output Current



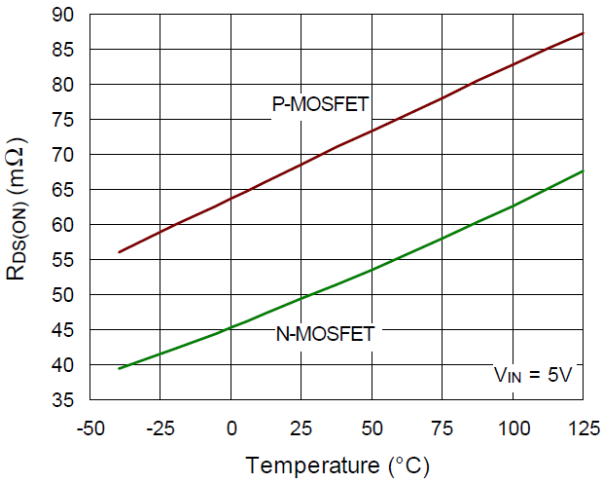
Current Limit vs. Input Voltage



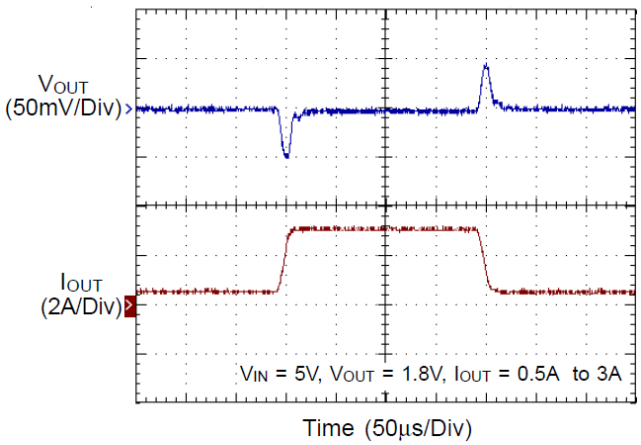
Current Limit vs. Temperature



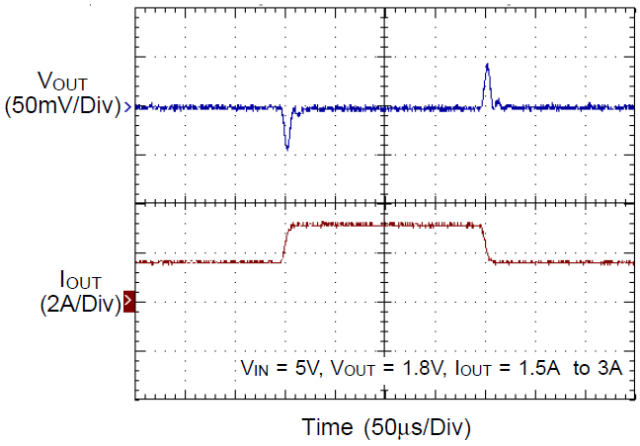
$R_{DS(ON)}$ vs. Temperature



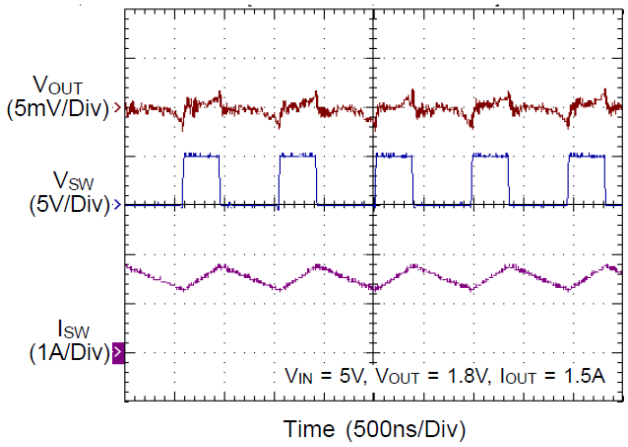
Load Transient Response



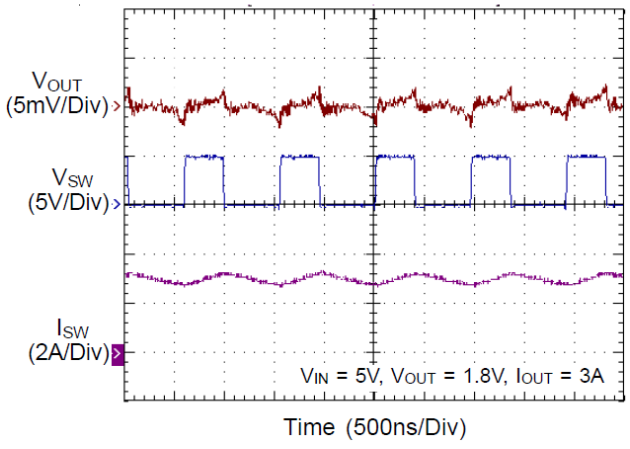
Load Transient Response



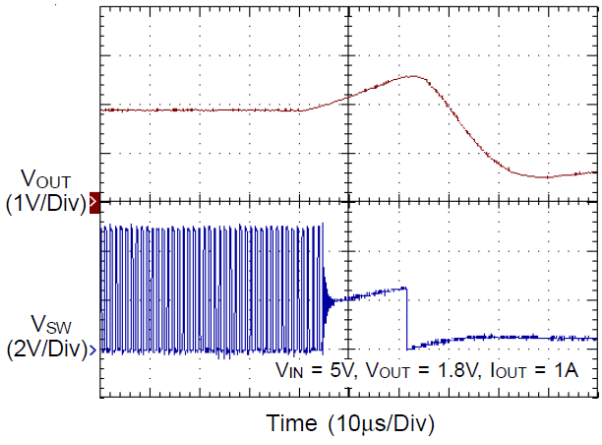
Switching



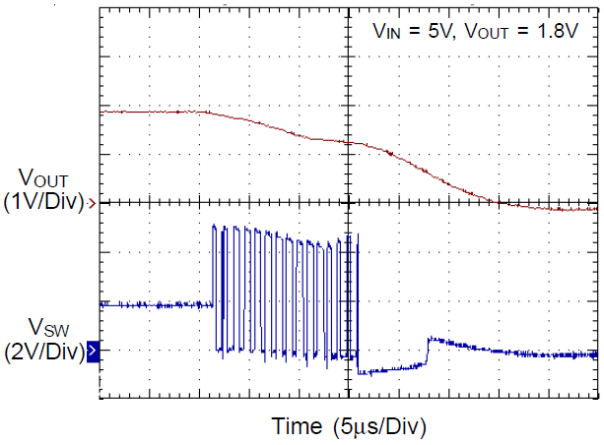
Switching



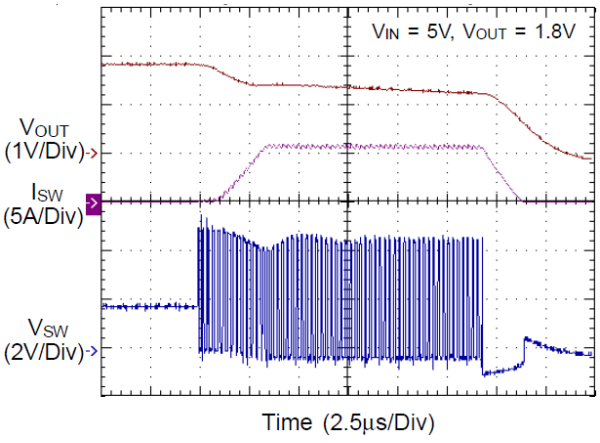
Over Voltage Protection



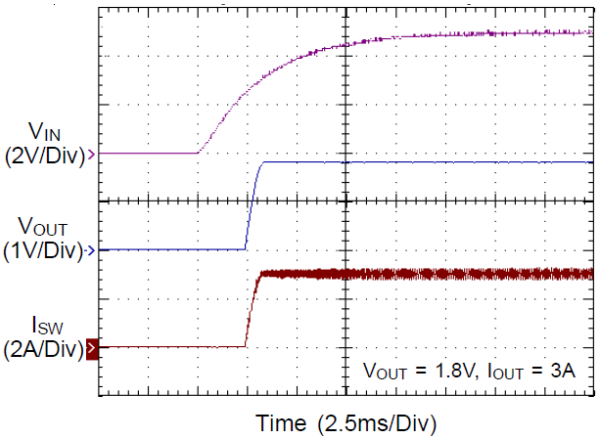
Under Voltage Protection



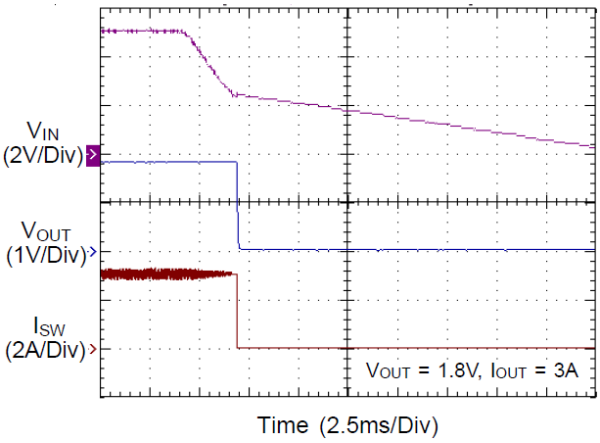
Over Current Protection



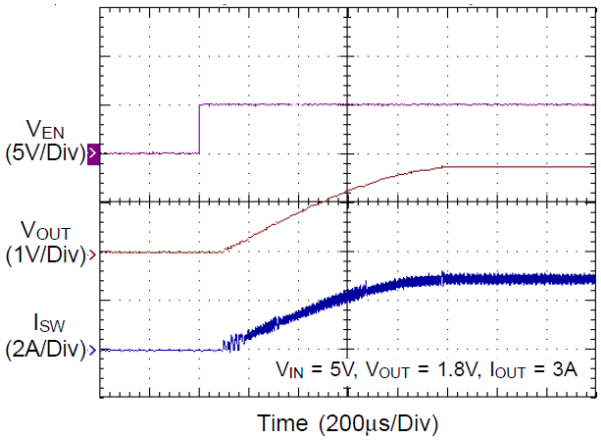
Power On from V_{IN}



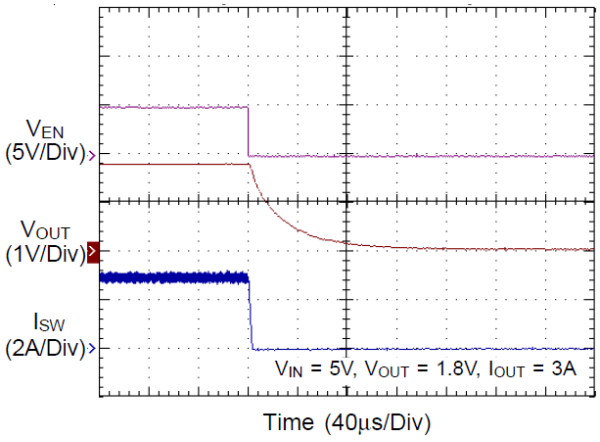
Power Off from V_{IN}



Power On from EN



Power Off from EN



15 Operation

The RT8068A is a single-phase buck converter. It provides single feedback loop, current mode control with fast transient response. An internal 0.6V reference allows the output voltage to be precisely regulated for low output voltage applications. A fixed switching frequency (1MHz) oscillator and internal compensation are integrated to minimize external component count. Protection features include overcurrent protection, undervoltage protection, overvoltage protection, and over-temperature protection.

15.1 Output Voltage Setting

Connect a resistive voltage divider at the FB between V_{OUT} and GND to adjust the output voltage. The output voltage is set according to the following equation:

$$V_{OUT} = V_{REF}\left(1+\frac{R1}{R2}\right)$$

where V_{REF} is 0.6V (typical).

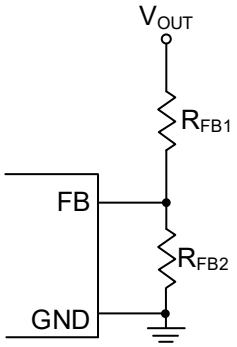


Figure 2. Setting VOUT with a Voltage Divider

15.2 Chip Enable and Disable

The EN pin allows for power sequencing between the controller bias voltage and another voltage rail. The RT8068A remains in shutdown if the EN pin is lower than 400mV. When the EN pin rises above the V_{EN} trip point, the RT8068A begins a new initialization and soft-start cycle.

15.3 Internal Soft-Start

The RT8068A provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During the soft-start, the internal soft-start capacitor becomes charged and generates a linear ramping up voltage across the capacitor. This voltage clamps the voltage at the FB pin, causing PWM pulse width to increase slowly and in turn reduce the output surge current. The internal 0.6V reference takes over the loop control once the internal ramping-up voltage becomes higher than 0.6V.

15.4 UVLO Protection

The RT8068A has input undervoltage lockout protection (UVLO). If the input voltage exceeds the UVLO rising threshold voltage (2.4V typical), the converter resets and prepares the PWM for operation. If the input voltage falls below the UVLO falling threshold voltage during normal operation, the device will stop switching. The UVLO rising and falling threshold voltage has a hysteresis to prevent noise-caused reset.

15.5 Power-Good Indicator (PG)

PG is an open-drain type output and requires a pullup resistor. PG is actively held low in soft-start, standby, and shutdown. It is released when the output voltage rises above 90% of nominal regulation point. The PG signal goes low if the output is turned off or is 10% below its nominal regulation point.

15.6 Undervoltage Protection (UVP)

The output voltage can be continuously monitored for undervoltage. When undervoltage protection is enabled, both UGATE and LGATE gate drivers will be forced low if the output voltage is less than 66% of its set voltage threshold. The UVP will be ignored for at least 3ms (typical) after startup or a rising edge on the EN threshold. Toggling EN threshold or cycle VIN resets the UVP fault latch and restarts the controller.

15.7 Overvoltage Protection (OVP)

The RT8068A is latched once OVP is triggered and can only be released by toggling EN threshold or cycling VIN. There is a 10μs delay built into the overvoltage protection circuit to prevent false transition.

15.8 Overcurrent Protection (OCP)

The RT8068A provides overcurrent protection by detecting high-side MOSFET peak inductor current. If the sensed peak inductor current is over the current-limit threshold (4A minimum), the OCP will be triggered. When OCP is tripped, the RT8068A will keep the overcurrent threshold level until the overcurrent condition is removed.

15.9 Internal Output Voltage Discharge

An internal open-drain logic output is implemented on the SW pin. During the conditions of OVP, UVP, OTP, and enable low, the internal discharge path is activated and the left energy from output terminal is able to be released with an internal resistance about 100Ω to ground.

15.10 Over-Temperature Protection (OTP)

The device implements an internal thermal shutdown function when the junction temperature exceeds 150°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal shutdown threshold. Once the die temperature decreases below the hysteresis of 20°C, the device reinstates the power up sequence.

16 Application Information

(Note 8)

16.1 Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher VIN and decreases with higher inductance.

$$\Delta I_L = \left(\frac{V_{OUT}}{f \times L}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of ΔI_L= 0.24(I_{MAX}) will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left(\frac{V_{OUT}}{f \times 0.24 \times I_{(max)}}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right)$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient temperature) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit.

16.2 Input Capacitor and Output Capacitor Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the Source of the high-side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The approximate RMS current equation is given:

$$I_{RMS} = I_{OUT(max)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at V_{IN} = 2xV_{OUT}, where I_{RMS} = I_{OUT}/2. The worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, two 10μF low ESR ceramic capacitors are suggested. The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8 \times f \times C_{OUT}}\right)$$

The output ripple will be the highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

16.3 Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA(EFFECTIVE)}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 (Exposed Pad) packages, the thermal resistance, θ_{JA}, is 75°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WDFN-10L 3x3 packages, the thermal resistance, θ_{JA}, is 70°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formulas:

$P_{D(MAX)}$ = (125°C – 25°C) / (75°C /W) = 1.333W for SOP-8 (Exposed Pad) package

$P_{D(MAX)}$ = (125°C – 25°C) / (70°C /W) = 1.43W for WDFN-10L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT8068A package, the derating curves in Figure 3 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

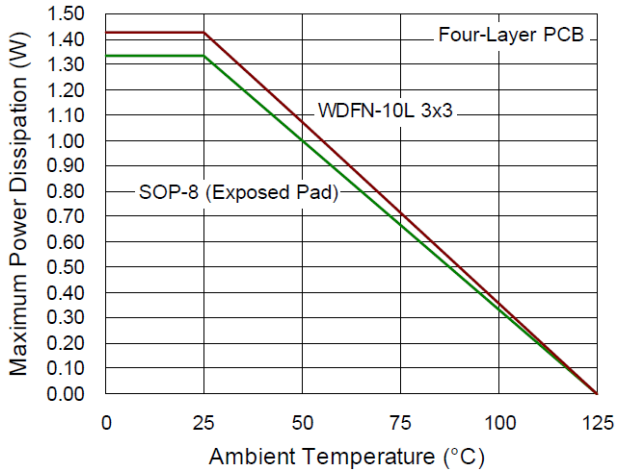


Figure 3. Derating Curves of Maximum Power Dissipation

16.4 Layout Considerations

Layout is very important in high frequency switching converter design. If designed improperly, the PCB can radiate excessive noise and contribute to the converter instability. The following points must be considered before starting a layout for the RT8068A.

- Make the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (PVIN, SVIN and GND).
- SW node encounters high frequency voltage swings so it should be kept in a small area. Keep sensitive components away from the SW node to prevent stray capacitive noise pick-up.
- Ensure all feedback network connections are short and direct. Place the feedback network as close to the chip as possible.
- The GND pin and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection.

An example of PCB layout guide is shown in Figure 4.

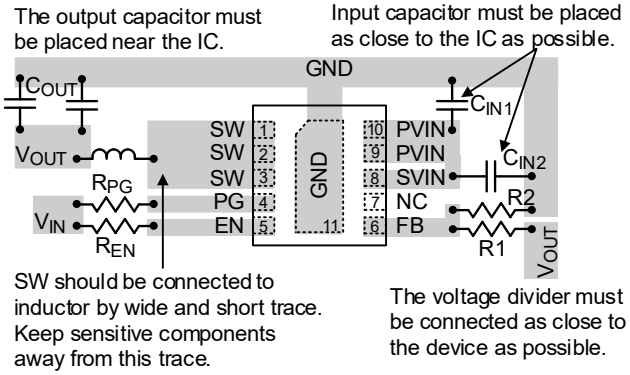
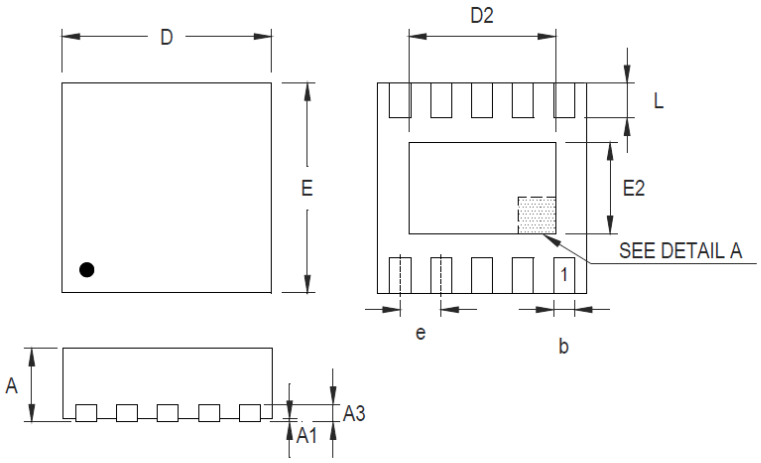


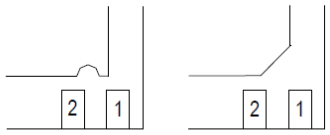
Figure 4. PCB Layout Guide

Note 8. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

17 Outline Dimension

17.1 WDFN-10L 3x3 Package





DETAIL A

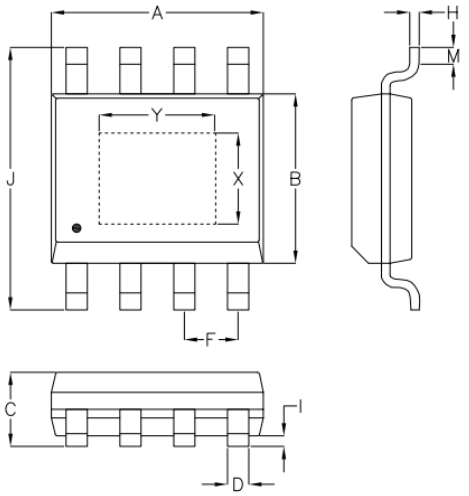
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

17.2 SOP-8 (Exposed Pad) Package



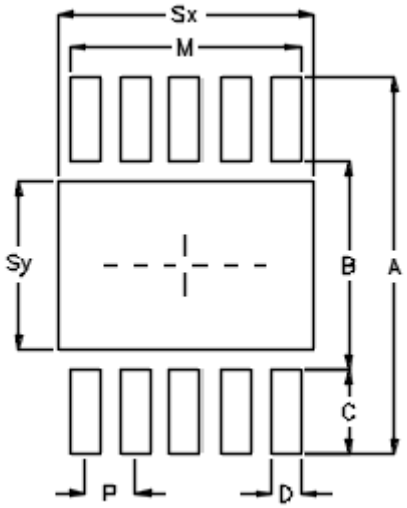
Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

Note 9. The package of the RT8068A uses Option 2.

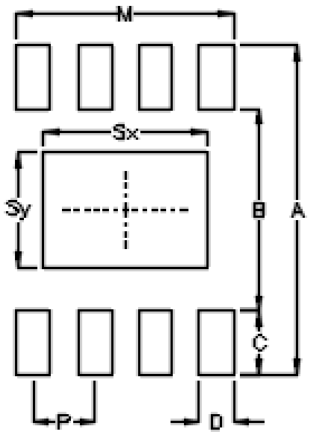
18 Footprint Information

18.1 WDFN-10L 3x3 Package



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/X/ZDFN3*3-10	10	0.50	3.80	2.10	0.85	0.30	2.55	1.70	2.30	±0.05

18.2 SOP-8 (Exposed Pad) Package



Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
PSOP-8	Option1	8	1.27	6.80	4.20	1.30	0.70	2.30	2.30	4.51	±0.10
	Option2							3.40	2.40		

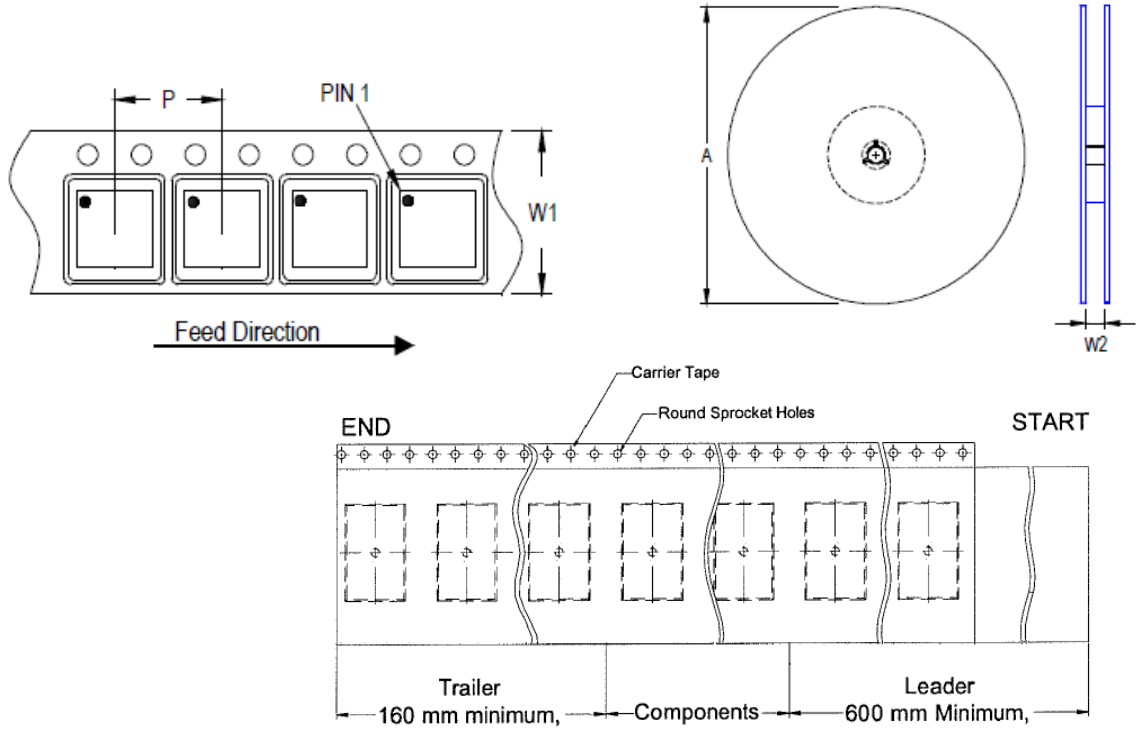
Note 10. The package of the RT8068A uses Option 2.

19 Packing Information

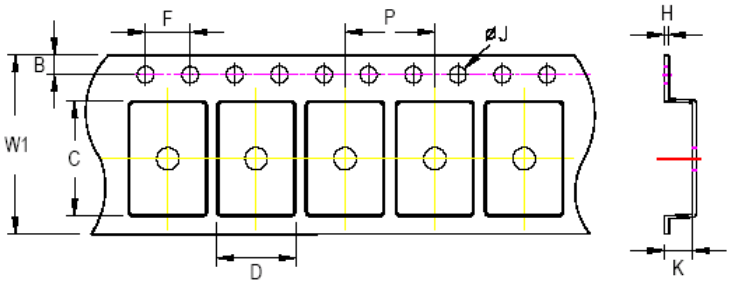
19.1 Tape and Reel Data

19.1.1 WDFN-10L 3x3 Package

19.1.1.1 Units per Reel: 1500



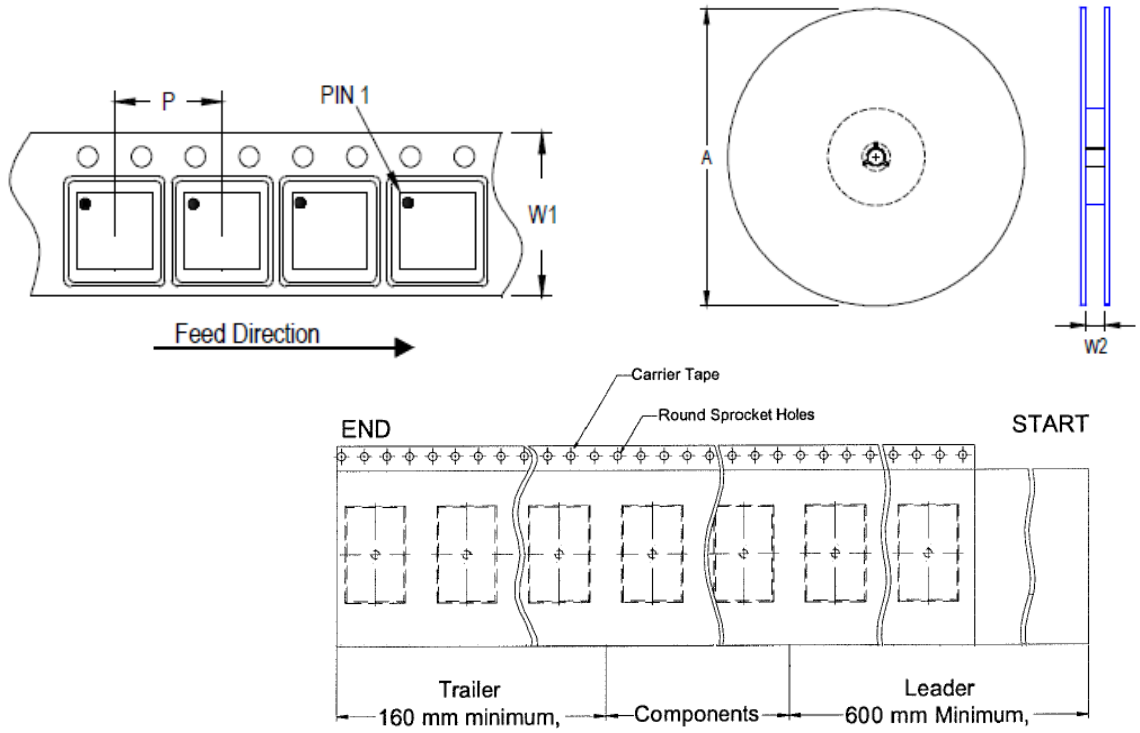
Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



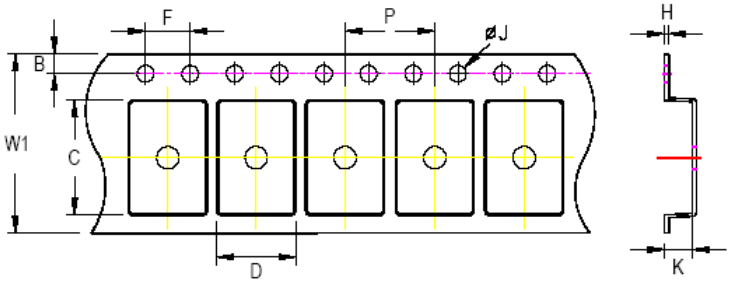
C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

19.1.1.2 Units per Reel: 2500



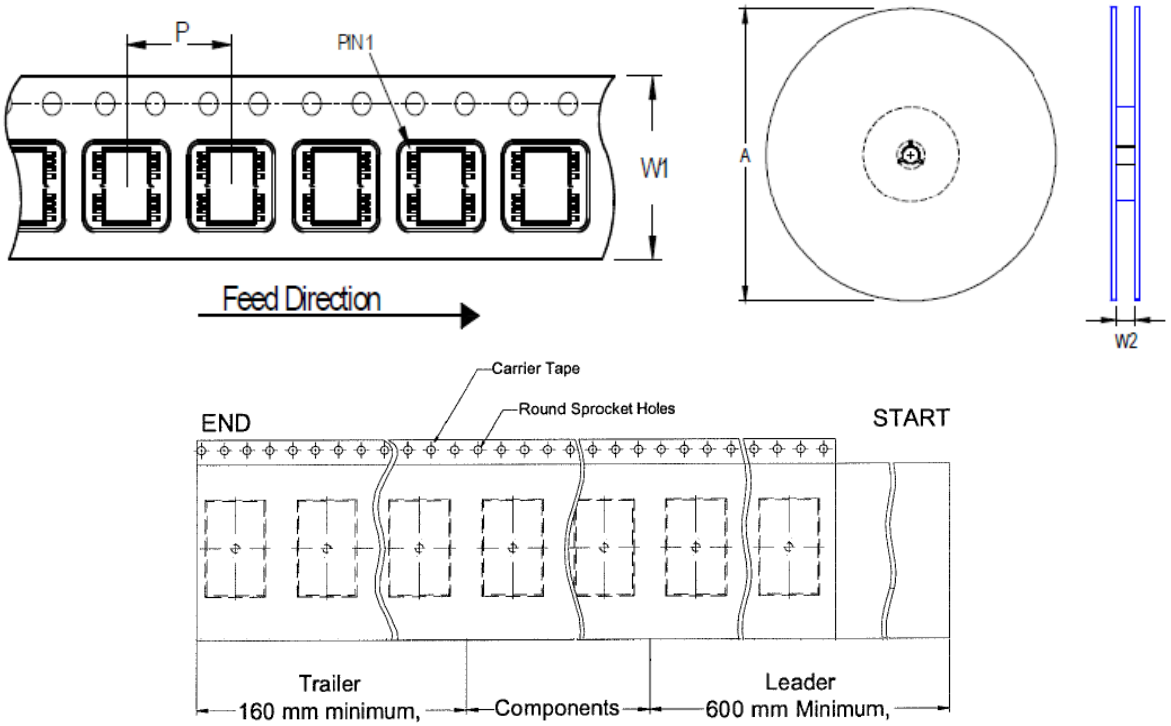
Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer(mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x3	12	8	330	13	2,500	160	600	12.4/14.4



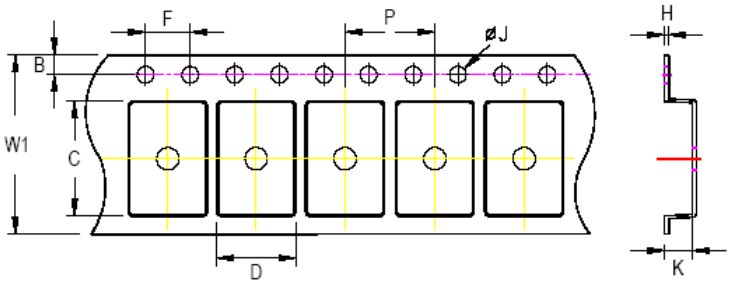
C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

19.1.2 SOP-8 (Exposed Pad) Package



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
PSOP-8	12	8	330	13	2,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.9mm	2.3mm	0.6mm

19.2 Tape and Reel Packing

19.2.1 WDFN-10L 3x3 Package

19.2.1.1 Units per Reel: 1500

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 3x3	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

19.2.1.2 Units per Reel: 2500

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
(V, W) QFN and DFN 3x3	13”	2,500	Box G	1	2,500	Carton A	6	15,000

19.2.1.3 SOP-8 (Exposed Pad) Package

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Package \ Container	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
PSOP-8	13”	2,500	Box G	1	2,500	Carton A	6	15,000

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Taiyuan 1st St., Zhubei City,
Hsinchu County 302082, Taiwan (R.O.C.)
Tel: 886-3-5526-789

20 Datasheet Revision History

Version	Date	Description
09	2025/10/1	Changed the names PGOOD to PG and LX to SW Changed the Step-Down to Buck Absolute Maximum Ratings