High Efficiency Dual-Channel Output Synchronous Buck PWM Controller with Phase Interleaving and Two LDO Regulators

General Description

The RT8127A is a high efficiency Dual-Channel output synchronous Buck PWM controller with integrated MOSFET drivers and two LDOs. This part features Green Voltage Mode (GVM^{TM}) control, which is specifically designed to improve efficiency at light load condition. At light load condition, the RT8127A is pin configurable to automatically operate in diode emulation mode with constant on-time PFM to reduce switching frequency so as to improve conversion efficiency. As the load current increases, the RT8127A leaves the diode emulation mode and operates in Continuous Conduction Mode (CCM) with fixed-frequency, 180° out of phase interleaved PWM to reduce input capacitance. The RT8127A supports 4.5V to 26V input voltage range and has integrated 5V LDO which supplies the internal gate drivers as well as the controller. When channel 1 Buck regulator output voltage is higher than 5V, the supply voltage will be automatically switched to the Buck regulator output from the integrated 5V LDO. The RT8127A supports enable/disable function for each channel and also features external soft-start, adjustable switching frequency and power good indication. This device utilizes lossless inductor DCR current sensing for over current protection. Other protections include over voltage, under voltage, thermal shutdown and under voltage lockout.

The RT8127A is available in a WQFN-28L 4x4 small footprint package.

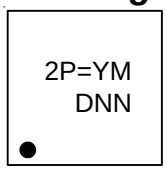
Features

- **Green Voltage Mode (GVM^{TM}) Control**
- **High Light Load Efficiency**
- **Audio-Skip Mode (ASM) at Light Load**
- **Pin Configurable CCM/DEM Operation**
- **180° Interleaving PWM in CCM Operation**
- **Support 4.5V to 26V Input Voltage Range**
- **Integrated 5V MOSFET Driver and Bootstrap Circuit**
- **Integrated 5V and 12V LDO**
- **Enable Control for Each Channel**
- **External/Internal Soft-Start**
- **Programmable LGATE PWM Frequency Setting (LGFS)**
- **Automatic Switchable 5V Regulator**
- **Power Good Indication**
- **VIN Feed-Forward in Control Loop**
- **Lossless DCR Current Sensing**
- **OVP, UVP, OCP, Thermal Shutdown and UVLO**
- **RoHS Compliant and Halogen Free**

Applications

- Motherboard, Server, Graphic Card
- System Power Supplies
- Power Module

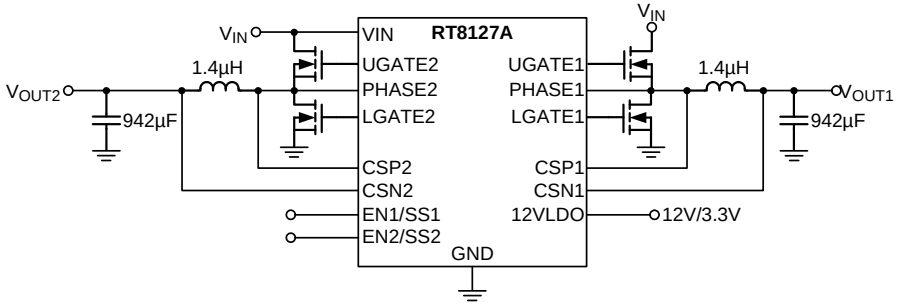
Marking Information



2P= : Product Code

YMDNN : Date Code

Simplified Application Circuit



Ordering Information

RT8127A □□

- Package Type
  QW : WQFN-28L 4x4 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

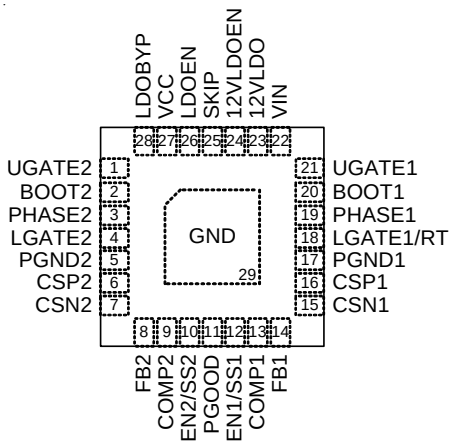
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)



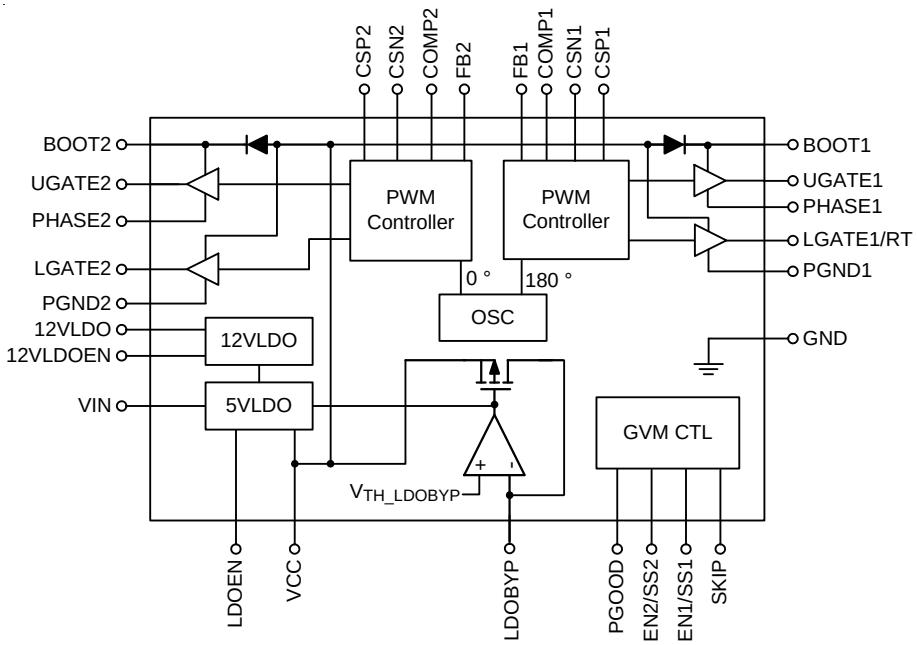
WQFN-28L 4x4

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	UGATE2	Channel 2 High Side MOSFET Floating Gate Driver Output. Connect this pin to the channel 2 high side MOSFET gate.
2	BOOT2	Channel 2 Bootstrap Flying Capacitor Connection Pin. This pin powers channel 2 high side MOSFET driver. Connect this pin to PHASE2 with a ceramic capacitor.
3	PHASE2	Channel 2 Switching Node Connection Pin. Connect this pin to the joint of high side MOSFET source and low side MOSFET drain, and the inductor of channel 2.
4	LGATE2	Channel 2 Low Side MOSFET Gate Driver Output. Connect this pin to the gate of channel 2 low side MOSFET.
5	PGND2	Power Ground of Channel 2. This pin is the return ground of channel 2 low side MOSFET gate driver. Connect this pin to the PCB ground plane layer with vias.
6	CSP2	Positive Current Sense Input for Channel 2.
7	CSN2	Negative Current Sense Input for Channel 2.
8	FB2	Channel 2 Regulator Output Voltage Feedback Pin. This pin is the inverting input node of the error amplifier.
9	COMP2	Channel 2 Regulator Compensation Pin. This pin is the output of the error amplifier.
10	EN2/SS2	Channel 2 Enable Pin. Pull this pin to ground to disable channel 2. This pin is internally pulled high. Leave this pin unconnected to enable channel 2 with default soft-start time. This pin can also be used for external soft-start interval setting. Connect a ceramic capacitor to this pin to extend soft-start time. The input voltage at EN2/SS2 pin must be higher than 2.97V to make sure soft-start can be finished and PGOOD assertion.
11	PGOOD	Power Good Indicator Output. This pin has an open drain structure. Pull this pin high to a voltage source with a resistor.
12	EN1/SS1	Channel 1 Enable Pin. Pull this pin to ground to disable channel 1. This pin is internally pulled high. Leave this pin unconnected to enable channel 1 with default soft-start time. This pin can also be used for external soft-start interval setting. Connect a ceramic capacitor to this pin to extend soft-start time. The input voltage at EN1/SS1 pin must be higher than 2.97V to make sure soft-start can be finished and PGOOD assertion.

Pin No.	Pin Name	Pin Function
13	COMP1	Channel 1 Regulator Compensation Pin. This pin is the output of the error amplifier.
14	FB1	Channel 1 Regulator Output Voltage Feedback Pin. This pin is the inverting input node of the error amplifier.
15	CSN1	Negative Current Sense Input for Channel 1.
16	CSP1	Positive Current Sense Input for Channel 1.
17	PGND1	Power Ground of Channel 1. This pin is the return ground of channel 1 low side MOSFET gate driver. Connect this pin to the PCB ground plane layer with vias.
18	LGATE1/RT	Channel 1 Low Side MOSFET Gate Driver Output. Connect this pin to the gate of channel 1 low side MOSFET. This pin is also used to set the PWM switching frequency in CCM. Connect a resistor from this pin to GND to set the PWM switching frequency.
19	PHASE1	Channel 1 Switching Node Connection Pin. Connect this pin to the joint of high side MOSFET source and low side MOSFET drain, and the inductor of channel 1.
20	BOOT1	Channel 1 Bootstrap Flying Capacitor Connection Pin. This pin powers channel 1 high side MOSFET driver. Connect this pin to PHASE1 with a ceramic capacitor.
21	UGATE1	Channel 1 High Side MOSFET Floating Gate Driver Output. Connect this pin to the gate of channel 1 high side MOSFET.
22	VIN	IC Power Supply Input. Connect this pin to a voltage source with a bypass ceramic capacitor connected to GND for noise decoupling. This pin is the power source of the two integrated LDOs.
23	12VLDO	12V LDO Output. It is recommended to connect a minimum 1μF ceramic capacitor from this pin to GND.
24	12VLDOEN	12V LDO Enable Pin. Logic-high at this pin enables the integrated 12V LDO.
25	SKIP	CCM/DEM Programming Pin. Voltage at this pin determines the operation mode in each channel. Connect this pin to GND : both of the channels are set to automatic CCM/DEM transition operation with audio-skip operation in DEM. Connect this pin to VCC : both of the channels are set to CCM operation. Leave this pin floating : channel 1 is set to automatic CCM/DEM transition operation with audio-skip operation in DEM and channel 2 is set to CCM operation.
26	LDOEN	5V LDO Enable Pin. Logic-high at this pin enables the integrated 5V LDO.
27	VCC	Integrated 5V LDO Output. It is recommended to connect a minimum 4.7μF ceramic capacitor between this pin and ground. VCC is the power supply for the control circuit and MOSFET drivers.
28	LDOBYP	5V LDO Bypass Input. Connect this pin to channel 1 regulator output (usually 5V). The LDOBYP pin voltage, V_{LDOBYP}, is monitored for controller supply power swap. When V_{LDOBYP} is higher than the threshold, the controller will automatically switch the chip power supply from 5V LDO to channel 1 output and disable the 5V LDO for power saving.
29 (Exposed Pad)	GND	Return Ground of Controller. The exposed pad must be soldered to a large PCB and connected to ground plane for maximum power dissipation.

Function Block Diagram



Operation

The RT8127A is a dual output voltage mode synchronous Buck controller with integrated MOSFET drivers and two LDOs. The 12VLDO output also can be stepped down to 3.3V by the controlling of 12VLDOEN pin.

The controller has a fixed frequency control with 180° phase shift in CCM. The fixed frequency can be adjusted from typical 300kHz to 600kHz.

The controller supports dynamic mode transition function with three operating states : forced CCM, Diode Emulation Mode (DEM) and audio skipping modes at light load.

Enable

The recommended ON / OFF control can tie the ENx to GND with a switch.

Under Voltage Lockout (UVLO)

During normal operation, if the voltage at the VCC pin drops below UVLO falling edge threshold. The VCC UVLO circuitry inhibits switching by keeping UGATEx and LGATEx low.

Over Current Protection (OCP)

The over current protection is triggered if the voltage difference between CSPx and CSNx over 40mV for 16 switching cycles. Both UGATEx and LGATEx will go low until VCC is resupplied and exceeds the POR rising threshold voltage.

Over Voltage Protection (OVP)

If the FBx voltage is higher than the OVP threshold (typically 120% x V_{REF}) during normal operation, OVP will be triggered. When OVP is triggered, UGATEx goes low and LGATEx is forced to high.

Under Voltage Protection (UVP)

If the FBx voltage is lower than the UVP threshold (typically 50% x V_{REF}) during normal operation, UVP will be triggered. When UVP is triggered, both UGATEx and LGATEx go low until VCC is resupplied and exceeds the POR rising threshold voltage.

PGOOD

PGOOD is actively held low in soft-start, standby, and shutdown conditions. It is released when both output voltages of VFB1 and VFB2 are within ±20% of the nominal regulation point.

LDOBYP

When V_{LDOBYP} is higher than the threshold, the controller will automatically switch the chip power supply from 5V LDO to channel 1 output and disable the 5V LDO for power saving.

Soft-Start

An internal current source charges the internal soft-start capacitor such that the internal soft-start voltage ramps up uniformly. The FB voltage will track the internal soft-start voltage during the soft-start interval.

The RT8127A also provides an external soft-start function. An additional capacitor connected at SSx pin will be charged by a 10μA current source and determines the soft-start time.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN ---------- –0.3V to 30V
- VCC, PVCC, LDOBYP ---------- –0.3V to 6V
- PGOOD ---------- –0.3V to 6V
- LDOEN ---------- –0.3V to 30V
- BOOT to PHASE ---------- –0.3V to 6V
- PHASE to GND
  - DC ---------- –0.7V to (V_{IN} + 0.3V)
  - <20ns ---------- –5V to 30V
  - <10ns ---------- –10V to 30V
  - <5ns ---------- –15V to 30V
- UGATE to GND
  - DC ---------- (V_{PHASE} – 0.3V) to (V_{BOOT} + 0.3V)
  - <20ns ---------- (V_{PHASE} – 5V) to (V_{BOOT} + 5V)
- LGATE to GND
  - DC ---------- (GND – 0.3V) to (VCC + 0.3V)
  - <20ns ---------- (GND – 5V) to (VCC + 5V)
- Other Pins ---------- (GND – 0.3V) to 6V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-28L 4x4 ---------- 3.5W
- Package Thermal Resistance (Note 2)
  - WQFN-28L 4x4, θ_{JA} ---------- 28.5°C/W
  - WQFN-28L 4x4, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VIN ---------- 4.5V to 26V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
General						
VIN Supply Voltage	V_{IN}		4.5	12	26	V
VIN Supply Current	I_{VIN}		--	2	--	mA
VCC Power On Reset	V_{POR}		--	4.2	--	V
VCC POR Hysteresis	ΔV_{POR}		--	0.3	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Current	I_{VIN_SHDN}	EN1, EN2, LDOEN, 12VLDOEN = 0V	--	--	5	μA
		EN1, EN2, LDOEN = 0V, 12VLDOEN = 5V / 2.5V	--	100	150	
Standby Current	I_{VIN_SBY}	EN1, EN2 = 0V, LDOEN = 5V, 12VLDOEN = 5V / 2.5V	--	350	400	μA
		EN1, EN2 = 0V, LDOEN = 5V, 12VLDOEN = 0V	--	300	350	
5V LDO						
Output Voltage Regulation	V_{CC}	V_{IN} = 12V, Load Current = 100mA	4.9	5	5.15	V
Current Capability	I_{VCC_SRC}		60	--	--	mA
LDOBYP						
LDOBYP Threshold	V_{TH_LDOBYP}		4.8	4.9	5	V
LDOBYP Hysteresis	ΔV_{TH_LDOBYP}		--	0.1	0.25	V
LDOBYP Internal Switch On-Resistance	R_{LDOBYP}		--	--	1	Ω
12V LDO						
Source Current Capability	I_{12VLDO}		25	--	--	mA
Voltage Regulation for 12V Output	V_{12VLDO}	V_{IN} = 15V, Load Current = 25mA	11.4	12	12.6	V
Voltage Regulation for 3.3V Output	$V_{3.3VLDO}$	V_{IN} = 15V, Load Current = 25mA	3.1	3.3	3.5	V
Enable Control						
EN1/EN2 Threshold	V_{EN}		0.58	0.68	0.78	V
EN1/EN2 Hysteresis	ΔV_{EN}		--	78	--	mV
LDOEN Threshold	V_{TH_LDOEN}		1.4	1.6	1.8	V
LDOEN Hysteresis	ΔV_{TH_LDOEN}		--	0.2	--	V
12VLDOEN Input for 3.3V Output	$V_{TH\_12VLDOEN\_3.3V}$	12VLDO Output = 3.3V	2	2.5	3	V
12VLDOEN Input for 12V Output	$V_{TH\_12VLDOEN\_12V}$	12VLDO Output = 12V	4.5	5	5.5	V
12VLDOEN Disable	$V_{TH\_12VLDOEN}$		--	--	0.4	V
PGOOD						
PGOOD Threshold	V_{PGOOD}	With Respect to V_{REF}	80	--	120	%
Error Amplifier						
Open Loop Gain	A_{OL}	(Note 5)	--	80	--	dB
Gain Bandwidth	GBW	(Note 5)	--	15	--	MHz
Slew Rate	SR	COMP Pin to GND with 10pF	--	2	--	V/μs
Reference Voltage						
Reference Voltage	V_{REF}		792	800	808	mV
PWM Controller						
Switching Frequency	f_{SW}	R_{LGFS} = 1.8k	255	300	345	kHz
		R_{LGFS} = 4.7k	297	350	402	
		R_{LGFS} = 9.1k	340	400	460	
		R_{LGFS} = 16k	510	600	690	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Duty Cycle		D_{MAX}		80	--	--	%
Ramp Amplitude		ΔV_{OSC}	V_{IN} = 12V	--	2.4	--	V
Ramp Valley		$V_{RAMPOFS}$		--	0.8	--	V
PWM Clock Interleaving			CCM Operation (Note 5)	--	180	--	Deg
MOSFET Driver							
UGATE Driver Source		$R_{UGATEsr}$	$V_{BOOT} - V_{PHASE}$ = 5V	--	2.5	--	Ω
UGATE Driver Sink		$R_{UGATEsk}$		--	1.5	--	Ω
LGATE Driver Source		$R_{LGATEsr}$		--	2	--	Ω
LGATE Driver Sink		$R_{LGATEsk}$		--	1	--	Ω
Deadtime between UGATE Off and LGATE On			CCM Operation	--	40	--	ns
Deadtime between LGATE Off and UGATE On			CCM Operation	--	20	--	ns
Embedded Bootstrap Diode Voltage Drop		V_{DROP}	Current = 10mA	--	0.8	--	V
Soft-Start							
Internal Soft-Start Time		t_{SS}		6	9	--	ms
Soft-Stop Resistance		R_{PL}	Enabled when EN = L, measure CSN1/CSN2 resistance	--	--	80	Ω
SKIP Pin							
SKIP Input Threshold Voltage	Logic-High	V_{IH}	CH1 and CH2 : CCM	3.6	--	--	V
	Logic-Low	V_{IL}	CH1 and CH2 : Automatic CCM/DEM	--	--	1.4	
Audio Skip Mode PWM Frequency		f_{SW_ASM}		--	30	--	kHz
Protection							
Over Voltage Protection		V_{OVP}	After VCC POR, with Respect to V_{REF}	110	120	130	%
Under Voltage Protection		V_{UVP}	After Soft-Start, with Respect to V_{REF}	--	50	--	%
UVP Delay		t_{D_UVP}		1.4	2	--	ms
OCP Threshold Voltage		V_{OCP}	Measure $V_{ISP} - V_{ISN}$	35	40	45	mV
Short Circuit OCP Threshold Voltage		V_{SCP}	Measure $V_{ISP} - V_{ISN}$	--	60	--	mV
Thermal Shutdown Temperature		T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	40	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

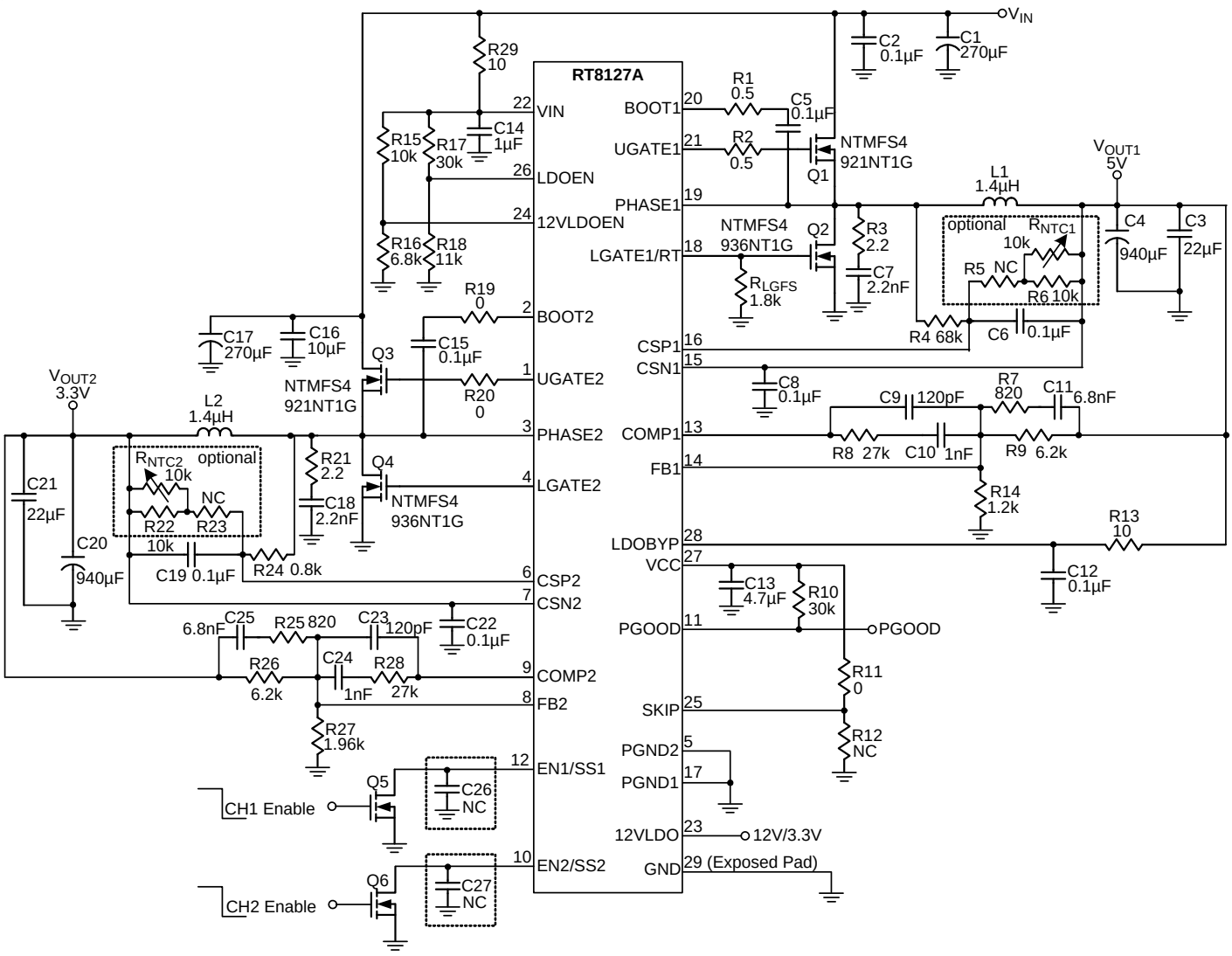
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

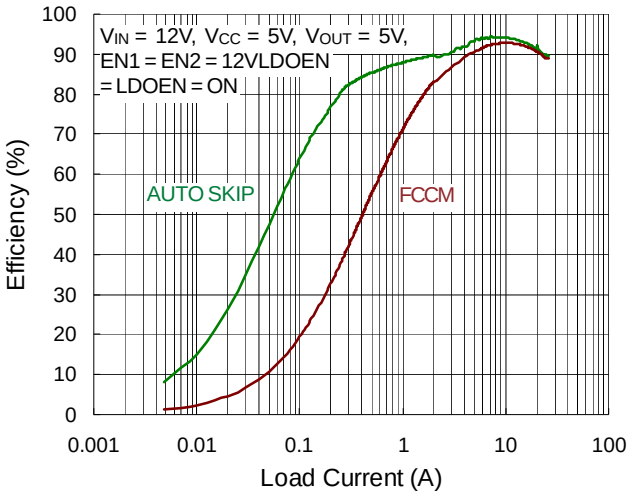
Note 5. Guaranteed by design.

Typical Application Circuit

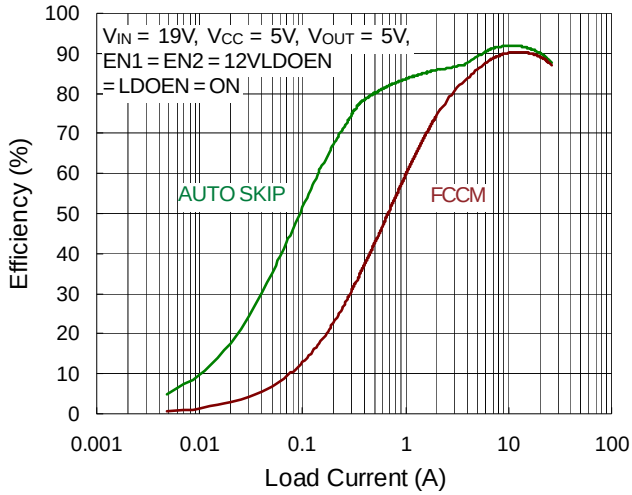


Typical Operating Characteristics

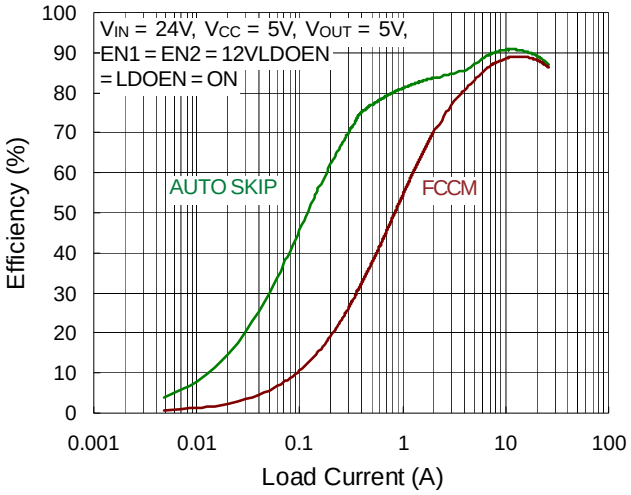
Efficiency vs. Load Current



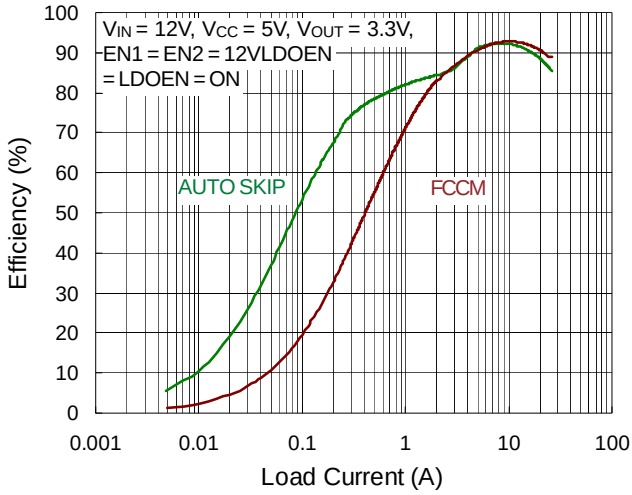
Efficiency vs. Load Current



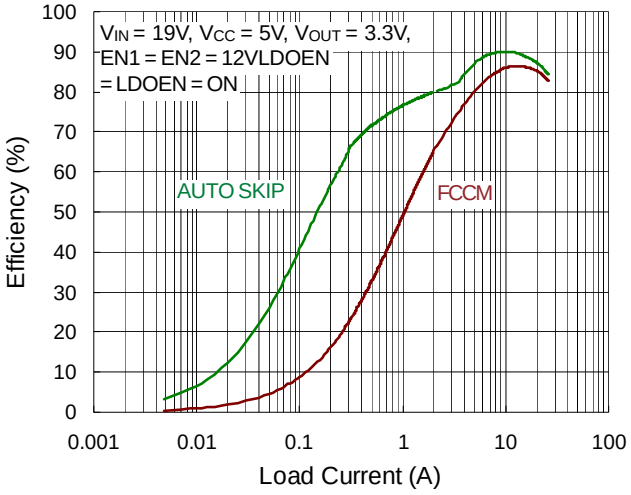
Efficiency vs. Load Current



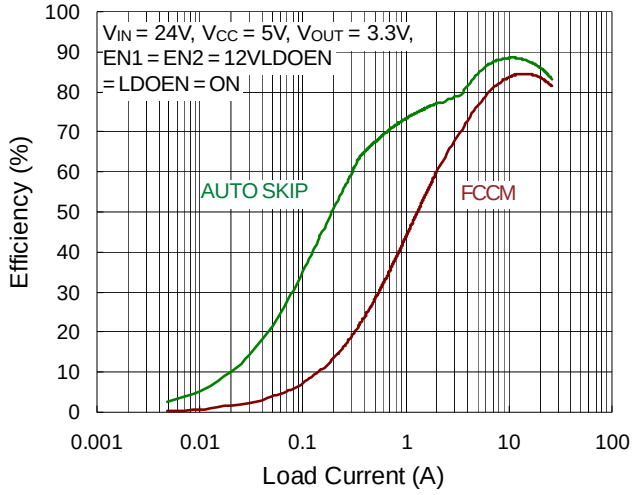
Efficiency vs. Load Current



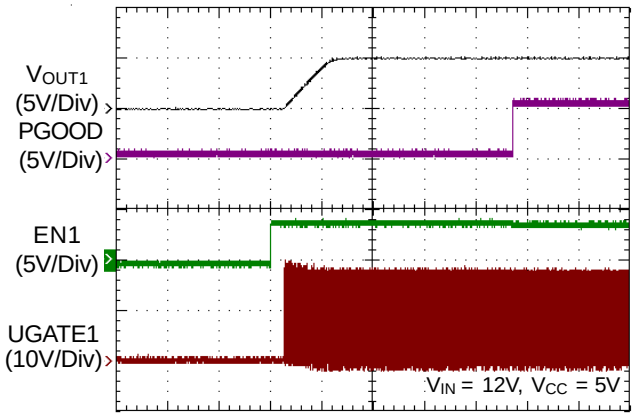
Efficiency vs. Load Current



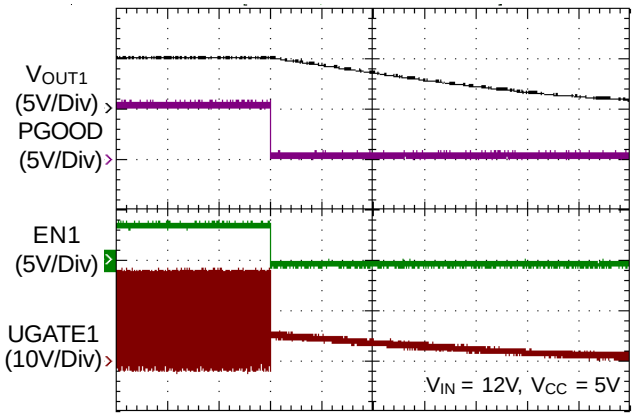
Efficiency vs. Load Current



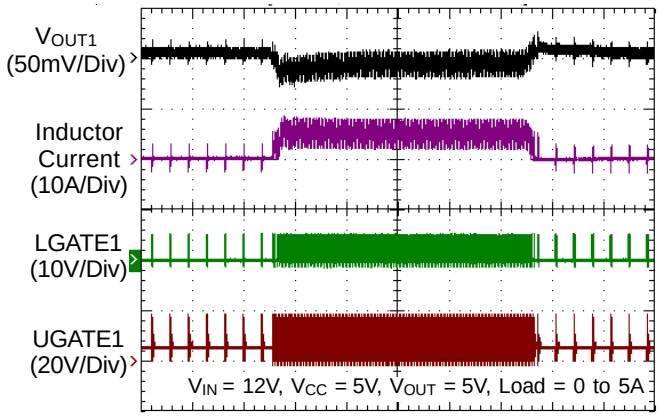
Power Up



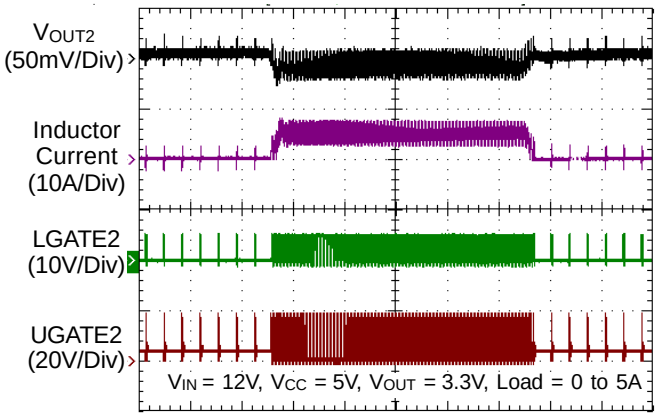
Shutdown Response



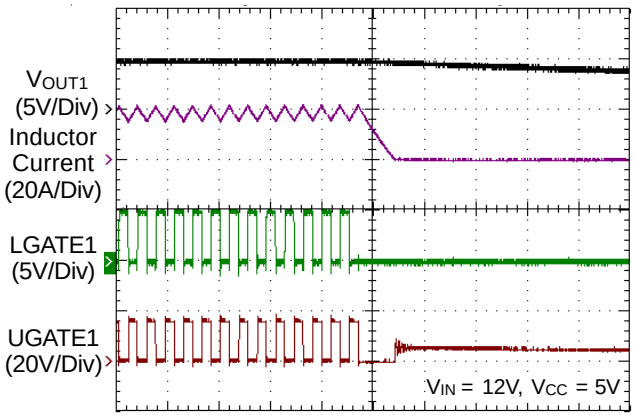
VOUT1 Load Transient Response



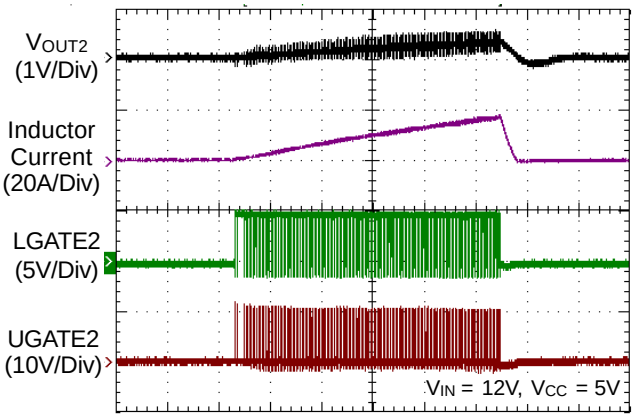
VOUT2 Load Transient Response



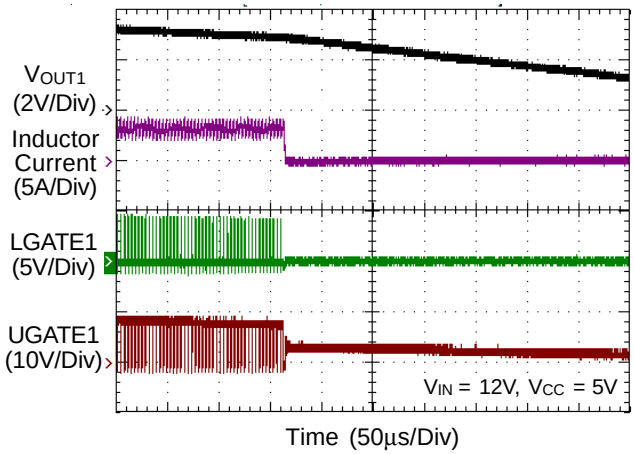
OCP



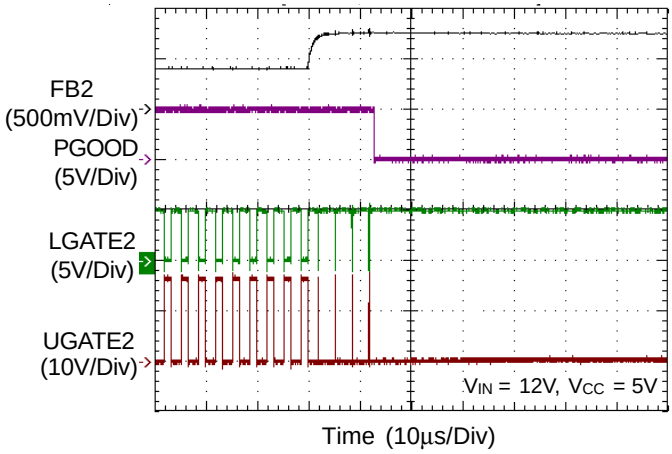
Shorted Start Up



UVP



OVP



Application Information

The RT8127A is a dual output voltage mode synchronous Buck controller with integrated MOSFET drivers and two LDOs. It is suited to 5V/3.3V low voltage power supplies with demanding high efficiency and fast transient response, such as graphic card and motherboard. The internal linear regulators named 5VLDO and 12VLDO respectively provides 5V and 12V outputs. The internal circuitry and gate drivers can be supplied by the 5VLDO or the output of 5V channel. When the output voltage of 5V channel is above 4.85V, the 5VLDO will be turned off and the device is supplied by the output of 5V channel.

The RT8127A supports dynamic mode transition function with three operating states: forced CCM, Diode Emulation Mode (DEM) and audio skipping modes at light load. These different operating states improve the system efficiency as high as possible. The RT8127A has a fixed frequency control with 180° phase shift in CCM. The fixed frequency can be adjusted from typical 300kHz to 600kHz by the external resistor R_{LGFS}.

Operation Mode Selection

The SKIP pin is used to select the operation mode. When the SKIP pin is tied to VCC, both of the channels operate in forced-CCM mode. When the SKIP pin is connected to GND, both of the channels operate in automatic CCM/DEM and transition operation with audio-skip mode in DEM. When the SKIP pin is floating, channel 1 operates in automatic CCM/DEM and transition operation with audio-skip mode in DEM, and channel 2 operates in forced-CCM mode.

Diode-Emulation Mode

In Diode Emulation Mode, the RT8127A automatically reduces switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly. As the output current decreases from heavy-load condition, the inductor current is also reduced, and eventually comes to the point that its current valley touches zero, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low side MOSFET allows only partial negative current to flow when the inductor free wheeling current becomes negative. As the load current is further decreased, it takes longer and longer time to discharge the output capacitor to the level that requires the next "ON" cycle. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction.

The transition load point to the light load operation is shown in Figure 1 and can be calculated as follows :

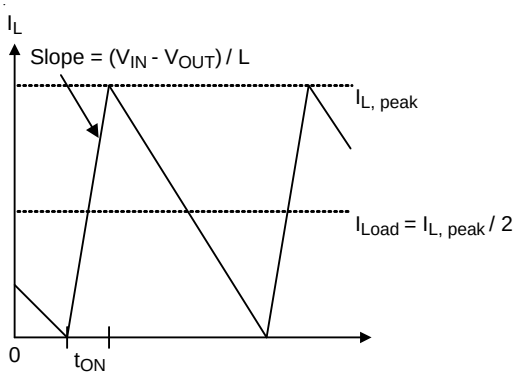


Figure 1. Boundary of Inductor current between DEM and CCM

$$I_{Load\ (SKIP)} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is the on-time.

Audio Skip Mode

The RT8127A activates a unique type of Diode Emulation Mode with a minimum switching frequency of 30kHz, called Audio Skip Mode. This mode eliminates audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In Audio Skip Mode, the low side switch gate driver signal is "OR"ed with an internal oscillator (>30kHz). Once the internal oscillator is triggered, the ultrasonic controller pulls LGATEx high and turns on the low side MOSFET to induce a negative inductor current. After the output voltage falls below the reference voltage, the controller turns off the low side MOSFET (LGATEx pulled low) and triggers a constant on-time (UGATEx driven high). When the on-time has expired, the controller re-enables the low side MOSFET until the controller detects that the inductor current dropped below the zero crossing threshold.

Forced-CCM Mode

The low noise, forced-CCM mode (SKIP = VCC) disables the zero-crossing comparator, which controls the low side switch on-time. This causes the low side gate-driver waveform to become the complement of the high side gate-driver waveform. This in turn causes the inductor current to reverse at light loads as the PWM loop strives to maintain a duty ratio of VOUT/VIN. The benefit of forced-CCM mode is to keep the switching frequency fairly constant, but it comes at a cost : The no-load current will slightly increase, depending on the external MOSFET(s), reference and linear regulators.

MOSFET Gate Driver

The high side driver is designed to drive high current, low R_{DS}(on) N-MOSFET(s). When configured as a floating driver, 5V bias voltage is delivered from 5VLDO supply. The average drive current is also calculated by the gate charge at V_{GS} = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between BOOTx and PHASEx pins. A dead time to prevent shoot through is internally generated between high side MOSFET off to low side MOSFET on, and low side MOSFET off to high side MOSFET on. The low side driver is designed to drive high current low R_{DS}(on) N-MOSFET(s). The internal pull-down transistor that drives LGATEx low is robust, with a 0.6Ω typical on resistance. A 5V bias voltage is delivered from 5VLDO supply. For high current applications, some combinations of high and low side MOSFET(s) may cause excessive gate-drain coupling, which can lead to efficiency-killing and EMI producing shoot-through currents. This is often remedied by adding a resistor in series with BOOTx, which increases the turn-on time of the high side MOSFET without degrading the turn-off time.

Enable

The RT8127A provides external soft-start function and enables control through the ENx pin.

The internal soft-start function or external soft-start function will be chosen according to the slew rate of the ENx pin voltage. If the slew rate of ENx pin voltage is slower than the slew rate of internal soft-start ramp, the external soft-start function will be chosen. The external soft-start sequence is shown in Figure 2. During soft-start period, the FB voltage will track the reference voltage V_{REF} that slew rate is according to the slew rate of the ENx pin voltage. In order to prevent LGATEx turn on for a long time to induce violent inductor current, shutting down from ENx should be avioded during soft-start period, if it is necessary, the falling slew rate of the ENx pin voltage should not slower than 1V/ μs and the recommended inductor should be higher than 1μH. As the PGOOD signal goes high, the VREF behavior is independent with the slew rate of ENx. Until the ENx voltage drops below the EN shutdown threshold, the RT8127A is shut down, and then the RT8127A turns off UGATEx and LGATEx simultaneously.

The recommended ON / OFF control is to connect the ENx to GND with a MOSFET. If the external source is directly connected to the ENx pin to control ON / OFF, the external source must be higher than 2.97V to make sure soft-start can be finished and PGOOD assertion.

The enable logic states are shown in Table1. When LDOEN is Low, both VOUT1 and VOUT2 will shut down even though EN1 or EN2 are ON state. When LDOEN is ON state, VOUT1 and VOUT2 are controlled independently by EN1 and EN2. The 12VLDO stays alive only consider if 12VLDOEN is ON state.

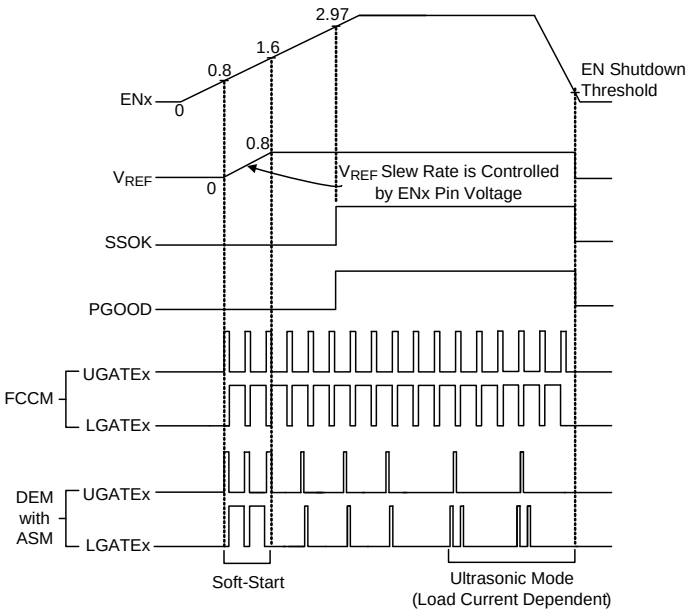


Figure 2. External Soft-Start Sequence

Table1. Enable Logic States

12VLDOEN	5VLDOEN	EN1	EN2	12VLDO	5VLDO	VOUT1	VOUT2
L	L	X (don't care)	X (don't care)	OFF	OFF	OFF	OFF
H	L	X (don't care)	X (don't care)	ON	OFF	OFF	OFF
L/H	H	L	L	OFF/ON	ON	OFF	OFF
L/H	H	H	L	OFF/ON	ON	ON	OFF
L/H	H	L	H	OFF/ON	ON	OFF	ON
L/H	H	H	H	OFF/ON	ON	ON	ON

Soft-Start

The RT8127A provides an internal soft-start function. The soft-start function is used to prevent large inrush current and output voltage overshoot while the converter is being powered up. The soft-start function automatically begins once the chip is enabled. An internal current source charges the internal soft-start capacitor such that the internal soft-start voltage ramps up uniformly. The FB voltage will track the internal soft-start voltage during the soft-start interval. The PWM pulse width increases gradually to limit the input current. After the internal soft-start voltage exceeds the reference voltage, the FB voltage no longer tracks the soft-start voltage but rather follows the reference voltage. Therefore, the duty cycle of the UGATE signal as well as the input current at power up are limited.

The RT8127A also provides a proximate external soft-start function shown in Figure 3. An additional capacitor connected from ENx/SSx pin to the GND will be charged by a 10μA current source and determines the soft-start time.

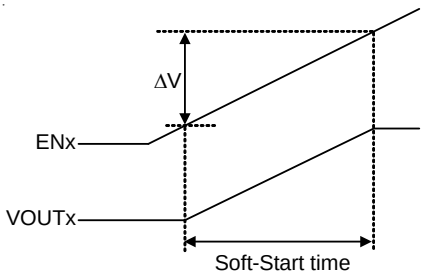


Figure 3. External Soft-Start

The soft-start time can be calculated as :

$$t_{SS} = \frac{(C \times \Delta V)}{I_{SS}}$$

Where, I_{SS} = 10μA, ΔV = 1V, and C is the external capacitor placed from ENx/SSx to GND. The recommend C is 0.15μF to 0.2μF.

Supply Voltage and Power On Reset (POR)

VCC is the power supply for the control circuit and MOSFET driver. An internal linear regulator regulates the supply voltage for internal control logic circuit. A minimum 0.1μF ceramic capacitor is recommended to bypass the supply voltage. Place the bypassing capacitor physically near the IC. VCC also supplies the integrated MOSFET drivers. A bootstrap diode is embedded to facilitate PCB design and reduce the total BOM cost. No external Schottky diode is required in real applications. The Power On Reset (POR) circuit monitors the supply voltage at the VCC pin. If VCC exceeds the POR rising threshold voltage (typ. 4.2V), the controller resets and prepares the PWM for operation. If VCC falls below the POR falling threshold during normal operation, all MOSFET(s) stop switching. The POR rising and falling threshold has a hysteresis (typ. 0.3V) to prevent unintentional noise based reset.

Low Dropout Regulators (LDOx)

The RT8127A includes 5V and 12V low dropout regulators. The 5V regulator can supply up to 60mA for external loads. Bypass LDOx with a minimum 1μF ceramic capacitor. When the output voltage of 5V channel is higher than the switch over threshold (4.85V), an internal 1Ω P-MOSFET switch connects LDOBYP to the 5VLDO pin while simultaneously disconnects the internal linear regulator.

The 12VLDO output can be stepped down to 3.3V by connecting 12VLDOEN pin to 2V to 3V.

Under Voltage Lockout (UVLO)

During normal operation, if the voltage at the VCC pin drops below UVLO falling edge threshold.

The VCC Under Voltage Lockout (UVLO) circuitry inhibits switching by keeping UGATEx and LGATEx low.

Power Good Output (PGOOD)

PGOOD is an open-drain output and requires a pull up resistor. PGOOD is actively held low in soft-start, standby, and shutdown. It is released when both output voltages are within ±20% of the nominal regulation point for RT8127A.

The PGOOD delay time is from FB exceeding 80% of VREF to PGOOD rising high, the delay time is around 3 times the soft-start time t_{SS}.

Current Sensing

The CSPx and CSNx denote the positive and negative input of the current sense amplifier. Users can either use a current sense resistor or the inductor's DCR for current sensing. Using inductor's DCR allows higher efficiency as shown in Figure 4.

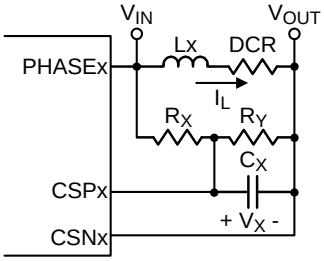


Figure 4. Lossless Inductor Sensing

The sensing voltage V_X can be set as :

$$V_X = \frac{R_Y}{R_X + R_Y} \times I_L \times DCR$$

Then the value of R_X, R_Y and C_X can be calculated as :

$$\frac{L_X}{DCR} = (R_X \,//\, R_Y) \times C_X$$

Over Current Protection

The Over Current Protection (OCP) of RT8127A is detected from the inductor current sensing for good accuracy. Therefore, the controller can be less noise sensitive. The over current protection is triggered if the voltage difference between CSPx and CSNx exceeds 40mV for continuous 16 switching cycles. Once the OCP is triggered, both of the UGATE and LGATE will go low until VCC is resupplied and exceeds the POR rising threshold voltage.

Except the OCP function described above, the controller provides Short Circuit Protection (SCP) function. Since short circuit may cause catastrophic damage over a very short period, the SCP should be triggered with a very short delay and latched. Also to prevent false triggering, the SCP threshold is designed to be 1.5 times of OCP threshold.

The over current threshold of inductor peak current (I_{LPK_OC}) and load current (I_{LOAD_OC}) can be calculated by the following equations :

$$I_{LPK\_OC} = \frac{V_{X\_OC}}{DCR} \times \frac{R_X + R_Y}{R_Y}$$

Where V_{X_OC} = 40mV

$$I_{LOAD\_OC} = I_{LPK\_OC} - \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L_X \times V_{IN} \times f_{SW}}$$

Over Voltage Protection (OVP)

The voltage on the FBx pin is monitored for over voltage protection. If the FBx voltage is higher than the OVP threshold (typically 120% x V_{REF}) during normal operation, OVP will be triggered. When OVP is triggered, UGATEx goes low and LGATEx is forced high. The controller is latched until VCC is resupplied and exceeds the POR rising threshold voltage.

Under Voltage Protection (UVP)

The voltage on the FBx pin is also monitored for under voltage protection. If the FBx voltage is lower than the UVP threshold (typically 50% x V_{REF}) during normal operation, UVP will be triggered. When UVP is triggered, both UGATEx and LGATEx go low until VCC is resupplied and exceeds the POR rising threshold voltage.

Output Voltage Setting

The RT8127A allows the output voltage of the DC/DC converter to be adjusted from 0.8V to 80% of VIN via an external resistor divider as shown in Figure 5. It will try to maintain the feedback pin at internal reference voltage.

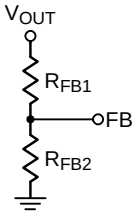


Figure 5. Output Voltage Setting

The output voltage can be set according to :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

Output Inductor Selection

Inductor plays an important role in the Buck converter because the energy from the input power rail is stored in it and then released to the load. From the viewpoint of efficiency, the DC Resistance (DCR) of inductor should be as small as possible because inductor carries current all the time. Using inductor that has lower DCR can obtain higher efficiency. In addition, because inductor takes most of the board space, its size is also important. Low profile inductors can save board space especially when the height has limitation. Additionally, larger inductance results in lower ripple current, and therefore the lower power loss. However, the inductor current rising time increases with inductance value. This means the inductor will have a longer charging time before its current reaches the required output current. Since the response time is increased, the transient response performance will be decreased. Therefore, the inductor design is a trade-off between performance, size and cost. In general, inductance is designed such that the ripple current ranges between 20% to 30% of full load current. The inductance can be calculated by using the following equation :

$$L_{(MIN)} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times k \times I_{OUT\_FullLoad}} \times \frac{V_{OUT}}{V_{IN}}$$

where k is 0.2 to 0.3.

Output Capacitor Selection

The output capacitor and the inductor form a low-pass filter in the Buck topology. In steady state condition, the ripple current flowing into/out of the capacitor results in voltage ripple. The output voltage ripples contains two parts, ΔV_{OUT_ESR} and ΔV_{OUT_C}.

$$\Delta V_{OUT\_ESR} = \Delta I_L \times ESR$$

$$\Delta V_{OUT\_C} = \Delta I_L \times \frac{1}{8 \times C_{OUT} \times f_{SW}}$$

When load transient occurs, the output capacitor supplies the load current before controller can respond. Therefore, the ESR will dominate the output voltage sag during load transient. The output voltage sag can be calculated by using the following equation :

$$V_{OUT\_SAG} = ESR \times \Delta I_{OUT}$$

For a given output voltage sag specification, the ESR value can be determined. Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient. Therefore ESL contributes to part of the voltage sag. Using a capacitor with low ESL will obtain better transient performance. Generally, using several capacitors connected in parallel will also have better transient performance than just one single capacitor with the same total ESR. Unlike electrolytic capacitors, the ceramic capacitor has relatively low ESR and can reduce the voltage deviation during load transient. However, the ceramic capacitor can only provide low capacitance value. Therefore, it is suggested to use a mixed combination of electrolytic capacitor and ceramic capacitor for achieving better transient performance.

MOSFET Selection

The majority of power loss in the step-down power conversion is due to the loss in the power MOSFET(s). For low voltage high current applications, the duty cycle of the high side MOSFET is small. Therefore, the switching loss of the high side MOSFET is of concern. Power MOSFET(s) with lower total gate charge are preferred in such kind of application. However, the small duty cycle means the low side MOSFET is on for most of the switching cycle. Therefore, the conduction loss tends to dominate the total power loss of the converter. To improve the overall efficiency, MOSFET(s) with low $R_{DS(ON)}$ are preferred in the circuit design. In some cases, more than one MOSFET are connected in parallel to further decrease the on-state resistance. However, this depends on the low side MOSFET driver capability and the budget.

Compensation Network Design

The RT8127A is a voltage mode synchronous Buck controller. To compensate a typical voltage mode Buck converter, there are two ordinary compensation schemes, well known as type-II compensator and type-III compensator. The choice of using type-II or type-III compensator will be up to platform designers, and the main concern will be the position of the capacitor ESR zero and mid-frequency to high frequency gain boost. Typically, the ESR zero of output capacitor will tend to

stabilize the effect of output LC double poles, hence the position of the output capacitor ESR zero in frequency domain may influence the design of voltage loop compensation. If $f_{Z(ESR)}$ is <1/2f_C, where f_C denotes 0dB crossing frequency, type-II compensation will be sufficient for voltage stability. If $f_{Z(ESR)}$ is > 1/2f_C (or higher gain and phase margin is required at mid frequency to high frequency), then type-III compensation may be a better solution for voltage loop compensation.

The frequency of the double-pole is determined as follows.

$$f_{P(LC)} = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}}$$

The frequency of the ESR zero is determined as follows.

$$f_{Z(ESR)} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

A typical type-II compensation network is shown in Figure 6.

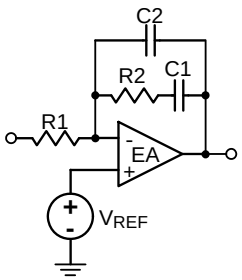


Figure 6. Type-II Compensation Network

After determining the phase margin at crossover frequency, the position of zero and pole produced by type-II compensation network, F_{Z1} and F_{P2}, can then be determined. The bode plot of type-II compensation is shown in Figure 7.

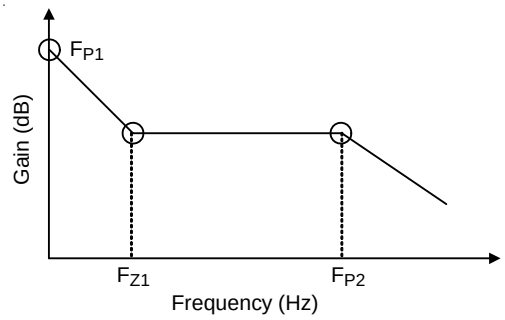


Figure 7. Bode Plot of the Type-II Compensation

the frequencies of poles and zero are :

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1}$$

$$f_{P1} = 0$$

$$f_{P2} = \frac{1}{2\pi \times R2 \times \frac{C1 \times C2}{C1 + C2}}$$

Determining the 0dB crossing frequency (f_C, control loop bandwidth) is the first step of compensator design. Usually, the f_C is set to 0.1 to 0.3 times of the switching frequency. The second step is to calculate the open loop modulator gain and find out the gain loss at f_C. The third step is to design a compensator gain that can compensate the modulator gain loss at f_C. The final step is to design f_{Z1} and f_{P2} to allow the loop sufficient phase margin. f_{Z1} is designed to cancel one of the double-pole of modulator. Usually, place f_{Z1} before $f_{P(LC)}$. f_{P2} is usually placed below the switching frequency (typically, 0.5 to 1 times of the switching frequency) to cancel high frequency noise.

A typical type-III compensation contains two zeros and two poles, where the extra one zero and one pole compared with type-II compensation are added for stabilizing the system when ESR zero is relatively far from LC double-pole in frequency domain. Figure 8 and Figure 9 show the typical circuit and bode plot of the type-III compensation.

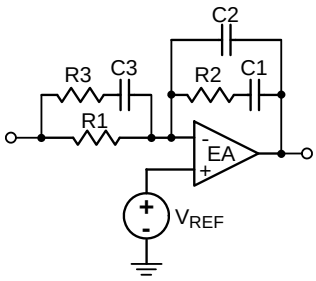


Figure 8. Type-III Compensation Network

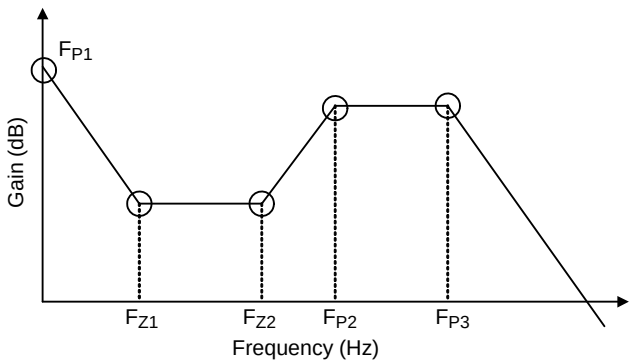


Figure 9. Bode Plot of the Type-III Compensation

A well-designed compensator regulates the output voltage according to the reference voltage V_{REF} with fast transient response and good stability. In order to achieve fast transient response and accurate output regulation, an adequate compensator design is necessary. The goal of the compensation network is to provide adequate phase margin (usually greater than 45°) and the highest bandwidth (0dB crossing frequency, f_C) possible. It is also recommended to manipulate the loop frequency response such that its gain crosses 0dB with a slope of –20dB/dec. According to Figure 9, the frequencies of poles and zeros are :

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1}$$

$$f_{Z2} = \frac{1}{2\pi \times (R1 + R3) \times C3}$$

$$f_{P1} = 0$$

$$f_{P2} = \frac{1}{2\pi \times R3 \times C3}$$

$$f_{P3} = \frac{1}{2\pi \times R2 \times \frac{C1 \times C2}{C1 + C2}}$$

Generally, f_{Z1} and f_{Z2} are designed to cancel the double-pole of the modulator. Usually, place f_{Z1} at a fraction of $f_{P(LC)}$, and place f_{Z2} at $f_{P(LC)}$. f_{P2} is usually placed at $f_{Z(ESR)}$ to cancel the ESR zero, and f_{P3} is placed below the switching frequency to cancel high frequency noise.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-28L 4x4 package, the thermal resistance, θ_{JA}, is 28.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (28.5°C/W) = 3.5W for WQFN-28L 4x4 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 10 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

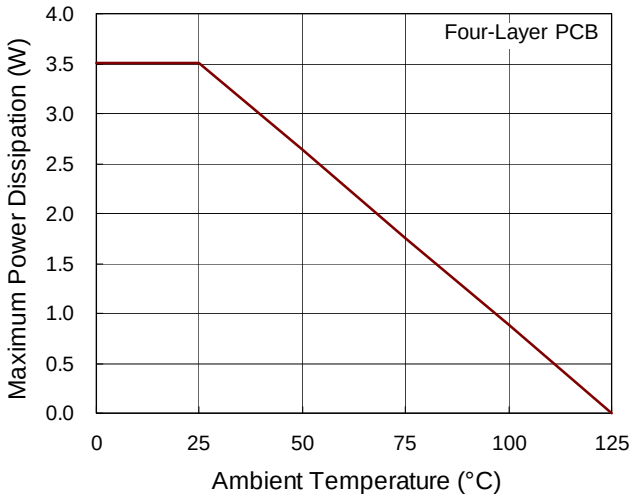


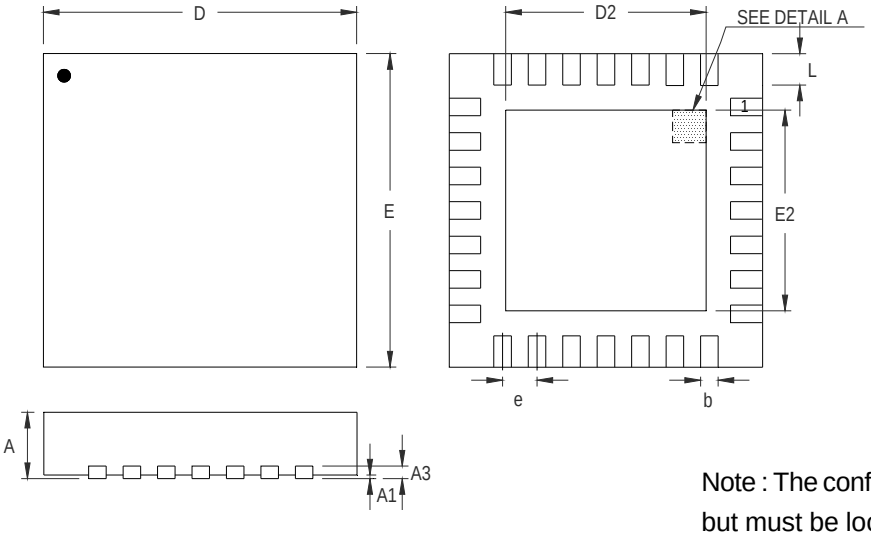
Figure 10. Derating Curve of Maximum Power Dissipation

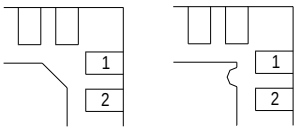
Layout Consideration

Layout planning plays a critical role in modern high frequency switching converter design. Circuit boards with good layout can help the IC functions properly and achieve low losses, low switching noise, and stable operation with good performance. For the best performance of the RT8127A, the following PCB Layout guidelines must be strictly followed.

- Place the filter capacitor close to the device pin, within 12mm (0.5 inch) if possible.
- Place the frequency setting resistor close to the IC frequency setting pin.
- Place feedback and compensation circuits as close to the device pin as possible.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching node.
- Connections from the drivers to the respective gate of the high side or the low side MOSFET should be as short as possible to reduce stray inductance. Use 0.65mm (25 mils) or wider trace.
- All sensitive analog traces and components such as VOUTx, FBx, GND, PGOOD and VCC should be placed away from high voltage switching nodes such as PHASEx, LGATEx, UGATEx, or BOOTx nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Gather ground terminal of VIN capacitor(s), VOUTx capacitor(s), and source of low side MOSFETs as close as possible. PCB trace defined as PHASEx node, which connects to source of high side MOSFET, drain of low side MOSFET and high voltage side of the inductor, should be as short and wide as possible.
- Keep Channel 1 and Channel 2 network isolated to avoid mutually noise coupling.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	3.900	4.100	0.154	0.161
D2	2.350	2.450	0.093	0.096
E	3.900	4.100	0.154	0.161
E2	2.350	2.450	0.093	0.096
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 28L QFN 4x4 Package

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