12V Synchronous Buck PWM DC/DC and Linear Regulator Controller

General Description

The RT8159E is a dual-channel DC/DC regulator controller specifically designed for dual outputs application in which 12V power source is available. This part consists of a synchronous rectified buck PWM controller and a low-dropout linear regulator (LDO) controller. The buck PWM controller utilizes voltage-mode control with external compensation. The MOSFET gate drivers and bootstrap diode are all integrated in the controller to minimize external component count. The MOSFET gate drivers provide 12V driving voltage for high side and low side MOSFETs to achieve high efficiency power conversion. The LDO controller drives an external N-MOSFET for low power application. Other features include adjustable oscillator frequency, internal soft start, fast transient response, under voltage protection, over voltage protection, enable/disable control, and over current protection for PWM output. With the above functions, RT8159E provides customers a compact, high efficiency, and cost-effective solution.

Ordering Information

RT8159E□□

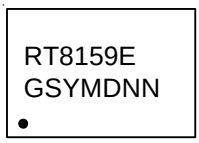
- Package Type
  S : SOP-14
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



RT8159EGS : Product Number

YMDNN : Date Code

Features

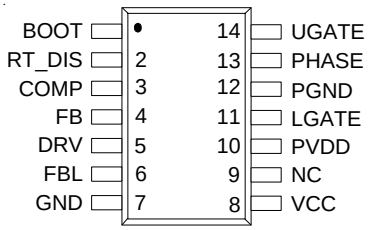
- **Single 12V Bias Supply**
- **5.25V MOSFET Driving Voltage**
- **Support Dual Channel Power Conversion**
  - **Synchronous Rectified Buck PWM Controller**
  - **Linear Regulator Controller**
- **Both Controllers Drive Low Cost N-MOSFETs**
- **Adjustable Oscillator Frequency up to 1MHz with 230kHz Free-Running Frequency**
- **Enable/ Disable Control**
- **Integrated MOSFET Drivers and Bootstrap Diode**
- **±1% Internal Reference Voltage Accuracy**
- **External Compensation for PWM Controller**
- **Under Voltage Protection for Both Outputs**
- **Low Side MOSFET $R_{DS(ON)}$ Current Sense**
- **RoHS Compliant and Halogen Free**

Applications

- Graphic Card GPU, Memory Core Power
- Graphic Card Interface Power
- Motherboard, Desktop and Servers Chipset and Memory Core Power
- IA Equipments
- Telecomm Equipments
- High Power DC/DC Regulators

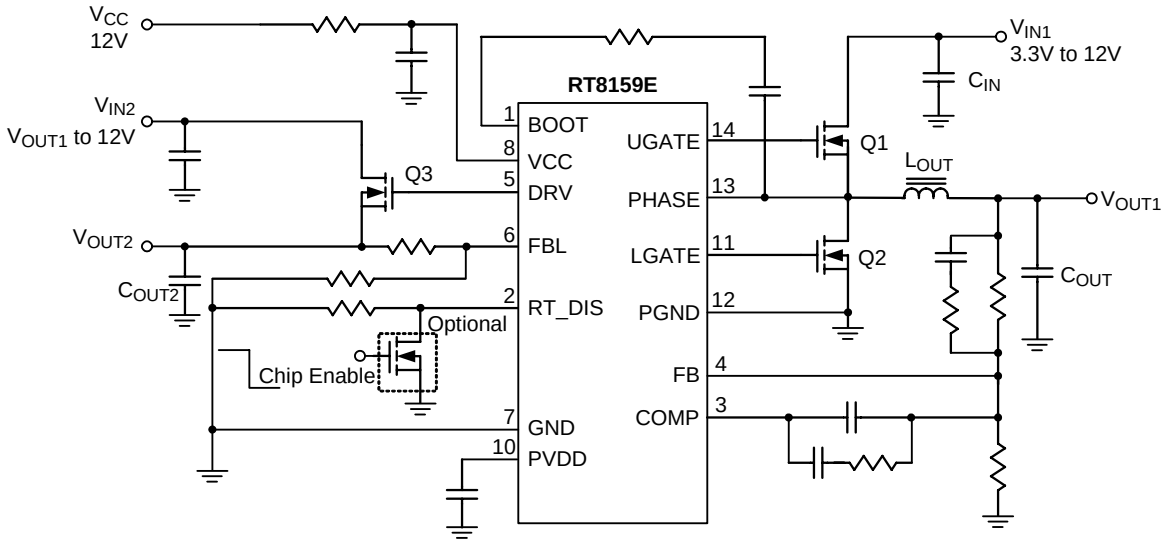
Pin Configurations

(TOP VIEW)



SOP-14

Typical Application Circuit



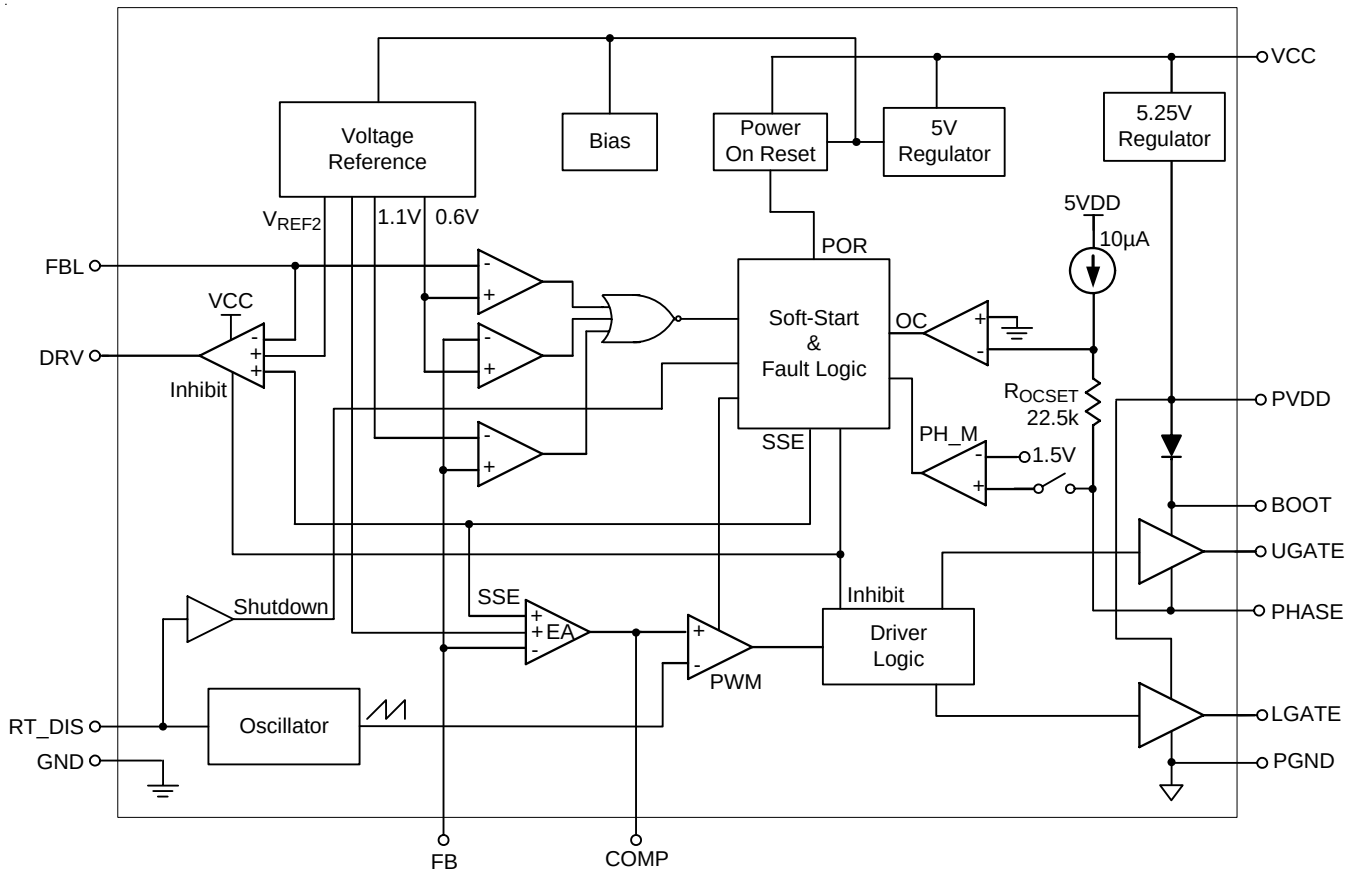
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap Supply for the High Side MOSFET Gate Driver. Connect a bootstrap capacitor from BOOT pin to PHASE pin. The bootstrap capacitor provides the charge to turn on the high side MOSFET.
2	RT_DIS	This pin provides two functions : oscillator frequency setting and enable/disable control. Connect a resistor from this pin to GND to set the internal oscillator frequency for PWM switching regulator. The voltage at this pin is monitored for enable/disable control. If this pin is externally pulled down below 0.4V, both switching regulator output and LDO output will be disabled until it is released.
3	COMP	Error Amplifier Output Pin. Connect an R-C network between COMP pin and FB pin to compensate the control loop of the buck converter.
4	FB	This pin is the inverting input of the error amplifier of PWM controller. Connect this pin to the buck converter output via resistor divider for output voltage sensing. The voltage at FB pin is also monitored for under voltage protection. If FB voltage falls below 0.4V (50% of V_{REF}), under voltage protection will be tripped to shutdown the controller.
5	DRV	Linear Regulator Controller Driver Output Pin. Connect this pin to the gate of an external N-MOSFET.
6	FBL	This pin is the inverting input of the error amplifier of LDO controller. Connect this pin to the LDO output via resistor divider for output voltage sensing. The voltage at FBL pin is also monitored for under voltage protection. If FBL voltage falls below 0.4V (50% of V_{REF}), under voltage protection will be tripped to shutdown the controller.
7	GND	Return Ground of the PWM and LDO Controller. Output voltage is regulated with respect to this pin.
8	VCC	Controller Power Supply Pin. Connect this pin to a well-decoupled 12V bias supply. This pin is also the power supply for the low-side MOSFET gate driver.
9	NC	No Internal Connection.
10	PVDD	Output of the Internal 5.25V Regulator. PVDD is the power supply for the low side and high side MOSFET gate driver. Connect this pin to GND with a 1μF or greater MLCC.
11	LGATE	Low Side MOSFET Gate Driver Output. Connect this pin to the gate of low side N-MOSFET. The voltage at this pin is monitored by the shoot-through protection circuitry to prevent cross-conduction.

To be continued

Pin No.	Pin Name	Pin Function
12	PGND	Return Ground of the Low Side MOSFET Gate Driver.
13	PHASE	Connect this pin to the switching node of the buck converter. This pin is also the return ground of the high side MOSFET gate driver. The voltage at this pin is monitored by the shoot-through protection circuitry to prevent cross-conduction.
14	UGATE	High Side MOSFET Gate Driver Output. Connect this pin to the gate of high side N-MOSFET.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- 15V
- BOOT to PHASE ---------- –0.3V to 6V
- PHASE to GND
  - DC ---------- –0.5V to 15V
  - < 20ns ---------- –5V to 25V
- UGATE to PHASE
  - DC ---------- –0.3V to 6V
  - < 20ns ---------- –5V to 7.5V
- LGATE to GND
  - DC ---------- –0.3V to 6V
  - < 20ns ---------- –5V to 7.5V
- DRV ---------- GND – 0.3V to V_{CC} + 0.3V
- Input, Output or I/O Voltage ---------- GND – 0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  - SOP-14 ---------- 1.000W
- Package Thermal Resistance (Note 2)
  - SOP-14, θ_{JA} ---------- 100°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –40°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{CC} ---------- 12V ± 10%
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Power Supply Voltage	V_{CC}		10.8	12	13.2	V
Power On Reset	V_{VCCRTH}	V_{CC} Rising	3.9	4.1	4.3	V
Power On Reset Hysteresis	V_{VCCHYS}		--	0.2	--	V
Power Supply Current	I_{VCC}	UGATE, LGATE, and DRV open, running at 300kHz	--	5	10	mA

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator						
Switching Frequency	f_{OSC}	R_{RT} = 110kΩ	250	300	350	kHz
		R_{RT} = 20.8kΩ	500	600	700	
Free Running Frequency	$f_{OSC,fr}$	R_{RT} = NC	--	230	--	kHz
Ramp Amplitude	ΔV_{OSC}		--	1.6	--	V
Reference Voltage						
PWM Error Amplifier Reference	V_{REF1}		0.792	0.8	0.808	V
Linear Regulator Controller Reference	V_{REF2}		0.792	0.8	0.808	V
Error Amplifier (Note 5)						
DC Gain			--	88	--	dB
Gain-Bandwidth Product	GBW		--	15	--	MHz
Slew Rate	SR	C_{LOAD} = 5pF	--	6	--	V/μs
MOSFET Gate Driver						
UGATE Drive Source	$R_{UGATEsr}$	Fully Turn On, I_{UGATE} = 50mA	--	0.8	1.2	Ω
UGATE Drive Sink	$R_{UGATEsk}$	Fully Turn On, I_{UGATE} = 50mA	--	1	1.5	Ω
LGATE Drive Source	$R_{LGATEsr}$	Fully Turn On, I_{LGATE} = 50mA	--	0.8	1.2	Ω
LGATE Drive Sink	$R_{LGATEsk}$	Fully Turn On, I_{LGATE} = 50mA	--	0.6	0.9	Ω
Protection						
Under Voltage Protection	V_{UVP_PWM}	V_{FB} /V_{REF1}	68	75	82	%
	V_{UVP_LDO}	V_{FBL} /V_{REF2}	--	75	--	%
Over Voltage Protection	V_{OVP_PWM}	V_{FB} /V_{REF1}	125	137.5	150	%
	V_{OVP_LDO}	V_{FBL} /V_{REF2}	125	137.5	150	%
Soft-Start Time Interval	T_{SS}	FB Rising from 10% to 90%	--	3	--	ms
Over Current Threshold	V_{OC}	Measure V_{PHASE}	–200	–225	–250	mV
RT_DIS Shutdown Threshold	V_{SHDN_RT}		--	--	0.3	V
Linear Regulator Controller						
Output High Voltage	V_{DRVH}		9.5	10.3	--	V
Output Low Voltage	V_{DRVL}		--	0.1	1	V
Source Current	I_{DRVsr}	V_{FBL} = 0.75V, V_{DRV} = 9V	--	30	--	mA
Sink Current	I_{DRVsk}	V_{FBL} = 0.85V, V_{DRV} = 4V	--	4.5	--	mA
PVDD Regulator						
Output Voltage	V_{PVDD}		--	5.25	--	V
On Resistance		I_{PVDD} = 20mA	--	10	--	Ω

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective 4-layers 2S2P thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

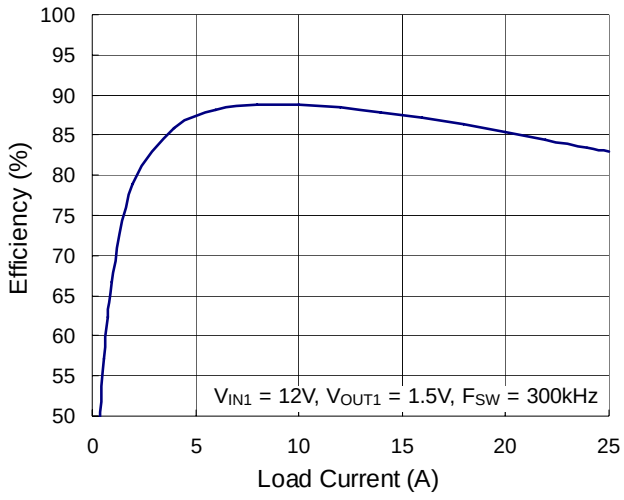
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

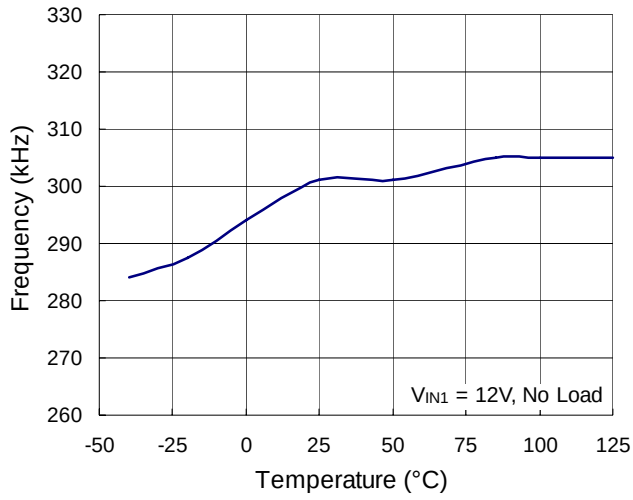
Note 5. Guarantee by design.

Typical Operating Characteristics

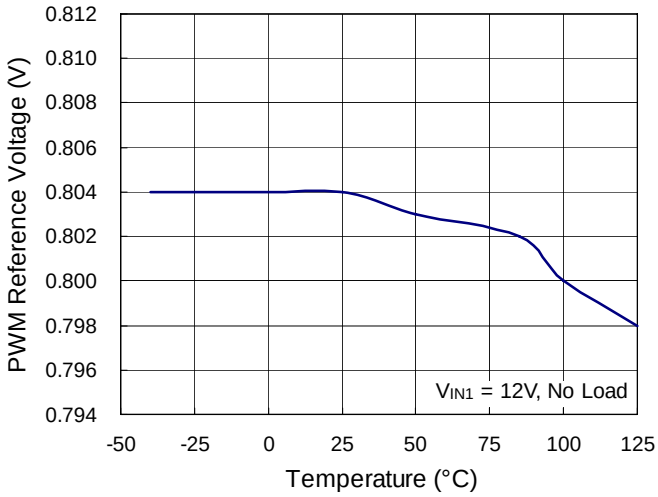
PWM Efficiency vs. Load Current



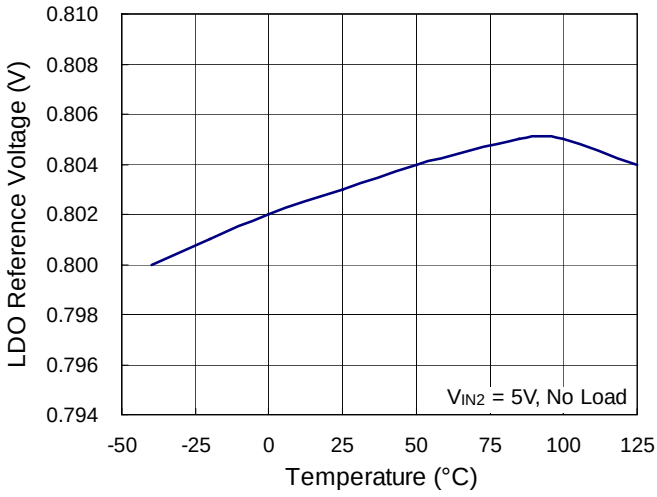
Frequency vs. Temperature



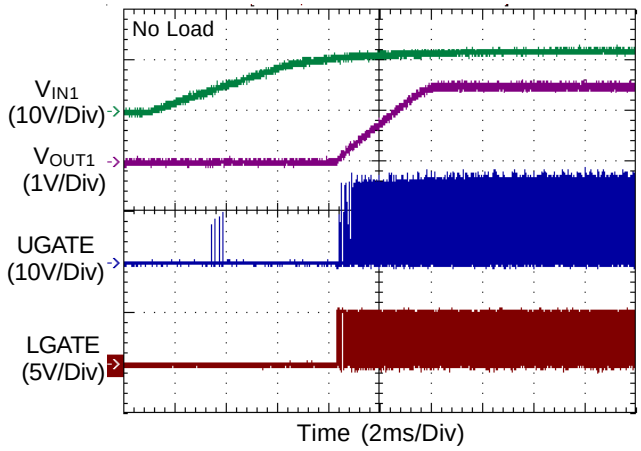
PWM Reference Voltage vs. Temperature



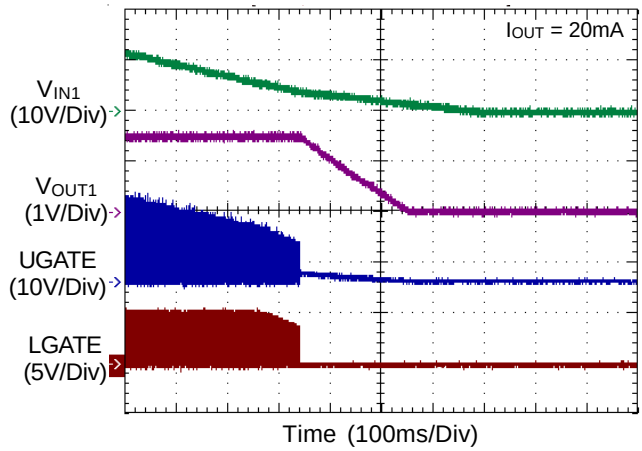
LDO Reference Voltage vs. Temperature



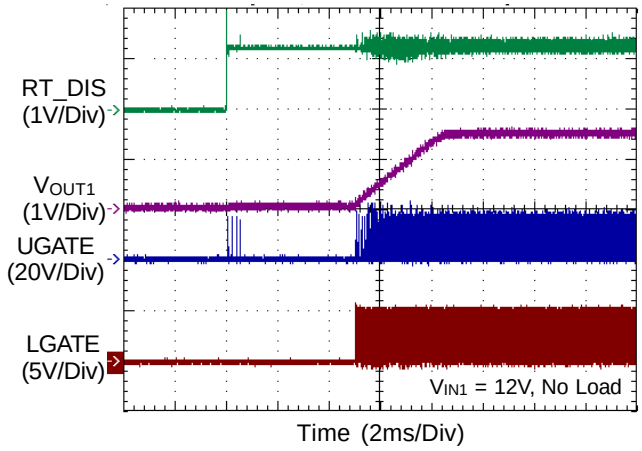
Power On From VIN1



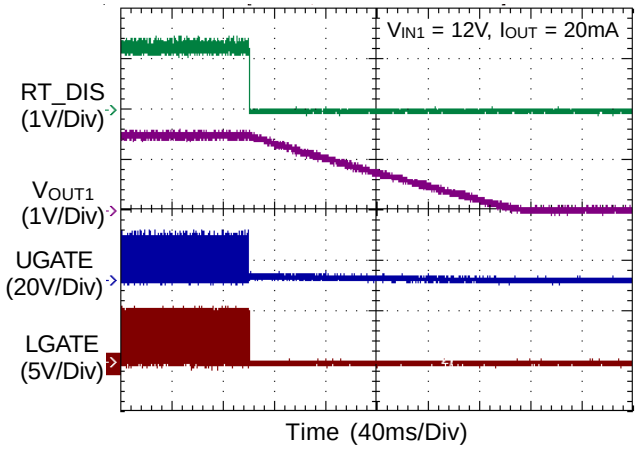
Power Off From VIN1



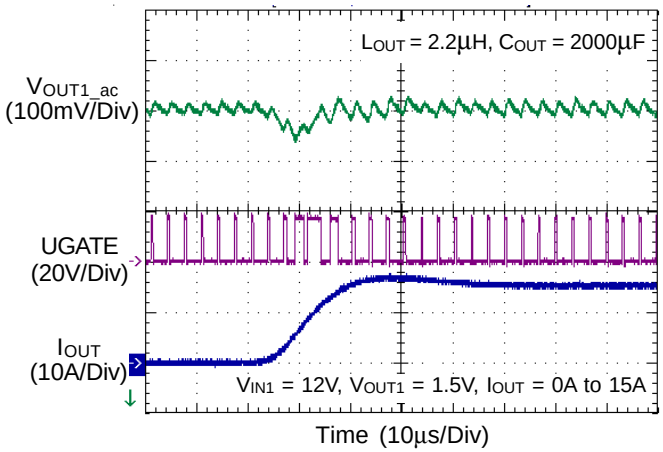
Power On From RT_DIS



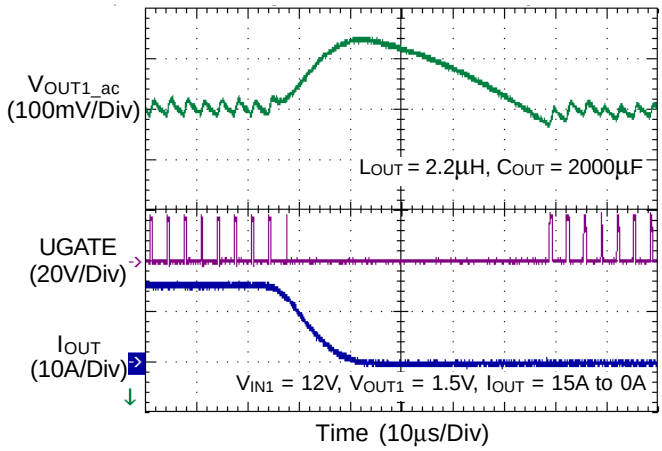
Power Off From RT_DIS



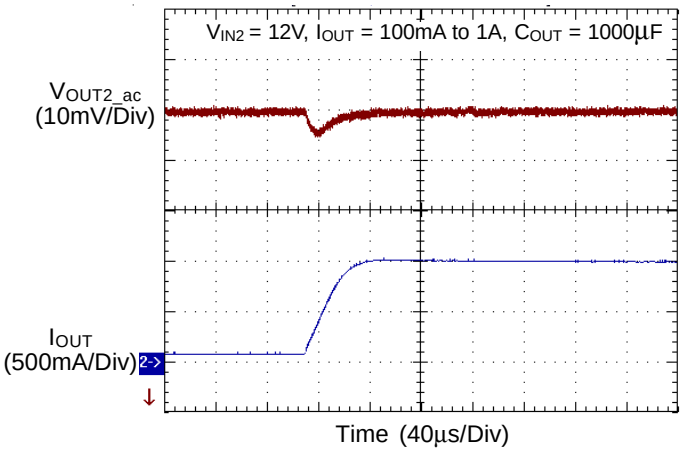
PWM Load Transient Response



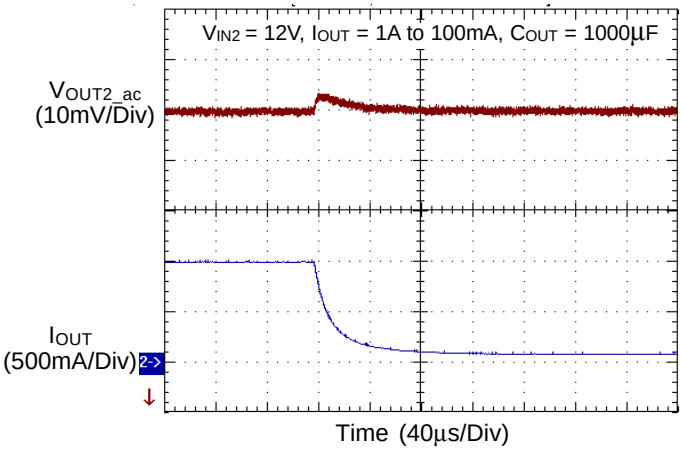
PWM Load Transient Response



LDO Load Transient Response



LDO Load Transient Response



Application Information

Introduction

The RT8159E is a dual-channel DC/DC controller specifically designed to deliver high quality power where 12V power source is available. This part consists of a synchronous buck controller and an LDO controller. The synchronous buck controller integrates internal MOSFET drivers that support 5V+12V bootstrapped voltage for high efficiency power conversion. The bootstrap diode is built-in to simplify the circuit design and minimize external part count. The LDO controller drives an external N-MOSFET for lower power requirement.

Internal 5.25V and 5V Regulators

It is highly recommended to power the RT8159E with well-decoupled 12V to VCC pin. An internal regulator regulates VCC input to 5.25V PVDD. PVDD powers the low side gate driver and bootstrap circuit for high side gate driver. A bootstrap diode is embedded to facilitates PCB design and reduce the total BOM cost. No external Schottky diode is required.

Another internal linear regulator regulates VCC input to a 5V voltage for internal control logic circuit. No external bypass capacitor is required for filtering the 5V voltage. This further facilitates PCB design and reduces the total BOM cost.

Power On Reset

The input voltage of RT8159E at VCC pin is continuously monitored by the power on reset (POR) function. RT8159E begins to operate if VCC rises higher than the POR threshold voltage. If VCC falls below the POR threshold, RT8159E shuts down. There is hysteresis for the POR threshold to avoid inadvertently shutdown.

Frequency Setting and Enable/ Disable Control

The oscillator frequency of the switching regulator is determined by the resistor R_{RT} connected from RT_DIS pin to GND pin. The oscillator frequency can be approximately expressed as the function of R_{RT} as follows:

$$f_{SW} \cong 230 + \frac{6750}{R_{RT}} \text{ (kHz), } R_{RT} \text{ is in k}\Omega$$

If the RT_DIS pin is left open without any resistor connected, the switching regulator will operate at the free-running frequency, which is typically 230kHz. Figure 1 shows the curve of the operating frequency vs. R_{RT} value for quick reference.

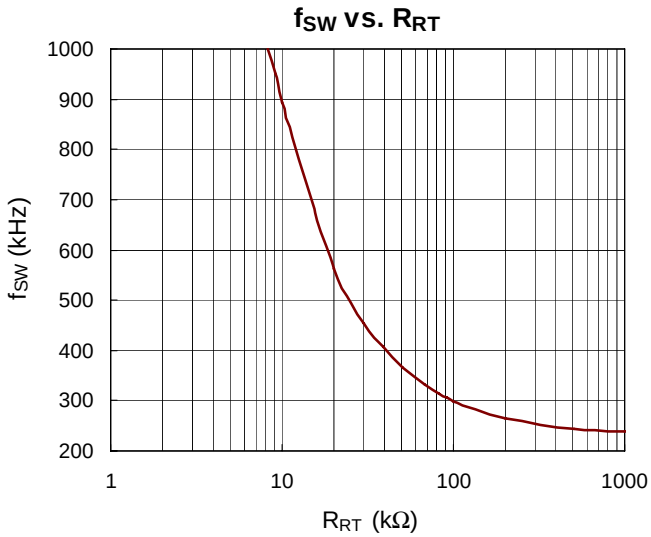


Figure 1. f_{SW} vs. R_{RT}

The voltage at RT_DIS pin is monitored for enable/disable function, which provides the flexibility in power sequence control. If RT_DIS pin is externally pulled down below 0.4V, RT8159E will be disabled with UGATE, LGATE and DRV go low. When RT_DIS pin is released, RT8159E initiates the VIN1 detection followed by the soft start operation.Connect a small-signal MOSFET from RT_DIS pin to GND to implement the enable/disable control.

PWM Switching Regulator Input Detection

The RT8159E has input voltage detection function for the PWM switching regulator. After RT8159E is enabled and VCC exceeds the POR threshold, a train of 10kHz pulse with 1μs width is generated at UGATE to detect the existence of input voltage of buck regulator. As shown in Figure 2, the voltage at PHASE pin is monitored during the detection. If the PHASE voltage crosses 1.5V (rising and falling) for four times, the existence of V_{IN1} is recognized ready. Once V_{IN1} is ready, RT8159E then initializes the soft start operation as described in the next section. Otherwise the 10kHz pulse at UGATE will continue.

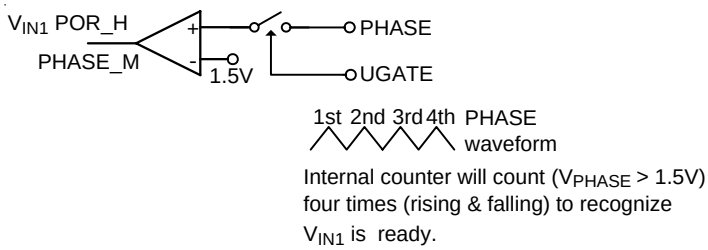


Figure 2. Switching Regulator's Input Voltage Detection

Soft-Start for Synchronous Buck Converter

A built-in soft-start is used to prevent surge current from power supply input during power on (referring to the Functional Block Diagram). The error amplifier EA is a three-input device. SSE or V_{REF1} whichever is smaller dominates the behavior non-inverting input. The internal soft start voltage SSE linearly ramps up to about 4V after VIN1 existence is recognized with about 2ms delay. According, the output voltage ramps up smoothly to its target level. The rise time of output voltage is about 4ms as shown in Figure 3. V_{REF1} takes over the behavior EA when SSE > V_{REF1}.

SSE is also used for LDO soft start.

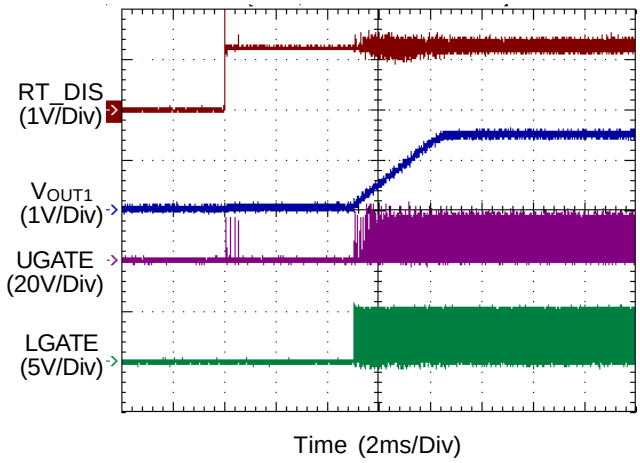


Figure 3. Start up by RT_DIS

Over Voltage Protection

The output voltage is scaled by the divider resistors and fed back to FB pin. The voltage on FB pin will be compared to the internal reference voltage V_{REF} for voltage-related protection functions, including over voltage protection and under voltage protection. If FB voltage is higher than the OVP threshold during operation, OVP will be triggered. When OVP is triggered, LDO regulator shuts down and PWM controller turns UGATE off and LGATE on to discharge the output capacitor. As shown in Figure 4, once OVP is triggered, controller will be latched unless VCC POR is detected again.

Besides, RT8159E also provides OVP even if VCC is below the POR threshold. This can protect the load even if the high side MOSFET is shorted before power-on-reset. Once OVP is triggered before POR, the LGATE signal will go high to discharge the output capacitor.

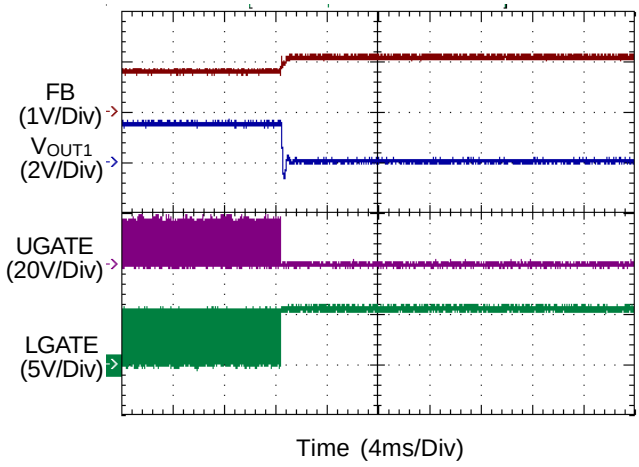


Figure 4. OVP

Under Voltage Protection

The voltages at FB and FBL pin are monitored for under voltage protection (UVP) after the soft start is completed. UVP is triggered if one of the feedback voltages is under (75% x VREFX) with a 30us delay. As shown in Figure 6, the RT8159E PWM controller will enter the hiccup mode and always try to restart when VFB drops lower than the UVP threshold. In Figure 7, the RT8159E shuts down after 4 time UVP hiccups triggered by FBL.

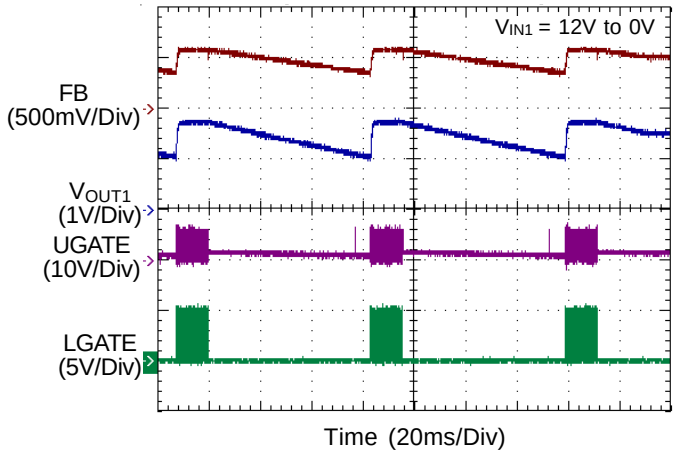


Figure 5. UVP triggered by FB

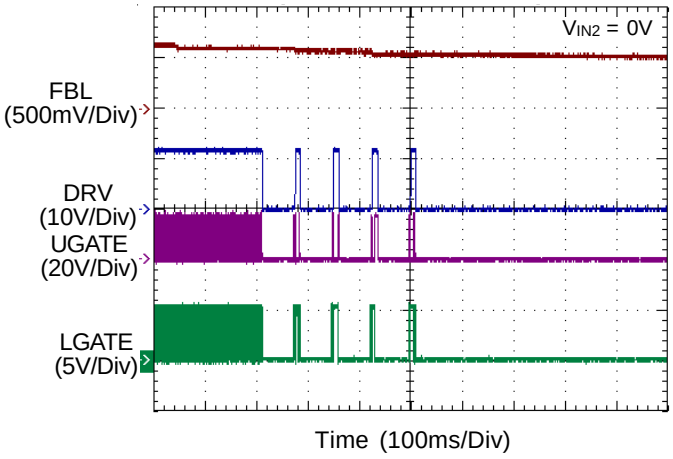


Figure 6. UVP hiccups triggered by FBL

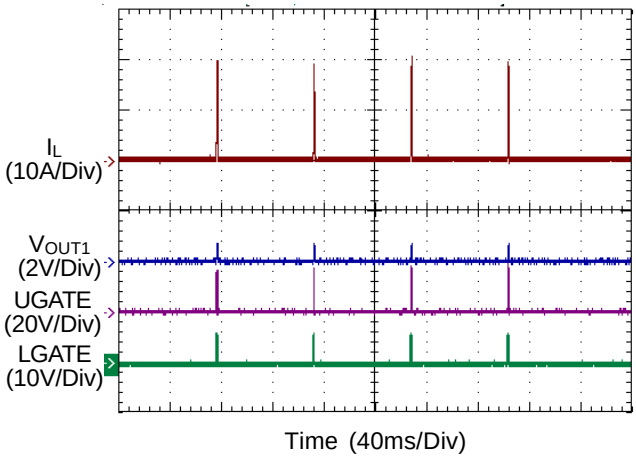


Figure 8. Shorted then Start Up

Over Current Protection

The RT8159E senses the peak current flowing through lower MOSFET for over current protection (OCP) by sensing the PHASE pin voltage as shown in the Functional Block Diagram. A 10μA current source flows through internal 22.5kΩ R_{OCSET} to PHASE pin and causes 225mV voltage drop across the resistor. OCP is triggered if the voltage at the PHASE pin (drop of lower MOSFET V_{DS}) is lower than −225mV when low side MOSFET is conducting. Accordingly, inductor peak current threshold for OCP is a function of conducting resistance of lower MOSFET $R_{DS(ON)}$ as :

$$I_{OCSET} = \frac{10\mu A \times R_{OCSET}(22.5k\Omega)\text{-}0V}{R_{DS(ON)}} = \frac{225mV}{R_{DS(ON)}}$$

If MOSFET with $R_{DS(ON)}$ = 6mΩ is used, the OCP threshold current is about 37.5A. Once OCP is triggered, the RT8159E enters hiccup mode and re-soft starts again. The RT8159E shuts down after 4 time OCP hiccups.

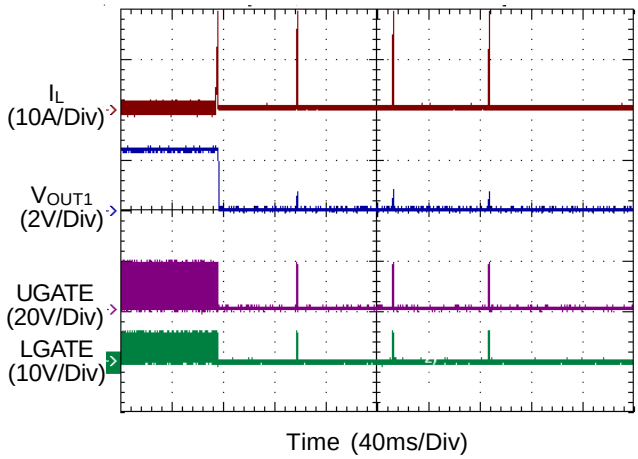


Figure 7. OCP

PWM Feedback Loop Compensation

RT8159E operates with fixed frequency and uses voltage mode control for output voltage regulation. The IC utilizes voltage error amplifier with external compensation to provide flexibility in feedback loop compensator design. Figure 9 shows the voltage mode control loop of a buck converter. The control loop consists of the modulator, power stage and the compensator.

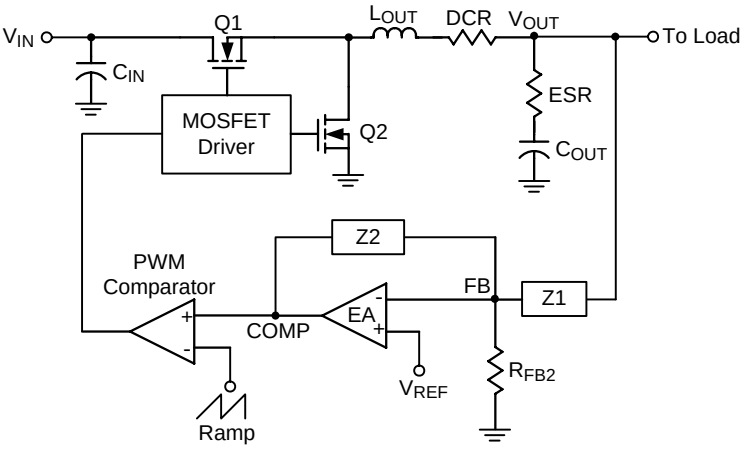


Figure 9. Voltage Mode Control Loop of Buck Converter

Output voltage of the converter is scaled by the divider resistors and then compared to the reference voltage, which is the regulation level seen by the controller. The error amplifier output voltage V_{COMP} is compared to the saw-tooth waveform from the oscillator to generate PWM signal. The output voltage is then regulated according to the duty cycle of the PWM signal.

The system open loop gain $\frac{\hat{V}_{OUT}}{\hat{V}_{COMP}}$ has one pole at F_{LC} and one zero at F_{ESR}. The frequency of F_{LC} and F_{ESR} can be calculated using the following expressions :

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

$$F_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

In order to obtain an accurate output voltage regulation and fast transient response, a compensator is necessary. Depends on the inductor and output capacitor, different type of compensator can be used to finish the feedback loop compensation. By inserting a well designed compensator into the feedback loop, the closed loop control-to-output transfer function can be shaped to have adequate crossover frequency and sufficient phase margin.

The design goals are:

- Obtain high gain at low frequency for DC regulation accuracy
- Obtain sufficient bandwidth for transient performance (generally, 1/10 to 1/5 switching frequency)
- Obtain sufficient phase margin for stability (generally >45°)

Figure 10 shows the Type-III compensator, which is composed of voltage error amplifier, impedance network Z1 and Z2.

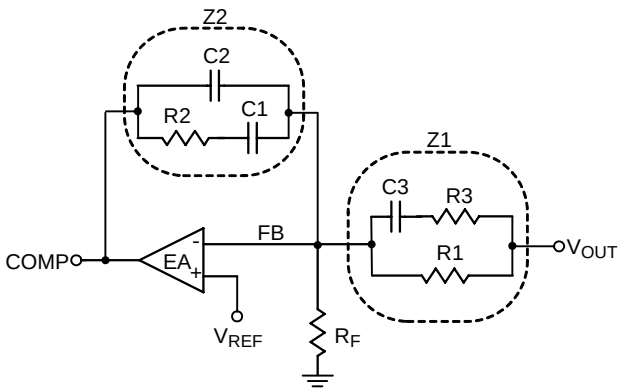


Figure 10. Type-III Compensator

The Type-III compensator introduces three poles and two zeros to the system. The first pole is located in low frequency to increase the DC gain for voltage regulation accuracy and is usually referred to as the pole-at-zero. The location of rest of the two poles and two zeros can be determined as follows :

$$F_{Z1} = \frac{1}{2\pi \times R2 \times C1}, \quad F_{Z2} = \frac{1}{2\pi \times (R3 + R1) \times C3}$$

$$F_{P1} = \frac{1}{2\pi \times R2 \times \left(\frac{C1 \times C2}{C1 + C2}\right)}, \quad F_{P2} = \frac{1}{2\pi \times R3 \times C3}$$

Figure 11 shows the system Bode plot. The close loop gain is the sum of modulation gain and the compensation gain. The modulation DC gain is determined by $V_{IN}/\Delta V_{OSC}$, where ΔV_{OSC} is peak to peak voltage of the saw-tooth ramp. In general, F_{Z1} is placed at half of F_{LC}, and F_{Z2} is placed at F_{LC} to boost the large phase lag created by the double pole especially when ESR is low. F_{P1} is typically placed at F_{ESR} to obtain a –20dB/dec slope at crossover frequency. F_{P2} is placed at half of the switching frequency to increase the attenuation in high frequency.

After calculating the compensation values, draw the system Bode plot to check the crossover frequency and phase margin. Due to the circuit parasitic components and the characteristic deviation in the inductor and output capacitors, further tuning of the compensation value to obtain the required crossover frequency and phase margin is necessary.

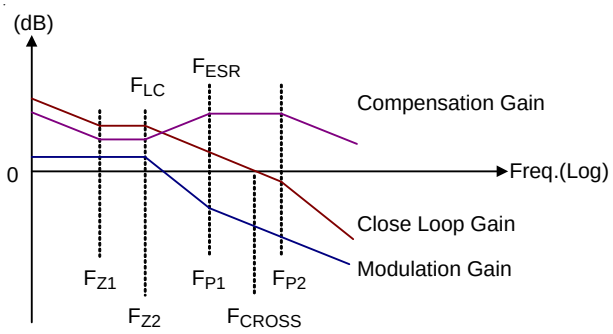


Figure 11. System Bode Plot

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8159E, The maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For SOP-14 package, the thermal resistance θ_{JA} is 100°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (100°C/W) = 1.000W for SOP-14 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. Figure 12 shows the derating curve of maximum power dissipation of RT8159E.

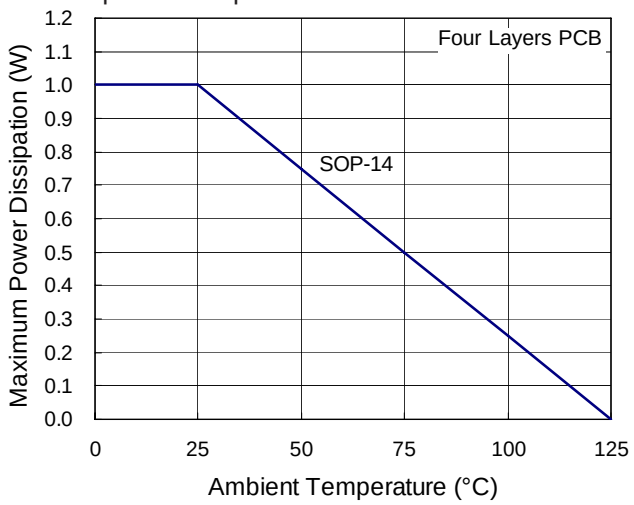


Figure 12. Derating Curve for RT8159E Package

Layout Considerations

PCB layout is critical to high-current high-frequency switching converter design. A good layout can help the controller to function properly and obtain better performance. On the other hand, the circuit may have more power loss, pool performance and even malfunction if without a carefully layout. Figure 13 shows the connections of the critical components in the buck converter. In order to obtain better performance, the general guidelines of PCB layout are listed as follows.

- Power stage components should be placed first. Place the input bulk capacitors close to the high side power MOSFETs, and then locate the output inductor then finally the output capacitors.
- Placing the ceramic capacitors physically close to the drain of the high side MOSFET. This can reduce the input voltage drop when high side MOSFET is turned on.
- Keep the high-current loops as short as possible. The current transition between MOSFETs usually causes di/dt voltage spike due to the parasitic components on PCB trace and component lead. Therefore, making the trace length between power MOSFETs and inductors wide and short can reduce the voltage spike and also reduce EMI.
- Make MOSFET gate driver path as short as possible. Since the gate driver uses high-current pulses to switch on/off power MOSFET, the driver path must be short to reduce the trace inductance. This is especially important for low side MOSFET because this can reduce the possibility of shoot-through. Besides, also make the width of gate driving path as wide as possible to reduce the trace resistance. The PCB traces between the PWM controller and the gate/source of MOSFET should be sized to carry 2A peak currents.
- Providing enough copper area around power MOSFETs to help heat dissipation. Using thick copper also reduces the trace resistance and inductance to have better performance.
- The output capacitors should be placed physically close to the load. This can minimize the trace parasitic components and improve transient response.
- All small signal components should be placed close to the controller. The small signal components include the feedback voltage divider resistors, compensator, function setting components and high-frequency bypass capacitors. The feedback voltage divider resistor and the compensator must be placed close to FB pin and COMP pin, because these pins are inherently noise-sensitive.
- Voltage feedback path must be kept away from switching nodes. The switching nodes, such as the interconnection between high side MOSFET, low side MOSFET and inductor, is extremely noisy. Feedback path must be kept away from this kind of noisy node to avoid noise pick-up.
- A multi-layer PCB design is recommended. Use one single layer as the ground and have separate layers for power rail or signal.

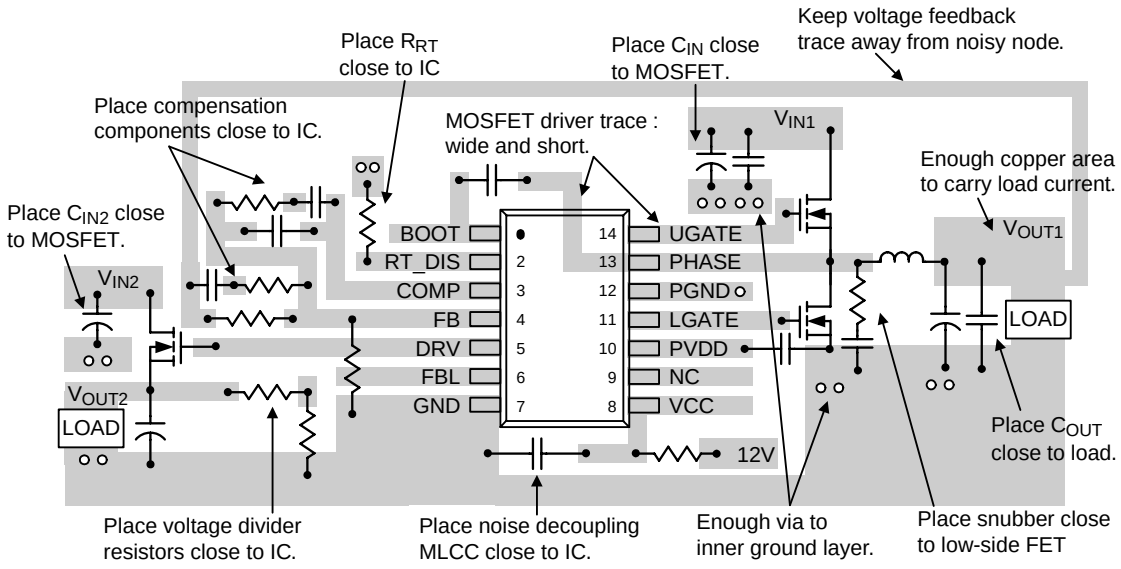
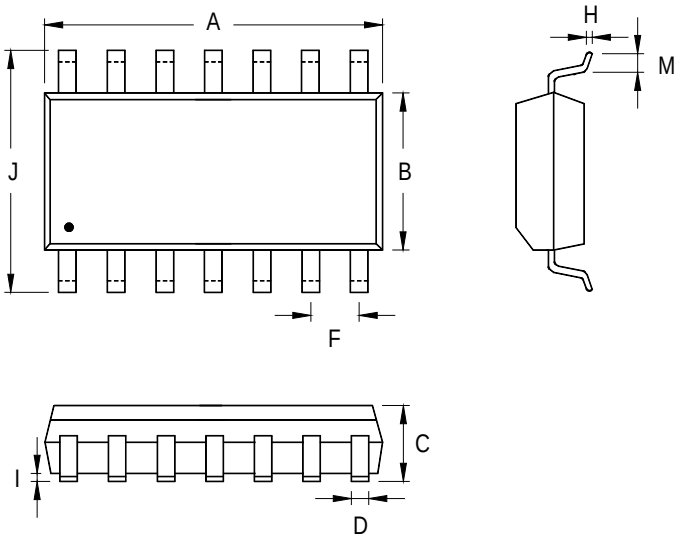


Figure 13. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	8.534	8.738	0.336	0.344
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050

14-Lead SOP Plastic Package

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