Single-Phase Controller with Integrated Driver for VR12.1 Mobile CPU Core Power Supply

General Description

The RT8171B is a VR12.1 compliant CPU power controller which includes one voltage rails : a 1 phase synchronous buck controller, the CORE VR. The RT8171B has zero load-line function to support zero load-line application. The RT8171B adopts G-NAVP™ (Green Native AVP), which is Richtek's proprietary topology derived from finite DC gain compensator with current mode control, making it an easy to set the PWM controller, meeting all Intel CPU requirements of AVP (Active Voltage Positioning). Based on the G-NAVP™ topology, the RT8171B also features a quick response mechanism for optimized AVP performance during load transient. The RT8171B supports mode transition function with various operating states. A Serial VID (SVID) interface is built in the RT8171B to communicate with Intel VR12.1 compliant CPU. The RT8171B supports VID on-the-fly function with three different slew rates : Fast, Slow and Decay. By utilizing the G-NAVP™ topology, the operating frequency of the RT8171B varies with VID, load and input voltage to further enhance the efficiency even in CCM. The built-in high accuracy DAC converts the SVID code ranging from 0.25V to 1.52V with 5mV per step, as shown in Table 1. The RT8171B integrates a high accuracy ADC for platform setting functions, such as quick response or over current level. The RT8171B provides VR ready output signals. It also features complete fault protection functions including Over Voltage (OV), Under Voltage (UV), Negative Voltage (NV), Over Current (OC) and Under Voltage Lockout (UVLO). The RT8171B is available in a WQFN-32L 4x4 small foot print package.

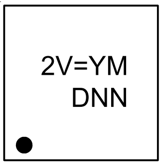
Features

- **VR12.1 Compatible Power Management States**
- **Switching Frequency up to 1MHz**
- **Serial VID Interface**
- **Signal Phase PWM Controller**
- **G-NAVP™ Topology**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Built-in ADC for Platform Programming**
- **System Thermal Compensated AVP**
- **Diode Emulation Mode at Light Load Condition**
- **Fast transient Response**
- **VR Ready Indicator**
- **Thermal Throttling**
- **Current Monitor Output**
- **Low Quiescent Power at PS3 and PS4**
- **OVP, UVP, OCP, UVLO, NVP**
- **Address Flip Function**
- **DVID Improvement**

Applications

- VR12.1 Intel Core Supply
- Notebook CPU Core Supply
- AVP Step-Down Converter

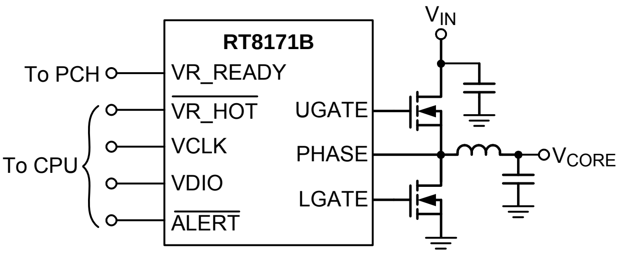
Marking Information



2V= : Product Code

YMDNN : Date Code

Simplified Application Circuit



Ordering Information

RT8171B ☐☐

Package Type
QW : WQFN-32L 4x4 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

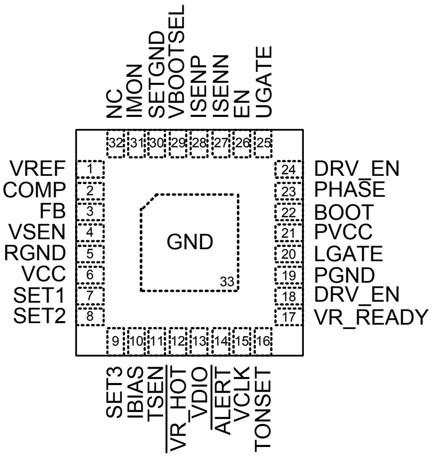
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)



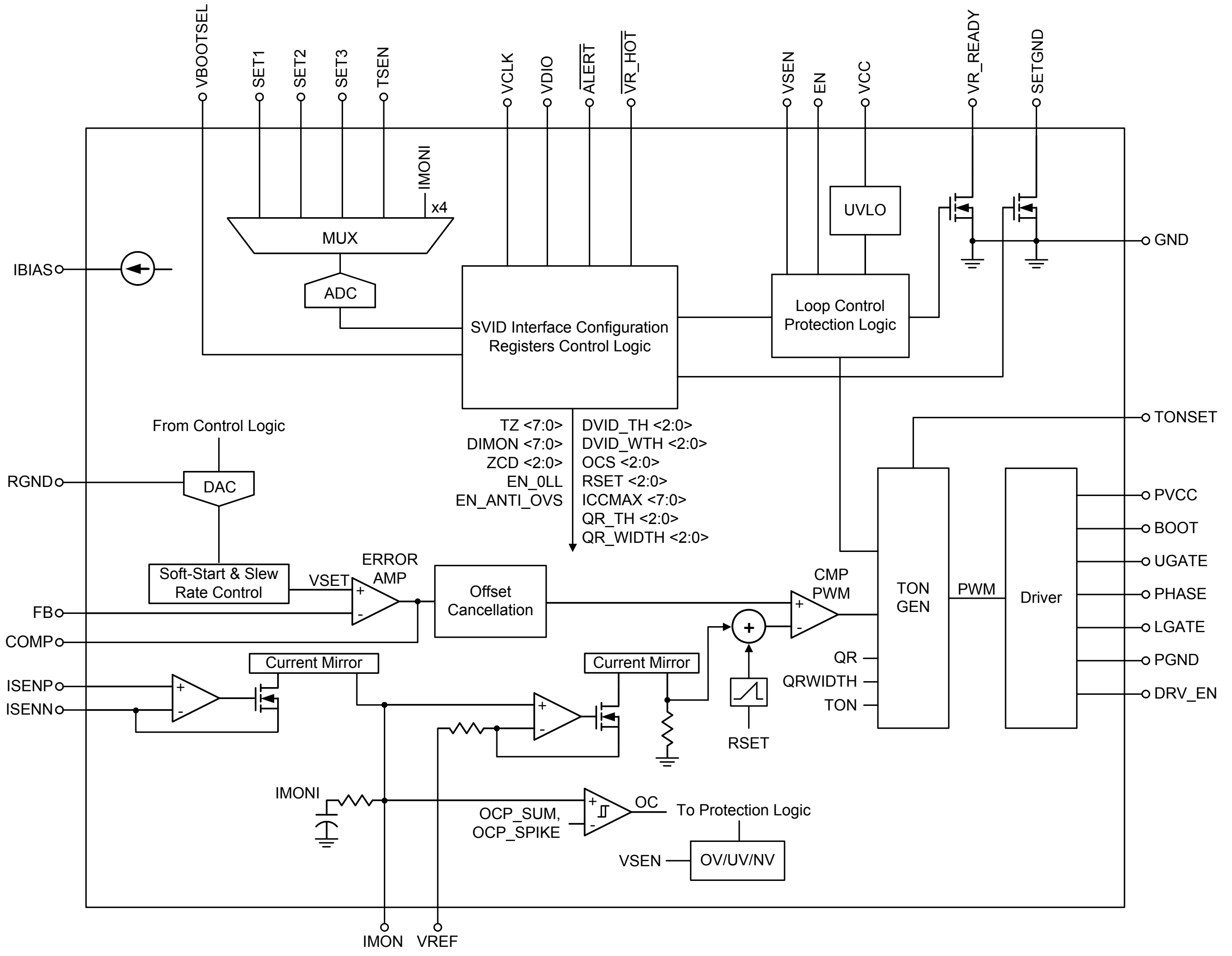
WQFN-32L 4x4

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VREF	Fixed 0.6V Output Reference Voltage. This voltage is only used to offset the output voltage of the IMON pin. Between this pin and GND must be placed a exact 0.47μF decoupling capacitor.
2	COMP	CORE VR Compensation Node. This pin is the output node of the error amplifier.
3	FB	CORE VR Feedback Voltage Input. This pin is the negative input node of the error amplifier.
4	VSEN	CORE VR Voltage Sense Input. This pin is connected to the terminal of CORE VR output voltage.
5	RGND	Return Ground for CORE VR. This pin is the negative node of the differential remote voltage sensing.
6	VCC	Supply Voltage Input. Connect this pin to GND via a ceramic capacitor larger than 2.2μF. The decoupling capacitor should be placed as close to the controller as possible. If the ripple of voltage source is large, RC low pass filter is recommended. (R = 20Ω, C = 2.2μF)
7	SET1	1st Platform Setting. Platform can use this to set DVID compensation time, RSET, DVID compensation width and OCS.
8	SET2	2nd Platform Setting. Platform can use this to set ICCMAX, QRTH and QRWIDTH.
9	SET3	3rd Platform Setting. Platform can use this to set zero load-line, anti-overshoot, ADDR, switching frequency range and ZCD threshold voltage.
10	IBIAS	Internal Bias Current Setting. Connecting this pin to GND by a 100k resistor can set the internal current. Do not connect this pin to GND by a bypass capacitor.
11	TSEN	Thermal Sense Input of CORE VR.

Pin No.	Pin Name	Pin Function
12	$\overline{\text{VR\_HOT}}$	Thermal Monitor Output. (Active Low).
13	VDIO	VR and CPU Data Transmission Interface.
14	$\overline{\text{ALERT}}$	SVID Alert. (Active Low).
15	VCLK	Synchronous Clock from the CPU.
16	TONSET	CORE VR On-Time Setting. Connect this pin to input voltage with one resistor. By this resistor value, ripple size in PWM-mode can be set.
17	VR_READY	VR Ready Indicator of CORE VR.
18, 24	DRV_EN	Internal Driver Enable Control. These two pins should be floating and be connected together.
19	PGND	Driver Power Ground.
20	LGATE	Low-Side Gate Driver Output. This pin drives the Gate of low-side MOSFET.
21	PVCC	Driver Power. Connect this pin to GND by a ceramic capacitor 2.2μF at least.
22	BOOT	Bootstrap Supply for High-Side MOSFET.
23	PHASE	Switch Node. This Pin is Return Node of The Core VR high-side driver. Connect this pin to the high-side MOSFET Source together with the low-side MOSFET Drain and the inductor.
25	UGATE	High-Side Gate Driver Output. This pin drives the Gate of high-side MOSFET.
26	EN	VR Enable Control Input.
27	ISENN	Negative Current Sense Input.
28	ISENP	Positive Current Sense Input.
29	VBOOTSEL	Boot Voltage Setting. Connect to a resistor divider between VCC and SETGND pins. By using this pin, BOOT voltage can be set to 0.9V, 1V or 1.1V.
30	SETGND	Ground Return for the Platform Setting Pins : SET1, SET2, SET3, VBOOTSEL and TSEN. The SETGND pin is connected to ground except at PS3 and PS4.
31	IMON	CPU Core Current Monitor Output. This pin outputs a voltage proportional to the inductor current. Do not connect a bypass capacitor from this pin to GND or the VREF pin.
32	NC	No Internal Connection.
33 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Operation

The RT8171B adopts G-NAVP^{TM} (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning).

The RT8171B adopts the G-NAVP^{TM} controller, which is one type of current mode constant on-time control with DC offset cancellation. The approach can not only improve DC offset problem for increasing system accuracy but also has fast transient response. When current feedback signal reaches COMP signal, the RT8171B generates an on-time width to achieve PWM modulation.

Besides, RT8171B also can support zero load-line application.

TON GEN

Generate the PWM signal sequentially according to the phase control signal from the Loop Control Protection Logic.

SVID Interface/Configuration Registers/Control Logic

The interface that receives the SVID signal from CPU and sends the relative signals to Loop Control Protection Logic to execute the action by CPU.

The registers save the pin setting data from ADC output.

The Control Logic controls the ADC timing and generates the digital code of the VID that is relative to VSEN.

Loop Control Protection Logic

It controls the power on sequence and the protection behavior.

Offset Cancellation

Cancel the current/voltage ripple issue to get the accurate VSEN.

UVLO

Detect the PVCC and VCC voltage and issue POR signal as they are high enough.

DAC

Generate an analog signal according to the digital code generated by Control Logic.

Soft-Start & Slew Rate Control

Control the Dynamic VID slew rate of VSET according to the SetVID fast or SetVID slow. And the soft-start slew rate is the slow slew rate.

Table 1. VR12.1 VID Code Table

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	0	0	0	0	0	0	1	01	0.250
0	0	0	0	0	0	1	0	02	0.255
0	0	0	0	0	0	1	1	03	0.260
0	0	0	0	0	1	0	0	04	0.265
0	0	0	0	0	1	0	1	05	0.270
0	0	0	0	0	1	1	0	06	0.275
0	0	0	0	0	1	1	1	07	0.280
0	0	0	0	1	0	0	0	08	0.285
0	0	0	0	1	0	0	1	09	0.290
0	0	0	0	1	0	1	0	0A	0.295
0	0	0	0	1	0	1	1	0B	0.300
0	0	0	0	1	1	0	0	0C	0.305
0	0	0	0	1	1	0	1	0D	0.310
0	0	0	0	1	1	1	0	0E	0.315
0	0	0	0	1	1	1	1	0F	0.320
0	0	0	1	0	0	0	0	10	0.325
0	0	0	1	0	0	0	1	11	0.330
0	0	0	1	0	0	1	0	12	0.335
0	0	0	1	0	0	1	1	13	0.340
0	0	0	1	0	1	0	0	14	0.345
0	0	0	1	0	1	0	1	15	0.350
0	0	0	1	0	1	1	0	16	0.355
0	0	0	1	0	1	1	1	17	0.360
0	0	0	1	1	0	0	0	18	0.365
0	0	0	1	1	0	0	1	19	0.370
0	0	0	1	1	0	1	0	1A	0.375
0	0	0	1	1	0	1	1	1B	0.380
0	0	0	1	1	1	0	0	1C	0.385
0	0	0	1	1	1	0	1	1D	0.390
0	0	0	1	1	1	1	0	1E	0.395
0	0	0	1	1	1	1	1	1F	0.400
0	0	1	0	0	0	0	0	20	0.405
0	0	1	0	0	0	0	1	21	0.410
0	0	1	0	0	0	1	0	22	0.415
0	0	1	0	0	0	1	1	23	0.420
0	0	1	0	0	1	0	0	24	0.425
0	0	1	0	0	1	0	1	25	0.430
0	0	1	0	0	1	1	0	26	0.435
0	0	1	0	0	1	1	1	27	0.440
0	0	1	0	1	0	0	0	28	0.445

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	0	1	0	1	0	0	1	29	0.450
0	0	1	0	1	0	1	0	2A	0.455
0	0	1	0	1	0	1	1	2B	0.460
0	0	1	0	1	1	0	0	2C	0.465
0	0	1	0	1	1	0	1	2D	0.470
0	0	1	0	1	1	1	0	2E	0.475
0	0	1	0	1	1	1	1	2F	0.480
0	0	1	1	0	0	0	0	30	0.485
0	0	1	1	0	0	0	1	31	0.490
0	0	1	1	0	0	1	0	32	0.495
0	0	1	1	0	0	1	1	33	0.500
0	0	1	1	0	1	0	0	34	0.505
0	0	1	1	0	1	0	1	35	0.510
0	0	1	1	0	1	1	0	36	0.515
0	0	1	1	0	1	1	1	37	0.520
0	0	1	1	1	0	0	0	38	0.525
0	0	1	1	1	0	0	1	39	0.530
0	0	1	1	1	0	1	0	3A	0.535
0	0	1	1	1	0	1	1	3B	0.540
0	0	1	1	1	1	0	0	3C	0.545
0	0	1	1	1	1	0	1	3D	0.550
0	0	1	1	1	1	1	0	3E	0.555
0	0	1	1	1	1	1	1	3F	0.560
0	1	0	0	0	0	0	0	40	0.565
0	1	0	0	0	0	0	1	41	0.570
0	1	0	0	0	0	1	0	42	0.575
0	1	0	0	0	0	1	1	43	0.580
0	1	0	0	0	1	0	0	44	0.585
0	1	0	0	0	1	0	1	45	0.590
0	1	0	0	0	1	1	0	46	0.595
0	1	0	0	0	1	1	1	47	0.600
0	1	0	0	1	0	0	0	48	0.605
0	1	0	0	1	0	0	1	49	0.610
0	1	0	0	1	0	1	0	4A	0.615
0	1	0	0	1	0	1	1	4B	0.620
0	1	0	0	1	1	0	0	4C	0.625
0	1	0	0	1	1	0	1	4D	0.630
0	1	0	0	1	1	1	0	4E	0.635
0	1	0	0	1	1	1	1	4F	0.640
0	1	0	1	0	0	0	0	50	0.645
0	1	0	1	0	0	0	1	51	0.650

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	1	0	1	0	0	1	0	52	0.655
0	1	0	1	0	0	1	1	53	0.660
0	1	0	1	0	1	0	0	54	0.665
0	1	0	1	0	1	0	1	55	0.670
0	1	0	1	0	1	1	0	56	0.675
0	1	0	1	0	1	1	1	57	0.680
0	1	0	1	1	0	0	0	58	0.685
0	1	0	1	1	0	0	1	59	0.690
0	1	0	1	1	0	1	0	5A	0.695
0	1	0	1	1	0	1	1	5B	0.700
0	1	0	1	1	1	0	0	5C	0.705
0	1	0	1	1	1	0	1	5D	0.710
0	1	0	1	1	1	1	0	5E	0.715
0	1	0	1	1	1	1	1	5F	0.720
0	1	1	0	0	0	0	0	60	0.725
0	1	1	0	0	0	0	1	61	0.730
0	1	1	0	0	0	1	0	62	0.735
0	1	1	0	0	0	1	1	63	0.740
0	1	1	0	0	1	0	0	64	0.745
0	1	1	0	0	1	0	1	65	0.750
0	1	1	0	0	1	1	0	66	0.755
0	1	1	0	0	1	1	1	67	0.760
0	1	1	0	1	0	0	0	68	0.765
0	1	1	0	1	0	0	1	69	0.770
0	1	1	0	1	0	1	0	6A	0.775
0	1	1	0	1	0	1	1	6B	0.780
0	1	1	0	1	1	0	0	6C	0.785
0	1	1	0	1	1	0	1	6D	0.790
0	1	1	0	1	1	1	0	6E	0.795
0	1	1	0	1	1	1	1	6F	0.800
0	1	1	1	0	0	0	0	70	0.805
0	1	1	1	0	0	0	1	71	0.810
0	1	1	1	0	0	1	0	72	0.815
0	1	1	1	0	0	1	1	73	0.820
0	1	1	1	0	1	0	0	74	0.825
0	1	1	1	0	1	0	1	75	0.830
0	1	1	1	0	1	1	0	76	0.835
0	1	1	1	0	1	1	1	77	0.840
0	1	1	1	1	0	0	0	78	0.845
0	1	1	1	1	0	0	1	79	0.850
0	1	1	1	1	0	1	0	7A	0.855

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	1	1	1	1	0	1	1	7B	0.860
0	1	1	1	1	1	0	0	7C	0.865
0	1	1	1	1	1	0	1	7D	0.870
0	1	1	1	1	1	1	0	7E	0.875
0	1	1	1	1	1	1	1	7F	0.880
1	0	0	0	0	0	0	0	80	0.885
1	0	0	0	0	0	0	1	81	0.890
1	0	0	0	0	0	1	0	82	0.895
1	0	0	0	0	0	1	1	83	0.900
1	0	0	0	0	1	0	0	84	0.905
1	0	0	0	0	1	0	1	85	0.910
1	0	0	0	0	1	1	0	86	0.915
1	0	0	0	0	1	1	1	87	0.920
1	0	0	0	1	0	0	0	88	0.925
1	0	0	0	1	0	0	1	89	0.930
1	0	0	0	1	0	1	0	8A	0.935
1	0	0	0	1	0	1	1	8B	0.940
1	0	0	0	1	1	0	0	8C	0.945
1	0	0	0	1	1	0	1	8D	0.950
1	0	0	0	1	1	1	0	8E	0.955
1	0	0	0	1	1	1	1	8F	0.960
1	0	0	1	0	0	0	0	90	0.965
1	0	0	1	0	0	0	1	91	0.970
1	0	0	1	0	0	1	0	92	0.975
1	0	0	1	0	0	1	1	93	0.980
1	0	0	1	0	1	0	0	94	0.985
1	0	0	1	0	1	0	1	95	0.990
1	0	0	1	0	1	1	0	96	0.995
1	0	0	1	0	1	1	1	97	1.000
1	0	0	1	1	0	0	0	98	1.005
1	0	0	1	1	0	0	1	99	1.010
1	0	0	1	1	0	1	0	9A	1.015
1	0	0	1	1	0	1	1	9B	1.020
1	0	0	1	1	1	0	0	9C	1.025
1	0	0	1	1	1	0	1	9D	1.030
1	0	0	1	1	1	1	0	9E	1.035
1	0	0	1	1	1	1	1	9F	1.040
1	0	1	0	0	0	0	0	A0	1.045
1	0	1	0	0	0	0	1	A1	1.050
1	0	1	0	0	0	1	0	A2	1.055
1	0	1	0	0	0	1	1	A3	1.060

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
1	0	1	0	0	1	0	0	A4	1.065
1	0	1	0	0	1	0	1	A5	1.070
1	0	1	0	0	1	1	0	A6	1.075
1	0	1	0	0	1	1	1	A7	1.080
1	0	1	0	1	0	0	0	A8	1.085
1	0	1	0	1	0	0	1	A9	1.090
1	0	1	0	1	0	1	0	AA	1.095
1	0	1	0	1	0	1	1	AB	1.100
1	0	1	0	1	1	0	0	AC	1.105
1	0	1	0	1	1	0	1	AD	1.110
1	0	1	0	1	1	1	0	AE	1.115
1	0	1	0	1	1	1	1	AF	1.120
1	0	1	1	0	0	0	0	B0	1.125
1	0	1	1	0	0	0	1	B1	1.130
1	0	1	1	0	0	1	0	B2	1.135
1	0	1	1	0	0	1	1	B3	1.140
1	0	1	1	0	1	0	0	B4	1.145
1	0	1	1	0	1	0	1	B5	1.150
1	0	1	1	0	1	1	0	B6	1.155
1	0	1	1	0	1	1	1	B7	1.160
1	0	1	1	1	0	0	0	B8	1.165
1	0	1	1	1	0	0	1	B9	1.170
1	0	1	1	1	0	1	0	BA	1.175
1	0	1	1	1	0	1	1	BB	1.180
1	0	1	1	1	1	0	0	BC	1.185
1	0	1	1	1	1	0	1	BD	1.190
1	0	1	1	1	1	1	0	BE	1.195
1	0	1	1	1	1	1	1	BF	1.200
1	1	0	0	0	0	0	0	C0	1.205
1	1	0	0	0	0	0	1	C1	1.210
1	1	0	0	0	0	1	0	C2	1.215
1	1	0	0	0	0	1	1	C3	1.220
1	1	0	0	0	1	0	0	C4	1.225
1	1	0	0	0	1	0	1	C5	1.230
1	1	0	0	0	1	1	0	C6	1.235
1	1	0	0	0	1	1	1	C7	1.240
1	1	0	0	1	0	0	0	C8	1.245
1	1	0	0	1	0	0	1	C9	1.250
1	1	0	0	1	0	1	0	CA	1.255
1	1	0	0	1	0	1	1	CB	1.260
1	1	0	0	1	1	0	0	CC	1.265

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
1	1	0	0	1	1	0	1	CD	1.270
1	1	0	0	1	1	1	0	CE	1.275
1	1	0	0	1	1	1	1	CF	1.280
1	1	0	1	0	0	0	0	D0	1.285
1	1	0	1	0	0	0	1	D1	1.290
1	1	0	1	0	0	1	0	D2	1.295
1	1	0	1	0	0	1	1	D3	1.300
1	1	0	1	0	1	0	0	D4	1.305
1	1	0	1	0	1	0	1	D5	1.310
1	1	0	1	0	1	1	0	D6	1.315
1	1	0	1	0	1	1	1	D7	1.320
1	1	0	1	1	0	0	0	D8	1.325
1	1	0	1	1	0	0	1	D9	1.330
1	1	0	1	1	0	1	0	DA	1.335
1	1	0	1	1	0	1	1	DB	1.340
1	1	0	1	1	1	0	0	DC	1.345
1	1	0	1	1	1	0	1	DD	1.350
1	1	0	1	1	1	1	0	DE	1.355
1	1	0	1	1	1	1	1	DF	1.360
1	1	1	0	0	0	0	0	E0	1.365
1	1	1	0	0	0	0	1	E1	1.370
1	1	1	0	0	0	1	0	E2	1.375
1	1	1	0	0	0	1	1	E3	1.380
1	1	1	0	0	1	0	0	E4	1.385
1	1	1	0	0	1	0	1	E5	1.390
1	1	1	0	0	1	1	0	E6	1.395
1	1	1	0	0	1	1	1	E7	1.400
1	1	1	0	1	0	0	0	E8	1.405
1	1	1	0	1	0	0	1	E9	1.410
1	1	1	0	1	0	1	0	EA	1.415
1	1	1	0	1	0	1	1	EB	1.420
1	1	1	0	1	1	0	0	EC	1.425
1	1	1	0	1	1	0	1	ED	1.430
1	1	1	0	1	1	1	0	EE	1.435
1	1	1	0	1	1	1	1	EF	1.440
1	1	1	1	0	0	0	0	F0	1.445
1	1	1	1	0	0	0	1	F1	1.450
1	1	1	1	0	0	1	0	F2	1.455
1	1	1	1	0	0	1	1	F3	1.460
1	1	1	1	0	1	0	0	F4	1.465
1	1	1	1	0	1	0	1	F5	1.470

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
1	1	1	1	0	1	1	0	F6	1.475
1	1	1	1	0	1	1	1	F7	1.480
1	1	1	1	1	0	0	0	F8	1.485
1	1	1	1	1	0	0	1	F9	1.490
1	1	1	1	1	0	1	0	FA	1.495
1	1	1	1	1	0	1	1	FB	1.500
1	1	1	1	1	1	0	0	FC	1.505
1	1	1	1	1	1	0	1	FD	1.510
1	1	1	1	1	1	1	0	FE	1.515
1	1	1	1	1	1	1	1	FF	1.520

Table 2. Standard Serial VID Commands

Code	Commands	Master Payload Contents	Slave Payload Contents	Description
00h	not supported	N/A	N/A	N/A
01h	SetVID_Fast	VID code	N/A	1. Set new target VID code, VR jumps to new VID target with controlled default "fast" slew rate 13.2mV/μs. 2. Set VR_Settled when VR reaches target VID voltage.
02h	SetVID_Slow	VID code	N/A	1. Set new target VID code, VR jumps to new VID target with controlled default "slow" slew rate 3.3mV/μs. 2. Set VR_Settled when VR reaches target VID voltage.
03h	SetVID_Decay	VID code	N/A	1. Set new target VID code, VR jumps to new VID target, but does not control the slew rate. The output voltage decays at a rate proportional to the load current. 2. Low-side MOSFET is not allowed to sync current. 3. ACK 11b when target higher than current VOUT voltage. 4. ACK 10b when target lower than current VOUT voltage.
04h	SetPS	Byte indicating power states	N/A	1. Set power state. 2. ACK 11b when not support. 3. ACK 10b even slave not change configuration. 4. ACK 11b for still running SetVID command. 5. VR remains in lower state when receiving SetVID (decay).
05h	SetRegADR	Pointer of registers in data table	N/A	1. Set the pointer of the data register. 2. ACK 11b for address outside of support. 3. NAK 01b for SetADR (all call).
06h	SetReg DAT	New data register content	N/A	1. Write the contents to the data register. 2. NAK 01b for SetReg (all call).
07h	GetReg		Specified Register Contents	1. Slave returns the contents of the specified register as the payload. 2. ACK 11b for non support address. 3. NAK 01b for GetReg (all call).
08h to 1Fh	not supported	N/A	N/A	N/A

Table3. SVID Data and Configuration Register

Index	Register Name	Description	Access	Default
00h	Vendor ID	Vendor ID	RO, Vendor	1Eh
01h	Product ID	Product ID	RO, Vendor	76h
02h	Product Revision	Product Revision	RO, Vendor	00h
05h	Protocol ID	SVID Protocol ID	RO, Vendor	06h
06h	Capability	Bit mapped register, identifies the SVID VR Capabilities and which of the optional telemetry register is supported.	RO, Vendor	81h
10h	Status_1	Data register containing the status of VR.	R-M, W-PWM	00h
11h	Status_2	Data register containing the status of transmission.	R-M, W-PWM	00h
12h	Temperature Zone	Data register showing temperature zone that has been entered.	R-M, W-PWM	00h
15h	IOUT	At PS0 to PS2, IOUT report data from ADC sense IMON voltage. When power state at PS3, the IOUT report data is fix to 04h.	R-M, W-PWM	00h
1Ch	Status_2_lastread	The register contains a copy of the status_2.	R-M, W-PWM	00h
21h	ICC Max	Data register containing the ICC max the platform supports. Binary format in A IE 64h = 100A.	RO, Platform	7Dh
22h	Temp Max	Data register containing the temperature max the platform supports. Binary format in °C IE 64h = 100°C.	RO, Platform	64h
24h	SR-fast	Data register containing the capability of fast slew rate the platform can sustain. Binary format in mV/μS IE 0Ch = 12mV/μs.	RO	0Ch
25h	SR-slow	Data register containing the capability of slow slew rate. Binary format in mV/μS IE 03h = 3mV/μS.	RO	03h
2Ah	Slow Slew Rate Selector	The register is programmed by master and set the slow slew rate.	RW, Master	02h
2Bh	PS4 Exit Latency	Data register containing the latency of exiting PS4.	RO	77h
2Ch	PS3 Exit Latency	Data register containing the latency of exiting PS3.	RO	3Fh
2Dh	Enable to Ready for SVID	Data register containing the latency from Enable assertion to the VR being ready to accept an SVID command.	RO	BAh
30h	VOUT Max	The register is programmed by master and sets the maximum VID.	RW, Master	D5h
31h	VID Setting	Data register containing currently programmed VID.	RW, Master	00h
32h	Power State	Register containing the current programmed power state.	RW, Master	00h
33h	Offset	Set offset in VID steps.	RW, Master	00h
34h	Multi VR Configuration	Bit mapped data register which configures multiple VRs behavior on the same bus.	RW, Master	01h
35h	Pointer	Scratch pad register for temporary storage of the SetRegADR pointer register.	RW, Master	30h

Notes :

RO = Read Only

RW = Read/Write

R-M = Read by Master

W-PWM = Write by PWM Only

Vendor = Hard Coded by VR Vendor

Platform = Programmed by the Master

PWM = Programmed by the VR Control IC

Absolute Maximum Ratings (Note 1)

- VCC, PVCC to GND ---------- –0.3V to 6V
- RGND to GND ---------- –0.3V to 0.3V
- TONSET to GND ---------- –0.3V to 7.5V
- BOOT to PHASE ---------- –0.3V to 6V
- PHASE to GND
  DC ---------- –0.3V to 32V
  < 20ns ---------- –8V to 38V
- LGATE to GND
  DC ---------- (GND – 0.3V) to 6V
  < 20ns ---------- (GND – 5V) to 7.5V
- UGATE to PHASE
  DC ---------- (GND – 0.3V) to 6V
  < 20ns ---------- (GND – 5V) to 7.5V
- Other Pins ---------- –0.3V to (V_{CC} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-32L 4x4 ---------- 3.59W
- Package Thermal Resistance (Note 2)
  WQFN-32L 4x4, θ_{JA} ---------- 27.8°C/W
  WQFN-32L 4x4, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, PVCC ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{VCC}	V_{EN} = H, No switching	--	3.6	--	mA
Supply Current at PS3	I_{VCC_PS3}	V_{EN} = H, No switching	--	1.2	--	mA
Supply Current at PS4	I_{VCC_PS4}	V_{EN} = H, No switching	--	--	200	μA
Power Supply Voltage	PVCC		4.5	--	5.5	V
Power Supply Current	I_{PVCC}	No Switching	--	80	--	μA
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	5	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference and DAC						
DAC Accuracy	V_{FB}	V_{DAC} = 0.8V – 1.52V	–0.5	0	0.5	% of VID
		V_{DAC} = 0.5V – 0.795V	–8	0	8	mV
		V_{DAC} = 0.25V – 0.495V	–10	0	10	
PVCC Power On Reset (POR)						
POR Threshold	V_{POR_r}	PVCC Rising	--	4.2	4.5	V
	V_{POR_f}	PVCC Falling	3.5	3.84	--	
POR Hysteresis	V_{POR_HYS}		--	360	--	mV
Slew Rate						
Dynamic VID Slew Rate	SR	SetVID Slow	2.5	3.3	3.6	mV/μs
		SetVID Fast	12.5	13.2	14.4	
EA Amplifier						
DC Gain	A_{DC}	R_L = 47kΩ	70	--	--	dB
Gain-Bandwidth Product	G_{BW}	C_{LOAD} = 5pF	--	5	--	MHz
Slew Rate	SR_{EA}	C_{LOAD} = 10pF (Gain = –4, R_F = 47kΩ, V_{OUT} = 0.5V to –3V)	5	--	--	V/μs
Output Voltage Range	V_{COMP}	R_L = 47kΩ	0.5	--	3.6	V
Maximum Source/Sink Current	I_{OUTEA}	V_{COMP} = 2V	--	5	--	mA
Load-Line Current Gain Amplifier						
Input Offset Voltage	V_{ILOFS}	V_{IMON} = 1V	–5	--	5	mV
Current Gain	A_{ILGAIN}	$V_{IMON} – V_{VREF}$ = 1V, $V_{FB} = V_{COMP}$ = 1V	--	1/6	--	A/A
Current Sensing Amplifier						
Input Offset Voltage	V_{OSCS}		–0.8	--	0.8	mV
Impedance at Positive Input	R_{ISENP}		1	--	--	MΩ
Current Mirror Gain	A_{MIRROR}	$\Delta I_{IMON} / \Delta I_{SENN}$	0.97	1	1.03	A/A
TON Setting						
TONSET Pin Voltage	V_{TON}	$I_{RTON} = \frac{20}{3}\ \mu A$, V_{DAC} = 1V, SET3 = f_{SW} > 500kHz	--	1	--	V
On-Time Setting	T_{ON}	$I_{RTON} = \frac{20}{3}\ \mu A$, V_{DAC} = 1V, SET3 = f_{SW} > 500kHz	256	285	314	ns
Input Current Range	I_{RTON}	V_{DAC} = 1V, SET3 = f_{SW} > 500kHz	2	--	24	μA
Minimum Off-time	T_{OFF}	$I_{RTON} = \frac{20}{3}\ \mu A$, V_{DAC} = 1V, SET3 = f_{SW} > 500kHz	--	150	--	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IBIAS						
IBIAS Pin Voltage	V_{IBIAS}	R_{IBIAS} = 100kΩ	1.95	2	2.05	V
Protections						
Under Voltage Lockout Threshold	V_{UVLO}		4.1	4.3	4.45	V
	ΔV_{UVLO}	Falling edge hysteresis	--	200	--	mV
Over Voltage Protection Threshold	V_{OV}	VID higher than 1.2V	VID + 300	VID + 350	VID + 400	mV
		VID lower than 1.2V	1500	1550	1600	
Under Voltage Protection Threshold	V_{UV}	Respect to VID voltage	–400	–350	–300	mV
Negative Voltage Protection Threshold	V_{NV}		–100	–50	--	mV
EN and VR_READY						
EN Input Voltage Logic-High	V_{IH}		0.7	--	--	V
EN Input Voltage Logic-Low	V_{IL}		--	--	0.3	
Leakage Current of EN			–1	--	1	μA
VR_READY Delay	T_{VR_READY}	V_{SEN} = VBoot to VR_READY High	3	5	6	μs
VR_READY Pull Low Voltage	V_{PGOOD}	I_{VR_READY} = 10mA	--	--	0.13	V
Serial VID and $\overline{VR\_HOT}$						
VCLK, VDIO	V_{IH}	Respect to INTEL Spec. with 50mV hysteresis	0.65	--	--	V
	V_{IL}		--	--	0.45	
Leakage Current of VCLK, VDIO, $\overline{ALERT}$ and $\overline{VR\_HOT}$	I_{LEAK_IN}		–1	--	1	μA
VDIO, $\overline{ALERT}$ and $\overline{VR\_HOT}$ Pull Low Voltage		I_{VDIO} = 10mA	--	--	0.13	V
		$I_{\overline{ALERT}}$ = 10mA				
		$I_{\overline{VR\_HOT}}$ = 10mA				
V_{REF} and V_{BOOT}						
V_{REF} Voltage	V_{REF}		0.55	0.6	0.65	V
V_{BOOT} Voltage	V_{BOOT}	V_{BOOT} Voltage set to 1V	0.995	1	1.005	V
ADC						
Digital IMON Set	V_{IMON}	$V_{IMON} – V_{IMON\_INI}$ = 0.4V	--	255	--	Decimal
		$V_{IMON} – V_{IMON\_INI}$ = 0.2V	--	128	--	
		$V_{IMON} – V_{IMON\_INI}$ = 0V	--	0	--	
Update Period of IMON	T_{IMON}		--	400	--	μs
TSEN Threshold for Tmp_Zone [7] transition	V_{TSEN}	100°C	--	1.887	--	V
TSEN Threshold for Tmp_Zone [6] transition	V_{TSEN}	97°C	--	1.837	--	V
TSEN Threshold for Tmp_Zone [5] transition	V_{TSEN}	94°C	--	1.784	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TSEN Threshold for Tmp_Zone [4] transition	V_{TSEN}	91°C	--	1.729	--	V
TSEN Threshold for Tmp_Zone [3] transition	V_{TSEN}	88°C	--	1.672	--	V
TSEN Threshold for Tmp_Zone [2] transition	V_{TSEN}	85°C	--	1.612	--	V
TSEN Threshold for Tmp_Zone [1] transition	V_{TSEN}	82°C	--	1.551	--	V
TSEN Threshold for Tmp_Zone [0] transition	V_{TSEN}	75°C	--	1.402	--	V
Update Period of TSEN	t_{TSEN}		--	50	--	µs
Digital Code of ICCMAX	$C_{ICCMAX1}$	V_{ICCMAX} = 0.7V	58	64	70	Decimal
	$C_{ICCMAX2}$	V_{ICCMAX} = 0.8V	122	128	134	
	$C_{ICCMAX3}$	V_{ICCMAX} = 1V	248	256	260	
Switching Time						
UGATE Rise Time	t_{UGATEr}	3nF load	--	8	--	ns
UGATE Fall Time	t_{UGATEf}	3nF load	--	8	--	ns
LGATE Rise Time	t_{LGATEr}	3nF load	--	8	--	ns
LGATE Fall Time	t_{LGATEf}	3nF load	--	4	--	ns
UGATE Turn-Off Propagation Delay	t_{PDLU}	Outputs Unloaded	--	35	--	ns
LGATE Turn-Off Propagation Delay	t_{PDLL}	Outputs Unloaded	--	35	--	ns
UGATE Turn-On Propagation Delay	t_{PDHU}	Outputs Unloaded	--	20	--	ns
LGATE Turn-On Propagation Delay	t_{PDHL}	Outputs Unloaded	--	20	--	ns
UGATE/LGATE Tri-State Propagation Delay	t_{PTS}	Outputs Unloaded	--	35	--	ns
Output						
UGATE Driver Source Resistance	$R_{UGATEsr}$	100mA Source Current	--	1	--	Ω
UGATE Driver Source Current	$I_{UGATEsr}$	$V_{UGATE} - V_{PHASE}$ = 2.5V	--	2	--	A
UGATE Driver Sink Resistance	$R_{UGATEsk}$	100mA Sink Current	--	1	--	Ω
UGATE Driver Sink Current	$I_{UGATEsk}$	$V_{UGATE} - V_{PHASE}$ = 2.5V	--	2	--	A
LGATE Driver Source Resistance	$R_{LGATEsr}$	100mA Source Current	--	1	--	Ω
LGATE Driver Source Current	$I_{LGATEsr}$	V_{LGATE} = 2.5V	--	2	--	A
LGATE Driver Sink Resistance	$R_{LGATEsk}$	100mA Sink Current	--	0.5	--	Ω
LGATE Driver Sink Current	$I_{LGATEsk}$	V_{LGATE} = 2.5V	--	4	--	A

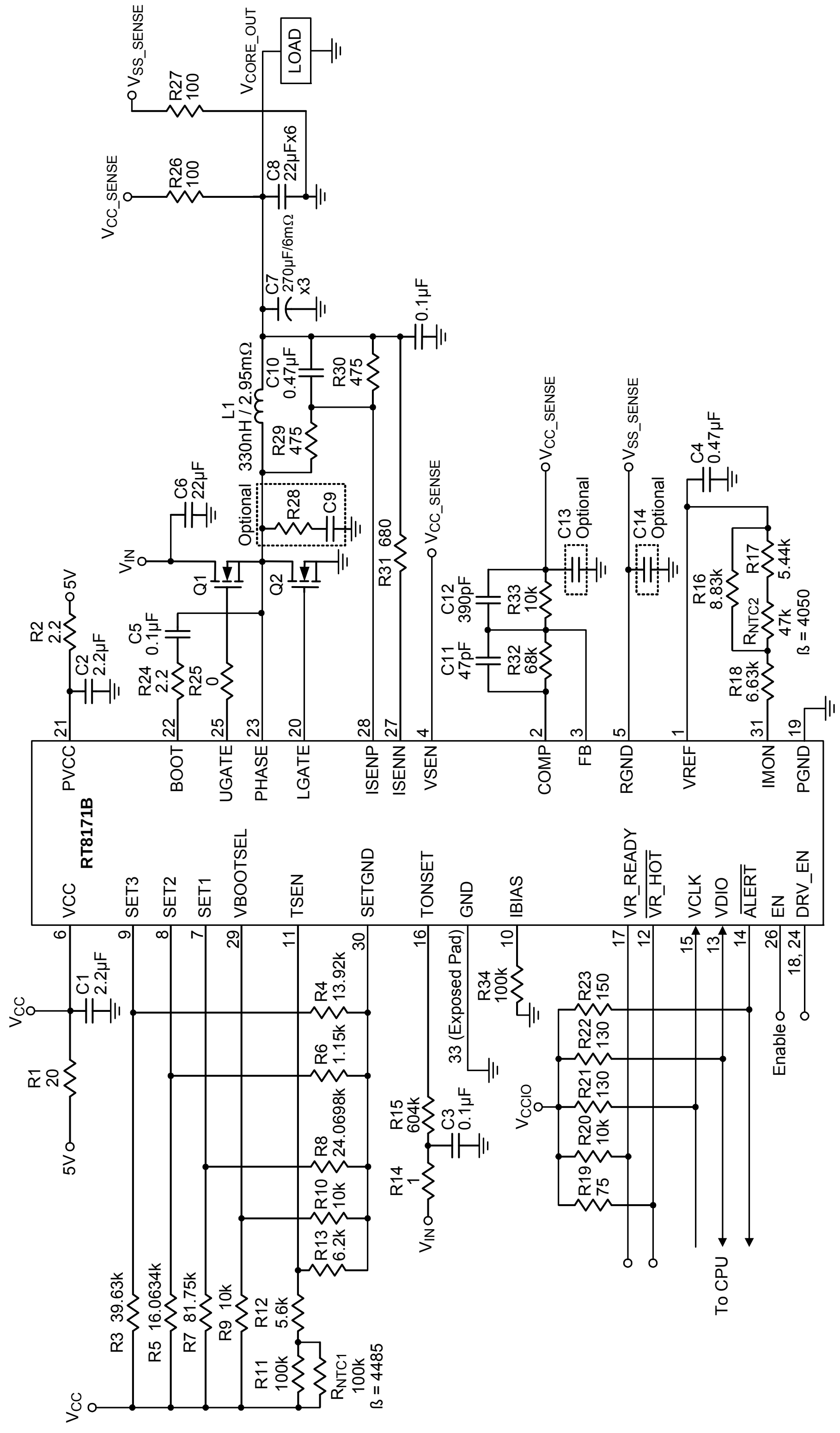
Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at $T_A = 25°C$ on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

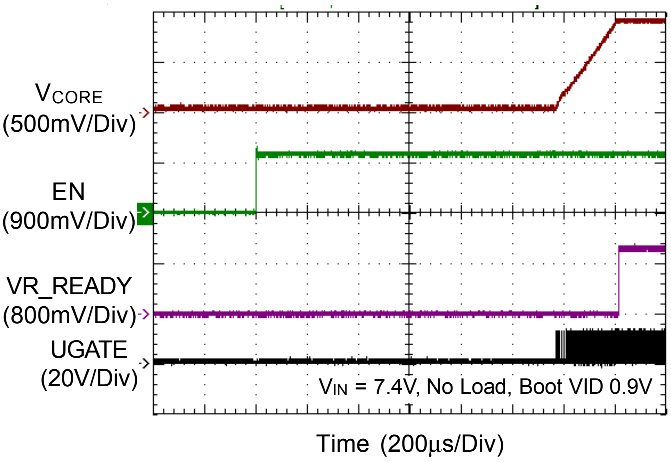
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

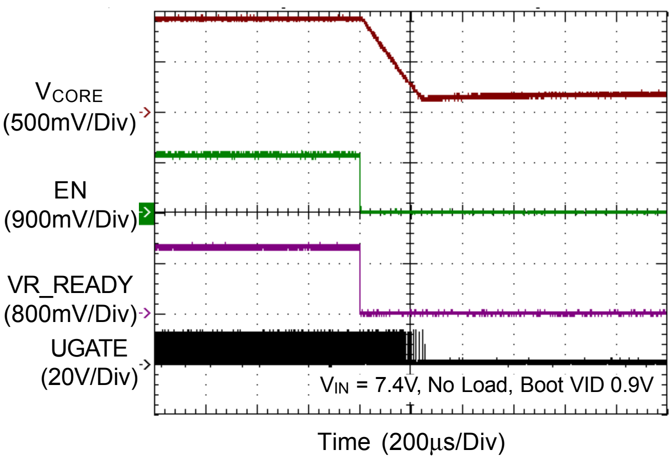


Typical Operating Characteristics

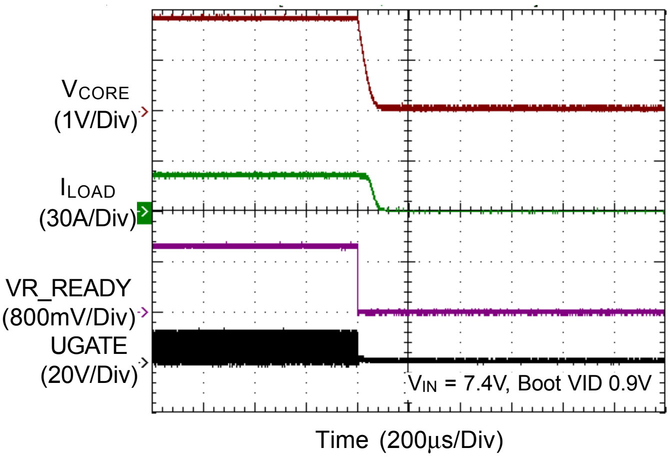
CORE VR Power On from EN



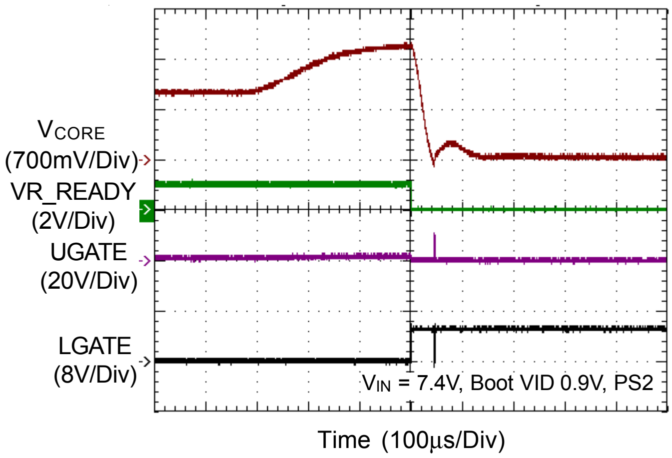
CORE VR Power Off from EN



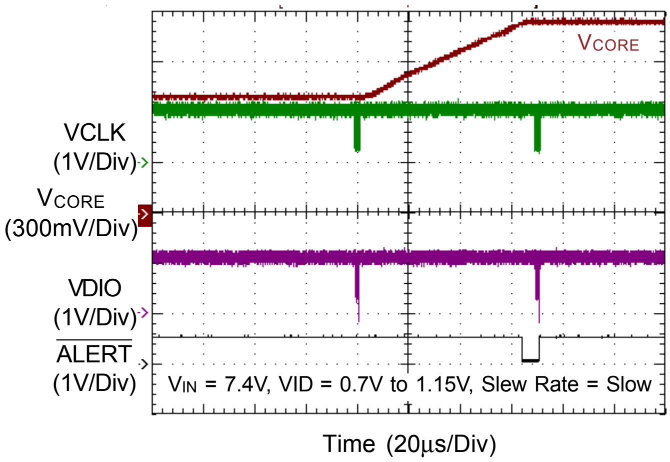
CORE VR OCP



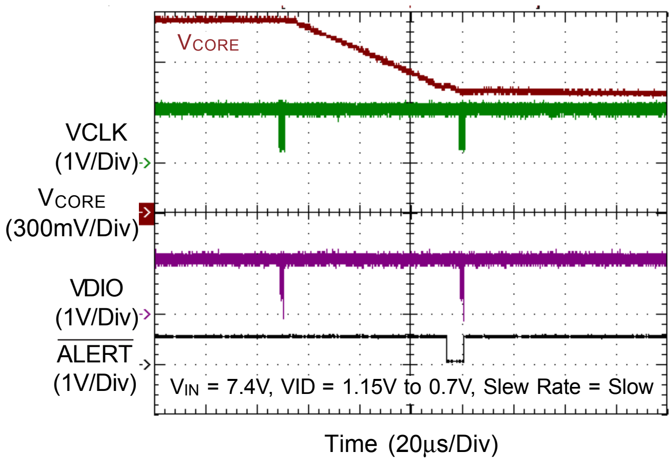
CORE VR OVP



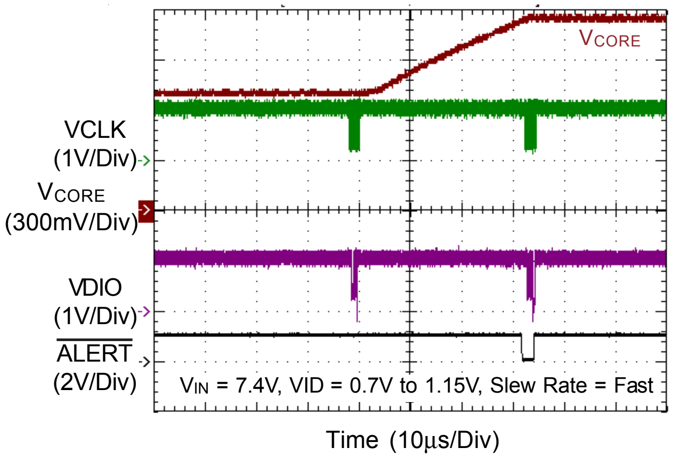
CORE VR Dynamic VID Up



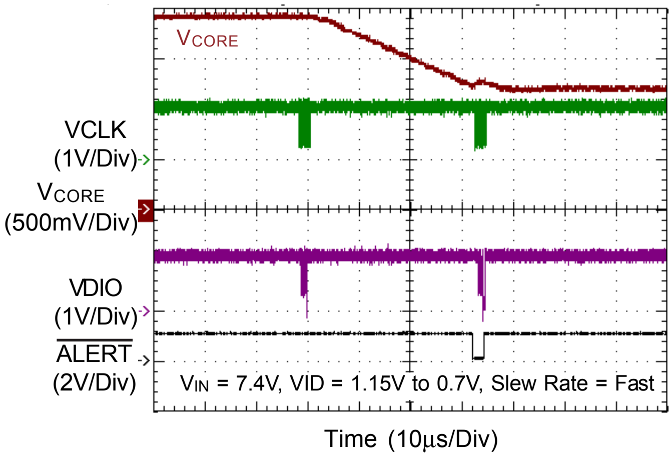
CORE VR Dynamic VID Down



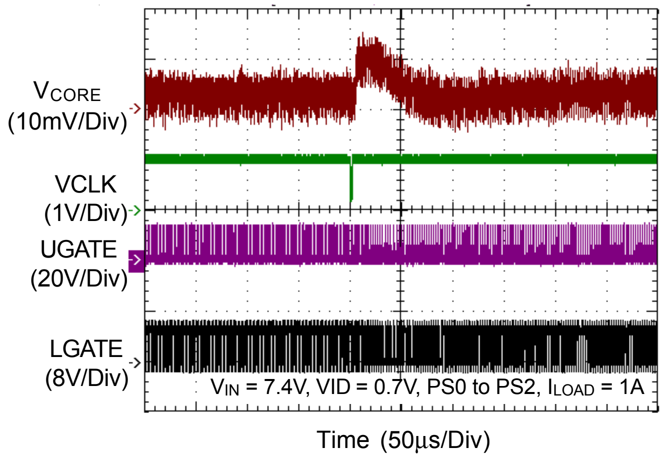
CORE VR Dynamic VID Up



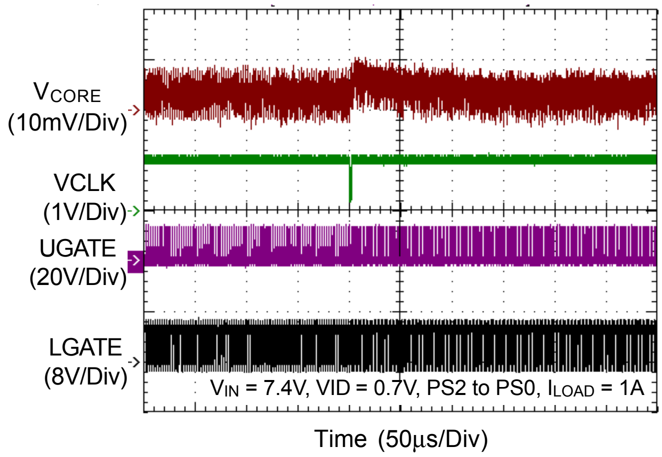
CORE VR Dynamic VID Down



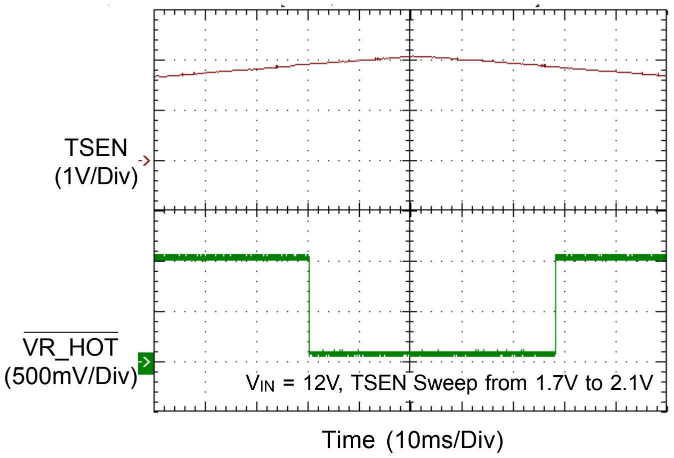
CORE VR Mode Transient



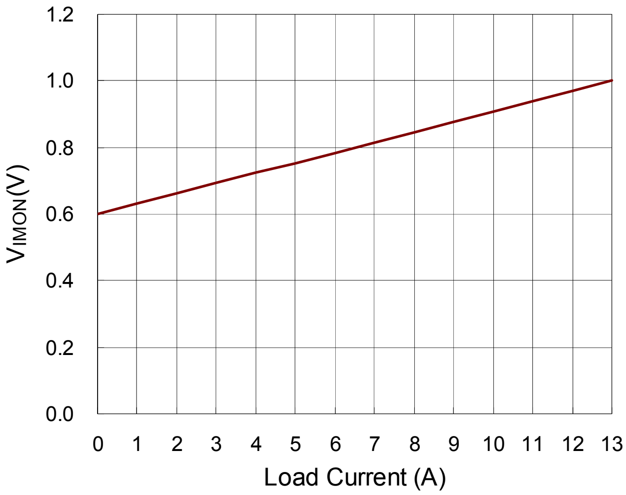
CORE VR Mode Transient



CORE VR Thermal Monitoring



V_{IMON} vs. Load Current



Applications Information

The RT8171B is a single phase synchronous Buck controller designed to meet Intel VR12.1 compatible CPU specification with a serial SVID control interface. The controller uses an ADC to implement all kinds of settings to save a total number of pins for easily using and increasing PCB space utilization.

G-NAVP^{TM} Control Mode

The RT8171B adopts the G-NAVP^{TM} controller, which is a current mode constant on-time control with DC offset cancellation. The approach can not only improve DC offset problem for increasing system accuracy but also provide fast transient response. For the RT8171B, when current feedback signal reaches comp signal to generate an on-time width to achieve PWM modulation. Figure 1 shows the basic G-NAVP^{TM} behavior waveforms in Continuous Conduct Mode (CCM).

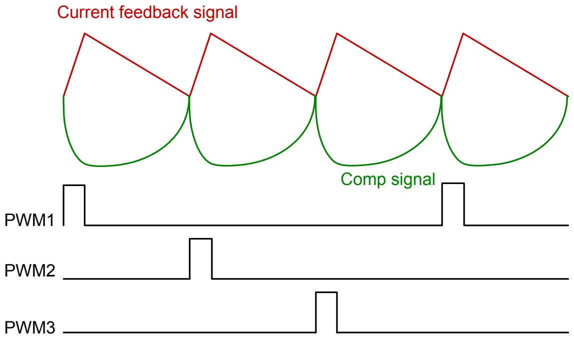


Figure 1 (a). G-NAVP^{TM} Behavior Waveforms in CCM in Steady State

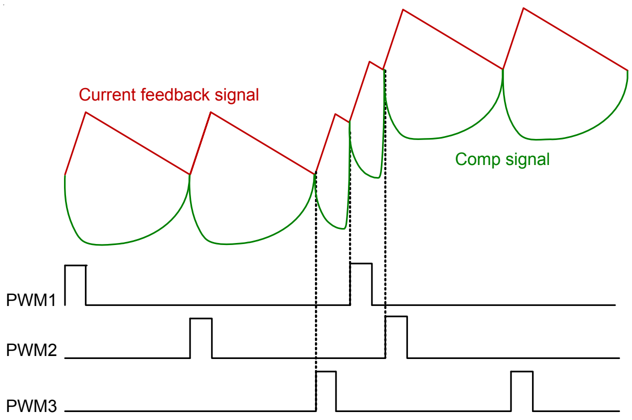


Figure 1 (b). G-NAVP^{TM} Behavior Waveforms in CCM in Load Transient

Diode Emulation Mode (DEM)

As well-known, the dominate power loss is switching related loss during light load, hence VR needs to be operated in asynchronous mode (or called discontinuous conduct mode, DCM) to reduce switching related loss since switching frequency is dependent on loading in the asynchronous mode. RT8171B can operate in Diode Emulation Mode (DEM) in order to improve light load efficiency. In DEM operation, the behavior of the low-side MOSFET needs to work like a diode, that is, the low-side MOSFET will be turned on when the DCR network voltage is higher than the ZCD_TH, i.e. the inductor current follows from source to drain of low-side MOSFET. The low-side MOSFET will be turned off when DCR network is lower than the ZCD_TH, i.e. reversed current is not allowed. The positive voltage threshold (ZCD threshold) of low-side MOSFET turn off is set by the SET3 pin in Table 9. Figure 2 shows the control behavior in DEM. Figure 3 shows the G-NAVP^{TM} operation in DEM to illustrate the control behaviors. When the load decreases, the discharge time of output capacitors increases during UGATE and LGATE are turned off. Hence, the switching frequency and switching losses will be reduced to improve efficiency in light load condition.

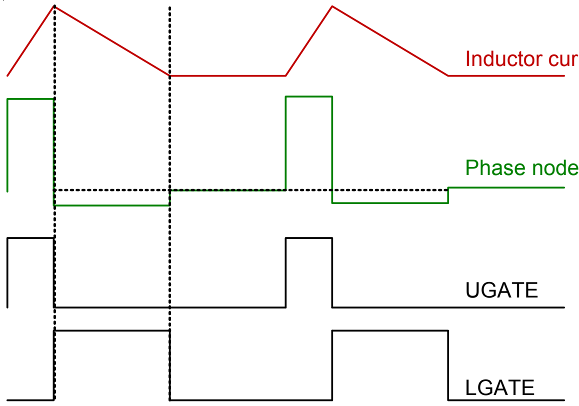
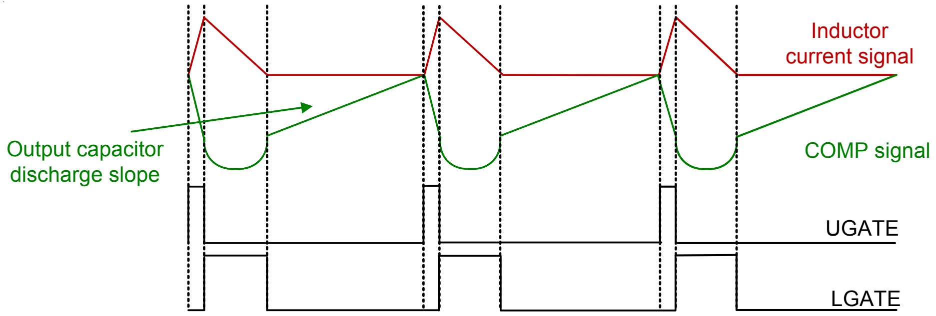
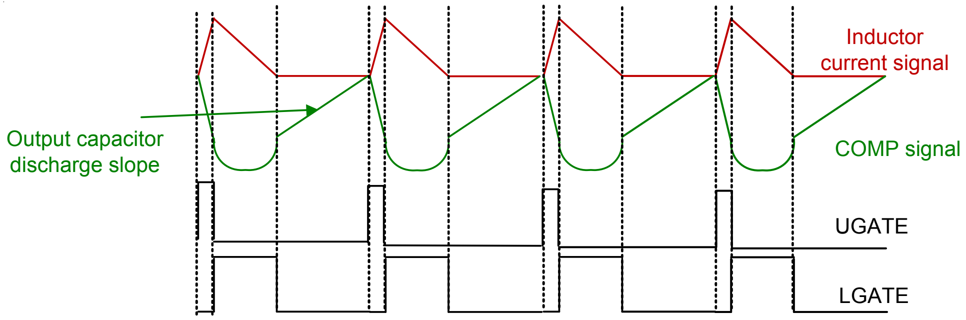


Figure 2. Diode Emulation Mode (DEM) in Steady State



(a) Lighter Load Condition in DEM.
Capacitor discharge slope is lower than Figure 3 (b).



(b) Load Increased Condition in DEM.
Capacitor discharge slope is Higher than Figure 3 (a).

Figure 3. G-NAVP^{TM} Operation in DEM.

Switching Frequency (TON) Setting

RT8171B is one kind of constant on-time control. The patented CCRCOT (Constant Current Ripple COT) technology can generate an adaptive on-time with input voltage and VID code to obtain a constant current ripple. So that the output voltage ripple can be controlled nearly like a constant as different input and output voltage change. Connect a resistor R_{TON} between input voltage terminal and TONSET pin to set the on-time width.

In order to meet Intel VR12.1 quiescent power specification at PS3 and PS4, RT8171B provides two different coefficients for T_{ON}. And these coefficients can be setting by SET3 pin, as shown in Tablet 9. So, RT8171B can pass quiescent power for all range switching frequency at PS3 and PS4 under battery mode condition.

For SET3 pin $f_{SW} \leq 500kHz$,

$$T_{ON} = \frac{R_{TON} \times C \times 0.22}{V_{IN} - V_{DAC}} \quad (V_{DAC} < 1.2V)$$

$$T_{ON} = \frac{R_{TON} \times C \times V_{DAC} / 5.45}{V_{IN} - 1.2} \quad (V_{DAC} \geq 1.2V)$$

For SET3 pin $f_{SW} > 500kHz$

$$T_{ON} = \frac{R_{TON} \times C \times 0.11}{V_{IN} - V_{DAC}} \quad (V_{DAC} < 1.2V)$$

$$T_{ON} = \frac{R_{TON} \times C \times V_{DAC} / 10.9}{V_{IN} - 1.2} \quad (V_{DAC} \geq 1.2V)$$

Where C = 18.2pF. By using the relationship between T_{ON} and f_{SW}, the switching frequency f_{SW} is :

$$f_{SW(MAX)} = \left(\frac{1}{T_{ON(MAX)}}\right) \times \left(\frac{V_{DAC(MAX)}}{V_{IN(MAX)}}\right)$$

Where

$f_{SW(MAX)}$ is the maximum switching frequency.

$V_{DAC(MAX)}$ is the maximum VDAC of application.

$V_{IN(MAX)}$ is the maximum application input voltage.

$T_{ON(MAX)}$ is the on-time width.

When load increases, on-time keeps constant. The off-time width will be reduced so that loading can load more power from input terminal to regulate output voltage. Hence, the loading current increases in case the switching frequency also increases. Higher switching frequency operation can reduce power component's size and PCB space, trading off the whole efficiency since switching related loss increases, vice versa.

Please note that the actual switching frequency is also dependent on the losses in the main power stage and the driver characteristic. So, in order to get more accuracy switching frequency the form of the switching frequency can be rewrote as below :

$$f_{SW(MAX)} = \frac{V_{DAC(MAX)} + I_{CC(MAX)} \times (DCR + R_{ON-LS} - R_{LL})}{\left[V_{IN(MAX)} + I_{CC(MAX)} \times (R_{ON-LS} - R_{ON-HS})\right] \times (T_{ON} - T_D + T_{ON,VAR}) + I_{CC(MAX)} \times R_{ON-LS} \times T_D}$$

Where $f_{SW(MAX)}$ is the maximum switching frequency, $V_{DAC(MAX)}$ is the maximum application VID, $V_{IN(MAX)}$ is the maximum input voltage, $I_{CC(MAX)}$ is the maximum load current, DCR is the inductor DC resistance, R_{ON-HS} is the equivalent high-side $R_{DS(ON)}$, R_{ON-LS} is the equivalent low-side $R_{DS(ON)}$, T_D is the driver dead time , R_{LL} is the loadline value, $T_{ON,VAR}$ is the T_{ON} variation value.

Above method can keep the constant current ripple, whether V_{IN} and VID are variation. But this method will generate large power consumption on TONSET pin. In order to reduce the power consumption on TONSET pin, here can connect a resister R_{TON} between V_{CC} and TONSET pin to set the on-time width.

The on-time width equation can be rewritten as below.

For SET3 pin $f_{SW} \leq 500\text{kHz}$,

$$T_{ON} = \frac{R_{TON} \times C \times 0.22}{V_{CC} - V_{DAC}} \quad (V_{DAC} < 1.2V)$$

$$T_{ON} = \frac{R_{TON} \times C \times V_{DAC} / 5.45}{V_{CC} - 1.2} \quad (V_{DAC} \geq 1.2V)$$

For SET3 pin $f_{SW} > 500\text{kHz}$,

$$T_{ON} = \frac{R_{TON} \times C \times 0.11}{V_{CC} - V_{DAC}} \quad (V_{DAC} < 1.2V)$$

$$T_{ON} = \frac{R_{TON} \times C \times V_{DAC} / 10.9}{V_{CC} - 1.2} \quad (V_{DAC} \geq 1.2V)$$

This method can saving power disspation on TONSET pin but it will loss the constant current ripple merit. So, this method can be used under V_{IN} is fixed application.

Current Sense

In the RT8171B, the current signal is used for load-line setting and OC (Over Current) protection. The inductor current sense method adopts the lossless current sensing for allowing high efficiency as illustrated in the Figure 4. When inductance and DCR_X time constant is equal to R_XC_X filter network time constant, a voltage $I_{LX} \times DCR_X$ will drop on C_X to generate inductor current signal. According to the Figure 4, the ISENN is as follows :

$$ISENN = \frac{I_{LX} \times DCR_X}{R_{CSX}}$$

Where $L_X / DCR_X = R_XC_X$ is held. The method can get high efficiency performance, but DCR_X value will be drifted by temperature, a NTC resistor should add in the resistor network in the IMON pin to achieve DCR_X thermal compensation.

It's noted that, in order to avoid current amplifier being saturated. When (I_{LX} x DCR_X) is larger than 140mV, the current sense method should be adopted method II as illustrated in Figure 5. According to Figure 5, the R_X is as follows :

$$R_X = R_{X1} \,//\, R_{X2}$$

The resistance accuracy of R_{CSX} is recommended to be 1% or higher. And in order to get impedance matching, the R_{CSX} must be placed 680Ω resistor.

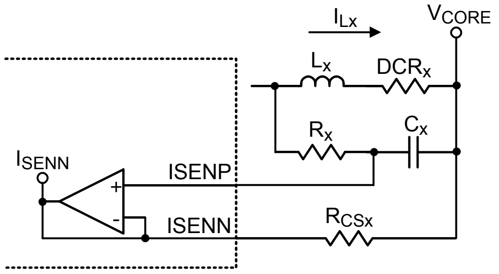


Figure 4. Lossless Current Sense Method I

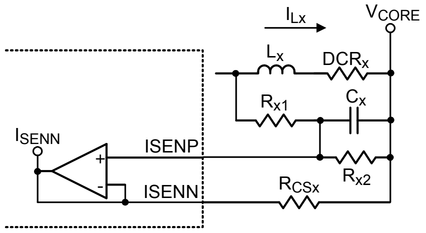


Figure 5. Lossless Current Sense Method II

Thermal Compensation for Current Sense

Thermal Compensation for Current Sense is a patented topology, unlike conventional current sense method requiring a NTC resistor in per phase current loop for thermal compensation. That is to say, this current sense of thermal compensation method can be applied to multi-phase condition and it only needs one NTC resistor. So, the NTC resistor cost can be saved by using the method. Figure 6 and Figure 7 show the current sense method which connecting the resistor network between the IMON and VREF pins to set a part of current loop gain for load-line (droop) setting and set accurate over current protection.

The method I current sense network equation is as follows :

$$V_{IMON} - V_{REF} = \frac{DCR_X}{R_{CSX}} \times R_{EQ} \times I_{LX}$$

The method II current sense network equation is as follows :

$$V_{IMON} - V_{REF} = \frac{DCR_X}{R_{CSX}} \times R_{EQ} \times I_{LX} \times \frac{R_{X2}}{R_{X1} + R_{X2}}$$

R_{EQ} includes a NTC resistor to compensate DCR_x thermal drifting for high accuracy load-line (droop).

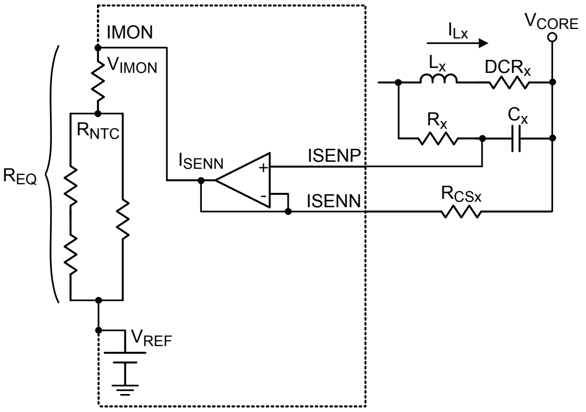


Figure 6. Total Current Sense Method I Network

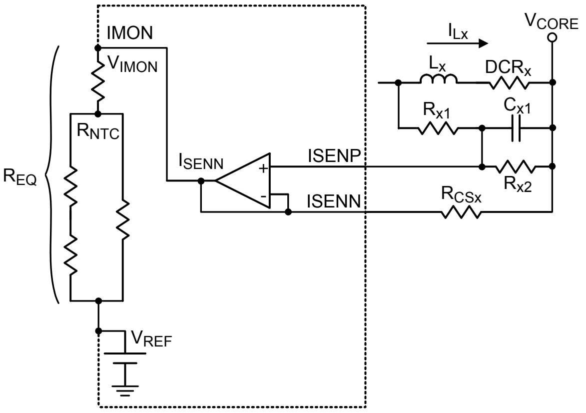


Figure 7. Total Current Sense Method II Network

Load-Line (Droop) Setting

The G-NAVP^{TM} topology can set load-line (droop) via the current loop and the voltage loop, the load-line is a slope between load current I_{CC} and output voltage V_{CORE} as shown in Figure 8. Figure 9 shows the voltage control and current loop. By using both loops, the load-line (droop) can easily be set. The load-line set equation is :

$$R_{LL} = \frac{A_I}{A_V} = \frac{\frac{1}{6} \times \frac{DCR_X}{R_{CSX}} \times R_{EQ}}{\frac{R2}{R1}} \ (\mathrm{m}\Omega)$$

The load-line can be set to zero by SET3 pin.

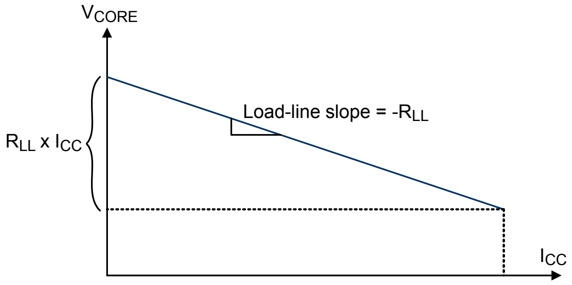


Figure 8. Load-Line (Droop)

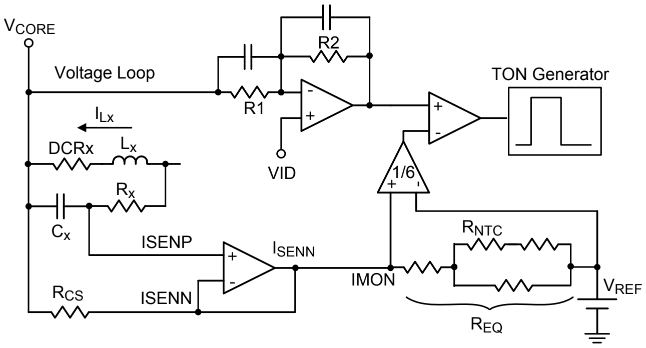


Figure 9. Voltage Loop and Current Loop

Compensator Design

The compensator of RT8171B doesn't need a complex type II or type III compensator to optimize control loop performance. It can adopt a simple type I compensator (one pole, one zero) in G-NAVP^{TM} topology to achieve constant output impedance design for Intel VR12.1 ACLL specification. The one pole one zero compensator is shown as Figure 10, the transfer function of compensator should be designed as the following transfer function to achieve constant output impedance, i.e. Zo(s) = load-line slope in the entire frequency range :

$$G_{CON}(s) \approx \frac{A_I}{R_{LL}} \times \frac{1+\frac{s}{\pi \times f_{SW}}}{1+\frac{s}{\omega_{ESR}}}$$

Where A_I is current loop gain, R_{LL} is load-line, f_{SW} is switching frequency and ω_{ESR} is a pole that should be located at 1 / (C_{OUT} x ESR). Then, the C1 and C2 should be designed as follows :

$$C1 = \frac{1}{R1 \times \pi \times f_{SW}}$$

$$C2 = \frac{C_{OUT} \times ESR}{R2}$$

It is noted that, the values of C1 and C2 may fine tune for better experimental performance.

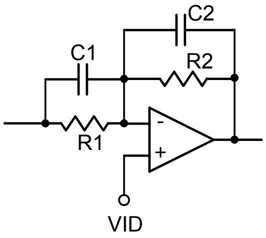


Figure 10. Type I Compensator

Multi-Function Pin Setting Mechanism

For reducing total pin number of package, the SET[1:3] pins adopt the multi-function pin setting mechanism in RT8171B. Figure 11 illustrates this operating mechanism. First, external voltage divider is to set the Function 1 and then internal current source 80μA is to set the Function 2. The setting voltage of Function 1 and Function 2 can be represented as follows :

$$V_{Function\ 1} = \frac{R2}{R1+R2} \times V_{CC}$$

$$V_{Function\ 2} = 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

All function setting will be done within 500μs after power ready (POR).

If $V_{Function\ 1}$ and $V_{Function\ 2}$ are determined, R1 and R2 can be calculated as follows :

$$R1 = \frac{V_{CC} \times V_{Function\ 2}}{80\mu A \times V_{Function\ 1}}$$

$$R2 = \frac{R1 \times V_{Function1}}{V_{CC} - V_{Function1}}$$

In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the SETx resistor network for RT8171B.

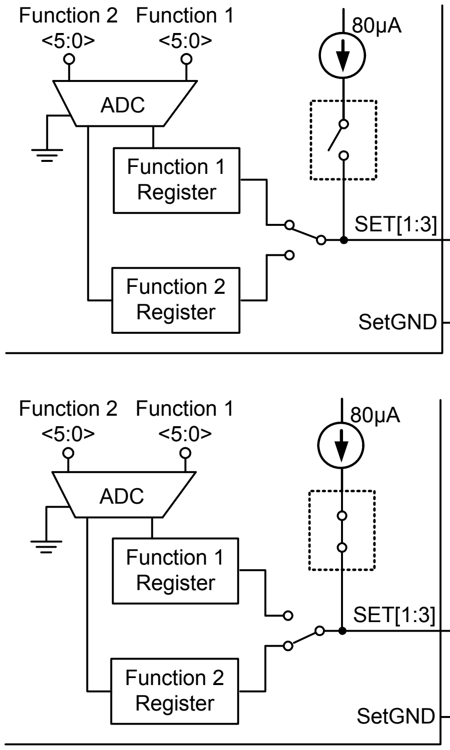
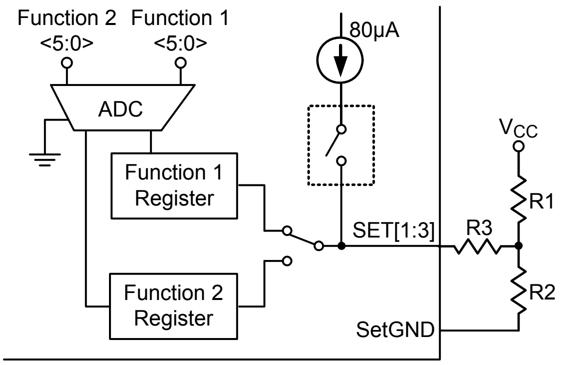


Figure 11. Multi-Function Pin Setting Mechanism

Connecting a R3 resistor from the SET[1:3] pin to the middle node of voltage divider can help to fine tune the set voltage of Function 2, which does not affect the set voltage of Function 1. The Figure 12 shows the setting method and the set voltage of Function 1 and Function 2 can be represented as :

$$V_{Function\ 1} = \frac{R2}{R1+R2} \times V_{CC}$$

$$V_{Function\ 2} = 80\mu A \times \left(R3 + \frac{R1 \times R2}{R1+R2}\right)$$



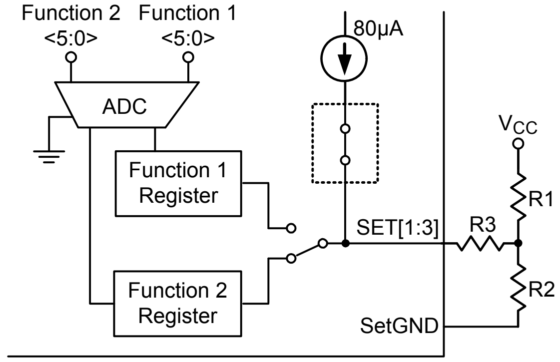


Figure 12. Multi-Function Pin Setting Mechanism with a R3 resistor to fine tune the set voltage of function 2

Quick Response (QR) Mechanism

When the transient load step-up becomes quite large, it is difficult for loop response to meet the energy transfer. Hence, that output voltage generate undershoot to fail specification. The RT8171B has Quick Response (QR) mechanism being able to help improve this issue. It adopts a nonlinear control mechanism which can enlarge the on time of PWM signal at instantaneous step-up transient load to restrain the output voltage drooping, Figure 13 shows the QR behavior.

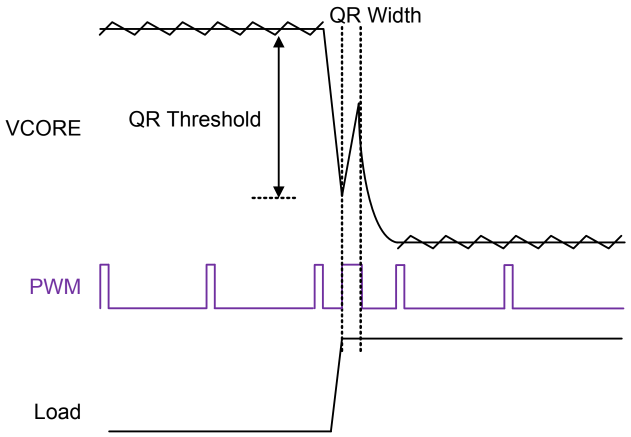


Figure 13. Quick Response Mechanism

The output voltage signal behavior needs to be detected so that QR mechanism can be trigged. The output voltage signal is via a remote sense line to connect at VSEN pin that is shown in Figure 14. The QR mechanism needs to set QR width and QR threshold. Both definitions are shown in Figure 13. A proper QR mechanism set can meet different applications. The SET2 pin is a multi-function pin which can set QR threshold, QR width and ICCMAX.

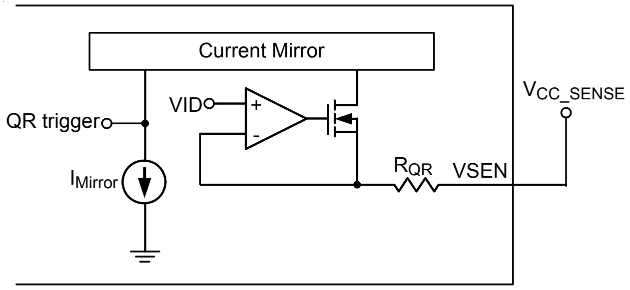


Figure 14. Simplified QR Trigger Schematic

An internal current source 80µA is used in multi-function pin setting mechanism. For example, 25mV QR threshold and 1.3 x TON QR width are set according to the Table 4, the set voltage should be between 0.6506V and 0.6725V. Please note that a high accuracy resistor is needed for this setting accuracy, <1% error tolerance is recommended.

In the Table 4, there are some "No Use" marks at QR Width section. It means that user should not use it to avoid the possibility of shift digital code due to tolerance concern.

Table 4. SET2 Pin Setting for QR Threshold and QR Width

$V_{QR\_SET} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$						QR Threshold	QR Width (%TON)
Min	**Typical**	**Max**	**unit**	**QR_TH <2:0>**	**QRWIDTH <2:0>**		
0.000	10.948	21.896	mV	000	000	Disable	No Use
25.024	35.973	46.921	mV		001		155%
50.049	60.997	71.945	mV		010		133%
75.073	86.022	96.970	mV		011		111%
100.098	111.046	121.994	mV		100		89%
125.122	136.070	147.019	mV		101		67%
150.147	161.095	172.043	mV		110		44%
175.171	186.119	197.067	mV		111		No Use
200.196	211.144	222.092	mV	001	000	15mV	No Use
225.220	236.168	247.116	mV		001		155%
250.244	261.193	272.141	mV		010		133%
275.269	286.217	297.165	mV		011		111%
300.293	311.241	322.190	mV		100		89%
325.318	336.266	347.214	mV		101		67%
350.342	361.290	372.239	mV		110		44%
375.367	386.315	397.263	mV		111		No Use
400.391	411.339	422.287	mV	010	000	20mV	No Use
425.415	436.364	447.312	mV		001		155%
450.440	461.388	472.336	mV		010		133%
475.464	486.413	497.361	mV		011		111%
500.489	511.437	522.385	mV		100		89%
525.513	536.461	547.410	mV		101		67%
550.538	561.486	572.434	mV		110		44%
575.562	586.510	597.458	mV		111		No Use
600.587	611.535	622.483	mV	011	000	25mV	No Use
625.611	636.559	647.507	mV		001		155%
650.635	661.584	672.532	mV		010		133%
675.660	686.608	697.556	mV		011		111%
700.684	711.632	722.581	mV		100		89%
725.709	736.657	747.605	mV		101		67%
750.733	761.681	772.630	mV		110		44%
775.758	786.706	797.654	mV		111		No Use
800.782	811.730	822.678	mV	100	000	30mV	No Use
825.806	836.755	847.703	mV		001		155%
850.831	861.779	872.727	mV		010		133%
875.855	886.804	897.752	mV		011		111%
900.880	911.828	922.776	mV		100		89%
925.904	936.852	947.801	mV		101		67%
950.929	961.877	972.825	mV		110		44%
975.953	986.901	997.849	mV		111		No Use

$V_{QR\_SET} = 80\mu A \times \frac{R1 \times R2}{R1+R2}$						QR Threshold	QR Width (%TON)
Min	Typical	Max	unit	QR_TH <2:0>	QRWIDTH <2:0>		
1000.978	1011.926	1022.874	mV	101	000	35mV	No Use
1026.002	1036.950	1047.898	mV		001		155%
1051.026	1061.975	1072.923	mV		010		133%
1076.051	1086.999	1097.947	mV		011		111%
1101.075	1112.023	1122.972	mV		100		89%
1126.100	1137.048	1147.996	mV		101		67%
1151.124	1162.072	1173.021	mV		110		44%
1176.149	1187.097	1198.045	mV		111		No Use
1201.173	1212.121	1223.069	mV	110	000	40mV	No Use
1226.197	1237.146	1248.094	mV		001		155%
1251.222	1262.170	1273.118	mV		010		133%
1276.246	1287.195	1298.143	mV		011		111%
1301.271	1312.219	1323.167	mV		100		89%
1326.295	1337.243	1348.192	mV		101		67%
1351.320	1362.268	1373.216	mV		110		44%
1376.344	1387.292	1398.240	mV		111		No Use
1401.369	1412.317	1423.265	mV	111	000	45mV	No Use
1426.393	1437.341	1448.289	mV		001		155%
1451.417	1462.366	1473.314	mV		010		133%
1476.442	1487.390	1498.338	mV		011		111%
1501.466	1512.414	1523.363	mV		100		89%
1526.491	1537.439	1548.387	mV		101		67%
1551.515	1562.463	1573.412	mV		110		44%
1576.540	1587.488	1598.436	mV		111		No Use

Dynamic VID (DVID) Compensation

When VID transition event occurs, a charge current will be generated in the loop to cause that DVID performance is deteriorated by this induced charge current, the phenomenon is called droop effect. The droop effect is shown in Figure 15. When VID up transition occurs, the output capacitor will be charged by inductor current. Since current signal is sensed in inductor, an induced charge current will appear in control loop. The induced charge current will produce a voltage drop in R1 to cause output voltage to have a droop effect. Due to this, VID transition performance will be deteriorated.

The RT8171B provides a DVID compensation function. A virtual charge current signal can be established by the SET1 pin to cancel the real induced charge current signal and the virtual charge current signal is defined in Figure 17. Figure 16 shows the operation of canceling droop effect. A virtual charge current signal is established first and then VID signal plus virtual charge current signal is generated in FB pin. Hence, an induced charge current signal flows to R1 and is cancelled to reduce droop effect.

As mention before, the charge current will be generated when VID transition event occurs. This charge current will not only deteriorated DVID performance but also may damage power switches. Due to this, user should consider the power rating current of power switches when choosing the power switches.

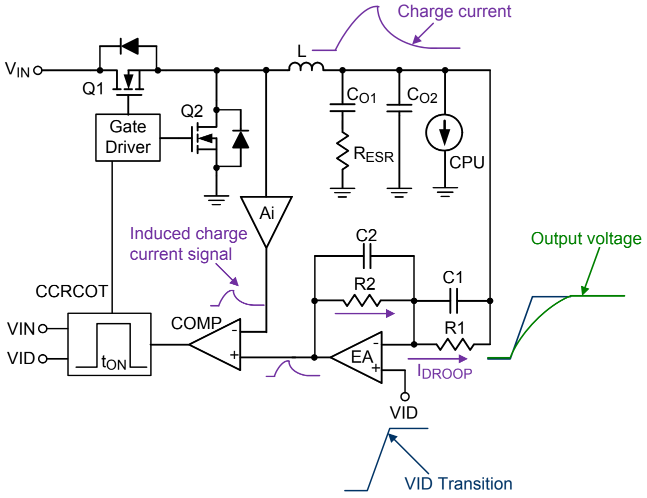


Figure 15. Droop Effect in VID Transition

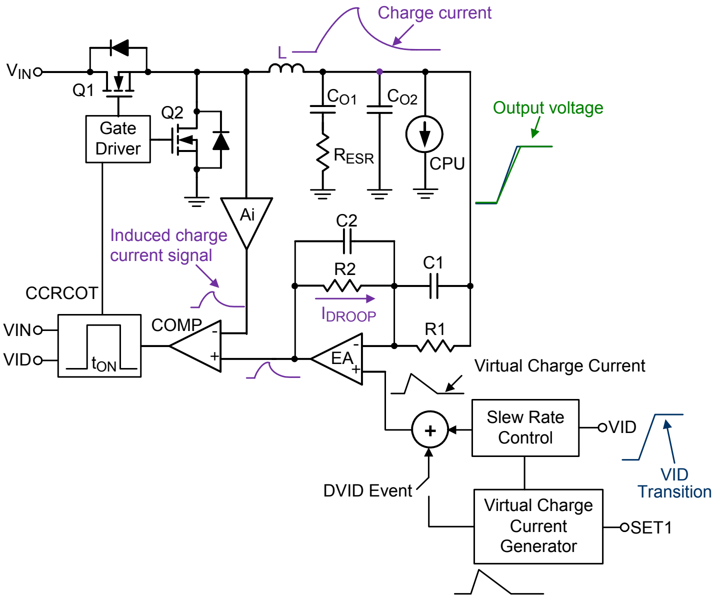


Figure 16. DVID Compensation

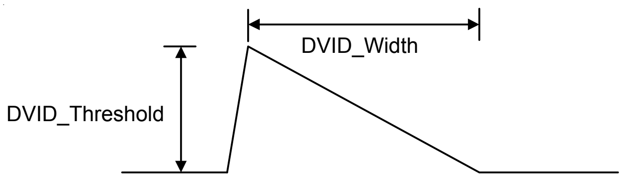


Figure 17. Definition of Virtual Charge Current Signal

Table 5 and Table 6 show the DVID_Threshold and DVID_Width settings in SET1 pin, respectively. For example, 25mV DVID_Threshold and 72μs DVID_Width are designed (OCP sets as 110% ICCMAX, and RSET sets as 100% Ramp current). The DVID_Threshold is set by an external voltage divider to set and the DVID_Width is set by an internal current source 80μA by the multi-function pin setting mechanism. According to the Table 5 and Table 6, the DVID_Threshold set voltage should be between 1.226V and 1.248V and the DVID_Width set voltage should be between 0.125V and 0.147V. Please note that a high accuracy resistor is needed for this setting, <1% error tolerance is recommended.

Table 5. SET1 Pin Setting for DVID_Threshold

$V_{DVID\_Threshold} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$						DVID_Threshold	OCP = %ICCMAX
Min	**Typical**	**Max**	**unit**	**DVID_TH <2:0>**	**OCS <2:0>**		
0.000	10.948	21.896	mV	111	000	85mV	No Use
25.024	35.973	46.921	mV		001		110%
50.049	60.997	71.945	mV		010		119%
75.073	86.022	96.970	mV		011		128%
100.098	111.046	121.994	mV		100		138%
125.122	136.070	147.019	mV		101		147%
150.147	161.095	172.043	mV		110		156%
175.171	186.119	197.067	mV		111		No Use
200.196	211.144	222.092	mV	110	000	75mV	No Use
225.220	236.168	247.116	mV		001		110%
250.244	261.193	272.141	mV		010		119%
275.269	286.217	297.165	mV		011		128%
300.293	311.241	322.190	mV		100		138%
325.318	336.266	347.214	mV		101		147%
350.342	361.290	372.239	mV		110		156%
375.367	386.315	397.263	mV		111		No Use
400.391	411.339	422.287	mV	101	000	65mV	No Use
425.415	436.364	447.312	mV		001		110%
450.440	461.388	472.336	mV		010		119%
475.464	486.413	497.361	mV		011		128%
500.489	511.437	522.385	mV		100		138%
525.513	536.461	547.410	mV		101		147%
550.538	561.486	572.434	mV		110		156%
575.562	586.510	597.458	mV		111		No Use
600.587	611.535	622.483	mV	100	000	55mV	No Use
625.611	636.559	647.507	mV		001		110%
650.635	661.584	672.532	mV		010		119%
675.660	686.608	697.556	mV		011		128%
700.684	711.632	722.581	mV		100		138%
725.709	736.657	747.605	mV		101		147%
750.733	761.681	772.630	mV		110		156%
775.758	786.706	797.654	mV		111		No Use
800.782	811.730	822.678	mV	011	000	45mV	No Use
825.806	836.755	847.703	mV		001		110%
850.831	861.779	872.727	mV		010		119%
875.855	886.804	897.752	mV		011		128%
900.880	911.828	922.776	mV		100		138%
925.904	936.852	947.801	mV		101		147%
950.929	961.877	972.825	mV		110		156%
975.953	986.901	997.849	mV		111		No Use

$V_{DVID\_Threshold} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$						DVID_Threshold	OCP = %ICCMAX
Min	**Typical**	**Max**	**unit**	**DVID_TH <2:0>**	**OCS <2:0>**		
1000.978	1011.926	1022.874	mV	010	000	35mV	No Use
1026.002	1036.950	1047.898	mV		001		110%
1051.026	1061.975	1072.923	mV		010		119%
1076.051	1086.999	1097.947	mV		011		128%
1101.075	1112.023	1122.972	mV		100		138%
1126.100	1137.048	1147.996	mV		101		147%
1151.124	1162.072	1173.021	mV		110		156%
1176.149	1187.097	1198.045	mV		111		No Use
1201.173	1212.121	1223.069	mV	001	000	25mV	No Use
1226.197	1237.146	1248.094	mV		001		110%
1251.222	1262.170	1273.118	mV		010		119%
1276.246	1287.195	1298.143	mV		011		128%
1301.271	1312.219	1323.167	mV		100		138%
1326.295	1337.243	1348.192	mV		101		147%
1351.320	1362.268	1373.216	mV		110		156%
1376.344	1387.292	1398.240	mV		111		No Use
1401.369	1412.317	1423.265	mV	000	000	15mV	No Use
1426.393	1437.341	1448.289	mV		001		110%
1451.417	1462.366	1473.314	mV		010		119%
1476.442	1487.390	1498.338	mV		011		128%
1501.466	1512.414	1523.363	mV		100		138%
1526.491	1537.439	1548.387	mV		101		147%
1551.515	1562.463	1573.412	mV		110		156%
1576.540	1587.488	1598.436	mV		111		No Use

Table 6. SET1 Pin Setting for DVID_Width

$V_{DVID\_Width} = \frac{R2}{R1+R2} \times 5V$						**RSET % 300kHz**	**DVID_Width**
Min	**Typical**	**Max**	**unit**	**RSET <3:0>**	**DVID_WTH <1:0>**		
0.000	10.948	21.896	mV	0000	00	83%	No Use
25.024	35.973	46.921	mV		01		72μs
50.049	60.997	71.945	mV		10		96μs
75.073	86.022	96.970	mV		11		No Use
100.098	111.046	121.994	mV	0001	00	100%	No Use
125.122	136.070	147.019	mV		01		72μs
150.147	161.095	172.043	mV		10		96μs
175.171	186.119	197.067	mV		11		No Use
200.196	211.144	222.092	mV	0010	00	117%	No Use
225.220	236.168	247.116	mV		01		72μs
250.244	261.193	272.141	mV		10		96μs
275.269	286.217	297.165	mV		11		No Use
300.293	311.241	322.190	mV	0011	00	133%	No Use
325.318	336.266	347.214	mV		01		72μs
350.342	361.290	372.239	mV		10		96μs
375.367	386.315	397.263	mV		11		No Use
400.391	411.339	422.287	mV	0100	00	150%	No Use
425.415	436.364	447.312	mV		01		72μs
450.440	461.388	472.336	mV		10		96μs
475.464	486.413	497.361	mV		11		No Use
500.489	511.437	522.385	mV	0101	00	167%	No Use
525.513	536.461	547.410	mV		01		72μs
550.538	561.486	572.434	mV		10		96μs
575.562	586.510	597.458	mV		11		No Use
600.587	611.535	622.483	mV	0110	00	183%	No Use
625.611	636.559	647.507	mV		01		72μs
650.635	661.584	672.532	mV		10		96μs
675.660	686.608	697.556	mV		11		No Use
700.684	711.632	722.581	mV	0111	00	200%	No Use
725.709	736.657	747.605	mV		01		72μs
750.733	761.681	772.630	mV		10		96μs
775.758	786.706	797.654	mV		11		No Use
800.782	811.730	822.678	mV	1000	00	217%	No Use
825.806	836.755	847.703	mV		01		72μs
850.831	861.779	872.727	mV		10		96μs
875.855	886.804	897.752	mV		11		No Use
900.880	911.828	922.776	mV	1001	00	233%	No Use
925.904	936.852	947.801	mV		01		72μs
950.929	961.877	972.825	mV		10		96μs
975.953	986.901	997.849	mV		11		No Use

$V_{DVID\_Width} = \frac{R2}{R1+R2} \times 5V$						RSET % 300kHz	DVID_Width
Min	Typical	Max	unit	RSET <3:0>	DVID_WTH <1:0>		
1000.978	1011.926	1022.874	mV	1010	00	250%	No Use
1026.002	1036.950	1047.898	mV		01		72μs
1051.026	1061.975	1072.923	mV		10		96μs
1076.051	1086.999	1097.947	mV		11		No Use
1101.075	1112.023	1122.972	mV	1011	00	267%	No Use
1126.100	1137.048	1147.996	mV		01		72μs
1151.124	1162.072	1173.021	mV		10		96μs
1176.149	1187.097	1198.045	mV		11		No Use
1201.173	1212.121	1223.069	mV	1100	00	283%	No Use
1226.197	1237.146	1248.094	mV		01		72μs
1251.222	1262.170	1273.118	mV		10		96μs
1276.246	1287.195	1298.143	mV		11		No Use
1301.271	1312.219	1323.167	mV	1101	00	300%	No Use
1326.295	1337.243	1348.192	mV		01		72μs
1351.320	1362.268	1373.216	mV		10		96μs
1376.344	1387.292	1398.240	mV		11		No Use
1401.369	1412.317	1423.265	mV	1110	00	317%	No Use
1426.393	1437.341	1448.289	mV		01		72μs
1451.417	1462.366	1473.314	mV		10		96μs
1476.442	1487.390	1498.338	mV		11		No Use
1501.466	1512.414	1523.363	mV	1111	00	333%	No Use
1526.491	1537.439	1548.387	mV		01		72μs
1551.515	1562.463	1573.412	mV		10		96μs
1576.540	1587.488	1598.436	mV		11		No Use

Ramp Compensation

G-NAVP^{TM} topology is one type of ripple based control that has fast transient response, no beat frequency issue in high repetitive load frequency operation and low BOM cost. But ripple based control usually has no good noise immunity. The RT8171B provides a ramp compensation to increase noise immunity and reduce jitter at the switching node. Figure 18 shows the ramp compensation.

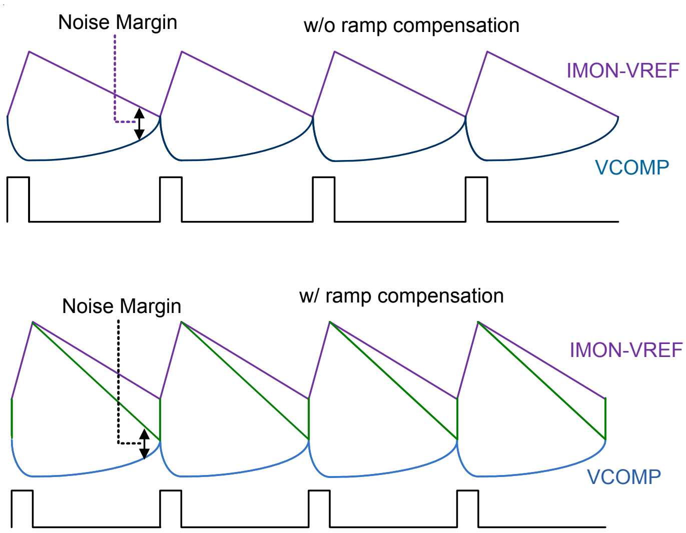


Figure 18. Ramp Compensation

For the RT8171B, the ramp compensation also needs to be considered during mode transition from PS0/1 to PS2. For achieving smooth mode transition into PS2, a proper ramp compensation design is necessary. Since the ramp compensation needs to be proportional to the switching frequency, in others words, ramp compensation is dependent on switching frequency. The Table 6 shows the relationship between switching frequency and ramp compensation. For example, when designed switching frequency is 400kHz, the RAMP is set as $\frac{400\text{kHz}}{300\text{kHz}} \times 100\%$.

Current Monitor, IMON

RT8171B includes a current monitor (IMON) function which can be used to detect over current protection and the maximum processor current ICCMAX, and also sets a part of current gain in the load-line setting. It produces an analog voltage proportional to output current between the IMON and VREF pins.

The calculation of current sense method I for IMON – VREF voltage is shown as below :

$$V_{IMON} - V_{REF} = \frac{DCR_X}{R_{CSx}} \times R_{EQ} \times I_{LX}$$

Where I_{LX} is output current and the definitions of DCR_X, R_{CS} and R_{EQ} can refer to Figure 6.

Maximum Processor Current Setting, ICCMAX

The maximum processor current ICCMAX can be set by the SET2 pin. ICCMAX register is set by an external voltage divider by the multi-function mechanism. The Table 7 shows the ICCMAX setting in SET2 pin. For example, I_{CCMAX} = 25A, the V_{ICCMAX} needs to be set as 0.635V typically. Additionally, $V_{IMON} - V_{REF}$ needs to be set as 0.4V when I_{LX} = 25A. The ICCMAX alert signal will be pulled to low level if $V_{IMON} - V_{REF}$ = 0.4V.

Table 7. SET2 Pin Setting for ICCMAX

$V_{ICCMAX} = \frac{R2}{R1+R2} \times 5V$				ICCMAX	Unit
Min	**Typical**	**Max**	**Unit**		
0.000	9.384	18.768	mV	0	A
25.024	34.409	43.793	mV	1	A
50.049	59.433	68.817	mV	2	A
75.073	84.457	93.842	mV	3	A
100.098	109.482	118.866	mV	4	A
125.122	134.506	143.891	mV	5	A
150.147	159.531	168.915	mV	6	A
175.171	184.555	193.939	mV	7	A
200.196	209.580	218.964	mV	8	A
225.220	234.604	243.988	mV	9	A
250.244	259.629	269.013	mV	10	A
275.269	284.653	294.037	mV	11	A
300.293	309.677	319.062	mV	12	A
325.318	334.702	344.086	mV	13	A
350.342	359.726	369.110	mV	14	A
375.367	384.751	394.135	mV	15	A
400.391	409.775	419.159	mV	16	A
425.415	434.800	444.184	mV	17	A
450.440	459.824	469.208	mV	18	A
475.464	484.848	494.233	mV	19	A
500.489	509.873	519.257	mV	20	A
525.513	534.897	544.282	mV	21	A
550.538	559.922	569.306	mV	22	A
575.562	584.946	594.330	mV	23	A
600.587	609.971	619.355	mV	24	A
625.611	634.995	644.379	mV	25	A
650.635	660.020	669.404	mV	26	A
675.660	685.044	694.428	mV	27	A
700.684	710.068	719.453	mV	28	A
725.709	735.093	744.477	mV	29	A
750.733	760.117	769.501	mV	30	A

Anti-Overshoot Function

When DVID slew rate increases, loop response is difficult to meet energy transfer so that output voltage generates overshoot to fail specification. The RT8171B has Anti-Overshoot function being able to help improve this issue. The VR will turn off low-side MOSFET when output voltage ramps up to the target VID (ALERT signal be pulled low). This function also can improve the overshoot during the load transient condition. When Anti-overshoot function is triggered, the UGATE and LGATE signal will be masked to reduce the overshoot. The Table 8 shows the Anti-Overshoot setting in SET3 pin and this function can be enabled/disabled by SET3 pin under load transient condition. Please note that, this function is always enabled under DVID condition.

Zero Load-Line

The RT8171B adopts G-NAVP^{TM} (Green Native AVP), which is Richtek's proprietary topology derived from finite DC gain compensator with current mode control, making it an easy to set the PWM controller, meeting all Intel CPU requirements of AVP (Active Voltage Positioning). The RT8171B also can support zero load-line application. This function can be enabled/disabled by SET3 pin, as shown in Table 8.

VR Address Setting

In VR 12.1 Intel SVID protocol, the data packet will contain a 4 bit addressing code for future platform flexibility. The RT8171B provides a VR address setting function that can be set by SET3 pin. The VR will react according to the SVID command when VR addressing setting bit is the same with the CPU addressing code. When VR addressing setting bit and the CPU addressing code are different, the VR will skip the SVID command.

The Table 8 and Table 9 show the VR Address setting in SET3 pin. It is noted that VR Address constructs from MSB and LSB. The Table 10 shows the more clearly relation about the real VR Address.

Table 8. SET3 Pin setting for Function 1

$V_{SET3\_1} = \frac{R2}{R1+R2} \times 5V$				**Anti-Overshoot**	**Zero Load-Line**	**VR Address MSB**
Min	**Typical**	**Max**	**Unit**			
0.000	10.948	21.896	mV	Disable	Disable	0
25.024	35.973	46.921	mV			
50.049	60.997	71.945	mV			
75.073	86.022	96.970	mV			
100.098	111.046	121.994	mV			
125.122	136.070	147.019	mV			
150.147	161.095	172.043	mV			
175.171	186.119	197.067	mV			
200.196	211.144	222.092	mV			1
225.220	236.168	247.116	mV			
250.244	261.193	272.141	mV			
275.269	286.217	297.165	mV			
300.293	311.241	322.190	mV			
325.318	336.266	347.214	mV			
350.342	361.290	372.239	mV			
375.367	386.315	397.263	mV			
400.391	411.339	422.287	mV		Enable	0
425.415	436.364	447.312	mV			
450.440	461.388	472.336	mV			
475.464	486.413	497.361	mV			
500.489	511.437	522.385	mV			
525.513	536.461	547.410	mV			
550.538	561.486	572.434	mV			
575.562	586.510	597.458	mV			

$V_{SET3\_1} = \frac{R2}{R1+R2} \times 5V$				Anti-Overshoot	Zero Load-Line	VR Address MSB
Min	**Typical**	**Max**	**Unit**			
600.587	611.535	622.483	mV	Disable	Enable	1
625.611	636.559	647.507	mV			
650.635	661.584	672.532	mV			
675.660	686.608	697.556	mV			
700.684	711.632	722.581	mV			
725.709	736.657	747.605	mV			
750.733	761.681	772.630	mV			
775.758	786.706	797.654	mV			
800.782	811.730	822.678	mV	Enable	Disable	0
825.806	836.755	847.703	mV			
850.831	861.779	872.727	mV			
875.855	886.804	897.752	mV			
900.880	911.828	922.776	mV			
925.904	936.852	947.801	mV			
950.929	961.877	972.825	mV			
975.953	986.901	997.849	mV			
1000.978	1011.926	1022.874	mV			1
1026.002	1036.950	1047.898	mV			
1051.026	1061.975	1072.923	mV			
1076.051	1086.999	1097.947	mV			
1101.075	1112.023	1122.972	mV			
1126.100	1137.048	1147.996	mV			
1151.124	1162.072	1173.021	mV			
1176.149	1187.097	1198.045	mV			
1201.173	1212.121	1223.069	mV		Enable	0
1226.197	1237.146	1248.094	mV			
1251.222	1262.170	1273.118	mV			
1276.246	1287.195	1298.143	mV			
1301.271	1312.219	1323.167	mV			
1326.295	1337.243	1348.192	mV			
1351.320	1362.268	1373.216	mV			
1376.344	1387.292	1398.240	mV			
1401.369	1412.317	1423.265	mV			1
1426.393	1437.341	1448.289	mV			
1451.417	1462.366	1473.314	mV			
1476.442	1487.390	1498.338	mV			
1501.466	1512.414	1523.363	mV			
1526.491	1537.439	1548.387	mV			
1551.515	1562.463	1573.412	mV			
1576.540	1587.488	1598.436	mV			

Table 9. SET3 Pin Setting for Function 2

Min	Typical	Max	unit	VR Address LSB	Switching Frequency	Shrink T_{ON}	ZCD_TH<1:0>
0.000	23.46041	46.921	mV	1	F_{SW} > 500kHz	Disable	0.75mV
50.049	73.48485	96.921	mV				1.5mV
100.098	123.5093	146.921	mV				2.25mV
150.147	173.5337	196.921	mV				3mV
200.196	223.5582	246.921	mV			Enable	0.75mV
250.244	273.5826	296.921	mV				1.5mV
300.293	323.607	346.921	mV				2.25mV
350.342	373.6315	396.921	mV				3mV
400.391	423.6559	446.921	mV		F_{SW} ≦ 500kHz	Disable	0.75mV
450.440	473.6804	496.921	mV				1.5mV
500.489	523.7048	546.921	mV				2.25mV
550.538	573.7292	596.921	mV				3mV
600.587	623.7537	646.921	mV			Enable	0.75mV
650.635	673.7781	696.921	mV				1.5mV
700.684	723.8025	746.921	mV				2.25mV
750.733	773.827	796.921	mV				3mV
800.782	823.8514	846.921	mV	0	F_{SW} > 500kHz	Disable	0.75mV
850.831	873.8759	896.921	mV				1.5mV
900.880	923.9003	946.921	mV				2.25mV
950.929	973.9247	996.921	mV				3mV
1000.978	1023.949	1046.921	mV			Enable	0.75mV
1051.026	1073.974	1096.921	mV				1.5mV
1101.075	1123.998	1146.921	mV				2.25mV
1151.124	1174.022	1196.921	mV				3mV
1201.173	1224.047	1246.921	mV		F_{SW} ≦ 500kHz	Disable	0.75mV
1251.222	1274.071	1296.921	mV				1.5mV
1301.271	1324.096	1346.921	mV				2.25mV
1351.320	1374.12	1396.921	mV				3mV
1401.369	1424.145	1446.921	mV			Enable	0.75mV
1451.417	1474.169	1496.921	mV				1.5mV
1501.466	1524.194	1546.921	mV				2.25mV
1551.515	1574.218	1596.921	mV				3mV

Table 10. Composing about Real VR Address

VR Address MSB/LSB		Real VR Address
0	0	0
0	1	1
1	0	4
1	1	5

Over Current Protection

The RT8171B has dual OCP mechanism. One is named OCP-SUM, the other is called OCP-SPIKE. The over current protection (OCP) forces high-side MOSFET and low-side MOSFET off by shutting down internal PWM logic drivers. RT8171B provides OCP-SUM which is set by SET1 pin. The OCP-SUM threshold setting can refer to ICCMAX current in the Table 7. For example, if ICCMAX is set as 25A, user can set voltage by using the external voltage divider in SET1 pin as 1.262V typically if DVID_Threshold = 25mV, then 30A OCP-SUM (120% x ICCMAX) threshold will be set. When output current is higher than the OCP-SUM threshold, OCP-SUM is latched with a 40μs delay time to prevent false trigger. Besides, the OCP-SUM function is masked when dynamic VID transient occurs and after dynamic VID transition, OCP-SUM is masked for 80μs. The other one is per phase OCP which should trip when the output current exceeds quintuple ICCMAX during soft-start. When output current is higher than the per phase OCP threshold, per phase OCP is latched with a 1μs delay time to prevent false trigger. Please note that, here is no OCP at PS3.

Over Output Voltage Protection

There are two conditions for OVP. One is when VSEN is higher than 1.2V. The other is when VSEN is smaller than 1.2V. For VSEN is higher than 1.2V, OVP condition is detected when the VSEN pin is 350mV more than VID. For VSEN is smaller than 1.2V, OVP is occurred when VSEN is higher than 1.55V. When OVP condition is detected, the upper gate voltage UGATE is pulled-low and lower gate voltage LGATE is pulled-high. OVP is latched with a 0.5μs delay time to prevent false trigger.

Negative Voltage Protection

Since the OVP latch continuously turns on low-side MOSFET of the VR, the VR will suffer negative output voltage. When the VSEN detects a voltage below −0.05V after triggering OVP, the VR will trigger NVP to turn off low-side MOSFET of the VR while the high-side MOSFET remains off. After triggering NVP, if the output voltage rises above 0V, the OVP latch will restart to turn on low-side MOSFET. Therefore, the output voltage may bounce between 0V and −0.05V due to OVP latch and NVP triggering. The NVP function will be active only after OVP is triggered.

Under Voltage Protection

When the VSEN pin voltage is 350mV less than VID, a UVP will be latched. When UVP latched, both the UGATE and LGATE will be pulled-low. A 3.5μs delay is used in UVP detection circuit to prevent false trigger. Besides, the UVP function is masked when dynamic VID transient occurs and after dynamic VID transition, UVP is masked for 80μs.

Under Voltage Lock Out (UVLO)

During normal operation, if the voltage at the VCC pin drops below POR threshold 4.1V (min), the VR will trigger UVLO. The UVLO protection forces high-side MOSFET and low-side MOSFET off by shutting down internal PWM logic drivers.

Power Ready (POR) Detection

During start-up, the RT8171B will detect the voltage at the voltage input pins : V_{CC}, EN and PVCC. When V_{CC} > 4.1V and PVCC > 4V the RT8171B will recognize the power state of system to be ready (POR = high) and wait for enable command at the EN pin. After POR = high and V_{EN} > 0.7V, the RT8171B will enter start-up sequence. If the voltage at any voltage pin drops below low threshold (POR = low), the RT8171B will enter power down sequence and all the functions will be disabled. Normally, connecting system voltage V_{TT} (1.05V) to the EN pin is recommended.1ms (max) after the chip has been enabled, the SVID circuitry will be ready. All the protection latches (OVP, OCP, UVP) will be cleared only by VCC. The condition of V_{EN} = low will not clear these latches. Figure 19 and Figure 20 show the POR detection and the timing chart for POR process, respectively.

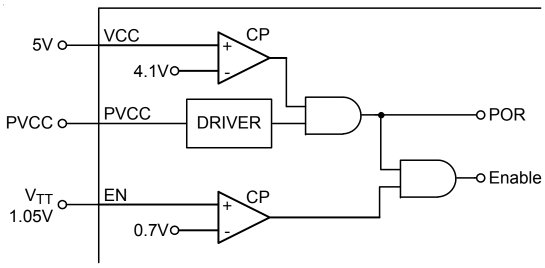


Figure 19. POR Detection

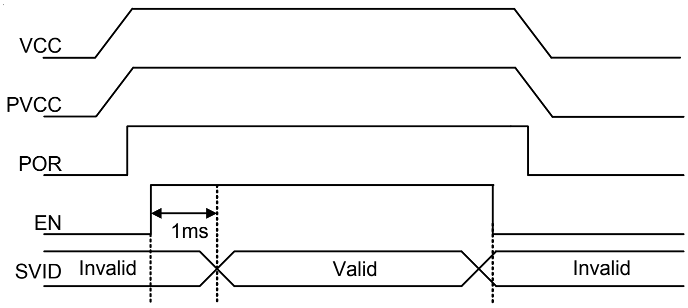


Figure 20. Timing Chart for POR Process

Precise Reference Current Generation, IBIAS

Analog circuits need very precise reference voltage/current to drive/set these analog devices. The RT8171B provides a 2V voltage source at the IBIAS pin, and a 100kΩ resistor is required to be connected between IBIAS pin and analog ground to generate a very precise reference current. Through this connection, the RT8171B will generate a 20μA current from the IBIAS pin to analog ground, and this 20μA current will be mirrored inside the RT8171B for internal use. The IBIAS pin can only be connected with a 100kΩ resistor to GND for internal analog circuit use. The resistance accuracy of this resistor is recommended to be 1% or higher. Figure 21 shows the IBIAS setting circuit.

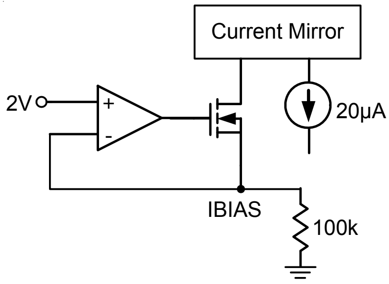


Figure 21. IBIAS Setting Circuit

TSEN and $\overline{\text{VR\_HOT}}$

The $\overline{\text{VR\_HOT}}$ signal is an open-drain signal which is used for VR thermal protection. When the sensed voltage in TSEN pin is over 1.887V under V_{CC} is exact 5V condition, the $\overline{\text{VR\_HOT}}$ signal will be pulled-low to notify CPU that the thermal protection needs to work. Please note that, the VR thermal protection is only valid under PS0, PS1 and PS2 condition. According to Intel VR definition, $\overline{\text{VR\_HOT}}$ signal needs acting if VR power chain temperature exceeds 100°C. Placing an NTC thermistor at the hottest area in the VR power chain and its connection is shown in Figure 22, to design the voltage divider elements (R1, R2 and NTC) so that V_{TSEN} = 1.887V at 100°C. The resistance accuracy of TSEN network is recommended to be 1% or higher.

$$V_{TSEN} = V_{CC} \times \frac{R2}{R2 + \left[R1//R_{NTC(100^\circ C)}\right]} = 1.887V$$

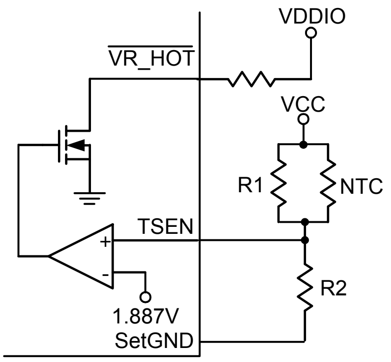


Figure 22. $\overline{\text{VR\_HOT}}$ Circuit

VBOOT

The RT8171B provides controllable VBOOT function as shown in Figure 23. The VBOOT voltage can be set by the VBOOTSEL pin. Table 11 shows the VBOOT voltage setting in VBOOTSEL pin. For example, when VBOOT = 1V, the VBOOTSEL set voltage will be between 1.3V and 3.7V. It's noted that, if floating VBOOTSEL pin that the VBOOT voltage will not be defined.

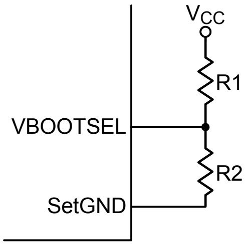


Figure 23. VBOOTSEL Circuit.

Table 11. VBOOTSEL Pin setting for VBOOT

$\text{VBOOTSEL} = \frac{R2}{R1+R2} \times 5V$				VBOOT
Min	**Typical**	**Max**	**Unit**	
0	0.6	1.2	V	0.9
1.3	2.5	3.7	V	1.0
3.8	4.4	5	V	1.1

Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces as signified as Figure 24. CPU internal power routes and socket contacts. The CPU contains on-die sense pins, V_{CC_SENSE} and V_{SS_SENSE}. Connecting RGND to V_{SS_SENSE} and connect FB to V_{CC_SENSE} with a resistor to build the negative input path of the error amplifier. The V_{DAC} and the precision voltage reference are referred to RGND for accurate remote sensing.

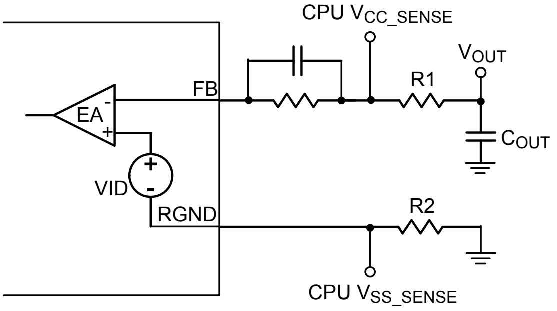


Figure 24. Remote Sensing Circuit

Current Loop Design in Details

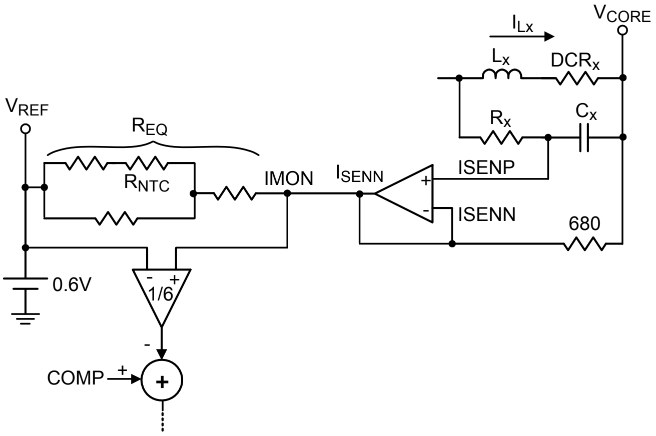
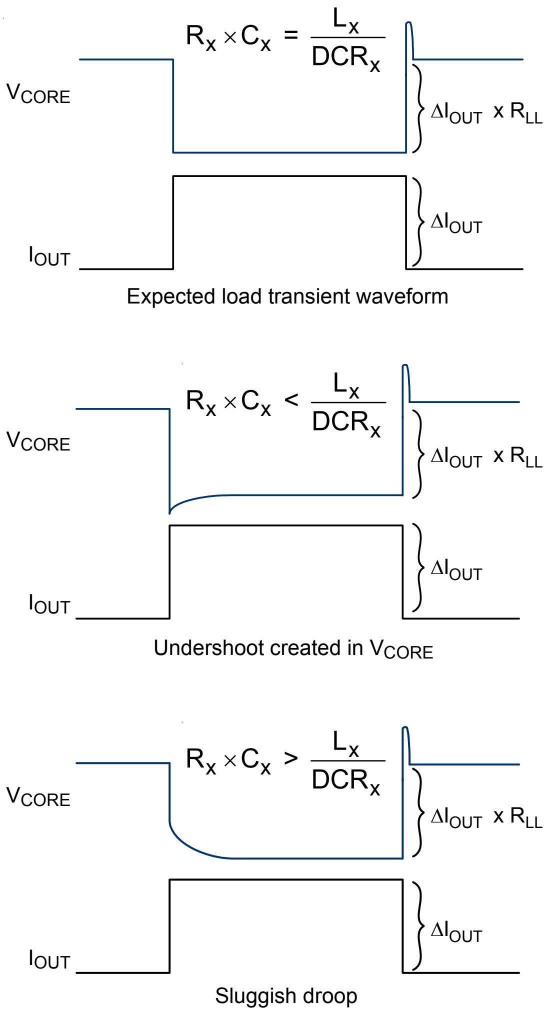


Figure 25. Current Loop Structure

Figure 25 shows the whole current loop structure. The current loop plays an important role in RT8171B that can decide ACLL performance (for load-line is required condition), DCLL accuracy and ICCMAX accuracy. For ACLL performance, the correct compensator design is assumed, if RC network time constant matches inductor time constant L_X / DCR_X, an expected load transient waveform can be designed. If R_XC_X network time constant is larger than inductor time constant L_X / DCR_X, V_{CORE} waveform has a sluggish droop during load transient. If R_XC_X network is smaller than inductor time constant L_X / DCR_X, a worst V_{CORE} waveform will sag to create an undershoot to fail the specification. Figure 26 shows the variety of R_XC_X constant corresponding to the output waveforms.



Expected load transient waveform

Undershoot created in V_{CORE}

Sluggish droop

Figure 26. All Kind of R_XC_X Constants

For DCLL performance and ICCMAX accuracy, since the copper wire of inductor has a positive temperature coefficient, when temperature goes high in the heavy load condition then DCR value goes large simultaneously. A resistor network with NTC thermistor compensation connecting between IMON pin and REF pin is necessary, to compensate the positive temperature coefficient of inductor DCR. The design flow is as follows :

Step1 : Given the three system temperature T_L, T_R and T_H, at which are compensated.

Step2 : Three equations can be listed as

$$\frac{DCR\ (T_L)}{680} \times \sum_{i=1}^{1} i_{Li} \times R_{EQ}(T_L) = 0.4$$

$$\frac{DCR\ (T_R)}{680} \times \sum_{i=1}^{1} i_{Li} \times R_{EQ}(T_R) = 0.4$$

$$\frac{DCR\,(T_H)}{680}\times\sum_{i=1}^{1} i_{Li}\times R_{EQ}(T_H) = 0.4$$

Where :

(1) The relationship between DCR and temperature is as follows :

$$DCR\,(T) = DCR\,(25°C)\times\left[1+0.00393\,(T-25)\right]$$

(2) $R_{EQ}(T)$ is the equivalent resistor of the resistor network with a NTC thermistor

$$R_{EQ}(T) = R_{IMON1}+\left\{R_{IMON2}\,//\left[R_{IMON3}+R_{NTC}(T)\right]\right\}$$

And the relationship between NTC and temperature is as follows :

$$R_{NTC}\,(T) = R_{NTC}\,(25°C)\times e^{\beta\left(\frac{1}{T+273}-\frac{1}{298}\right)}$$

β is in the NTC thermistor datasheet.

Step3 : Three equations and three unknowns, R_{IMON1}, R_{IMON2} and R_{IMON3} can be found out unique solution.

$$R_{IMON1} = K_{TR}-\frac{R_{IMON2}\times(R_{NTCTR}+R_{IMON3})}{R_{IMON2}+R_{NTCTR}+R_{IMON3}}$$

$$R_{IMON2} = \sqrt{\left[K_{R3}^2+K_{R3}(R_{NTCTL}+R_{NTCTR})+R_{NTCTL}R_{NTCTR}\right]\alpha_{TL}}$$

$$R_{IMON3} = -R_{IMON2}+K_{R3}$$

Where :

$$\alpha_{TH} = \frac{K_{TH}-K_{TR}}{R_{NTCTH}-R_{NTCTR}}$$

$$\alpha_{TL} = \frac{K_{TL}-K_{TR}}{R_{NTCTL}-R_{NTCTR}}$$

$$K_{R3} = \frac{(\alpha_{TH}/\alpha_{TL})R_{NTCTH}-R_{NTCTL}}{1-(\alpha_{TH}/\alpha_{TL})}$$

$$K_{TL} = \frac{0.4}{G_{CS(TL)}\times I_{CC\text{-}MAX}}$$

$$K_{TR} = \frac{0.4}{G_{CS(TR)}\times I_{CC\text{-}MAX}}$$

$$K_{TH} = \frac{0.4}{G_{CS(TH)}\times I_{CC\text{-}MAX}}$$

Design Step

RT8171B Excel based design tool is available. Users can contact your Richtek representative to get the spreadsheet. Three main design procedures of RT8171B design, first step is initial settings, second step is loop design and last step is protection settings. The following design example is to explain RT8171B design procedure:

	V_{CORE} Specification
Input Voltage	7.4
No. of Phase	1
VBoot	1
ICCMAX	13
ICC-Dyn	8
MAX Switching Frequency	800kHz

The output filter requirements of VRTB specification are as follows :

Output Inductor : 330nH/2.95mΩ

Output Bulk Capacitor : 270μF/2V.6mΩ (3pcs)

Output Ceramic Capacitor : 22μF/0603 (6pcs max sites on top side)

(1) Initial Settings

- RT8171B initial VBoot voltage is 1V

  $5\times\frac{R2}{R1+R2}$=2.5V, R_1 can be selected by user and here R1 is equal to 10kΩ so R2 is equal to 10kΩ.

- IBIAS needs to connect a 100kΩ resistor to ground.

(2) Loop Design

- On time setting :

where $V_{IN(MAX)}$ = 7.4V, $V_{DAC(MAX)}$ = 1V, $F_{SW(MAX)}$ = 800kHz, $I_{CC(MAX)}$ = 13A, DCR = 2.95mΩ, R_{LL} = 0Ω, $R_{ON\text{-}HS}$ = 6mΩ, $R_{ON\text{-}LS}$ = 6mΩ, T_D = 30ns, $T_{ON,VAR}$ = 15ns.

Using the Microsoft Excel-based spreadsheet from RICHTEK.

The R_{TON} resistance can be calculated after the switching frequency and the on-time are decided.

$$R_{TON} = \frac{(V_{IN}-V_{DAC})\times T_{ON}}{18.2p\times 0.11} = 652k\Omega$$

Choosing the nearest on-time setting resistor R_{TON} = 649kΩ

- Current sensor adopts lossless RC filter to sense current signal in DCR. For getting an expected load transient waveform R_XC_X time constant needs to match L_X / DCR_X. $C_X = 0.47\mu F$ is set, then

$$R_X = \frac{L_X}{0.47\mu F \times DCR_X} = 240\Omega$$

But $R_X = 240\Omega$ will let R_{EQ} is too small, so here the current sense method 2 should be selected. By using the design tool, R_{x1} and R_{x2} can be determined, both are equal to 475Ω.

- IMON resistor network design : $T_L = 25°C$, $T_R = 50°C$ and $T_H = 100°C$ are decided, NTC thermistor = 100kΩ @ 25°C, β = 4050 and ICCMAX = 13A. According to the sub-section "Current Loop Design in Details", R_{IMON1} = 6.63kΩ, R_{IMON2} = 8.83kΩ and R_{IMON3} = 5.44kΩ can be decided. The R_{EQ} (25°C) = 14.187kΩ.

- Load-line design : If load-line is required, the load-line can be determined by below equation and the voltage loop A_V gain is also decided by the following equation :

$$R_{LL} = \frac{A_V}{A_I} = \frac{\frac{1}{6} \times \frac{DCR}{R_{CS}} \times R_{EQ}}{\frac{R2}{R1}} \quad (m\Omega)$$

Here the load-line isn't required. The suggestion A_V gain is 5 to 10 for the zero load-line application. R1 = 10kΩ is usually decided and here R2 is chosen to 68kΩ.

- Typical compensator design can use the following equations to design C1 and C2 values

$$C1 = \frac{1}{R1 \times \pi \times f_{SW}} \approx 39.7pF$$

$$C2 = \frac{C_{OUT} \times ESR}{R2} \approx 28pF$$

For Intel platform, in order to induce the band width to enhance transient performance to meet Intel's criterion, the zero location can be designed close to 1/10 of the switching frequency or less than the 1/10 of switching frequency.

- SET1 resistor network design : First, the DVID compensation parameters need to be decided. The DVID_TH can be calculated as the following equation :

$$V_{DVID\_TH} = R_{LL} \times C_{OUT} \times \frac{dVID}{dt}$$

Where R_{LL} is load-line, C_{OUT} is total output capacitance and dVID/dt is DVID fast slew rate. Here the load-line is equal to zero. Thus the DVID compensation isn't work under the zero load-line application. So, DVID_TH and DVID_Width can be set to any value. Here DVID_TH and DVID_Width are chosen as 15mV and 72μs, respectively. Next, OCP threshold I is designed as 1.28 x ICCMAX. Last, RAMP = 800kHz / 300kHz = 267%, 267% is set. By using above information, the two equations can be listed by using multi-function pin setting mechanism :

$$5 \times \frac{R2}{R1 + R2} = 1137.3mV$$

$$80\mu \times \frac{R1 \times R2}{R1 + R2} = 1487.6mV$$

R1 = 81.757kΩ and R2 = 24.065kΩ.

- SET2 resistor network design : The QR mechanism parameters need to be designed at first. Due to the load current step is small and output capacitance is large, the QR mechanism isn't necessary. The QR_TH is set to disable and QR Width is designed as 1.11 x T_{ON}. The ICCMAX is designed as 13A. By using the information, the two equation can be listed by using multi-function pin setting mechanism :

$$5 \times \frac{R2}{R1 + R2} = 334.7mV$$

$$80\mu \times \frac{R1 \times R2}{R1 + R2} = 86.02mV$$

R1 = 16.063kΩ and R2 = 1.1524kΩ.

- SET3 resistor network design: The zero load-line function and anti-overshoot function are decided to enable at first. Then, the ZCD threshold is chosen as 0.75mV, switching frequency is chosen f_{SW} > 500kHz and VR address is usually set to 0. By using the information, the two equations can be listed by using multi-function pin setting mechanism:

$$5 \times \frac{R2}{R1 + R2} = 1299.7mV$$

$$80\mu \times \frac{R1 \times R2}{R1 + R2} = 824.24mV$$

R1 = 39.64kΩ and R2 = 13.92kΩ.

(3) Protection Settings

- OVP/UVP protections: When the VSEN pin voltage is 350mV higher than VID, the OVP will be latched. When the VSEN pin voltage is 350mV lower than VID, the UVP will be latched.
- TSEN and $\overline{\text{VR\_HOT}}$ design : Using the following equation to calculate related resistances for $\overline{\text{VR\_HOT}}$ setting.

$$V_{TSEN} = V_{CC} \times \frac{R2}{R2 + \left[R_{NTC(100^\circ C)} // R1\right]} = 1.887V$$

Choosing R1 = 100kΩ and an NTC thermistor R_{NTC} (25°C) = 100kΩ and its β = 4485. When temperature is 100°C, the R_{NTC}(100°C) = 4.85kΩ. Then R2 = 2.8kΩ can be calculated.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-32L 4x4 package, the thermal resistance, θ_{JA}, is 27.8°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (27.8°C/W) = 3.59W for WQFN-32L 4x4 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 27 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

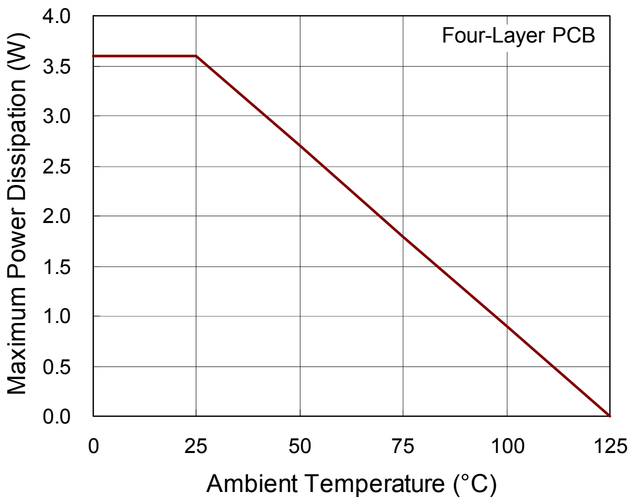
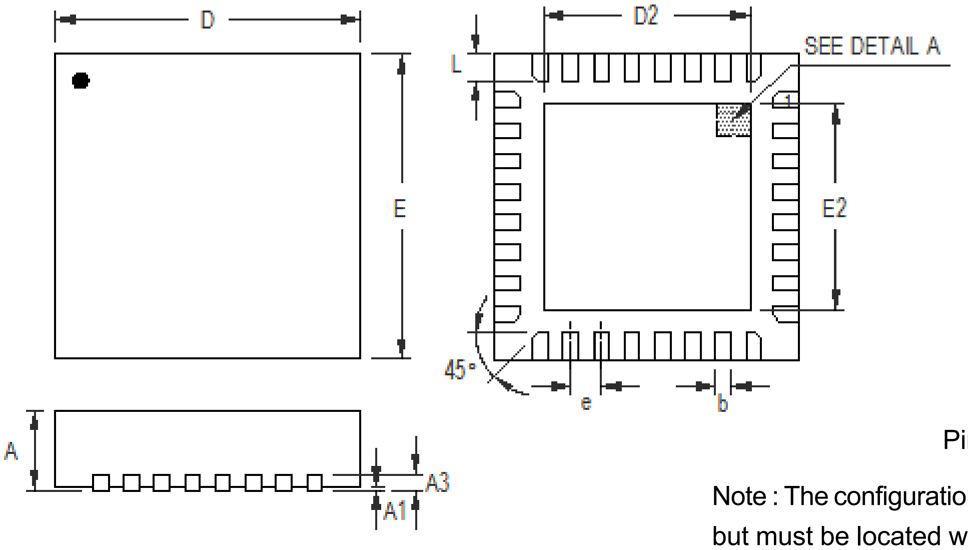
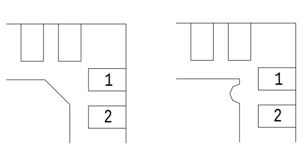


Figure 27. Derating Curve of Maximum Power Dissipation

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	3.900	4.100	0.154	0.161
D2	2.650	2.750	0.104	0.108
E	3.900	4.100	0.154	0.161
E2	2.650	2.750	0.104	0.108
e	0.400		0.016	
L	0.300	0.400	0.012	0.016

W-Type 32L QFN 4x4 Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789