RICHTEK® **RT8237M**

High Efficiency Single Synchronous Buck PWM Controller

1 General Description

The RT8237M PWM controller provides high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high-voltage batteries to generate low voltage CPU core, I/O, and chipset RAM supplies in notebook computers.

The constant on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns “instant-on” response to load transients while maintaining a relatively constant switching frequency.

The RT8237M achieves high efficiency at a reduced cost by eliminating the current sense resistor found in traditional current mode PWMs. Its efficiency is further enhanced by the ability to drive very large synchronous rectifier MOSFETs and to enter diode emulation mode under light load conditions. The buck conversion allows this device to directly step down high-voltage batteries at the highest possible efficiency. The preset frequency selections simplify the design process for new designs. The RT8237M is intended for CPU cores, chipsets, DRAM, or other low voltage supplies down to 0.7V. The RT8237M is available in a WDFN-10L 3x3 package. The recommended ambient temperature range is from –40°C to 85°C and the junction temperature range is from –40°C to 125°C.

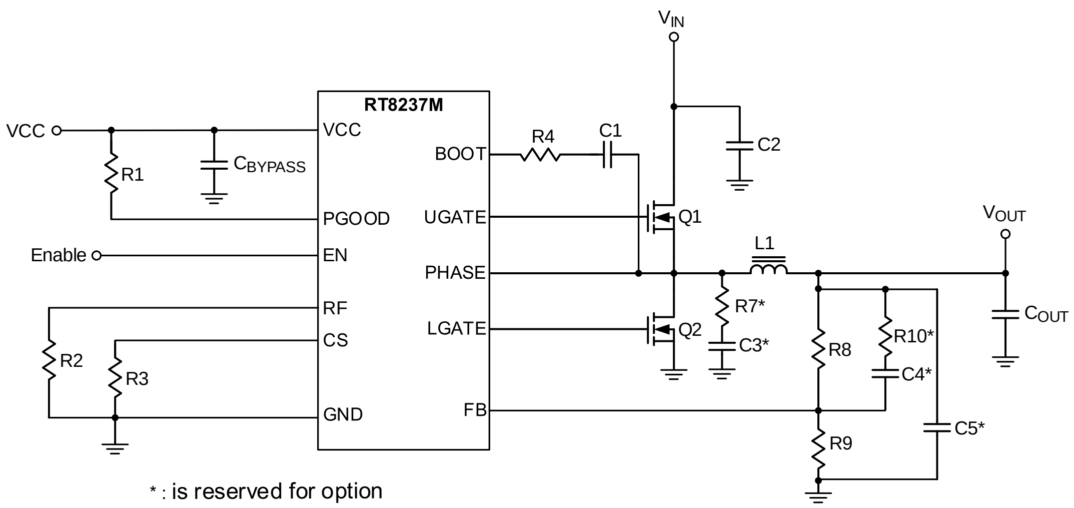
2 Features

- **Wide Input Voltage Range: 4.5V to 26V**
- **Output Voltage Range: 0.7V to 3.3V**
- **Built-In 0.5% 0.7V Reference Voltage**
- **Quick Load-Step Response within 100ns**
- **4700ppm/°C Current Source for Current Limit $R_{DS(ON)}$**
- **Adjustable Current Limit with Low-Side MOSFET**
- **Four Selectable Frequency Settings**
- **Soft-Start Control**
- **Drives Large Synchronous-Rectifier FETs**
- **Integrated Boot Switch**
- **Built-In OVP, OCP, and UVP**
- **Over-Temperature Protection**
- **Power-Good Indicator**

3 Applications

- Notebook Computers
- CPU Core Supply
- Chipsets/RAM Power Supply Down to 0.7V
- Generic DC-DC Power Regulators

4 Simplified Application Circuit



* : is reserved for option

5 Ordering Information

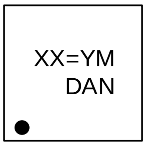
RT8237M □□□

- Pin 1 Orientation
  (2): Quadrant 2, Follow EIA-481
  (Empty means Pin1 orientation is Quadrant 1)
- Package Type[1]
  QW : WDFN-10L 3x3 (W-Type)
- Lead Plating System
  G: Richtek Green Policy Compliant[2]

Note 1.

- Marked with [1] indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with [2] indicated: Richtek products are Richtek Green Policy compliant.

6 Marking Information



XX= : Product Code

YMDAN : Date Code

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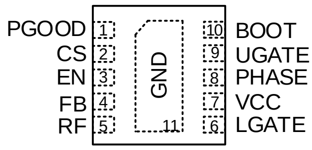
7 Pin Configuration

(TOP VIEW)

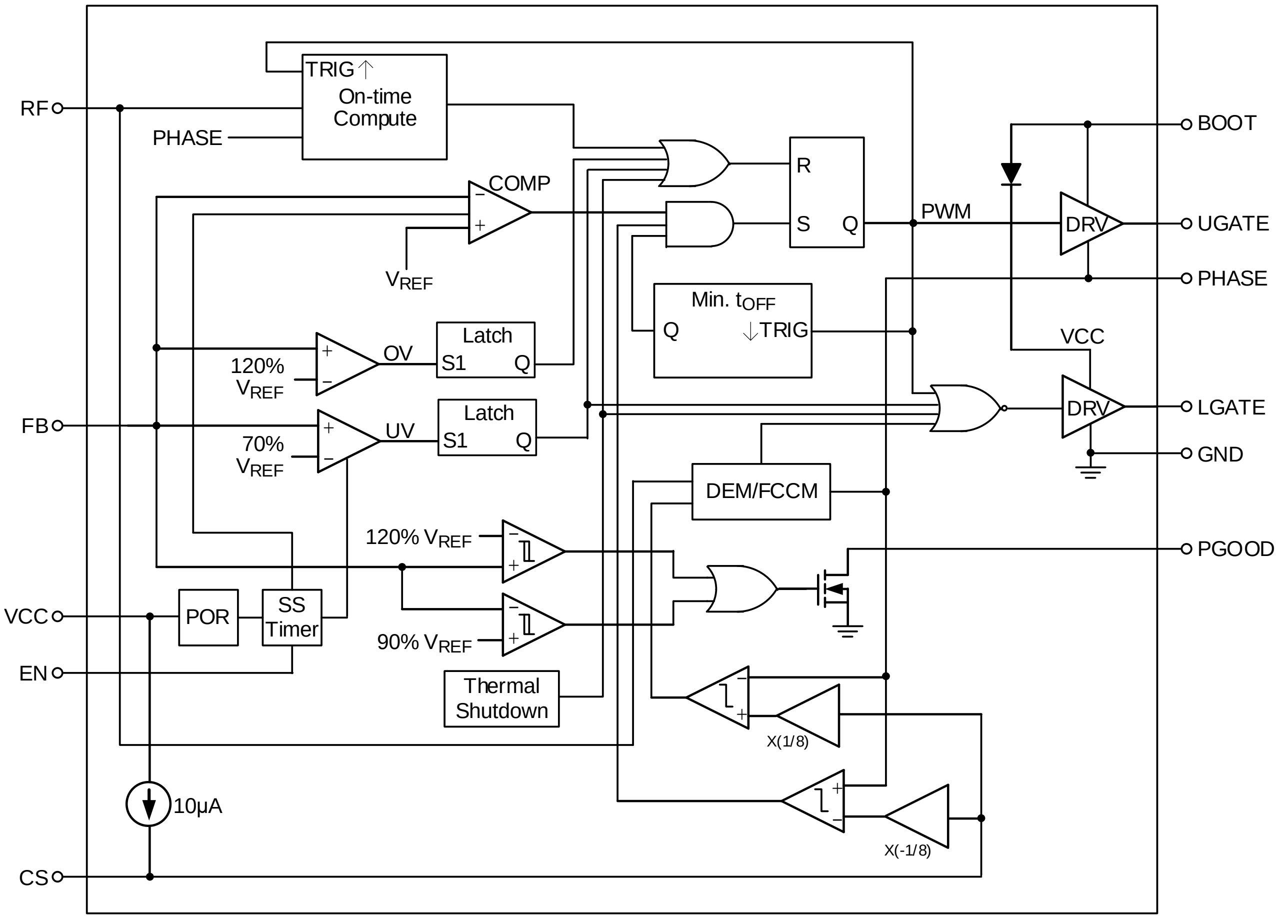


WDFN-10L 3x3

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PGOOD	Power-good indicator is an open-drain output. This pin is pulled low as UVP, OVP, OTP, when EN is low, or when the output voltage is not regulated (such as before soft-start). An external pull-up resistor to VCC or another external rail is required, and the recommended pull-up resistor is 100kΩ. Do not pull the PGOOD voltage higher than 6V.
2	CS	Current limit threshold setting input. Connect a setting resistor to GND and the current limit threshold is equal to 1/8 of the voltage at this pin.
3	EN	Enable control input. Pulling this pin voltage higher than 1.8V will enable this PWM controller. Pulling this pin to GND will disable this PWM controller. Do not leave this pin floating and avoid driving this pin voltage higher than VCC at any time.
4	FB	V_{OUT} feedback voltage input. Connect FB to a resistor voltage divider from V_{OUT} to GND to adjust the output from 0.7V to 3.3V
5	RF	Switching frequency selection. Connect a resistor to select switching frequency, as shown in Electrical Characteristics. The switching frequency is detected and latched after startup. This pin also controls the diode emulation mode or forced CCM selection. Pull down to GND with a resistor for Diode Emulation Mode. Connect to PGOOD with a resistor for forced CCM after PGOOD becomes high.
6	LGATE	Gate drive output for the low-side external MOSFET.
7	VCC	Supply voltage input. This pin provides the power for the buck controller, the low side driver, and the bootstrap circuit for the high-side driver. Bypass to GND with a 1μF ceramic capacitor.
8	PHASE	External inductor connection pin for the PWM converter. It behaves as the current sense comparator input for low-side MOSFET $R_{DS(ON)}$ sensing and as a reference voltage for on-time generation.
9	UGATE	Gate drive output for the high-side external MOSFET.
10	BOOT	Bootstrap supply for the high-side gate driver. Connect through a capacitor to the floating node (PHASE).
11 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VCC, FB, PGOOD, EN, CS, RF to GND ---------- –0.3V to 6V
- BOOT to GND
  DC ---------- –0.3V to 36V
  <100ns ---------- –5V to 42V
- BOOT to PHASE
  DC ---------- –0.3V to 6V
  <100ns ---------- –5V to 7.5V
- PHASE to GND
  DC ---------- –5V to 30V
  <100ns ---------- –10V to 42V
- UGATE to GND
  DC ---------- –5V to 36V
  <100ns ---------- –10V to 42V
- UGATE to PHASE ---------- –0.3V to 6V
  DC ---------- –0.3V to 6V
  <100ns ---------- –5V to 7.5V
- LGATE to GND ---------- –0.3V to 6V
  DC ---------- –0.3V to 6V
  <100ns ---------- –5V to 7.5V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-10L 3x3 ---------- 1.82W
- Package Thermal Resistance (Note 3)
  WDFN-10L 3x3, θ_{JA} ---------- 55.02°C/W
  WDFN-10L 3x3, θ_{JC} ---------- 63.3°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage ---------- 4.5V to 26V
- Control Voltage, VCC ---------- 4.5V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(VCC = 5V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Supply						
VCC Quiescent Supply Current	I_Q	FB forced above the regulation point, V_{EN} = 5V	--	0.5	1.25	mA
VCC Shutdown Current	I_{SHDN}	VCC current, V_{EN} = 0V	--	--	1	μA
CS Shutdown Current		CS pull to GND	--	--	1	μA
FB Error Comparator Threshold	V_{REF}	DEM	0.7005	0.704	0.7075	V
		DEM, T_A = –40°C to 85°C (Note 6)	0.697	0.704	0.711	
FB Input Bias Current		V_{FB} = 0.735V	–1	0.01	1	μA
V_{OUT} Voltage Range			0.7	--	3.3	V
Switching Frequency	f_{SW}	R_{RF} = 470kΩ (Note 7)	--	435	--	kHz
		R_{RF} = 200kΩ (Note 7)	--	510	--	
		R_{RF} = 100kΩ (Note 7)	--	570	--	
		R_{RF} = 39kΩ (Note 7)	--	645	--	
Minimum Off-Time	t_{OFF_MIN}		130	230	330	ns
Current Sensing						
CS Source Current	I_{CS}		9	10	11	μA
CS Source Current TC			--	4700	--	ppm/°C
Zero Crossing Threshold		DEM	–10	--	5	mV
Current-Limit Threshold	V_{LIM}	GND – PHASE, V_{CS} = 2.4V	280	300	320	mV
		GND – PHASE, V_{CS} = 1.6V	185	200	215	
		GND – PHASE, V_{CS} = 0.4V	40	50	60	
Negative Current-Limit Threshold		PHASE – GND, V_{CS} = 2.4V	--	300	--	mV
		PHASE – GND, V_{CS} = 1.6V	--	200	--	
		PHASE – GND, V_{CS} = 0.4V	--	50	--	
Protection Function						
Output UV Threshold		With respect to error comparator threshold	65	70	75	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OVP Threshold		With respect to error comparator threshold	115	120	125	%
OV Fault Delay		FB forced above OV threshold	--	5	--	μs
VCC Undervoltage Lockout Threshold	UVLO	Falling edge, hysteresis = 100mV, PWM disabled below this level	3.7	3.9	4.1	V
V_{OUT} Soft-Start		From EN = high to V_{OUT} = 95%	--	1.9	--	ms
UV Blank Time		From EN signal going high	--	3.7	--	ms
Thermal Shutdown Threshold	T_{SD}		--	150	--	°C
Driver On Resistance						
UGATE Drive Source	$R_{UGATEsr}$	BOOT – PHASE forced to 5V	--	1.8	3.6	Ω
UGATE Drive Sink	$R_{UGATEsk}$	BOOT – PHASE forced to 5V	--	1.2	2.4	Ω
LGATE Drive Source	$R_{LGATEsr}$	LGATE, High State	--	1.8	3.6	Ω
LGATE Drive Sink	$R_{LGATEsk}$	LGATE, Low State	--	0.8	1.6	Ω
Dead Time		LGATE Rising (V_{PHASE} = 1.5V)	--	30	--	ns
		UGATE Rising	--	30	--	
Internal Boost Charging Switch-On Resistance		VCC to BOOT, 10mA	--	--	80	Ω
EN Threshold						
EN Input Voltage Logic-High	V_{IH}		1.8	--	--	V
EN Input Voltage Logic-Low	V_{IL}		--	--	0.5	V
Mode Decision						
V_{RF} Threshold for DEM			--	--	0.5	V
V_{RF} Threshold for FCCM			1.8	--	--	V
PGOOD						
Trip Threshold (Falling, Leaving PGOOD)		Measured at FB, with respect to reference, Hysteresis = 3%	87	90	93	%
Trip Threshold (Rising, Leaving PGOOD)		Measured at FB, with respect to reference, Hysteresis = 3%	115	120	125	%
Fault Propagation Delay		Falling Edge, FB forced below PGOOD trip threshold	--	2.5	--	μs
Output Low Voltage		I_{SINK} = 1mA	--	--	0.4	V
Leakage Current		High State, forced to 5V	--	--	1	μA

Note 6. Guaranteed by design. Not production tested.

Note 7. Not production tested. Test condition is V_{IN} = 8V, V_{OUT} = 1.1V, I_{OUT} = 10A using application circuit.

13 Typical Application Circuit

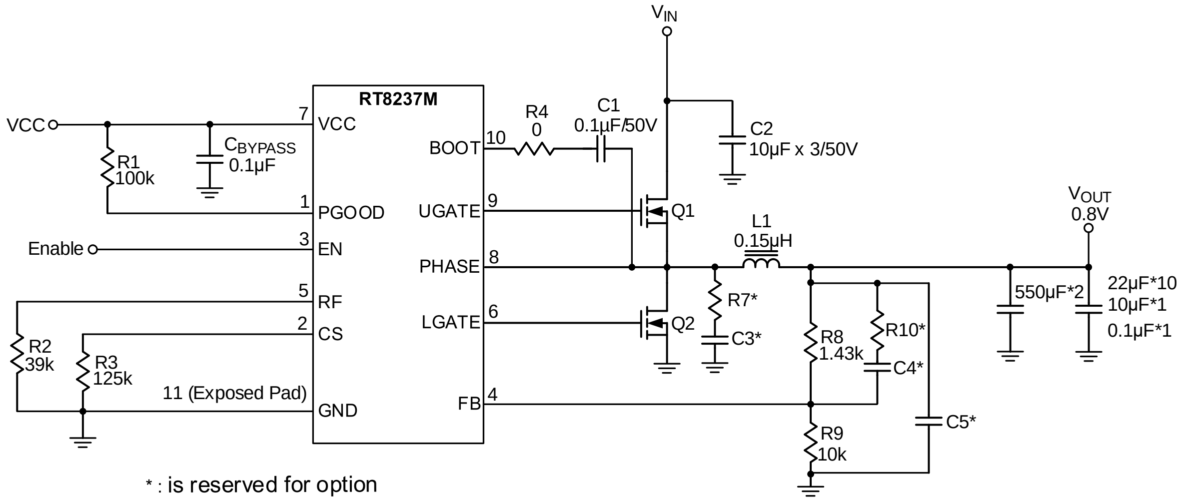


Figure 1. For VOUT = 0.8V

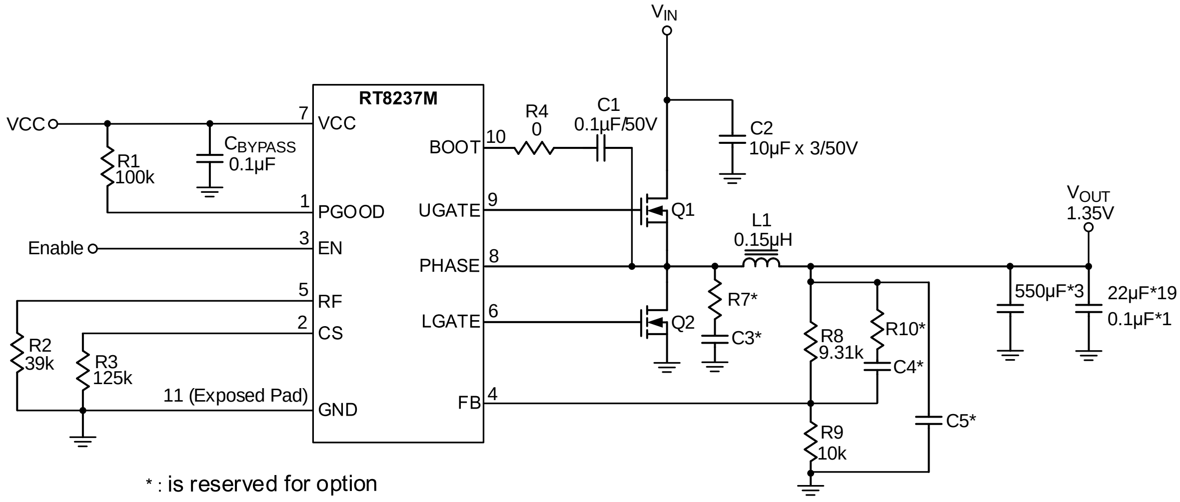


Figure 2. For VOUT = 1.35V

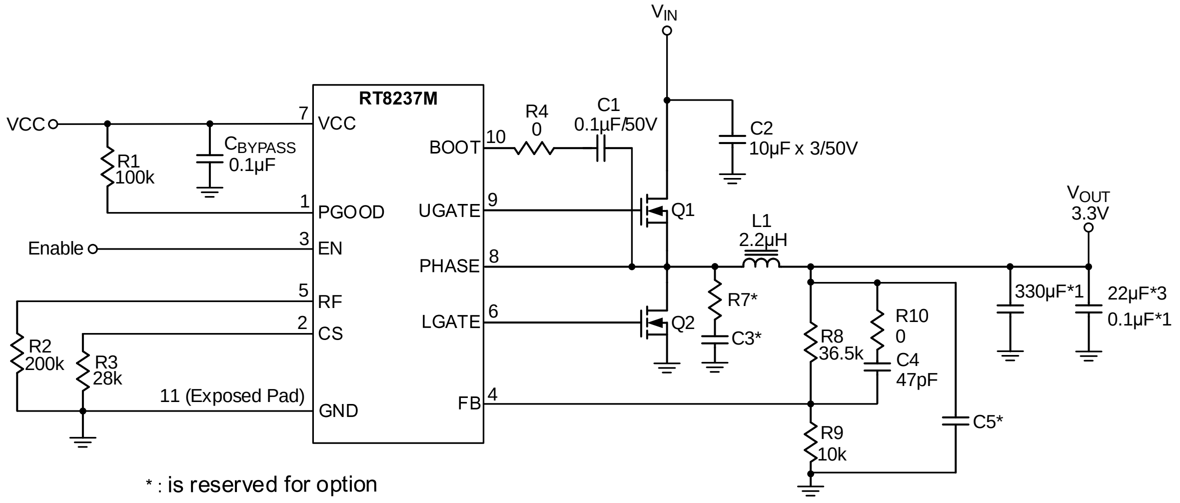
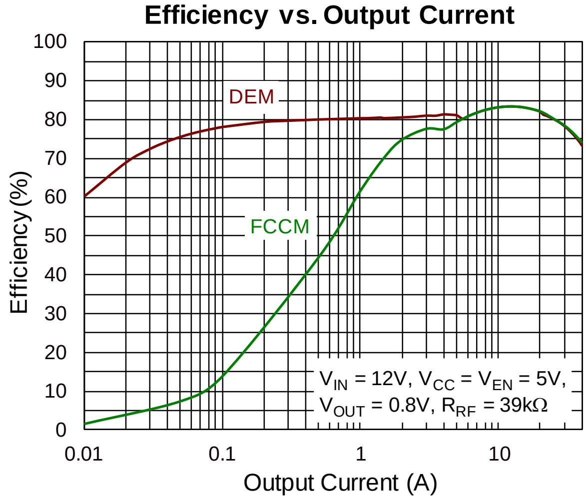
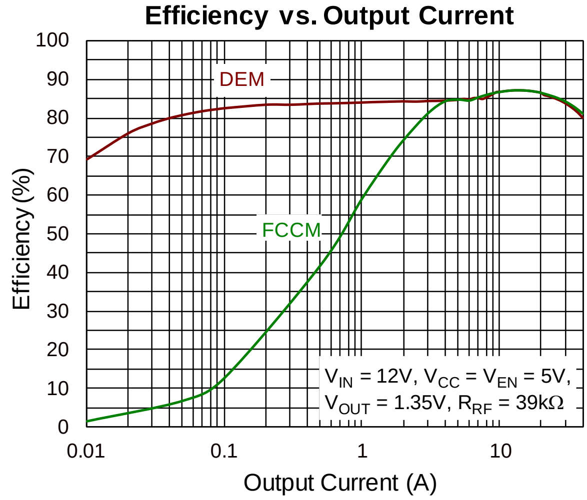
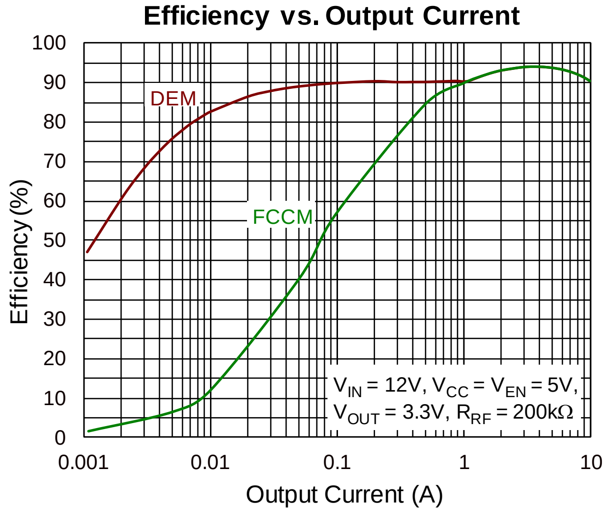


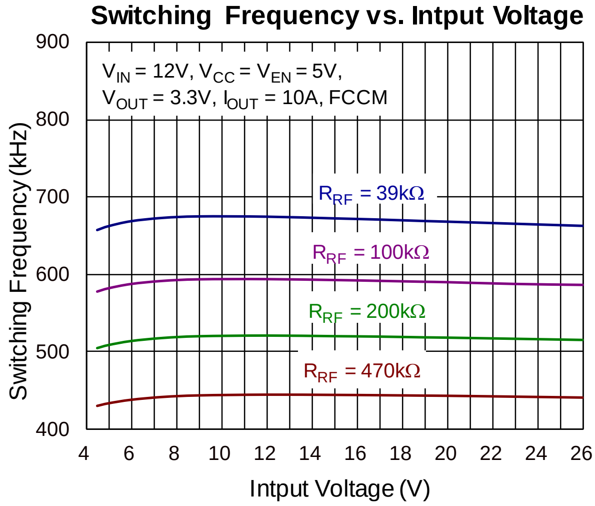
Figure 3. For VOUT = 3.3V

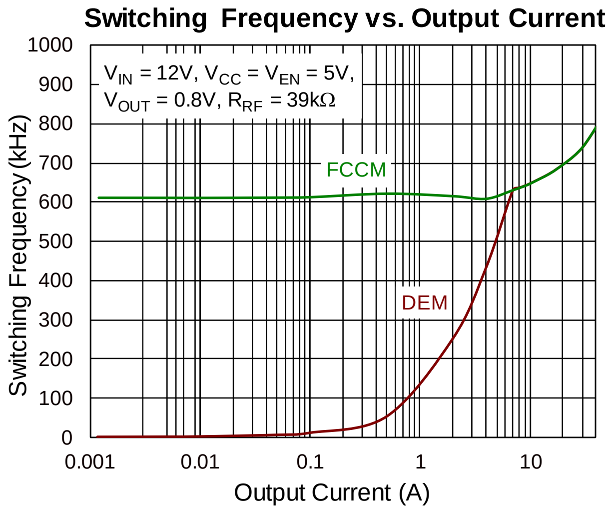
14 Typical Operating Characteristics

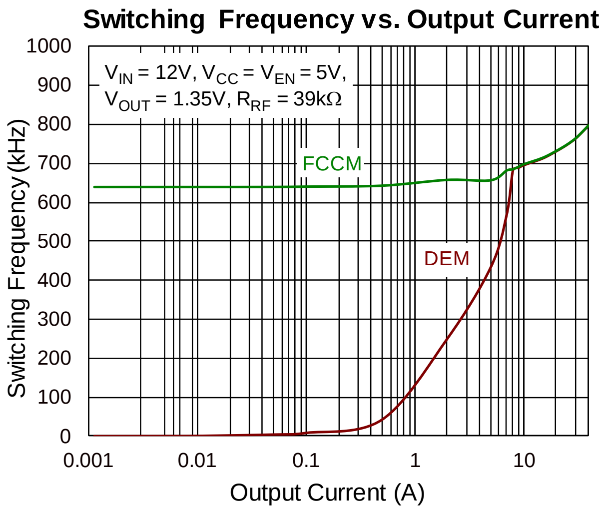


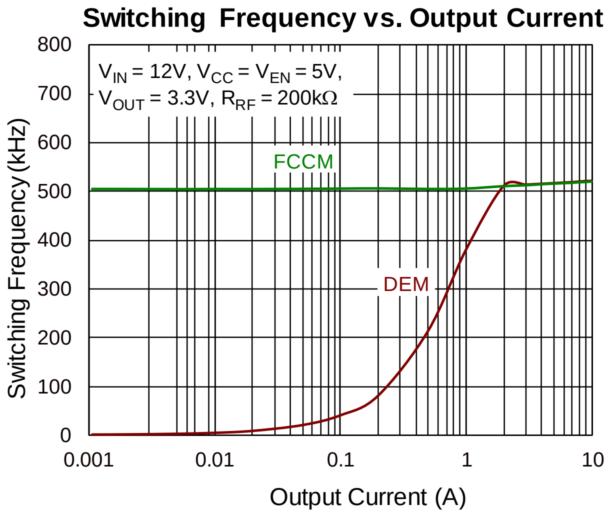


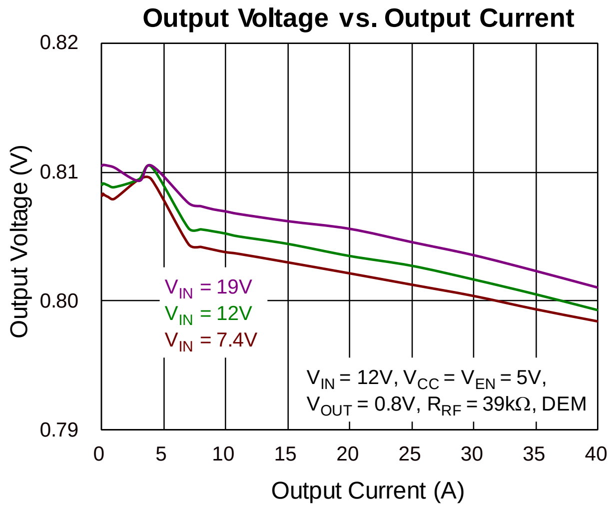


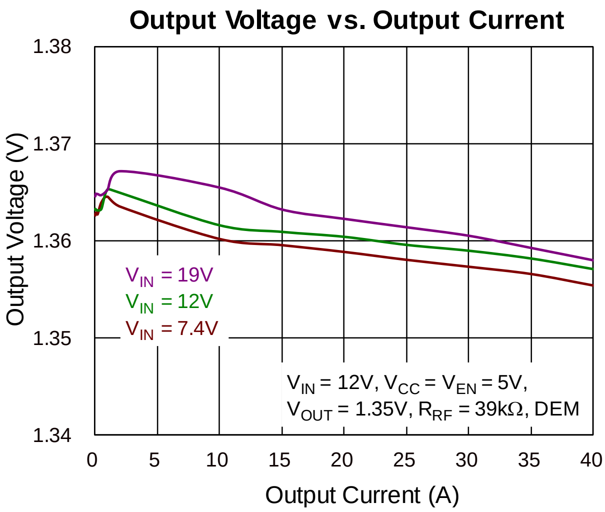


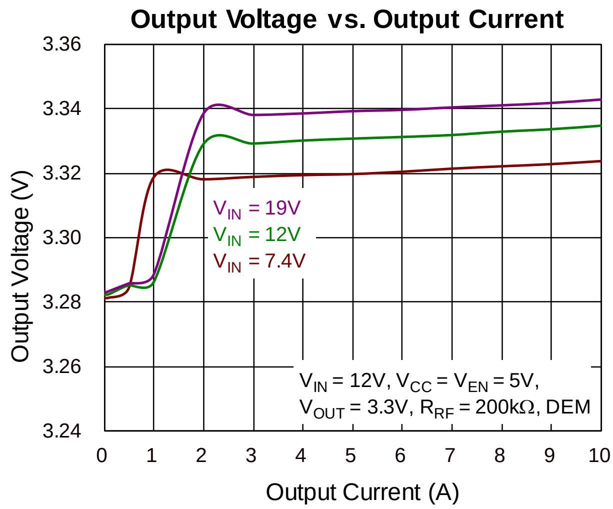


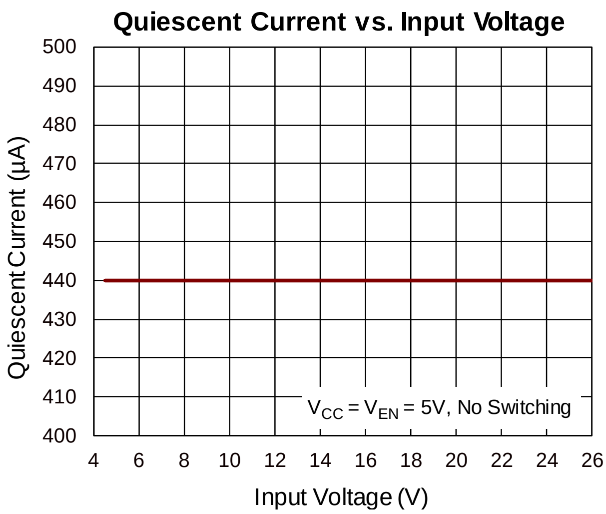


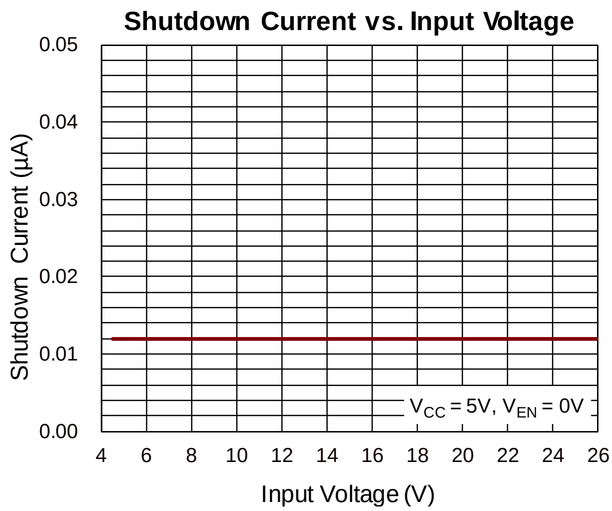

Switching Frequency vs. Output Current
VIN = 12V, VCC = VEN = 5V,
VOUT = 3.3V, RRF = 200kΩ
FCCM
DEM
Switching Frequency (kHz)
Output Current (A)
800
700
600
500
400
300
200
100
0
0.001
0.01
0.1
1
10


Output Voltage vs. Output Current
VIN = 19V
VIN = 12V
VIN = 7.4V
VIN = 12V, VCC = VEN = 5V,
VOUT = 0.8V, RRF = 39kΩ, DEM
Output Voltage (V)
Output Current (A)
0.82
0.81
0.80
0.79
0
5
10
15
20
25
30
35
40

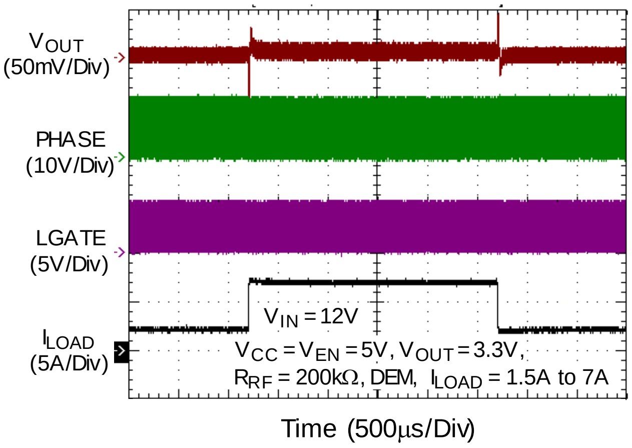

Output Voltage vs. Output Current
VIN = 19V
VIN = 12V
VIN = 7.4V
VIN = 12V, VCC = VEN = 5V,
VOUT = 1.35V, RRF = 39kΩ, DEM
Output Voltage (V)
Output Current (A)
1.38
1.37
1.36
1.35
1.34
0
5
10
15
20
25
30
35
40


Output Voltage vs. Output Current
VIN = 19V
VIN = 12V
VIN = 7.4V
VIN = 12V, VCC = VEN = 5V,
VOUT = 3.3V, RRF = 200kΩ, DEM
Output Voltage (V)
Output Current (A)
3.36
3.34
3.32
3.30
3.28
3.26
3.24
0
1
2
3
4
5
6
7
8
9
10

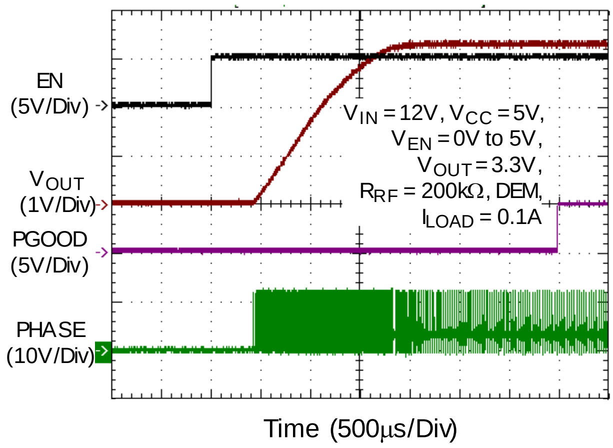

Quiescent Current vs. Input Voltage
VCC = VEN = 5V, No Switching
Quiescent Current (μA)
Input Voltage (V)
500
490
480
470
460
450
440
430
420
410
400
4
6
8
10
12
14
16
18
20
22
24
26


Shutdown Current vs. Input Voltage
VCC = 5V, VEN = 0V
Shutdown Current (μA)
Input Voltage (V)
0.05
0.04
0.03
0.02
0.01
0.00
4
6
8
10
12
14
16
18
20
22
24
26

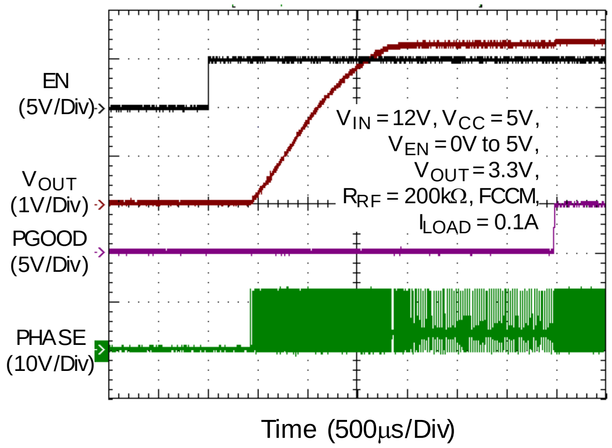
Load Transient Response



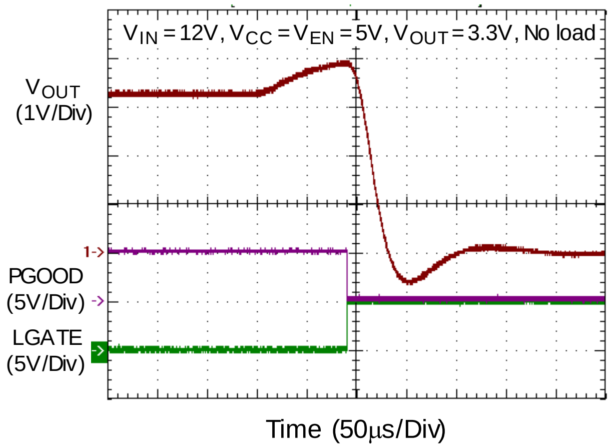
Power On from EN



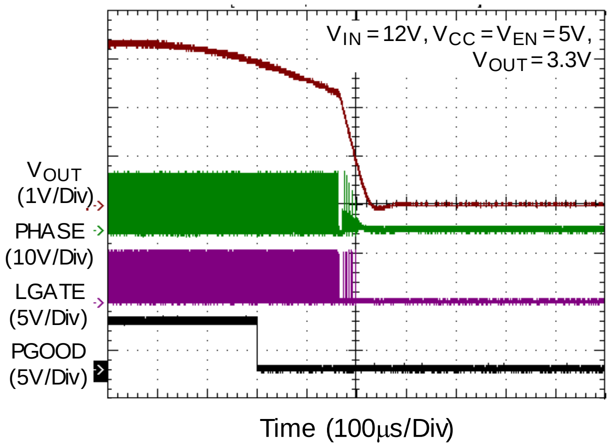
Power On from EN



OverVoltage Protection



UnderVoltage Protection



15 Operation

The RT8237M integrates a Constant-On-Time (COT) PWM controller that provides the PWM signal based on the comparison of the output ripple voltage with an internal reference voltage.

The UGATE driver is turned on at the beginning of each cycle. After the internal one-shot timer expires, the UGATE driver will be turned off. The pulse width of this one-shot is determined by the converter's input voltage and the output voltage to keep the frequency fairly constant across the range of the input and output voltages.

15.1 Power-On Reset and UVLO

The Power-On Reset (POR) occurs when VCC rises above approximately 4.1V (typical). At this threshold, the RT8237M resets the fault latch and prepares the PWM controller for operation. When the input voltage is below 3.7V(minimum), the Undervoltage Lockout (UVLO) circuitry inhibits switching by maintaining UGATE and LGATE low.

15.2 Soft-Start

The output voltage will track the internal ramp voltage during the soft-start interval to prevent large inrush currents and output voltage overshoot when the converter is powering up.

15.3 Mode Selection

The RT8237M supports mode selection through the RF by connecting a resistor from the RF pin to either GND or PGOOD. When the resistor is connected to GND, the controller operates in diode emulation mode. When the resistor is connected to PGOOD, the controller operates in CCM mode.

15.4 Current Limit Setting

The RT8237M has a cycle-by-cycle current limit control. The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the sensing signal at PHASE exceeds the current-limit threshold, the PWM is not allowed to initiate a new cycle.

15.5 Overvoltage Protection

The output voltage can be continuously monitored for overvoltage conditions. When the output voltage exceeds 20% of its set voltage threshold, the UGATE goes low and the LGATE is forced high.

15.6 Undervoltage Protection

The output voltage can be continuously monitored for undervoltage conditions. When the output voltage is less than 70% of its set voltage, the undervoltage protection is triggered and then both UGATE and LGATE gate drivers are forced low.

16 Application Information

(Note 9)

The RT8237M PWM controller provides high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high-voltage batteries to generate low voltage supply required for CPU cores, I/O, and chipset RAM supplies in notebook computers. Richtek Mach Response™ technology is specifically designed for providing a 100ns "instant-on" response to load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The topology solves the poor load transient response timing problems of fixed frequency current mode PWMs and avoids the problems caused by widely varying switching frequencies in conventional constant on-time and constant off-time PWM schemes.

16.1 On-Time Control (TON/MODE)

The on-time one-shot comparator has two inputs. One input monitors the output voltage from the PHASE pin, while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to VOUT, thereby making the on-time of the high-side switch directly proportional to output voltage and inversely proportional to input voltage.

The on-time is calculated using the following equation:

$t_{ON} = (V_{OUT}/V_{IN})/f_{SW}$

Table 1. RF Connection and Switching Frequency

R_{RF} (kΩ)	Switching Frequency (kHz)
470kΩ	435
200kΩ	510
100kΩ	570
39kΩ	645

Note 8. For DEM, connect R_{RF} to GND; for CCM, connect R_{RF} to PGOOD.

16.2 Enable and Disable

The EN pin allows for power sequencing between the controller bias voltage and another voltage rail. The RT8237M remains in shutdown if the EN pin is lower than 500mV. When the EN pin rises above the V_{EN} trip point, the RT8237M will begin a new initialization and soft-start cycle.

16.3 POR, UVLO, and Soft-Start

Power-On Reset (POR) occurs when VCC rises above approximately 4.1V. During this process, the RT8237M resets the fault latch and prepares the PWM for operation. When the input voltage is below 3.7V (minimum), the VCC Undervoltage Lockout (UVLO) circuitry inhibits switching by maintaining UGATE and LGATE low. A built-in soft-start is used to prevent the power supply input from surge currents after PWM is enabled. A ramping up current-limit threshold is implemented the V_{OUT} folded-back current during the soft-start duration.

16.4 Mode Selection (RF) Operation

To select the operation mode, connect a resistor from the RF pin to either GND or PGOOD. When the resistor is connected to GND, the controller operates in diode emulation mode. When the resistor is connected to PGOOD, the controller operates in CCM mode.

16.5 Diode-Emulation Mode (R_{RF} Connected to GND)

In diode-emulation mode, the RT8237M automatically reduces the switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly without increasing V_{OUT} ripple or load regulation. As the output current decreases from heavy load conditions, the inductor current is reduced and eventually reaches the point where its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. To emulate the behavior of diodes, the low-side MOSFET allows only partial negative current to flow when the inductor freewheeling current reaches negative. As the load current is further decreased, it takes longer and longer to discharge the output capacitor to the level that requires the next "ON" cycle. The on-time is kept the same as in heavy load conditions. On the contrary, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous condition. This is shown in Figure 4. The transition load point to the light load operation is calculated as follows:

$$I_{LOAD} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is the on-time.

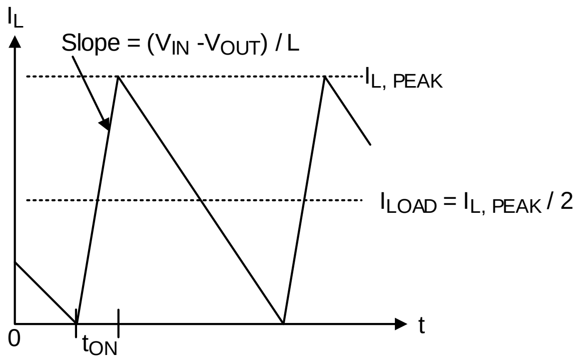


Figure 4. Boundary Condition of CCM/DCM

The switching waveforms may appear noisy and asynchronous when light loading causes diode-emulation operation, but this is a normal operating condition that results in high light load efficiency. Trade-offs between DEM noise and light load efficiency are achieved by varying the inductor value. The disadvantages for using higher inductor values include a larger physical size and degraded load transient response (especially at low input voltage levels).

16.6 Forced-CCM Mode (FCCM)

The low noise, forced-CCM mode disables the zero- crossing comparator, which controls the low-side switch on-time. This causes the low-side gate drive waveform to become the complement of the high-side gate drive waveform. This, in turn, causes the inductor current to reverse at light loads as the PWM loop works to maintain duty ratio of V_{OUT}/V_{IN}. A fairly constant switching frequency is the benefit of the forced-CCM mode, but this comes with a cost. The no-load battery current can range from 10mA to 40mA, depending on the external MOSFETs.

16.7 Current Limit Setting (CS)

The RT8237M has a cycle-by-cycle current limit control. The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current-limit threshold, the PWM is prevented from initiating a new cycle (see Figure 5). To ensure both accuracy and cost-effectiveness, the RT8237M supports temperature-compensated MOSFET $R_{DS(ON)}$ sensing.

The CS pin of RT8237M is the current limit threshold setting pin. The current limit threshold is equal to 1/8 of the voltage on this pin.

To choose a current limit resistor, use the following equation:

$$R_{OC\_SET} = \frac{V_{CS\_OC}}{I_{CS}} = \frac{\left(I_{LOAD\_OC} - \frac{I_{RIPPLE}}{2}\right) \times 8 \times R_{DS(ON)}}{I_{CS}}$$

The inductor current is monitored by the voltage between the GND and PHASE pins, so the PHASE pin should be connected to the Drain terminal of the low-side MOSFET. I_{CS} has a temperature coefficient to compensate for the temperature dependency of the $R_{DS(ON)}$. GND is used as the positive current sensing node, so GND should be connected to the Source terminal of the low-side MOSFET.

the comparison is performed during the OFF state, with V_{LIMIT} (current-limit threshold) establishing the valley level of the inductor current. Thus, the load current at the overcurrent threshold, I_{LOAD_OC}, can be calculated as follows:

$$I_{LOAD\_OC} = \frac{V_{CS\_OC}}{8 \times R_{DS(ON)}} + \frac{I_{RIPPLE}}{2} = \frac{V_{CS\_OC}}{8 \times R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

In an overcurrent condition, the current supplied to the load exceeds the current to the output capacitor. Thus, the output voltage falls and eventually crosses the undervoltage protection threshold, inducing IC shutdown.

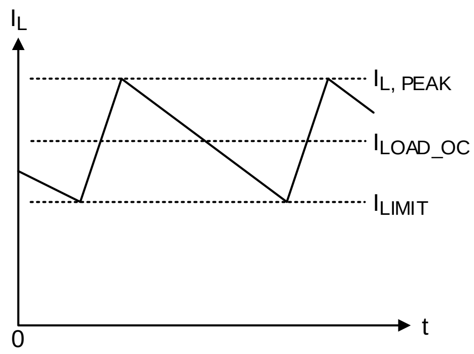


Figure 5. "Valley" Current Limit

When the device operates in the FCCM, the negative current limit protects the external component. The negative current limit detect threshold is set as the same value as positive current limit but negative polarity. The threshold still is the valley value of the inductor current.

16.8 MOSFET Gate Driver

The high-side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, a 5V bias voltage is delivered from the VCC supply. The average drive current is proportional to the gate charge at V_{GS} = 5V times the switching frequency. The instantaneous drive current is supplied by the flying capacitor between the BOOT and PHASE pins. To prevent shoot through, a dead-time is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on. The low-side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). The internal pull-down transistor that drives LGATE low is robust, with a 0.5Ω typical on-resistance. A 5V bias voltage is delivered from the VCC supply. The instantaneous drive current is supplied by the flying capacitor between VCC and GND.

For high current applications, certain combinations of high and low-side MOSFETs may cause excessive gate-drain coupling, which can lead to efficiency-killing, EMI-producing shoot-through currents. This is often remedied by adding a resistor in series with BOOT, which increases the turn-on time of the high-side MOSFET without degrading the turn-off time (see Figure 6).

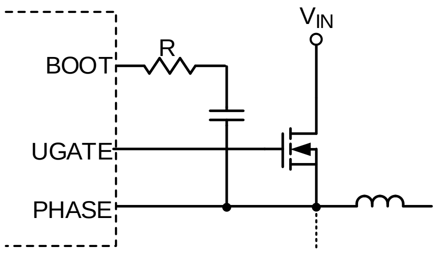


Figure 6. Reducing the UGATE Rise Time

16.9 Power-Good Output (PGOOD)

The power-good output is an open-drain output and requires a pull-up resistor. When the output voltage is 20% above or 10% below its set voltage, PGOOD will be pulled low. It is held low until the output voltage returns to within these tolerances once more. During soft-start, PGOOD is actively held low and transitions high only after soft- start is complete and the output reaches 90% of its set voltage. A 2.5μs delay is built into the PGOOD circuitry to prevent false transitions.

16.10 Output Overvoltage Protection (OVP)

The output voltage is continuously monitored for overvoltage conditions. When the output voltage exceeds 20% of its set voltage threshold, overvoltage protection is triggered, and the low-side MOSFET is latched on. This activates the low-side MOSFET to discharge the output capacitor. The RT8237M is latched once OVP is triggered and can only be released by VCC or EN power-on reset. A 5μs delay is built into the overvoltage protection circuit to prevent false transitions.

16.11 Output Undervoltage Protection (UVP)

The output voltage can be continuously monitored for undervoltage conditions. When the output voltage falls below 70% of its set voltage threshold, undervoltage protection is triggered, and then both UGATE and LGATE gate drivers are forced low. A 2.5μs delay built into the undervoltage protection circuit to prevent false transitions. During soft-start, the UVP blanking time is 3ms.

16.12 Thermal Shutdown (OTP)

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 150°C. When the junction temperature exceeds the thermal shutdown threshold, the OTP function is triggered, leading the RT8237M to shut down and enter Latch-Off Mode. In Latch-Off Mode, the RT8237M can be reset by EN or the power input VCC.

16.13 Output Voltage Setting (FB)

The output voltage can be adjusted from 0.7V to 3.3V by setting the feedback resistors, R1 and R2 (see Figure 7). Choose R2 to be approximately 10kΩ and solve for R1 using the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} is 0.704V (typical).

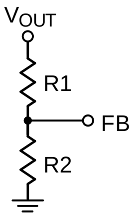


Figure 7. Setting V_{OUT} with a Resistive Voltage Divider

16.14 Inductor Selection

The inductor plays an important role in step-down converters because it stores the energy from the input power rail and then releases the energy to the load. From the viewpoint of efficiency, the DC resistance (DCR) of the inductor should be as small as possible to minimize the conduction loss. In addition, because the inductor occupies a significant portion of the board space, its size is also important. Low-profile inductors can save board space, especially when there is a height limitation. However, low DCR and low-profile inductors are usually cost ineffective.

Additionally, larger inductance results in lower ripple current, leading to lower power loss. The inductor current rising time increases with inductance value, resulting in slower transient response. Therefore, the inductor design involves a compromise between performance, size, and cost.

In general, the inductance is designed such that the ripple current ranges between 20% to 40% of the full load current. The inductance can be calculated using the following equation:

$$L_{MIN} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times k \times I_{OUT\_rated}} \times \frac{V_{OUT}}{V_{IN}}$$

where k is the ratio between inductor ripple current and rated output current.

16.15 Input Capacitor Selection

Voltage rating and current rating are the key parameters in selecting an input capacitor. For a conservatively safe design, an input capacitor should generally have a voltage rating 1.5 times greater than the maximum input voltage.

The input capacitor is used to supply the input RMS current, which is approximately calculated using the following equation:

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is to select a proper capacitor for RMS current rating. Placing more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank is a good design. Also, placing a ceramic capacitor close to the Drain of the high-side MOSFET is helpful in reducing the input voltage ripple at heavy load.

16.16 Output Capacitor Selection

The output capacitor and the inductor form a low-pass filter in the buck topology. In steady-state condition, the ripple current that flows into or out of the capacitor results in ripple voltage. The output voltage ripples contain two components, ΔV_{OUT_ESR} and ΔV_{OUT_C}.

$$\Delta V_{OUT\_ESR} = \Delta I_L \times ESR$$

$$\Delta V_{OUT\_C} = \Delta I_L \times \frac{1}{8 \times C_{OUT} \times f_{SW}}$$

When a load transient occurs, the output capacitor supplies the load current before the controller can respond. Therefore, the ESR will dominate the output voltage sag during a load transient. The output voltage sag can be calculated using the following equation.

$$V_{OUT\_sag} = ESR \times \Delta I_{OUT}$$

For a given output voltage sag specification, the ESR value can be determined.

Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). A rapid change in load current results in di/dt during a transient. Therefore, ESL contributes to part of the voltage sag. Use a capacitor that has low ESL to obtain better transient performance. Generally, using several capacitors in parallel will have better transient performance than using a single capacitor for the same total ESR.

Unlike the electrolytic capacitor, the ceramic capacitor has a relatively low ESR and can reduce the voltage deviation during a load transient. However, the ceramic capacitor can only provide a low capacitance value. Therefore, use a mixed combination of an electrolytic capacitor and a ceramic capacitor for better transient performance.

16.17 MOSFET Selection

The majority of power loss in the step-down power conversion comes from the loss in the power MOSFETs. For low-voltage, high-current applications, the duty cycle of the high-side MOSFET is small. Therefore, the switching loss of the high-side MOSFET is a concern. Power MOSFETs with lower total gate charge are preferred in such applications.

However, the small duty cycle means the low-side MOSFET is on for most of the switching cycle. Therefore, the conduction loss tends to dominate the total power loss of the converter. To improve the overall efficiency, MOSFETs with low $R_{DS(ON)}$ are preferred in circuit design. In some cases, more than one MOSFET is connected in parallel to further decrease the on-state resistance. However, this depends on the low-side MOSFET driver capability and the budget.

16.18 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating

Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-10L 3x3 package, the thermal resistance, θ_{JA}, is 55.02°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (125°C − 25°C) / (55.02°C/W) = 1.82W for a WDFN-10L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 8 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

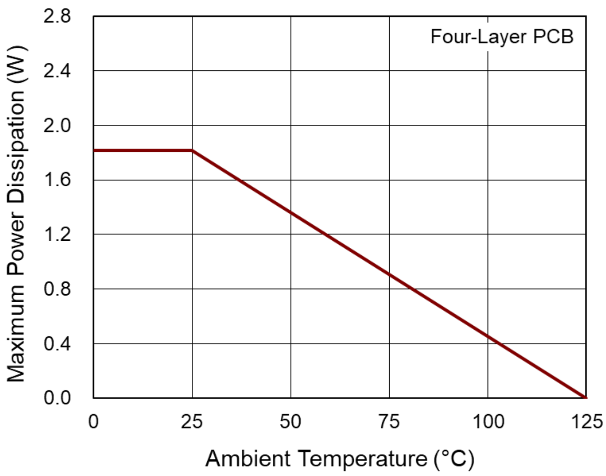


Figure 8. Derating Curve of Maximum Power Dissipation

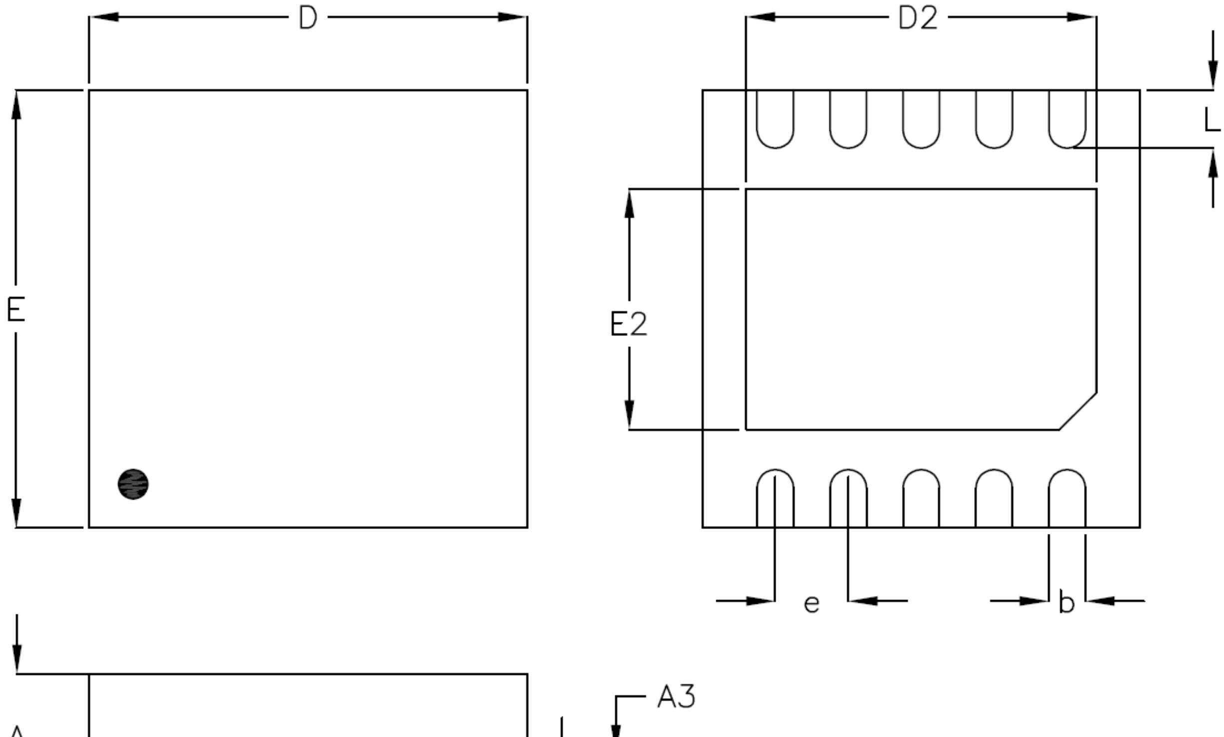
16.19 Layout Considerations

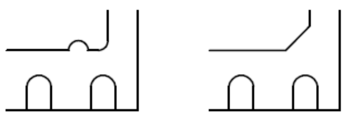
Layout is very important in high-frequency switching converter design. If designed improperly, the PCB may radiate excessive noise and contribute to converter instability. The following factors must be considered before starting a layout for the RT8237M.

- Connect an RC low-pass filter for VCC; 1μF and 10Ω are recommended. Place the filter capacitor close to the IC.
- Keep current limit setting network as close to the IC as possible. Routing of the network should avoid coupling to the high-voltage switching node.
- Connections from the drivers to the respective gate of the high-side or low-side MOSFET should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components such as FB, GND, EN, CS, PGOOD, VCC, and RF should be placed away from high-voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Current sense connections must always be made using Kelvin connections to ensure an accurate signal, with the current limit resistor located at the device.
- Power sections should directly connect to ground plane(s) using multiple vias as required for current handling (including the IC power ground connections). Power components should be placed close to the IC to minimize loops and reduce losses.

Note 9. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

17 Outline Dimension





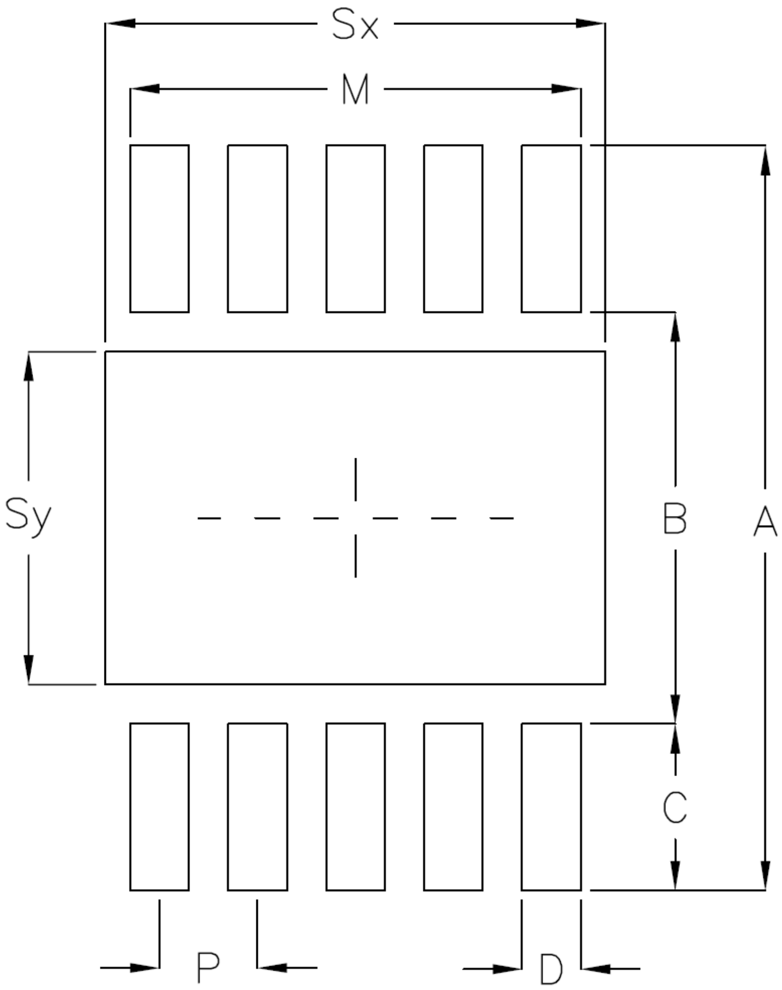
DETAIL A
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L QFN 3x3 Package

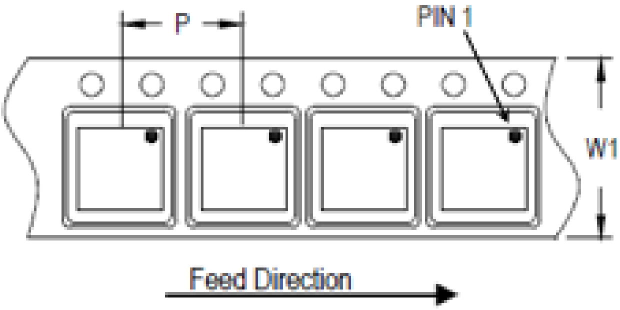
18 Footprint Information

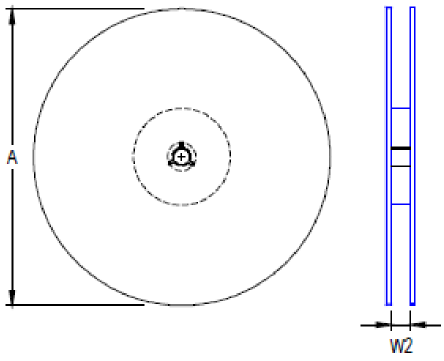


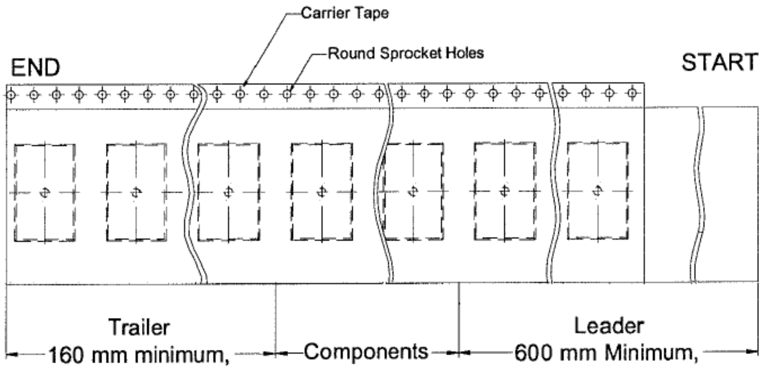
Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/X/ZDFN3*3-10	10	0.50	3.80	2.10	0.85	0.30	2.55	1.70	2.30	±0.05

19 Packing Information

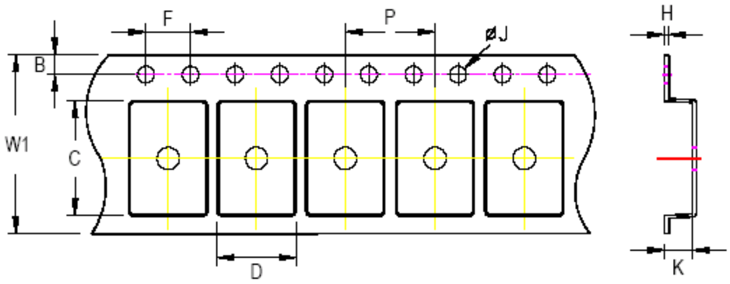
19.1 RT8237MGQW(2) Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4

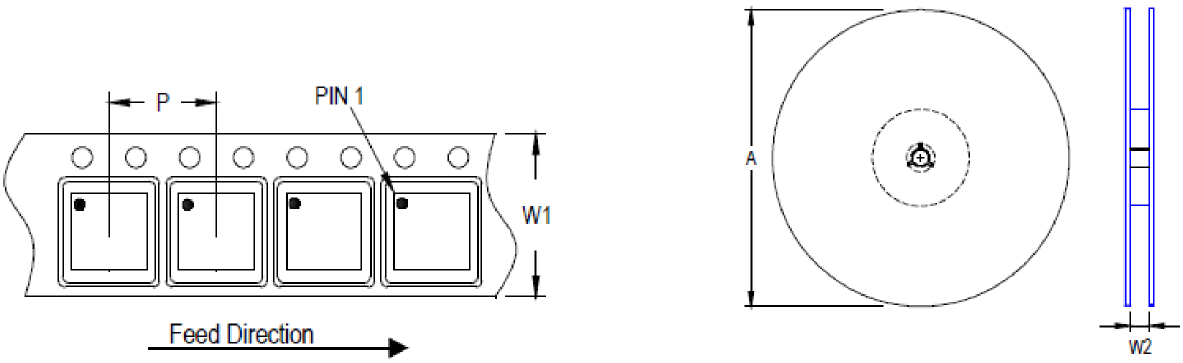


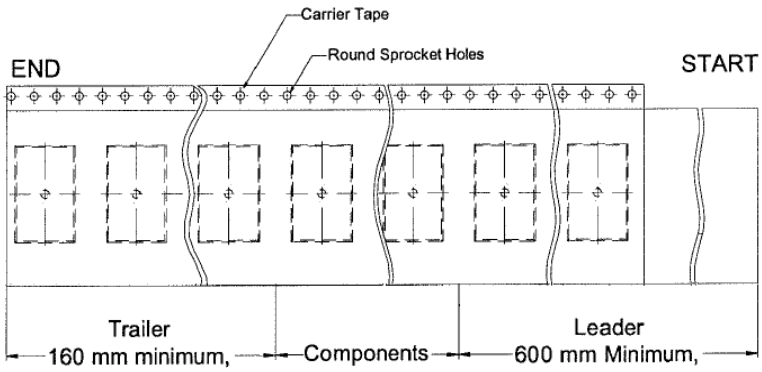
C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

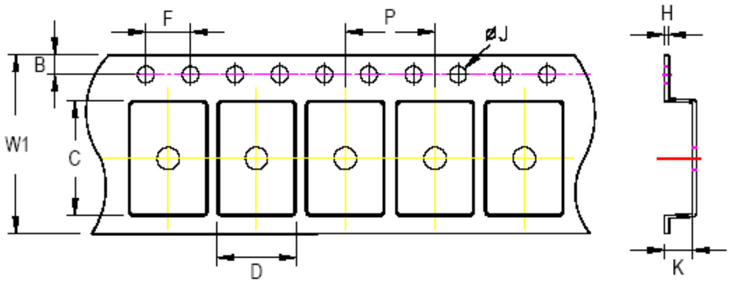
Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

19.2 RT8237MGQW Tape and Reel Data





Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

19.3 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN/DFN 3x3	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

19.4 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description	Item
00	2024/6/19	Final	