General Purpose 3-Phase PWM Controller for High-Density Power Supply

General Description

The RT8800A is a general-purposed multi-phase synchronous buck controller dedicating for high power density applications. The RT8800A operates with 2 or 3 synchronous buck switching stages in interleaved phase set automatically. The multiphase architecture provides high output current while maintaining low power dissipation on power devices and low stress on input and output capacitors.

The output voltage is precisely regulated to the external reference voltage at PI pin. The RT8800A can provide Intel® VRD10.x or AMD® K8 compliant output voltage when companioned with DAC generator RT9401A/B.

The RT8800A adopts innovative time-sharing DCR current sensing technique for channel current balance, droop tuning, and over current protection. Using one common GM amplifier for current sensing eliminates offset errors and linearity variation between GMs. As sub-milli-ohm-grade inductors are widely used in modern mother boards, slight mismatch of GM amplifiers offset and linearity results in considerable current shift between phases. The time-sharing DCR current sensing technique is extremely important to guarantee phase current balance at mass production.

Other features include overvoltage protection, undervoltage protection and internal softstart. The RT8800A comes to a VQFN-16L 3x3 package.

Ordering Information

RT8800A □ □

Package Type
QV : VQFN-16L 3x3 (V-Type)

Lead Plating System
P : Pb Free
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **5V Power Supply Voltage**
- **2/3-Phase Power Conversion with Automatic Phase Selection**
- **Output Voltage Controlled by External Reference Voltage**
- **Precise Core Voltage Regulation**
- **Power Stage Thermal Balance by DCR Current Sensing**
- **Extreme Low-Cost, Lossless Time Sharing Current Sensing**
- **Internal Soft-Start**
- **Hiccup Mode Over-Current Protection**
- **Over Voltage Protection**
- **Adjustable Operating Frequency and Typical at 300kHz Per Phase**
- **Power Good Indication**
- **Small 16-Lead VQFN Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

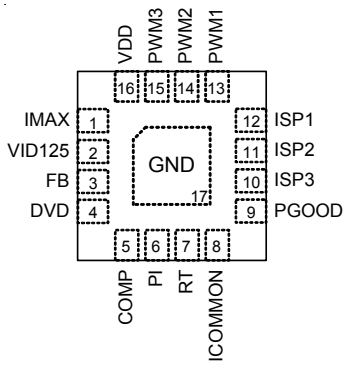
- Desktop CPU Core Power
- Low Output Voltage, High Power Density DC/DC Converters
- Voltage Regulator Modules

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Pin Configurations

(TOP VIEW)



VQFN-16L 3x3

Functional Pin Description

IMAX (Pin 1)

Over current protection setting.

VID125 (Pin 2)

Connect a resistor from this pin to GND can raise V_{OUT}.

FB (Pin 3)

The pin is defined as the inverting input of internal error amplifier.

DVD (Pin 4)

The pin is defined as a programmable power UVLO detection input. Trip threshold = 0.8V at V_{DVD} rising.

COMP (Pin 5)

The pin is defined as the output of the error amplifier and the input of all PWM comparators.

PI (Pin 6)

The pin is defined as the positive input of the error amplifier.

RT (Pin 7)

Switching frequency setting. Connect this pin to GND with a resistor to set the frequency.

ICOMMON (Pin 8)

Common negative input of current sense amplifiers for all three channels.

PGOOD (Pin 9)

Output power-good indication. The signal is implemented as an output signal with open-drain type.

ISP1 , ISP2 , ISP3 (Pin 12, Pin 11, Pin 10)

Current sense positive inputs for individual converter channel current sense.

PWM1 , PWM2 , PWM3 (Pin 13, Pin 14, Pin 15)

PWM outputs for each phase switching drive.

VDD (Pin 16)

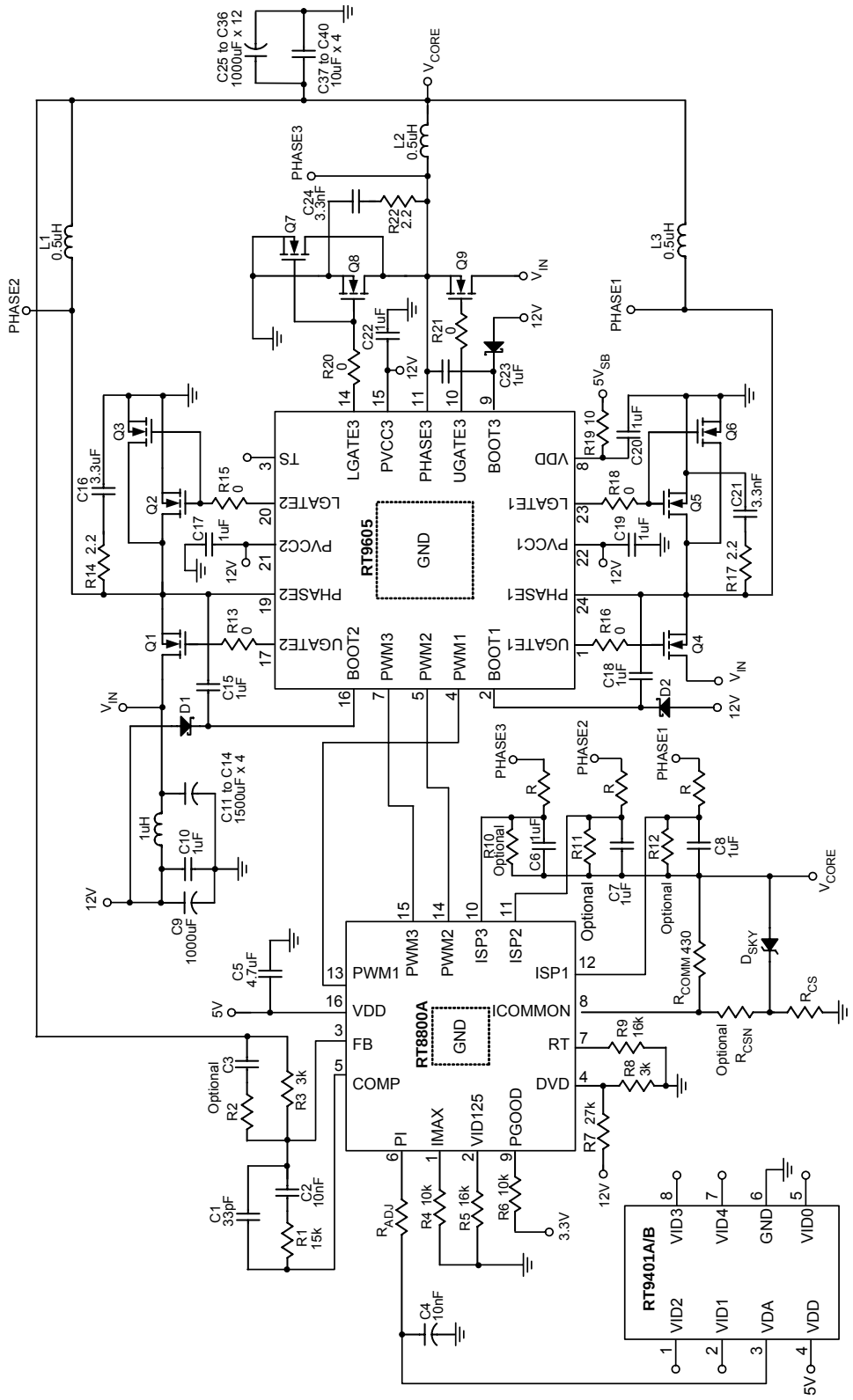
Chip power supply. Connect this pin to a 5V supply.

GND [Exposed Pad (17)]

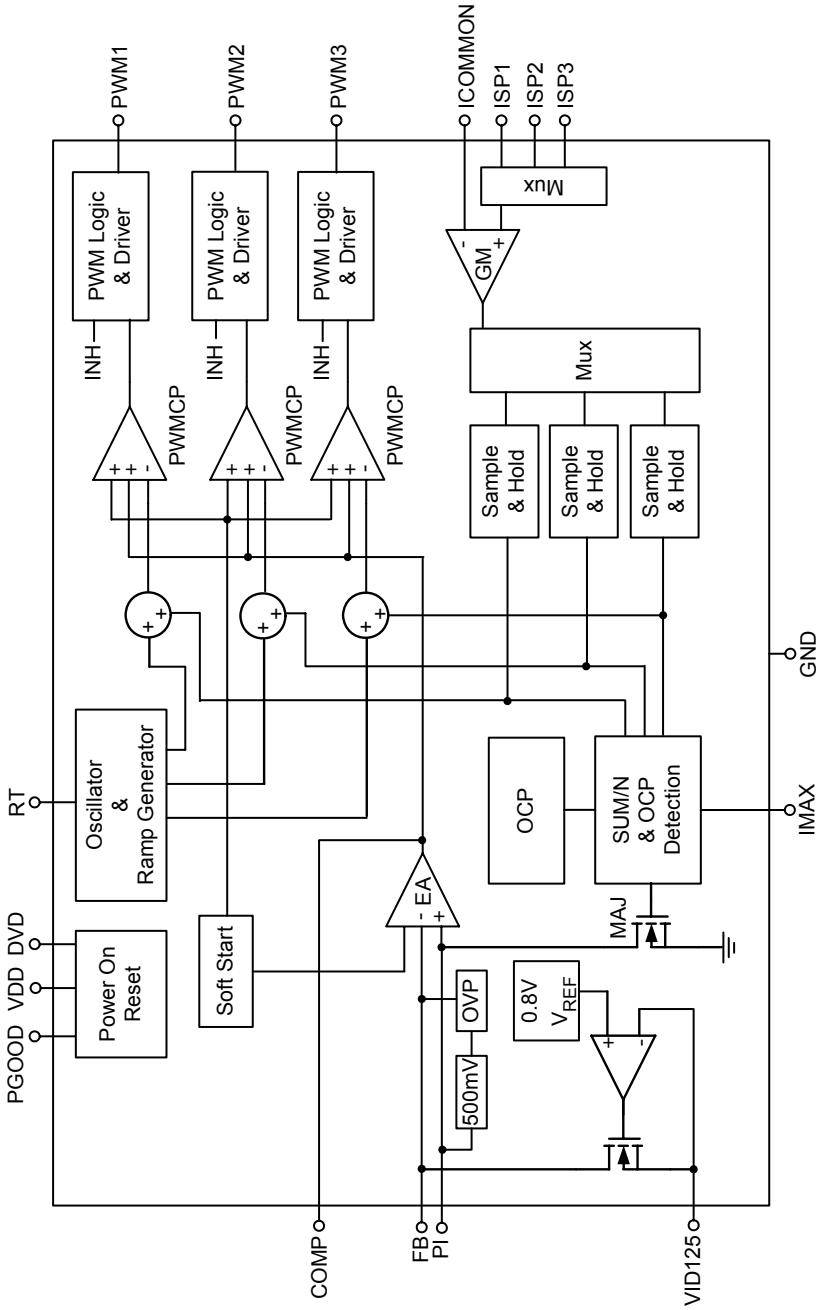
The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Typical Application Circuit

3-phase with RT9401A/B DAC generator



Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{DD} ---------- 7V
- Input, Output or I/O Voltage ---------- GND – 0.3V to V_{DD} + 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-16L 3x3 ---------- 1.47W
- Package Thermal Resistance (Note 2)
  VQFN-16L 3x3, θ_{JA} ---------- 68°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{DD} ---------- 5V ± 10%
- Ambient Temperature Range ---------- 0°C to 70°C
- Junction Temperature Range ---------- 0°C to 125°C

Electrical Characteristics

(V_{DD} = 5V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
V_{DD} Supply Current							
Nominal Supply Current		I_{DD}	PWM 1,2,3 Open	--	5	--	mA
Power-On Reset							
V_{DD} Threshold	Rising			4.0	4.2	4.5	V
	Hysteresis			0.2	0.5	--	
DVD Rising Threshold				0.75	0.8	0.85	V
DVD Hysteresis				--	65	--	mV
Oscillator							
Free Running Frequency		f_{OSC}	R_{RT} = 16kΩ	170	200	230	kHz
Frequency Adjustable Range		f_{OSC_ADJ}		50	--	400	kHz
Ramp Amplitude		ΔV_{OSC}	R_{RT} = 16kΩ	--	1.7	--	V
Ramp Valley		V_{RV}		--	1.0	--	V
Maximum On-Time of Each Channel				62	66	75	%
RT Pin Voltage		V_{RT}	R_{RT} = 16kΩ	0.77	0.82	0.87	V
Reference Voltage							
IMAX Reference Voltage		V_{IMAX}	R_{IMAX} = 16kΩ	0.75	0.8	0.85	V
VID125 Reference Voltage		V_{VID125}	R_{VID125} = 16kΩ	0.75	0.8	0.85	V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Error Amplifier						
DC Gain			--	65	--	dB
Gain-Bandwidth Product	GBW	C_L = 10pF	--	10	--	MHz
Slew Rate	SR	C_L = 10pF	--	8	--	V/μs
Current Sense GM Amplifier						
Recommended Full Scale Source Current			100	--	--	μA
Protection						
Over-Voltage Trip (V_{FB} – V_{PI})			360	460	560	mV
Power Good						
PGOOD Output Low Voltage	V_{PGOOD}	I_{PGOOD} = 4mA	--	--	0.2	V
PGOOD Delay	T_{PGOOD_Delay}	90% * V_{OUT} to PGOOD_H	4	--	8	ms

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

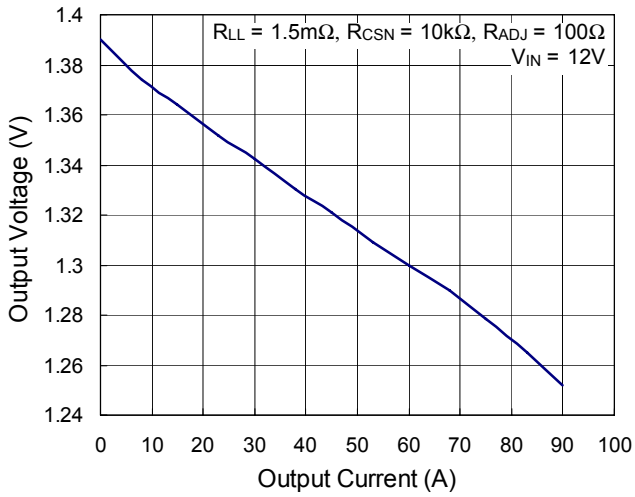
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

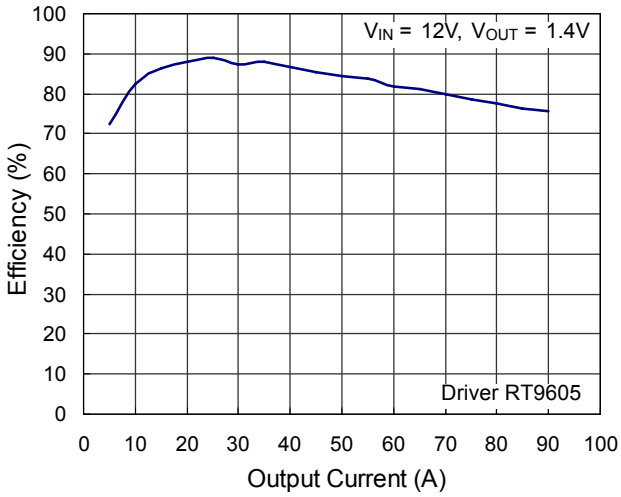
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

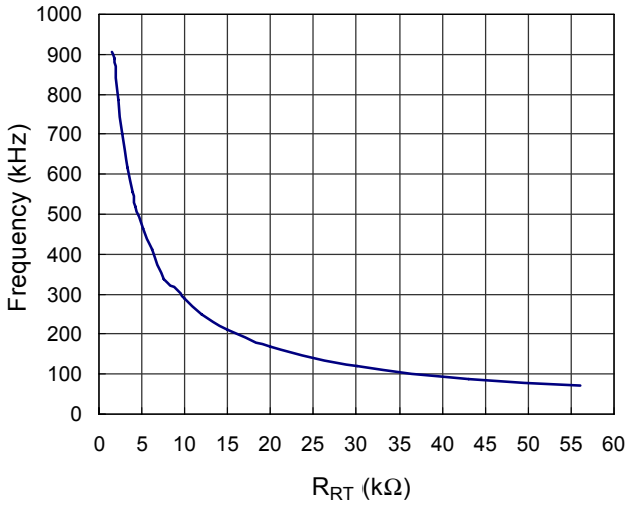
Load Line



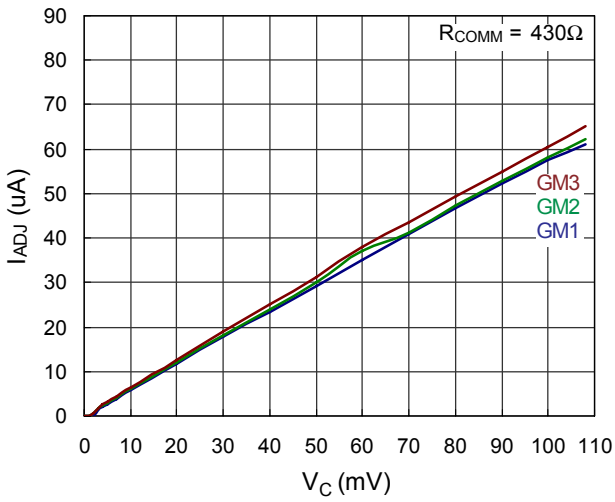
Efficiency vs. Output Current



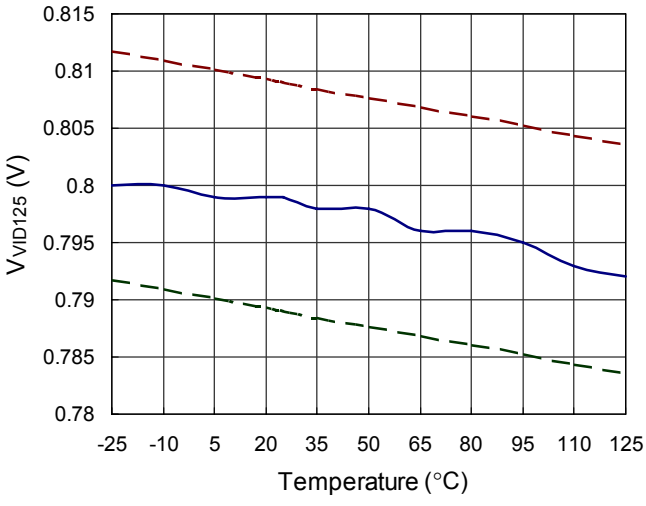
Frequency vs. R_{RT}



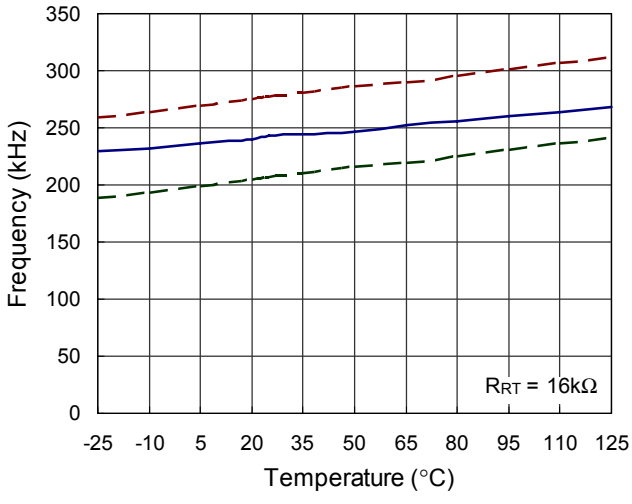
GM



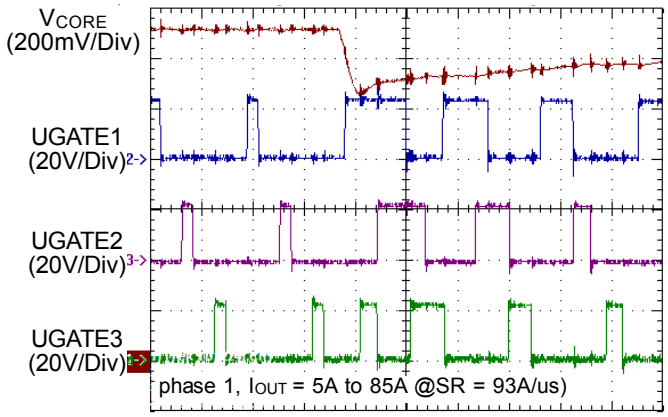
V_{VID125} vs. Temperature



Frequency vs. Temperature

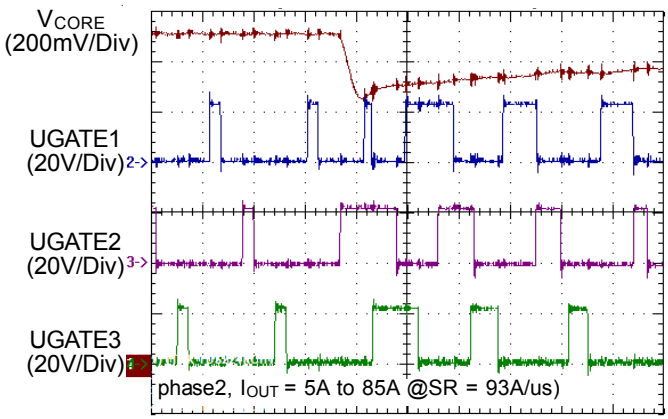


Load Transient Response



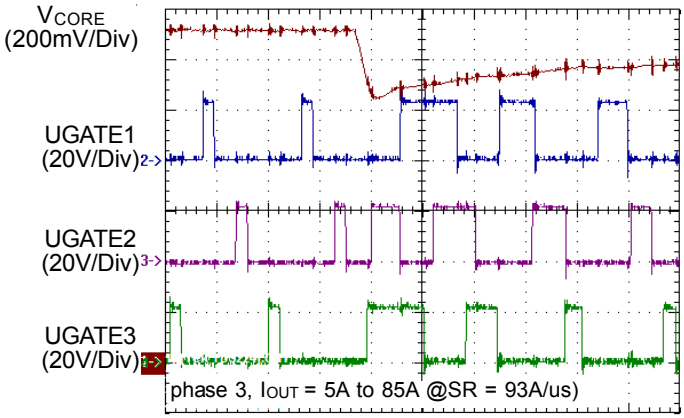
Time (2.5µs/Div)

Load Transient Response



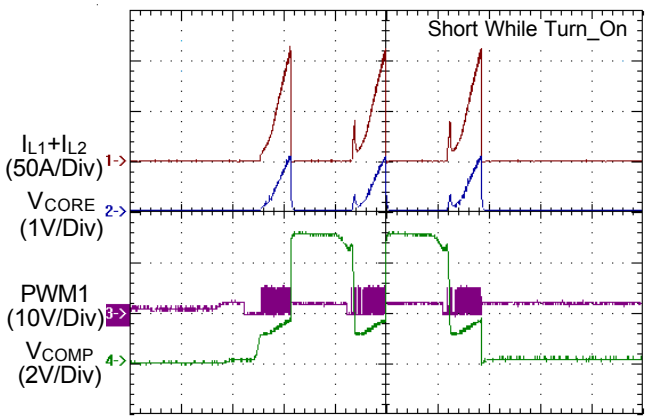
Time (2.5µs/Div)

Load Transient Response



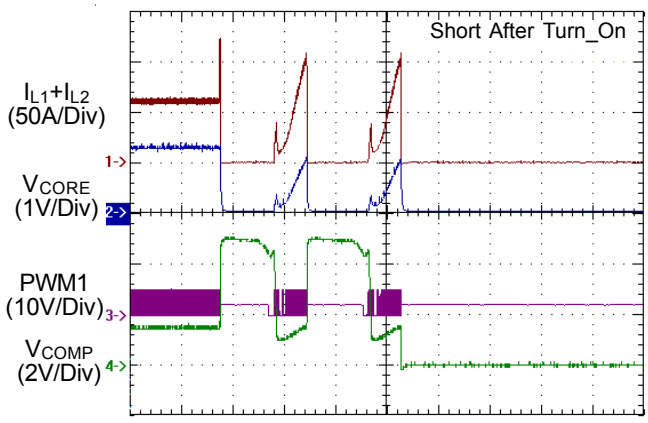
Time (2.5µs/Div)

Over Current Protection



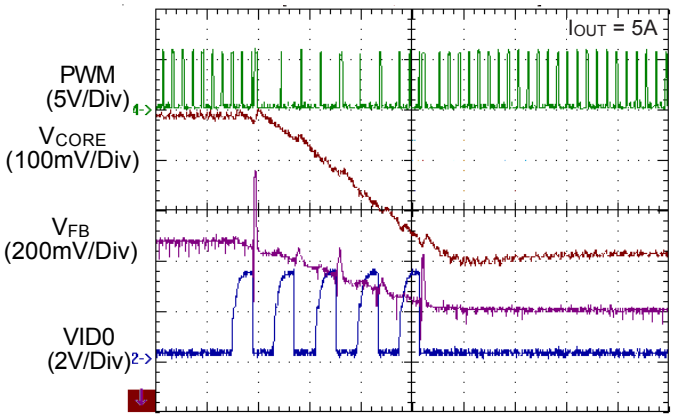
Time (10ms/Div)

Over Current Protection



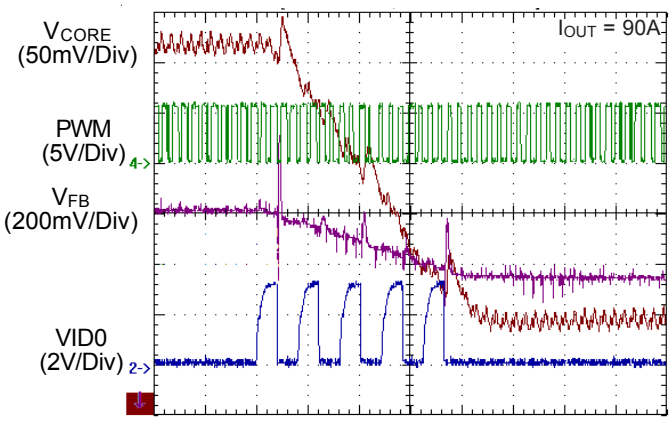
Time (10ms/Div)

VID On the Fly Falling

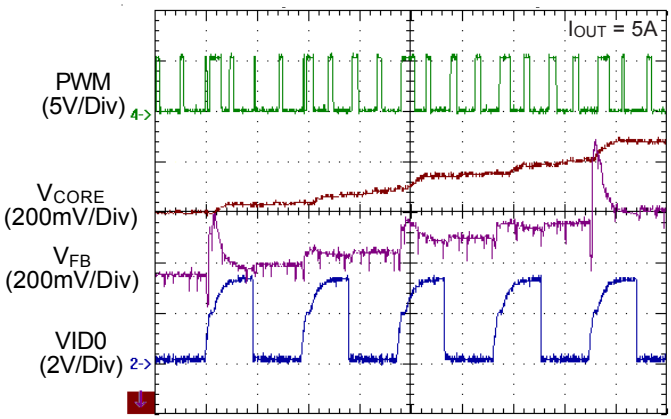


Time (25µs/Div)

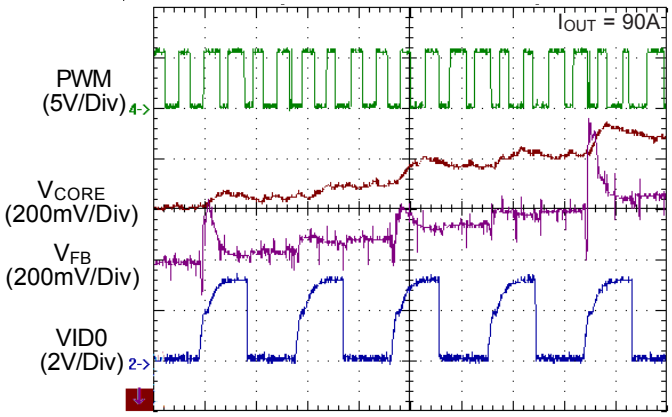
VID On the Fly Falling



VID On the Fly Rising



VID On the Fly Rising



Applications Information

The RT8800A is a general-purposed multi-phase synchronous buck controller dedicating for high power density applications. The RT8800A operates with 2 or 3 synchronous buck switching stages in interleaved phase set automatically. The multiphase architecture provides high output current while maintaining low power dissipation on power devices and low stress on input and output capacitors.

Initialization

The RT8800A initiates after 2 pins are ready : VDD pin power on reset (POR) and DVD pin is higher than 1V. VDD POR is to make sure RT8800A is powered by a voltage high enough for normal work. The rising threshold voltage of VDD POR is 4.2V typically. At VDD POR, RT8800A checks PWM3 status to determine phase number of operation. Pull high PWM3 for two-phase operation. The unused current sense pins should be connected to GND or left floating.

DVD is to make sure that ATX12V is ready for the companion MOSFET drivers to work normally. Connect a voltage divider from ATX12V to DVD pin as shown in the Typical Application Circuit. Make sure that DVD pin voltage is below its threshold voltage before drivers are ready and above its threshold voltage for minimum ATX12V during normal operation. If one of VDD and DVD is not ready, RT8800A keeps its PWM outputs high impedance and the companion drivers turn off both upper and lower MOSFETs.

Soft-Start

After VDD and DVD are ready, RT8800A initiates its soft start cycle as shown in Figure 1. The error amplifier and PWM comparator are triple-input devices. The non-inverting input whichever is smaller dominates the behavior of the device. The soft start function generates SS and SSE for the non-inverting input of PWM comparator and error amplifier respectively where SSE = SS - V_{GS}. VGS is threshold voltage of internal MOSFET. The typical soft-start duration is 3ms. The soft start can be sliced to several time frames with specific operation respectively.

1) Mode 1 (SS < V_{RAMP_Valley})

Initially the COMP stays in the positive saturation due to offset of the error amplifier. Since SS < V_{RAMP_Valley}, the PWM comparator keeps its output low and V_{OUT} is zero.

2) Mode 2 (V_{RAMP_Valley} < SS < Cross-over)

Since V_{RAMP_Valley} < SS < Cross-over, SS dominates the non-inverting inputs of the PWM comparators. The PWM duty cycles increase according to the ramping up SS signal. The output voltage ramps up accordingly. However as V_{OUT} increases, the difference between V_{OUT} and SSE (SS - V_{GS}) is reduced and COMP leaves the saturation and declines. The takeover of SS lasts until it meets the COMP. During this interval, since the feedback path is broken, the converter is operated in the open loop.

3) Mode3 (Cross-over < SS < V_{GS} + V_{PI})

When the V_{COMP} takes over the non-inverting input for PWM Amplifier and when SSE (SS - V_{GS}) < V_{PI}, the output of the converter follows the ramp input, SSE (SS - V_{GS}). Before the crossover, the output follows SS signal. And when V_{COMP} takes over SS, the output is expected to follow SSE (SS - V_{GS}). Therefore the deviation of V_{GS} is represented as the falling of V_{OUT} for a short while. The COMP is observed to keep its decline when it passes the cross-over, which shortens the duty width and hence the falling of V_{OUT} happens. Since there is a feedback loop for the error amplifier, the output's response to the ramp input, SSE (SS - V_{GS}) is lower than that in Mode 2.

4) Mode 4 (SS > V_{GS} + V_{PI})

When SS > V_{GS} + V_{PI}, the output of the converter follows the desired V_{PI} signal and the soft start completes. However, the SS keeps ramping up to 3.3V and stays there. The PGOOD pin trips to high impedance as SS reaches 3.3V.

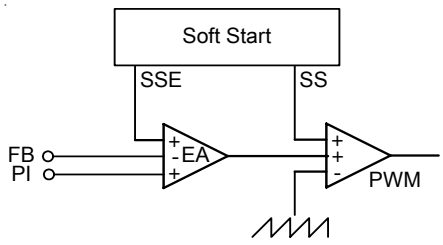


Figure 1. Soft Start Block Diagram.

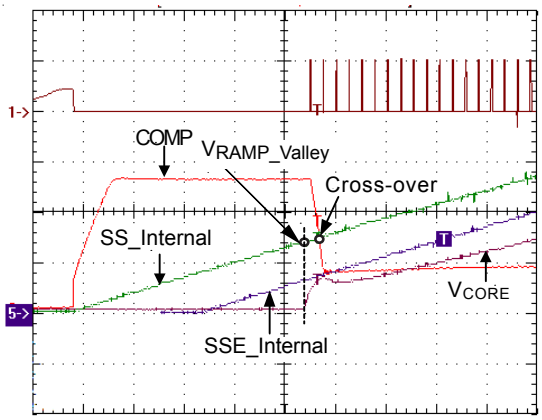


Figure 2

Time-Sharing DCR Current Sensing

RT8800A adopts an innovative time-sharing DCR current sensing technique to sense the phase currents for phase current balance (phase thermal balance), over current protection and load line regulation as shown in Figure 3. The current sensing amplifier GM samples and holds voltages V_X across the current sensing capacitor C_X by turns in a switching cycle. According to the Basic Circuit Theory, if

$$\frac{L_X}{R_{LX}} = R_X \times C_X \text{ then } V_X = I_{LX} \times R_{LX}$$

Consequently, the sensing current I_X is proportional to inductor current I_{LX} and is expressed as

$$I_X = \frac{I_{LX} \times R_{LX}}{R_{COMM}}$$

The sensed current I_X is used for current balance, over current protection, and droop tuning as described as followed. Since all phases share one common GM, GM offset and linearity variation effect are eliminated in practical applications. As sub-milli-ohmgrade inductors are widely used in modern motherboards, slight mismatch of GM amplifiers offset and linearity results in considerable current shift between phases. The time sharing DCR current sensing technical is extremely important to guarantee phase current balance at mass production.

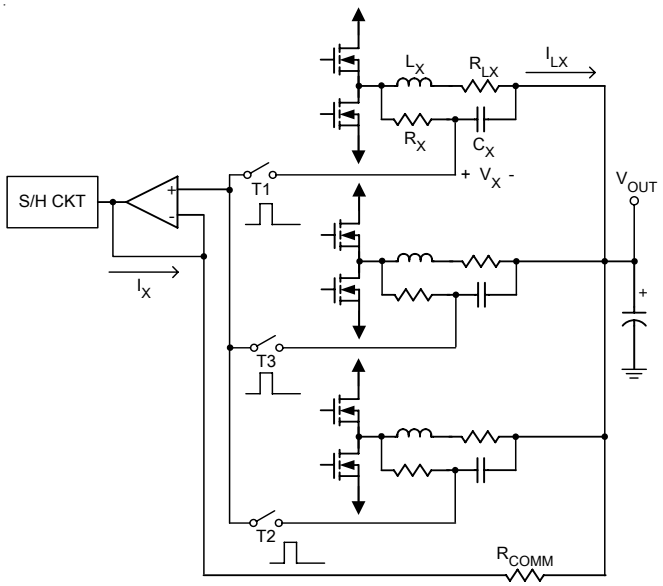


Figure 3

Figure 4 and 5 show the linearity of GM amplifier and its test circuit respectively. A voltage source is applied to ISPx while other ISPx pins are short to V_{OUT}. The voltage V_{ADJ} across resistor R_{ADJ} is measured. It is observed from Figure 5 shows that all ISPx share the same transconductance linearity and voltage offset.

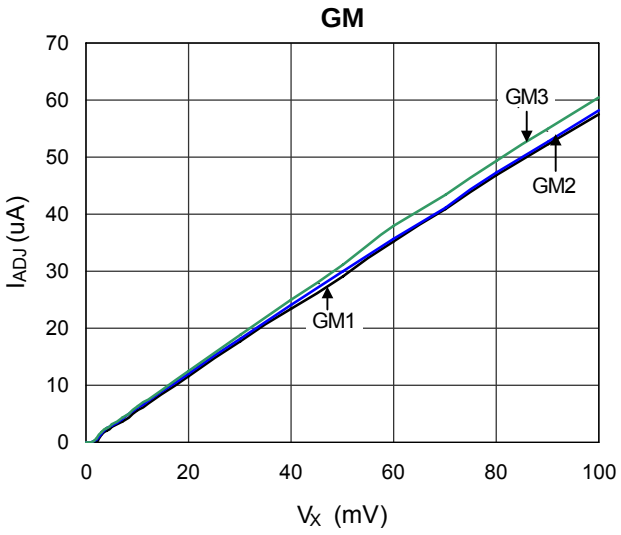


Figure 4. The Linearity of GMx

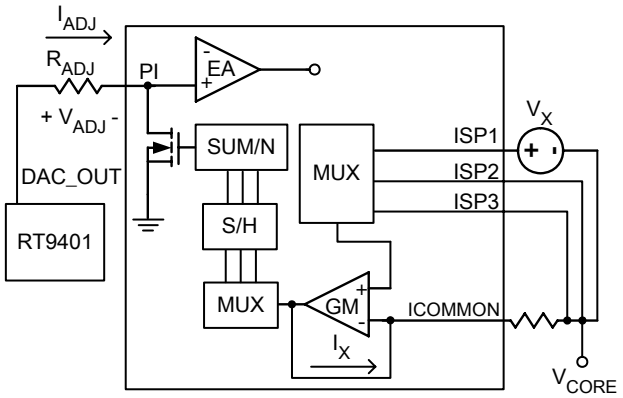


Figure 5. Test Circuit of GM.

Phase Current Balance

The sampled and held phase current I_X are injected to the corresponding saw tooth waveforms of PWM comparators. If phase current I_X is larger than other phase currents, its saw tooth waveform will be lift higher than the others. The RT8800A reduces the duty cycle of corresponding phase to decrease the phase current accordingly, vice versa.

Over Current Protection

RT8800A uses an external resistor R_{IMAX} connected to IMAX pin to generate a reference current I_{IMAX} for over current protection:

$$I_{IMAX} = \frac{V_{IMAX}}{R_{IMAX}}$$

where V_{IMAX} is 0.8V typical. OCP comparator compares each sensed phase current I_X with this reference current as shown in Figure 6. Equivalently, the maximum phase current is calculated as :

$$I_{LX(MAX)} = \frac{3}{2}\frac{V_{IMAX}}{R_{IMAX}}\frac{R_{COMM}}{R_{LX}}$$

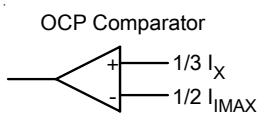


Figure 6. Over Current Comparator.

The RT8800A uses hiccup mode to eliminate nuisance detection of OCP or reduce output current when output is shorted to ground as shown in Figure 7 and 8. The RT8800A shuts down and latches off after 3 time OCP hiccups. It can only restart by resetting one of VDD or DVD pin.

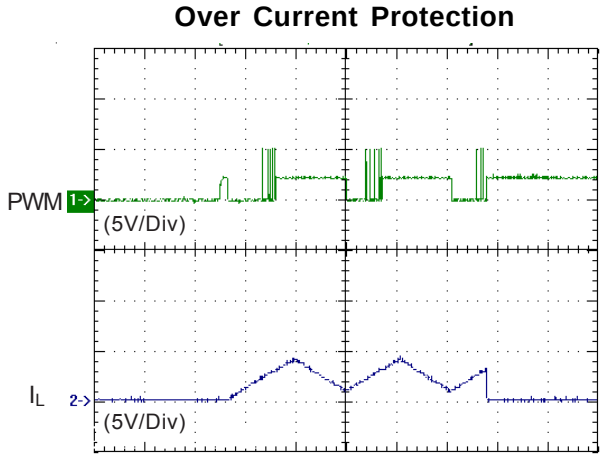


Figure 7. The Over Current Protection in the interval

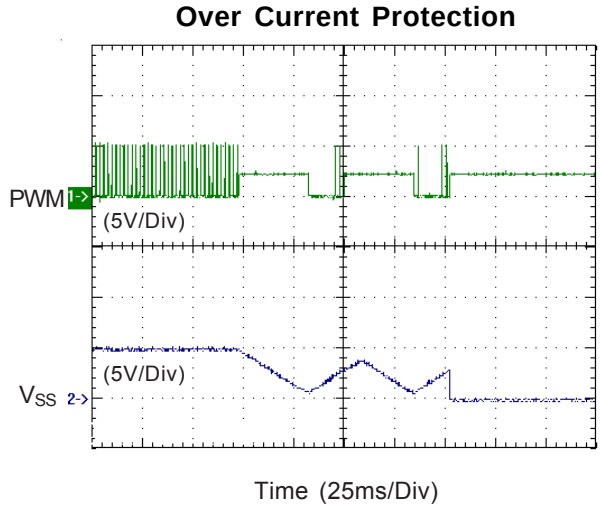


Figure 8. Over Current Protection at steady state

Voltage Reference for Converter Output & Load Droop

The output voltage is sensed at FB pin. The RT8800A receives an external reference voltage at PI pin as the non-inverting of the error amplifier and precisely regulates the FB voltage to this reference voltage. The RT8800A can provide Intel® VRD10.x or AMD® K8 compliant output voltage when companioned with DAC generator RT9401A/B as shown in Figure 9. The RT9401A/B receives VID[0:4] and produces DAC_OUT that complies with VRD10.x or K8 VID table. The DAC_OUT is fed to PI pin through a resistor R_{ADJ} as the reference voltage of the error amplifiers. The VID125 provides a 12.5mV offset for full compliance of VRD10.x table.

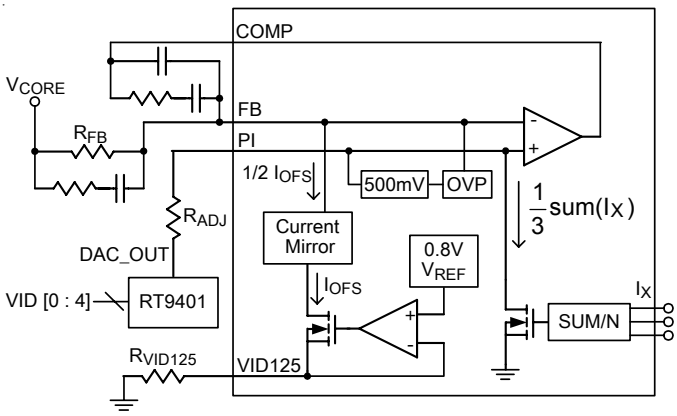


Figure 9

Droop and Load Lind Setting

The sampled and held phase current I_X are summed to get sum(I_X). RT8800A then sinks a current that is 1/3 sum(I_X) and produces a droop voltage that is proportional to the average phase voltage.

V_{ADJ} = 1/3 sum(I_X) x R_{ADJ}

V_{ADJ} is then subtracted form DAC generator output as the real reference voltage at non-inverting input of the error amplifier. Consequently, load line slope is calculated as:

$$\text{Load Line} = \frac{\Delta V_{CORE}}{\Delta I_{CORE}} = -\frac{R_{ADJ} \times R_{LX}}{3 \times R_{COMM}}$$

Output Voltage Offset Function

VID125 pin is internally regulated to be around 0.8V. An external resistor R_{VID125} between VID125 and GND generates the offset current $I_{OFS} = \frac{0.8V}{R_{VID125}}$.

FB pin will sink a current which is half of I_{OFS} because of a current mirror FB and VID125. The output offset voltage is calculated to be

$$V_{OFS} = \frac{0.8V}{R_{VID125}} \times \frac{1}{2} \times R_{FB}$$

Thus, the output voltage becomes

$$V_{CORE} = V_{FB} + V_{OFS} = V_{FB} + \frac{0.8V \times R_{FB}}{2 \times R_{VID125}}$$

Note : To maintain VID125 voltage around 0.8V, R_{VID125} must not be less than 16kΩ.

Dead Zone Elimination and Output Voltage Offset Function

RT8800A samples and holds inductor valley current by time-sharing sourcing a current I_X to R_{COMM}. At light load condition the inductor valley current and consequently the voltage V_X across the sensing capacitor may be negative.

A negative I_X is required to correctly sense the negative voltage. However, the RT8800A **CANNOT** provide a negative I_X and consequently cannot sense negative inductor current. This results in dead zone of load line performance as shown in Figure 10. Therefore a technique as shown in Figure 11 is required to eliminate the dead zone of load line at light load condition.

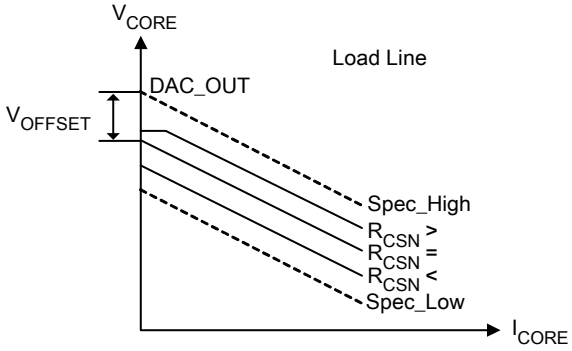


Figure 10

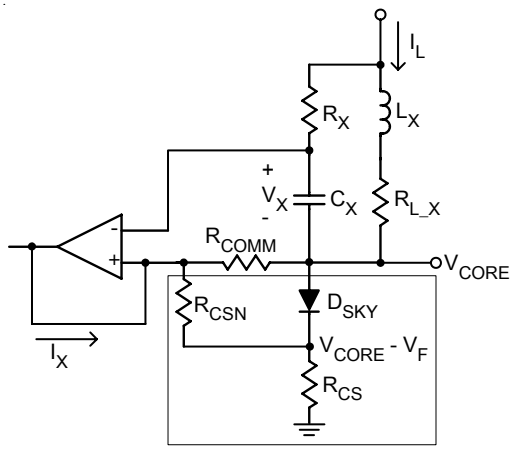


Figure 11

Referring to Figure 11, the Schottky diode provides a constant voltage drop V_F with enough bias current. I_X is expressed as:

$$I_X = \frac{V_F + I_{LX\_Valley} \times R_{LX}}{R_{CSN}} + \frac{I_{LX\_Valley} \times R_{LX}}{R_{COMM}} \quad (1)$$

To make sure RT8800A could sense the inductor current, right hand side of Equation (1) should always be positive:

$$\frac{V_F + I_{LX\_Valley} \times R_{LX}}{R_{CSN}} + \frac{I_{LX\_Valley} \times R_{LX}}{R_{COMM}} \geq 0 \quad (2)$$

Since V_F >> (I_{LX_Valley} x R_{LX}) in practical application, Equation (2) could be simplified as:

$$\frac{V_F}{R_{CSN}} \geq \left| \frac{I_{LX\_Valley} \times R_{LX}}{R_{COMM}} \right| \quad (3)$$

Rewriting Equation (3), we get

$$\left|\frac{V_F \times R_{COMM}}{I_{LX\_Valley} \times R_{LX}}\right| \geq R_{CSN} \quad (4)$$

The technique mentioned above also provides output voltage offset function specified by Intel® VRD10.x. The offset voltage level is calculated as:

$$V_{OFFSET} = \frac{R_{ADJ}}{R_{CSN}} V_F$$

Enough bias current is required for a Schottky to act like a voltage source. Users should choose the appropriate R_{CS} based on the IV characteristic of the diode (Figure 12)

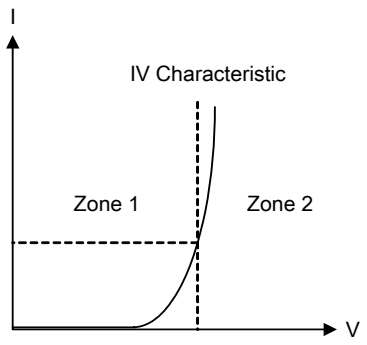


Figure 12

According to Figure 12, the forward voltage of diode will be different results from the different conduction current. So when the characteristic of diode in the circuit you design is in zone 1, this will result in Spec. mis-met. It is because when the V_{CORE} is changed during DVID, the node V_{CORE} - V_F is also changed to produce the differential conduction current of diode ΔI and the ΔI will result in producing the differential forward voltage of diode ΔV_F Referring to Equation (1). The ΔV_F would get ΔI_X. Then the V_{CORE} must be subtracted the extra voltage $V_{(EXT)}$(ΔI_X x R_{ADJ}) during DVID. So you will get the ΔV_{CORE} = $V_{(MAX)}$ - $V_{(MIN)}$ - $V_{(EXT)}$ during DVID tests. In order to reduce the effect results from diode. The better choice is to decrease the Rcs to increase the conduction current of diode I to get better V characteristic of diode in Zone 2.

Over Voltage Protection (OVP)

The RT8800A continuously monitors voltage at FB pin. OVP is triggered if FB voltage is 500mV higher than the voltage at PI pin. RT8800A latches off and turns on lower MOSFET to protect the load from damage upon on OVP trip. It can only be reset by DVD and VDD pins.

Current Ratio Setting

Current ratio adjustment is possible as described below. It is important for achieving thermal balance in practical application where thermal conditions between phases are not identical. Figure 13 shows the application circuit of GM for current ratio requirement. According to Basic Circuit Theory, if

$$\frac{L_X}{R_{LX}} = (R_{SX} // R_{PX}) \times C_X \text{ then}$$

$$V_X = \frac{R_{PX}}{R_{SX} + R_{PX}} \times I_{LX} \times R_{LX}$$

With other phase kept unchanged, this phase would share (R_{PX}+R_{SX})/R_{PX} times current than other phases. Figure 14 and 15 show different current ratio setting for the power stage when Phase 3 is programmed 2 times current than other phases. Figure 16 and 17 compare the above current ratio setting results.

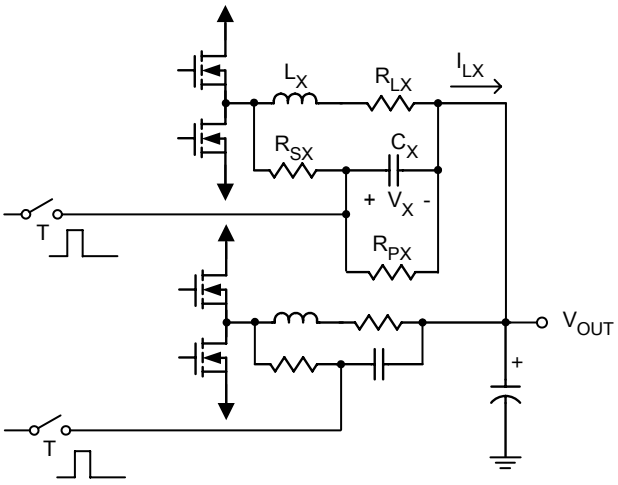


Figure 13

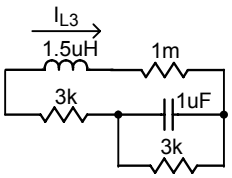


Figure 13. GM4 Setting for current ratio function.

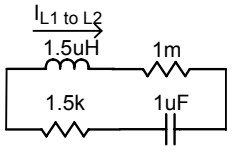


Figure 14. GM1 to GM3 Setting for current ratio function.

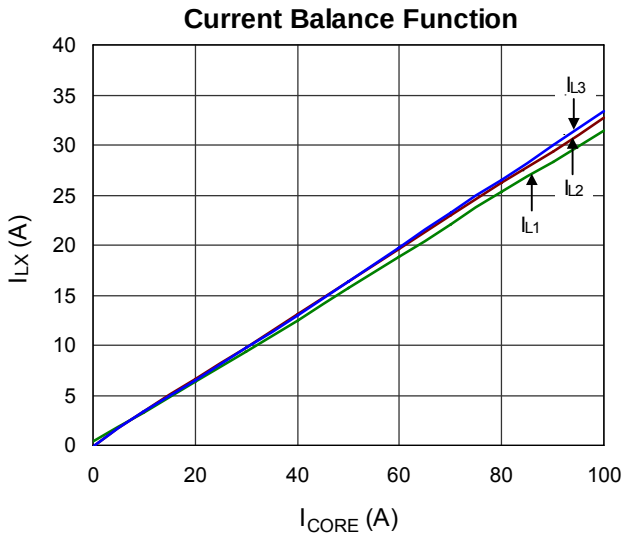


Figure 15

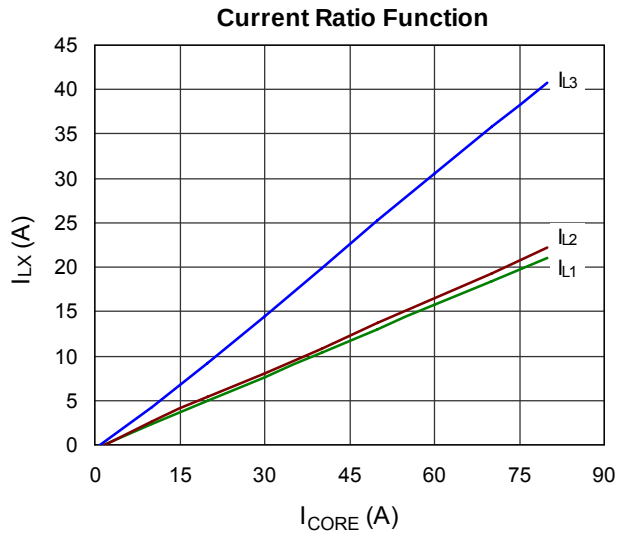


Figure 16

Design Procedure Suggestion

a. Output filter pole and zero (Inductor, output capacitor value & ESR).

b. Error amplifier compensation & sawtooth wave amplitude (compensation network).

Current Loop Setting

a. GM amplifier S/H current (current sense component DCR, ICOMMON pin external resistor value).

b. Over-current protection trip point ($R_{ICOMMON1}$ resistor).

VRM Load Line Setting

a. Droop amplitude (PI pin resistor).

b. No load offset ($R_{ICOMMON2}$)

Power Sequence & SS

DVD pin external resistor and SS pin capacitor.

PCB Layout

a. Sense for current sense GM amplifier input.

b. Refer to layout guide for other items.

Voltage Loop Setting

Design Example

Given:

Apply for four phase converter

V_{IN} = 12V

V_{CORE} = 1.5V

$I_{LOAD(MAX)}$ = 100A

V_{DROOP} = 100mV at full load (1mΩ Load Line)

OCP trip point set at 35A for each channel (S/H)

DCR = 1mΩ of inductor at 25°C

L = 1.5µH

C_{OUT} = 8000µF with 5mΩ equivalent ESR.

1. Compensation Setting

a. Modulator Gain, Pole and Zero:

From the following formula:

Modulator Gain =V_{IN}/V_{RAMP} =12/2.4=5 (i.e 14dB)

where V_{RAMP} : ramp amplitude of saw-tooth wave

LC Filter Pole = 1.45kHz and

ESR Zero =3.98kHz

b. EA Compensation Network:

Select R1 = 4.7k, R2 = 15k, C1 = 12nF, C2 = 68pF and use the Type 2 compensation scheme shown in Figure 21. By calculation, the F_Z = 0.88kHz, F_P = 322kHz and Middle Band Gain is 3.19 (i.e 10.07dB).

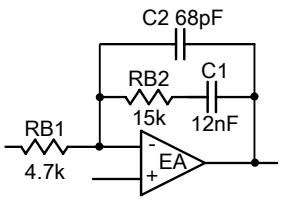


Figure 17. Type 2 compensation network of EA

2. Over-Current Protection Setting

Consider the temperature coefficient of copper 3900ppm/°C,

$$\frac{I_L \times DCR}{R_{ICOMMON1}} = 150\mu A$$

$$\frac{I_L \times 1.39m\Omega}{330\Omega} = 150\mu A$$

$$I_L = 35.6A$$

Layout Considerations

Place the high-power switching components first, and separate them from sensitive nodes.

1. Most critical path:

   The current sense circuit is the most sensitive part of the converter. The current sense resistors tied to ISP1,2,3 and ICOMMON should be located not more than 0.5 inch from the IC and away from the noise switching nodes. The PCB trace of sense nodes should be parallel and as short as possible. R&C filter of choke should place close to PWM and the R & C connect directly to the pin of each output choke, use 10 mil differencial pair, and 20 mil gap to other phase pair. Less via as possible.

2. Switching ripple current path:

   a. Input capacitor to high side MOSFET.

   b. Low side MOSFET to output capacitor.

   c. The return path of input and output capacitor.

   d. Separate the power and signal GND.

   e. The switching nodes (the connection node of high/ low side MOSFET and inductor) is the most noisy points. Keep them away from sensitive small-signal node.

   f . Reduce parasitic R, L by minimum length, enough copper thickness and avoiding of via.

3. MOSFET driver should be closed to MOSFET.

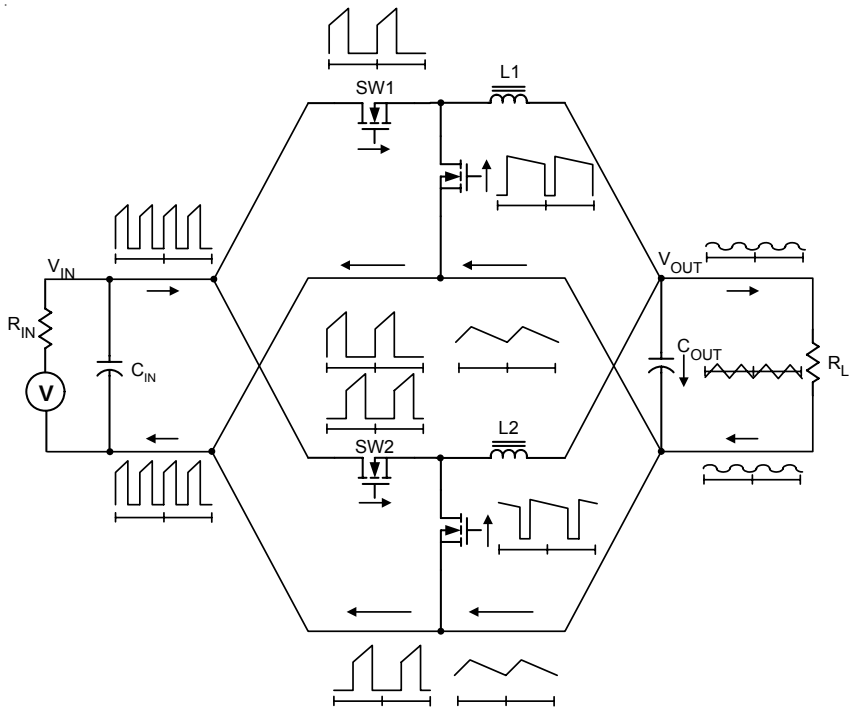


Figure 18. Power Stage Ripple Current Path

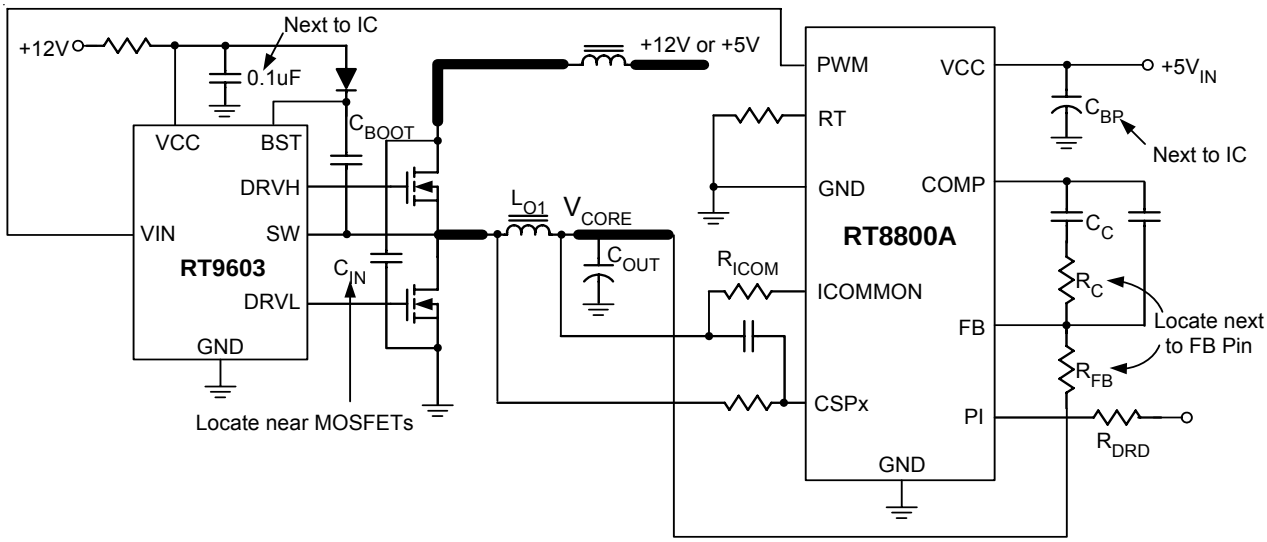


Figure 19. Layout Consideration

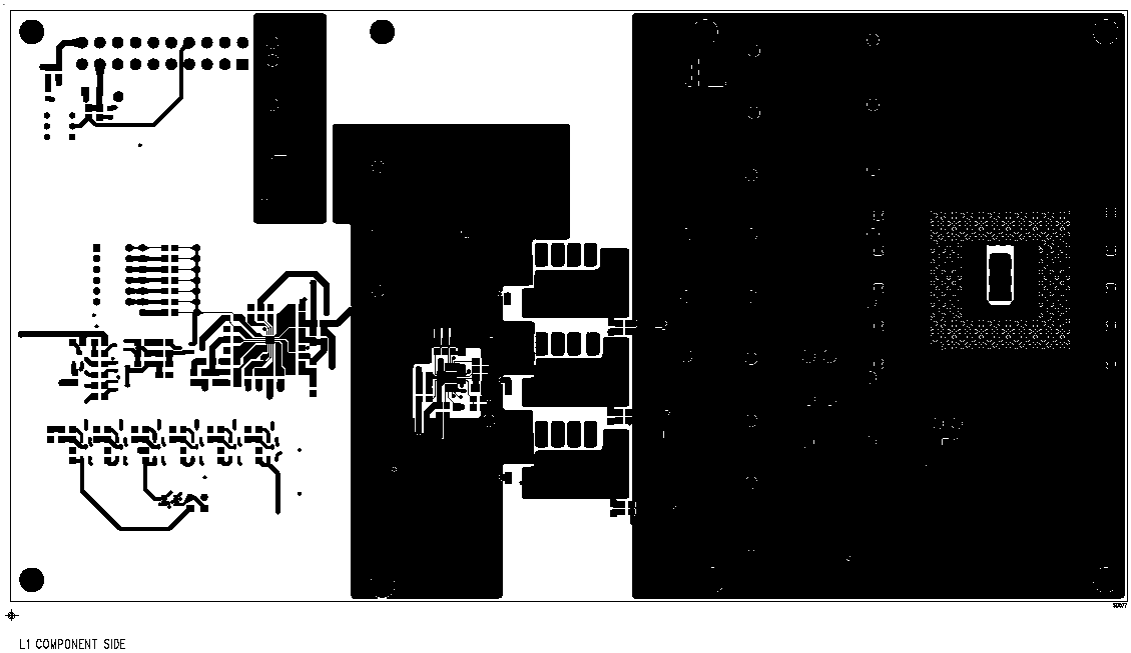


Figure 20

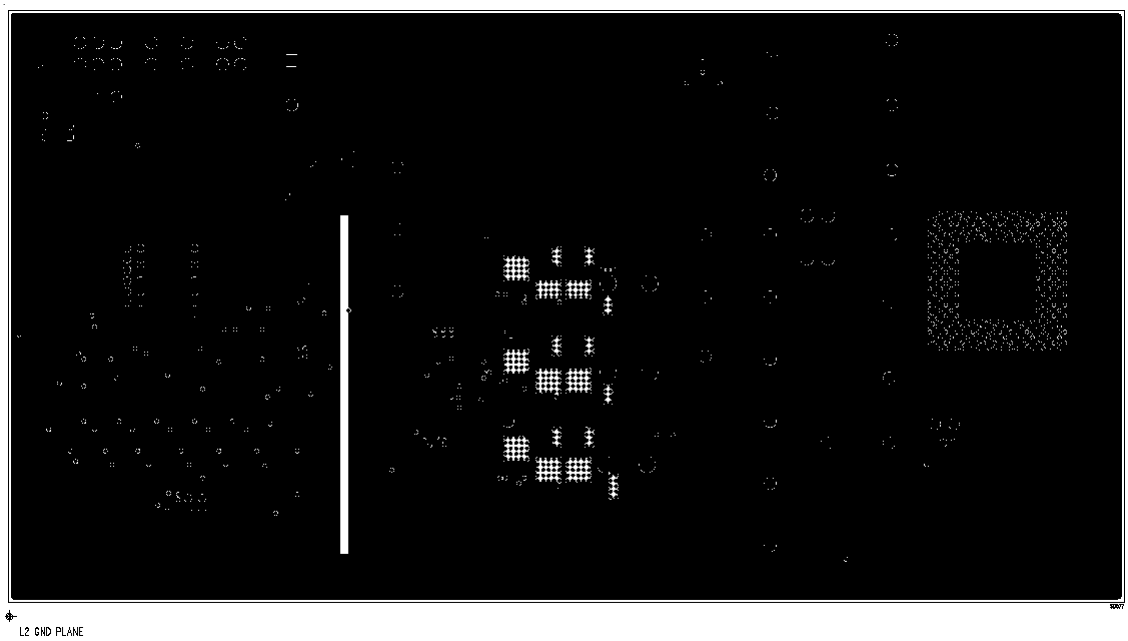


Figure 21

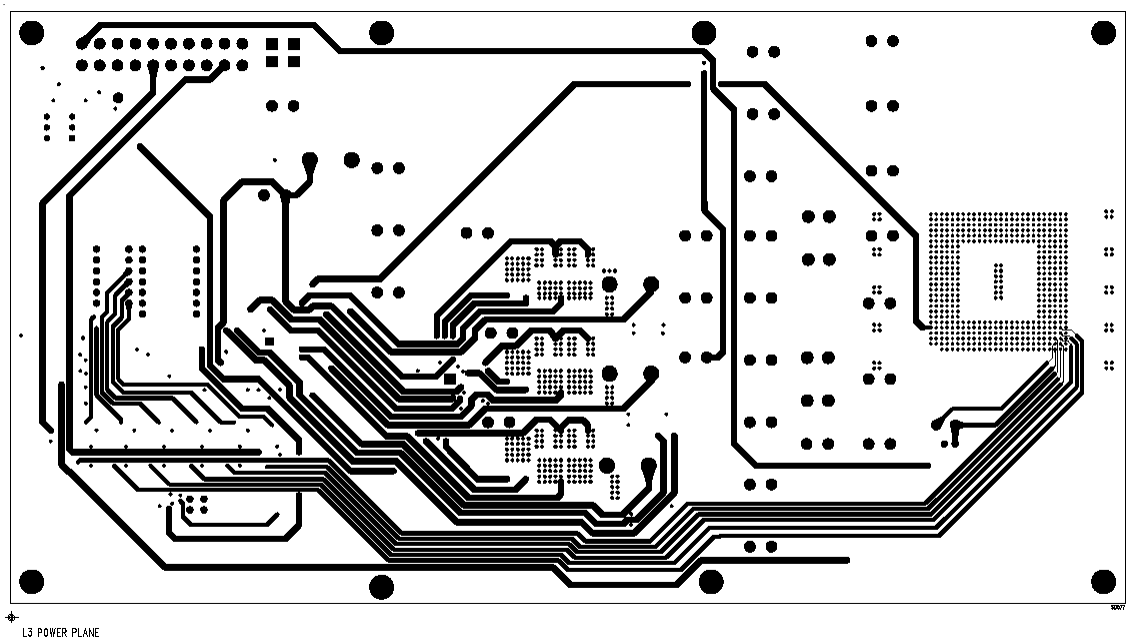


Figure 22

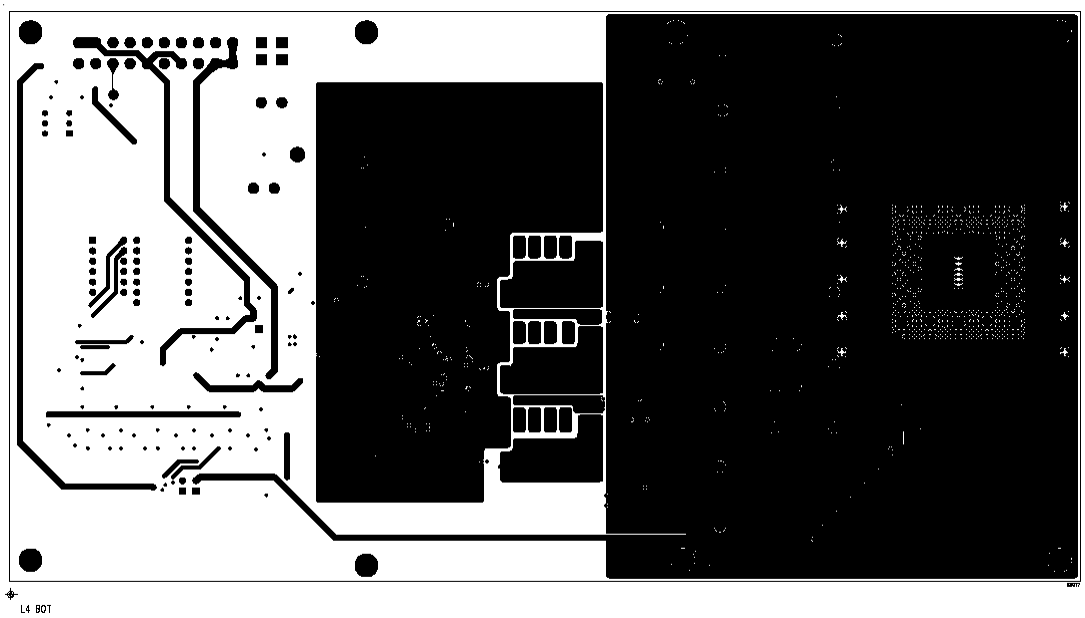
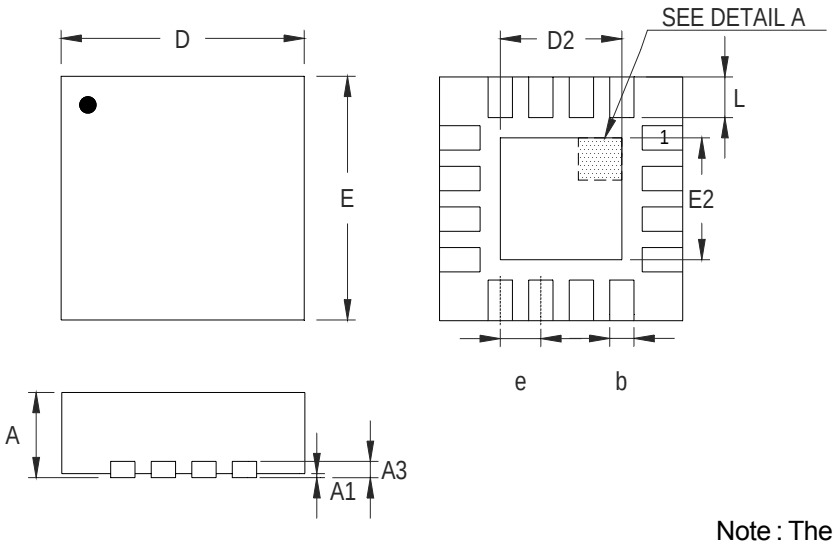
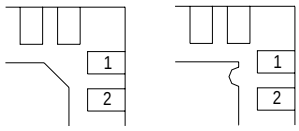


Figure 23

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 16L QFN 3x3 Package

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