Two Phase General Purpose PWM Controller

General Description

The RT8805E is the most compact dual-phase synchronous buck controller in the industry specifically designed for high power density applications. This part is capable of delivering up to 60A output current due to its embedded bootstrapped drivers that support 12V + 12V driving capability.

The phase currents are sensed by innovative time sharing $R_{DS(ON)}$ current sensing technique for current balance and over current protection. Using one common GM amplifier to sense two phase currents eliminates offset and nonlinearity of the GM amplifier and yields good current balance. Other features include adjustable operation frequency from 50kHz to 1MHz, adjustable soft-start, PGOOD, external compensation, enable/shutdown for various application and performance consideration.

The RT8805E comes to a tiny footprint package of WQFN-24L 4x4 package.

Ordering Information

RT8805E □ □

Package Type
QWA : WQFN-24L 4x4 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Features

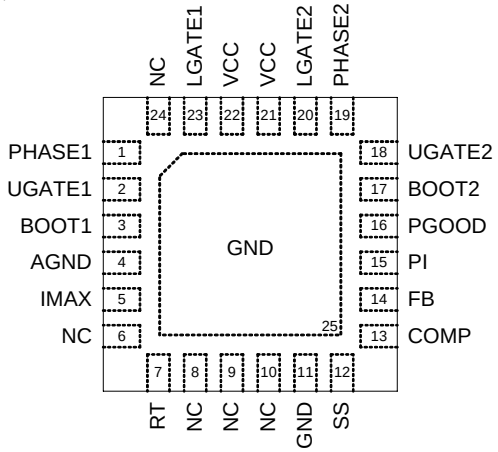
- **12V Power Supply Voltage**
- **2 Phase Power Conversion**
- **Embedded 12V Boot Strapped MOSFET Driver**
- **Precise Core Voltage Regulation**
- **Low Side MOSFET $R_{DS(ON)}$ Current Sensing for Power Stage Current Balance**
- **External Compensation**
- **Adjustable Soft-Start**
- **Adjustable Frequency and Typical at 300kHz Per Phase**
- **Power Good Indication**
- **Adjustable Over Current Protection**
- **External Reference Voltage Tracking**
- **Small 24-Lead WQFN Packages**
- **RoHS Compliant and Halogen Free**

Applications

- Middle-High End GPU Core Power
- High End Desktop PC Memory Core Power
- Low Output Voltage, High Power Density DC-DC Converters
- Voltage Regulator Modules

Pin Configurations

(TOP VIEW)



WQFN-24L 4x4

Note :
NC pins (6, 8, 9, 10, 24) have no internal bonding wire connection. The landing pad of these pins can be tied to GND plane for better thermal relief.

Typical Application Circuit

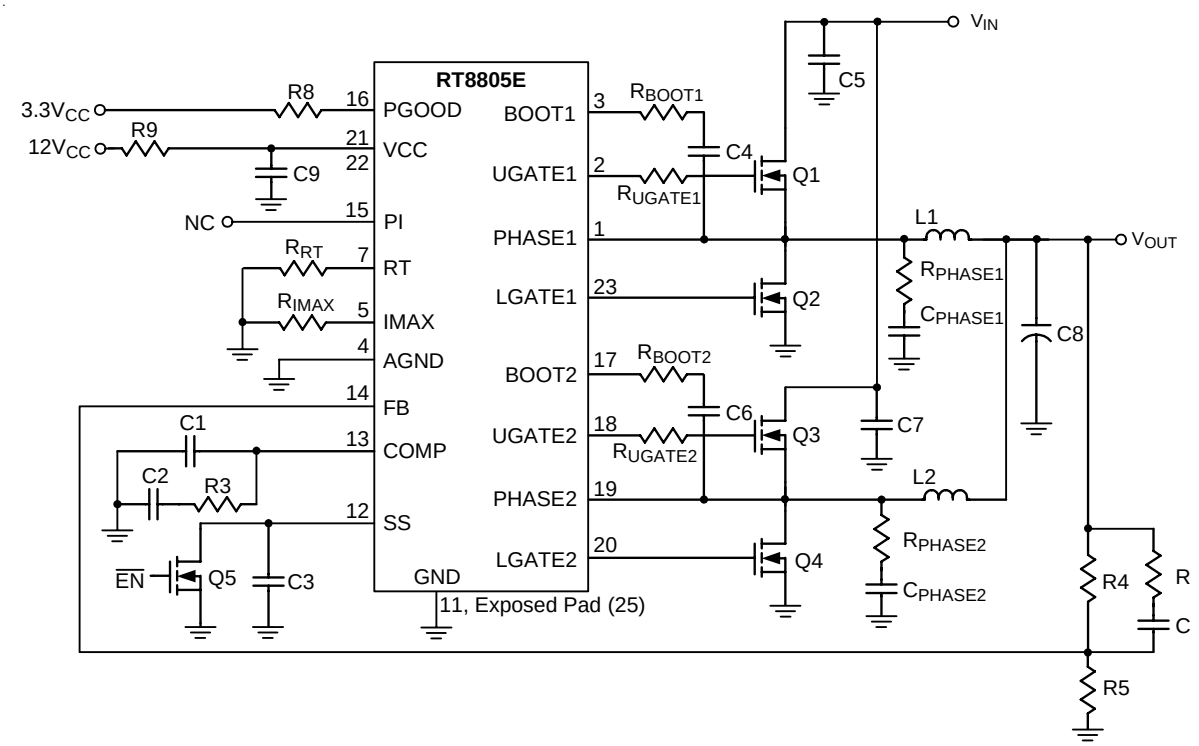


Figure A. Application Circuit for Standalone Mode (PI Disabled)

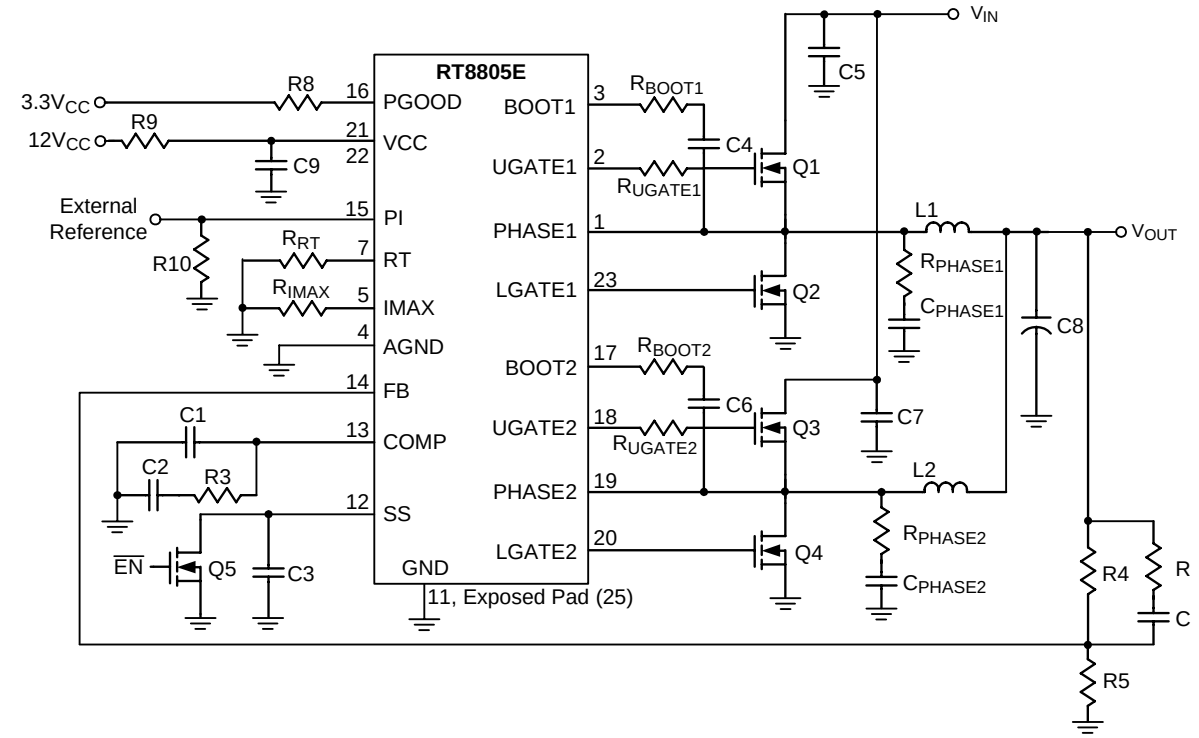
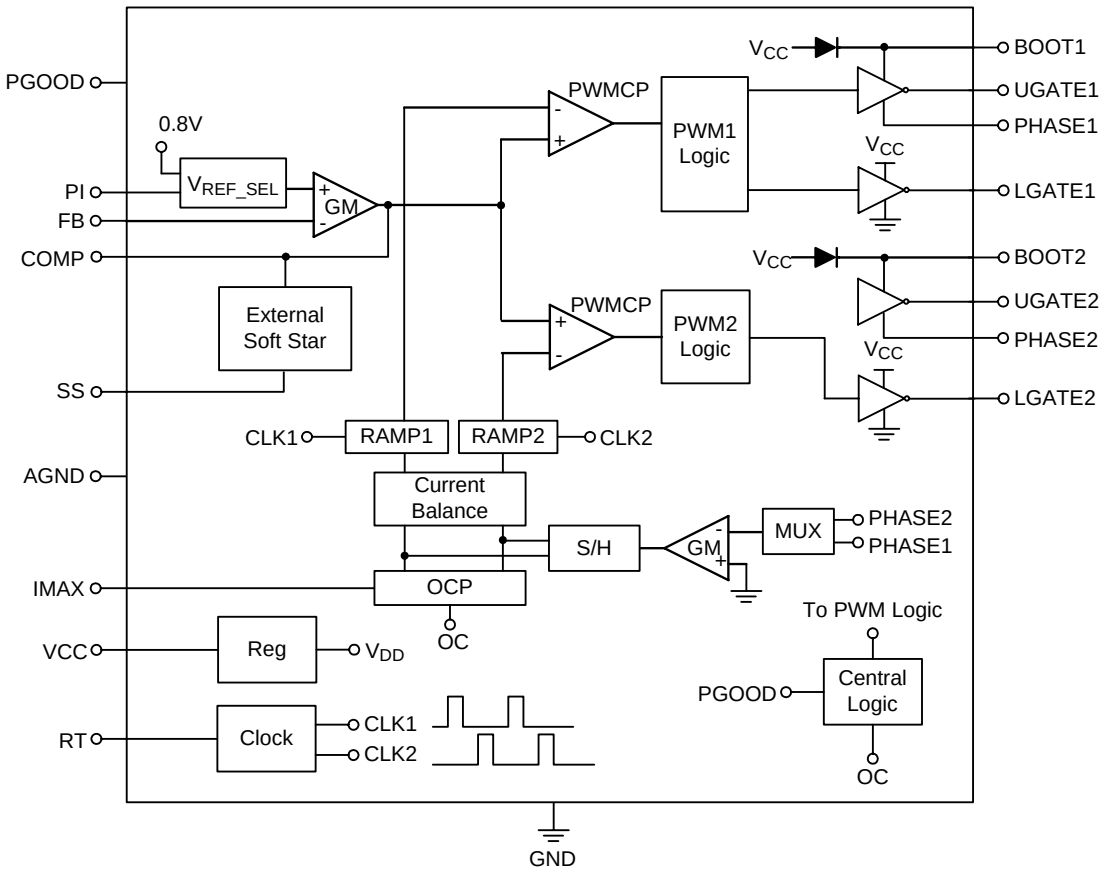


Figure B. Application Circuit for Tracking Mode (PI Enabled)

Function Block Diagram



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PHASE1	These pins are return nodes of the high-side MOSFET driver. Connect these pins to high-side MOSFET sources together with the low-side MOSFET drains and the inductors.
19	PHASE2	
2	UGATE1	Upper Gate Drive. These pins drive the gates of the high side MOSFETs.
18	UGATE2	
3	BOOT1	Bootstrap Power Pin. These pins power the high-side MOSFET drivers. Connect these pins to the junctions of the bootstrap capacitors.
17	BOOT2	
4	AGND	Chip Analog Ground.
5	IMAX	Maximum Current Setting. This pin sets the current limiting level. Connect this pin with resistor to ground to set the current limit threshold.
6, 8, 9, 10, 24	NC	No Internal Connection. Can be tied to GND for better thermal relief.
7	RT	Timing Resistor. Connect a resistor from RT to AGND to set the operation frequency.
11, 25 (Exposed Pad)	GND	The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
12	SS	Soft-Start Pin. This pin provides soft-start function for controller. Connect a capacitor from SS to AGND to set the soft-start time. The COMP voltage of the converter follows the ramping voltage on the SS pin at soft-start.
13	COMP	Compensation Pin. This pin is output node of the error amplifier.
14	FB	Feedback Pin. This pin is inverting input pin of the error amplifier.
16	PGOOD	Power Good. PGOOD is an open drain output used to indicate the status of the voltages on SS pin and FB pin. PGOOD will go to high impedance state when SS > 3.8V and FB > 0.6V.
23	LGATE1	Lower Gate Drive. These pins drive the gate of the low side MOSFETs.
20	LGATE2	
21, 22	VCC	Controller Power Supply Pin. This pin also powers the low-side MOSFET drivers. An regulates VCC to 5V (V_{DD}) for internal control logic circuitry.
15	PI	External Reference Voltage Input Pin. This pin sets the voltage of FB pin when close loop.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- –0.3V to 16V
- PHASE to GND
  - DC ---------- –5V to 15V
  - < 200ns ---------- –10V to 30V
- BOOT to PHASE ---------- 15V
- BOOT to GND
  - DC ---------- –0.3V to V_{CC}+15V
  - < 200ns ---------- –0.3V to 42V
- Input, Output or I/O Voltage ---------- GND-0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN–24L 4x4 ---------- 1.923W
- Package Thermal Resistance (Note 2)
  - WQFN–24L 4x4, θ_{JA} ---------- 52°C/W
  - WQFN–24L 4x4, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage ---------- 12V ±10%
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Power Supply Voltage	V_{CC}		10.8	12	13.2	V
Power On Reset	V_{POR}		5.2	5.7	6.2	V
Power On Reset Hysteresis			--	0.3	--	V
Power Supply Current	I_{VCC}	V_{SS} = 0V	--	10	--	mA
Soft Start						
Soft Start Current	I_{SS}		7	10	14	uA
Oscillator						
Frequency	f_{OSC}	R_{RT} = 33kΩ	255	300	345	kHz
		R_{RT} = 16.5kΩ	500	600	700	
Maximum Duty Cycle			70	75	80	%
Ramp Amplitude			--	1.6	--	V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Voltage						
Feedback Voltage	V_{FB}	Internal Reference	0.792	0.8	0.808	V
PI Input Range		External Reference	0.4	--	3	V
PI Input Offset		V_{PI} = 0.4V to 3V, Measure I $V_{PI} - V_{FB}$ I	–12	0	12	mV
Error Amplifier						
DC Gain			60	70	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF	6	10	--	MHz
Trans-conductance	GM	R_{LOAD} = 20kΩ	580	660	--	uA/V
MAX Current (Source & Sink)	I_{COMP}	V_{COMP} = 2.5V	270	350	--	uA
Current Sense GM Amplifier						
OC	V_{PHASE}	R_{IMAX} = 33kΩ	–130	–110	–90	mV
Gate Driver						
Maximum Upper Drive Source	$I_{UGATE(MAX)}$	BOOT – PHASE = 12V	--	1.2	--	A
Upper Drive Sink	R_{UGATE}	V_{UGATE} = 1V	--	2	4	Ω
Maximum Lower Drive Source	$I_{LGATE(MAX)}$	PV_{CC} = 12V	--	1.2	--	A
Lower Drive Sink	R_{LGATE}	V_{LGATE} = 1V	--	1.5	3	Ω
Protection						
Under Voltage Protection			0.55	0.6	0.65	V
Power Good						
Power Good Threshold		Measure SS Voltage	3.4	3.8	4.2	V
Power Good Output Low Voltage		I_{PGOOD} = 4mA	--	0.05	0.2	V

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

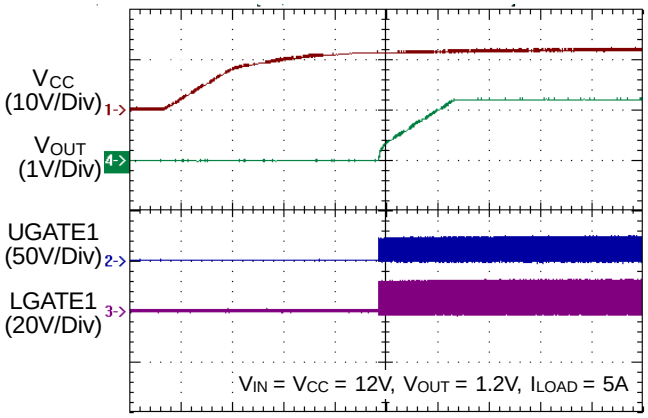
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

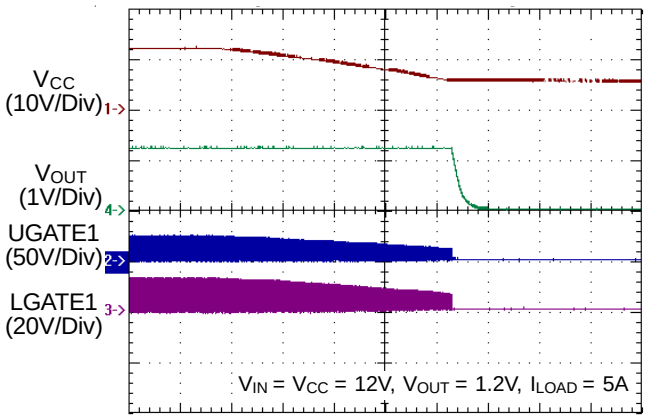
Typical Operating Characteristics

Power Up



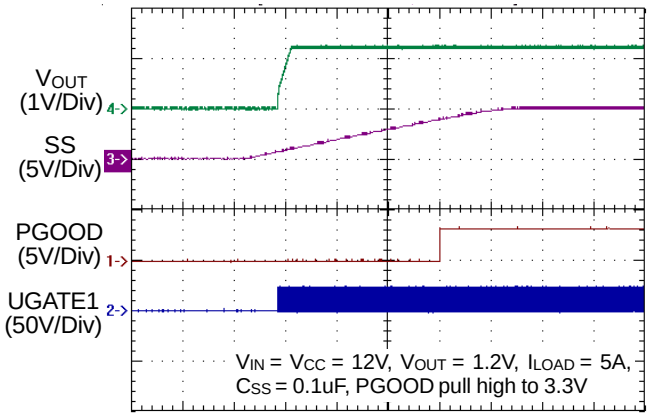
Time (2ms/Div)

Power Off



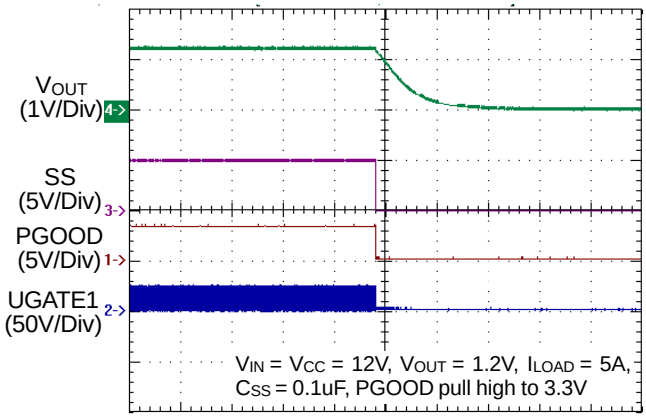
Time (4ms/Div)

Enable from SS



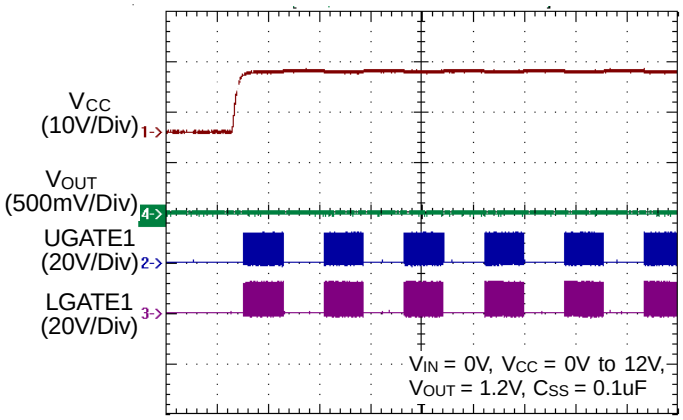
Time (10ms/Div)

Disable from SS



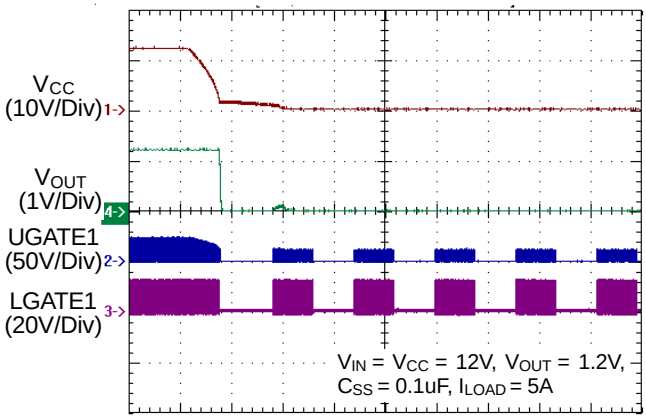
Time (1ms/Div)

Power On UVP



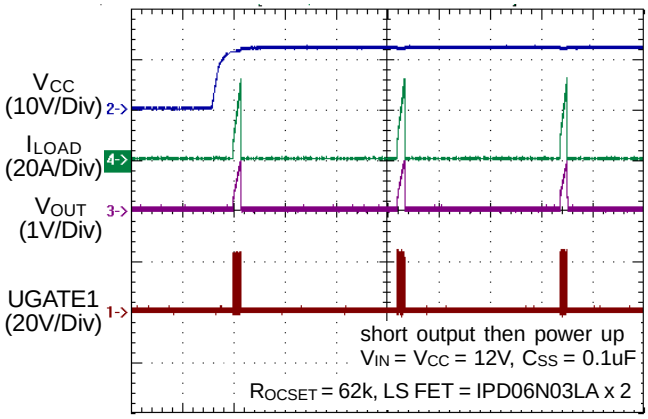
Time (40ms/Div)

Power Off UVP

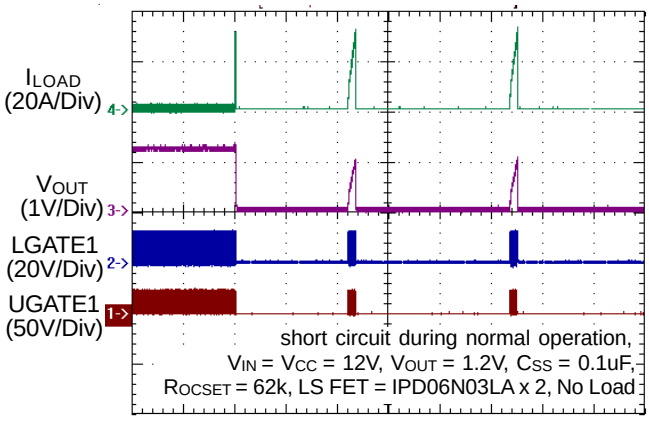


Time (40ms/Div)

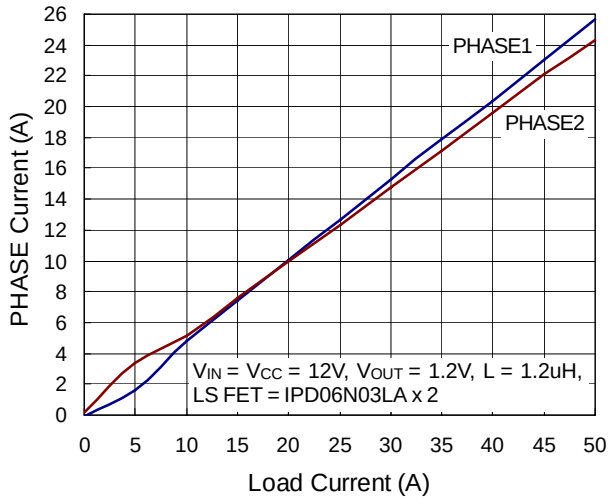
Short Circuit OCP



Short Circuit OCP



Current Balance



Application Information

The RT8805E is a voltage-mode two-phase buck controller for high current applications. The MOSFET gate drivers and bootstrap diodes are all integrated into the chip to minimize external component count and save board area. Inductor current is sensed by the $R_{DS(ON)}$ of low-side MOSFET. An innovative time-sharing technique is utilized to implement inductor current sensing and current signal processing for current balance and over current protection. In addition, the RT8805E provides power good function and enable/disable function that gives the flexibility in power sequence control. The external reference voltage input function (PI pin) provides dynamically adjustable output voltage for over-clocking applications.

VCC Power On Reset (POR)

The typical VCC supply voltage of the RT8805E is 12V. The embedded MOSFET gate drivers are directly supplied from VCC. Therefore, it is recommended to place a 1uF ceramic capacitor close to VCC pin for decoupling. An internal regulator regulates the VCC input voltage to 5V for internal control circuit. The power on reset (POR) circuit monitors the VCC supply voltage to ensure normal operation. When VCC exceeds the POR threshold V_{POR}, controller releases the reset state and begins to work. If VCC falls below V_{POR}, controller will be reset. V_{POR} has a 0.3V hysteresis to ensure that the controller will not be inadvertently turned off unless VCC falls substantially.

Soft Start and Power Good

The soft-start function is used to prevent the large inrush current while converter is powered up. Figure 1 illustrates the soft start and power good timing diagram. When VCC exceeds V_{POR}, controller begins its soft start operation. A 10uA internal current source begins to charge the external soft start capacitor C_{SS} such that V_{SS} ramps up from zero in a monotone during the soft start period. The error amplifier output voltage V_{COMP} is clamped by V_{SS} during this period. Since V_{COMP} ramps up gradually, therefore the duty cycle of UGATE signal will also increase gradually and so does the input current. The soft start operation is completed when V_{SS} exceeds 3.8V. Further rise of V_{SS} has no influence on controller operation. In addition, the soft start time period also acts as the timer for OCP and UVP, which are hiccupped protections and will be described in later sections.

The PGOOD pin is an open-drain output pin for output voltage state indication. Connect a resistor to this pin and pull high to a voltage source. If no fault occurs at the end of soft start, the PGOOD pin will be internally turned to high impedance state to indicate the power good state. If the power good function is not required, left the PGOOD pin open.

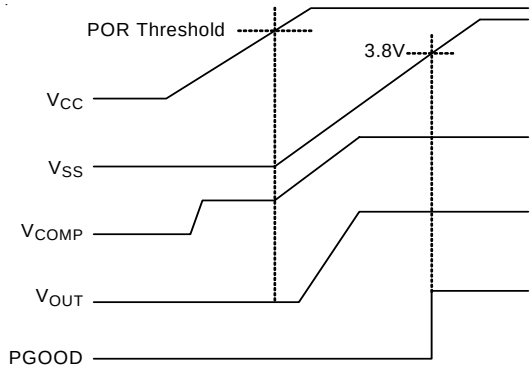


Figure 1. Soft start and power good timing diagram

Enable/Disable

The SS pin can also be used to enable/disable the controller. This function provides the flexibility in power sequence control. It is recommended to connect a small-signal MOSFET to the SS pin to implement the enable/disable function. If the soft start voltage V_{SS} is force to ground by the external MOSFET, the controller will be disabled. When the controller is disabled, both UGATE and LGATE will stop switching because the error amplifier output voltage V_{COMP} is clamped by the soft start voltage V_{SS}. Once SS pin is released, controller will initiate the soft start operation.

Switching Frequency

The switching frequency is determined by the resistor R_{RT} which is connected from RT pin to GND. Figure 2 illustrates the typical relationship between switching frequency and R_{RT}.

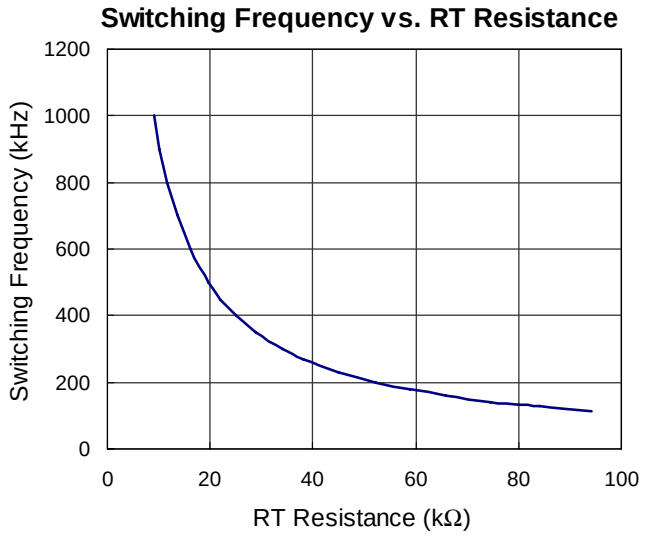


Figure 2. Switching Frequency vs. R_{RT}

Inductor Current Sensing

The RT8805E utilizes $R_{DS(ON)}$ current sense technique to sense the inductor valley current for phase current balance and over current protection. Figure 3 illustrates the inductor valley current sensing. When the low-side MOSFET is turned on, inductor current freewheels and ramps down. The controller samples and holds the valley voltage across the low-side MOSFET.

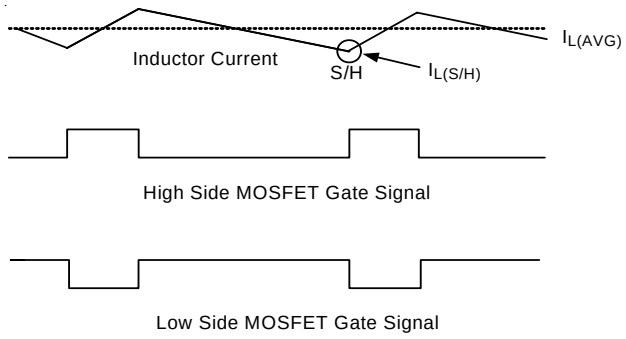


Figure 3. Inductor valley current sensing

The RT8805E uses innovative time-sharing current sense technique. Figure 4 shows the inductor current sense block diagram. The current sense GM amplifier converts the sensed voltage signal into current signal for the internal sample and hold circuit. The multiplexer determines which phase current should be sampled and held. Use one single GM amplifier and one multiplexer can sense the inductor current for each phase. The major advantage of using one single current sense GM amplifier is to avoid the offset caused by the difference between two GM amplifier.

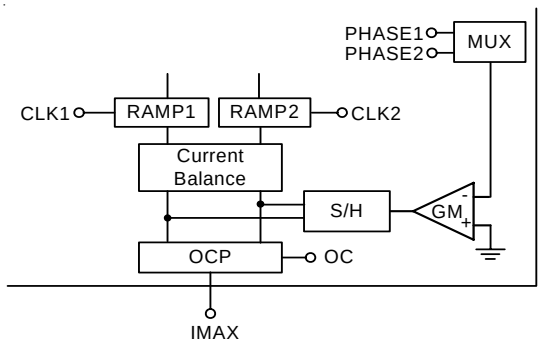


Figure 4. Inductor current sense block diagram

Current Balance

The RT8805E senses the inductor valley current for channel current balance and over current protection. Figure 5 shows the detailed function block diagram of current balance circuit. The sensed two phase current signals are summed and then averaged. Each phase current signal minuses the averaged signal and then injects into the ramp signal. Therefore, phase 1 current is proportional to (I_{L1} - I_{L2}); phase 2 is proportional to (I_{L2} - I_{L1}).

In steady state and current balance situation, there is no current signal injected into the ramp. If $I_{L1} > I_{L2}$, the bottom of RAMP1 will be lifted up that causes the duty cycle of UGATE1 decrease. On the other hand, the bottom RAMP2 will be pulled down to make the duty cycle of UGATE2 increase. As the results, I_{L1} will decrease and I_{L2} will increase. Finally, the phase current will be back to the balance state through the above procedure, which is negative feedback.

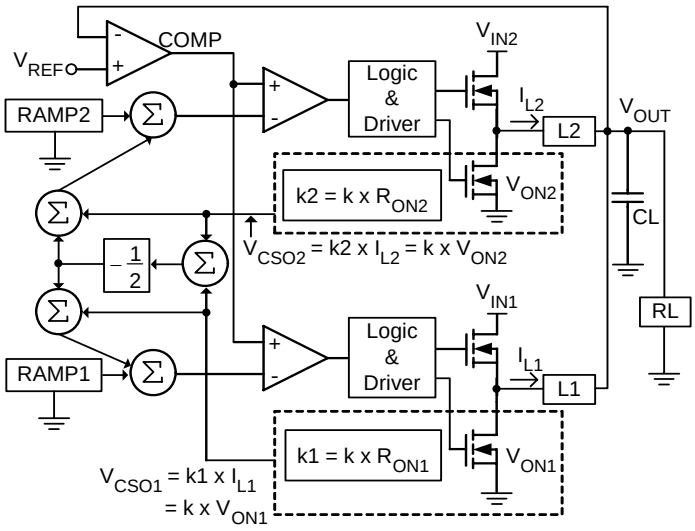


Figure 5. Current Balance

Over Current Protection (OCP)

RT8805E monitors the inductor current in each phase "cycle by cycle" for over current protection. Over current condition occurs in either phase can trip OCP. Once VCC exceeds POR, the controller starts to monitor each phase currents for over current protection.

When OCP is tripped, both UGATE and LGATE are off. At the same time, C_{SS} will be discharged by the internal circuit. Therefore V_{SS} will fall sharply. When the soft start voltage V_{SS} is down to about 0.4V, the 10uA current source starts to charge C_{SS} again. Controller will try to restart and initiate the soft start operation in a hiccupped way to eliminate fault detection of OCP. If the over current situation still exists, controller will be latched off after three times of hiccupped restart operation. Only VCC POR is cycled can reset OCP.

An external resistor R_{IMAX} connected from IMAX pin to GND programs the OCP trip point. Figure 6 shows the OCP comparator. The current which flows out of IMAX pin determines the OCP reference current I_{IMAX}. The OCP comparator compares the sensed inductor current I_{X1} and I_{X2} with the reference current I_{IMAX}, either one can trip OCP.

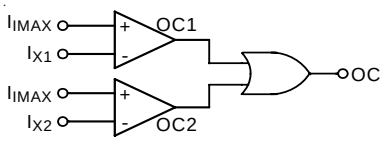


Figure 6. OCP comparator

Refer to the following example to determine the value of R_{IMAX}.

For example :

From *Electrical Specifications* : R_{IMAX} = 33kΩ

V_{PHASE} = –110mV

Assume low-side MOSFET $R_{DS(ON)}$ = 3mΩ

Get the OCP setting current is $\frac{110mV}{3m\Omega}$ = 37A per PHASE (the valley of inductor's current).

Change the setting current which you want from 37A per PHASE to 25A per PHASE.

Following below steps :

1. Calculate phase voltage. If Low side MOSFET

   $R_{DS(ON)}$ = 3mΩ, V_{PHASE_new} = –75mV.

2. $R_{IMAX\_new} = \frac{-110mV}{R_{DS(ON)} \times I_{OC}} \times 33k\Omega$

   $R_{IMAX\_new} = 48.4k\Omega$

where I_{OC} is the over current value per phase.

Under Voltage Protection (UVP)

The RT8805E monitors the voltage at FB pin, V_{FB}, after the end of soft start (V_{SS} > 3.8V) for under voltage protection. If V_{FB} <0.6V, UVP is tripped. When UVP is tripped, both UGATE and LGATE are all off. At the same time, C_{SS} will be discharged by the internal circuit. Therefore V_{SS} will fall sharply. When the soft start voltage V_{SS} is down to about 0.4V, the 10uA current source starts to charge C_{SS} again. Unlike UVP, the controller will always try to restart and initiate the soft start operation in a hiccupped way.

Over Temperature Protection (OTP)

The operating temperature within the chip is continuously monitored. The controller will be shut down when OTP occurs with a typical trip point of 150°C.

Gate Signal Control

a. Before V_{SS} signal reach the valley of the ramp voltage, both UGATE and LGATE are off.

b. If V_{SS} is down to 0.4V, both UGATE and LGATE will be off.

c. When UVP occurs (V_{FB} < 0.6V and soft start is completed, V_{SS} > 3.8V), controller will trigger Always Hiccup Mode.

d. When OCP is tripped and soft start is completed (V_{SS} > 3.8V), both UGATE and LGATE are off. C_{SS} will be discharged by internal circuit such that V_{SS} falls sharply. Controller will trigger three times of hiccupped restart. After three time of hiccup, the controller is latched off.

e. When fault conditions occur or V_{SS} < 0.4V, the current sense function will be disabled.

Internal/External Reference

The RT8805E supports selectable internal/external reference voltage to provide more flexibility in practical applications. When VCC exceeds POR, controller detects the voltage at PI pin to determine internal/external reference. The selection of internal/external reference is

described as follows.

a. Using internal reference

The internal reference voltage of the RT8805E is 0.8V. When using the internal reference voltage, PI pin should be left open.

b. Using external reference

If the voltage applied at PI pin is higher than 0.4V when VCC exceeds POR, controller recognizes the external input voltage as the reference voltage of the error amplifier. To use the external reference voltage, the applied voltage at PI pin should be within the recommended range (typically between 0.4V to 3V). This externally input voltage is used as the reference voltage for the error amplifier. It is recommended to add ceramic capacitor close to the PI pin for decoupling.

Feedback Loop Compensation

The RT8805E is a voltage-mode buck controller. The voltage feedback path is a single loop, which includes the modulator, error amplifier and compensator. The modulator consists of the PWM comparator and the power stage. A well-designed compensator regulates the output voltage to the reference voltage V_{REF} with fast transient response and good stability. In order to achieve fast transient response and obtain accurate dc regulation, an adequate compensator design is necessary. The goal of the compensation network design is to provide adequate phase margin (usually greater than 45 degrees) and the highest bandwidth (0dB crossing frequency). It is also recommended to manipulate loop frequency response that its gain crosses over 0dB at a slope of -20dB/dec.

The RT8805E uses an operational transconductance amplifier (OTA) as the error amplifier. As Figure 7 shows, the OTA works as the voltage controlled current source because it takes the difference of the two voltages as the input for current conversion.

$$GM = \frac{\Delta I_{OUT}}{\Delta V_M},\ \text{where}\ \Delta V_M = (V_{IN+}) - (V_{IN-})$$

$$\text{and}\ \Delta V_{COMP} = \Delta I_{OUT} \times Z_{OUT}$$

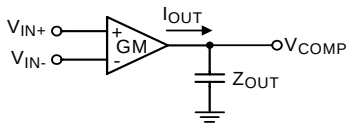


Figure 7. Operational Transconductance Amplifier, OTA

The OTA output current flows through impedance Z_{OUT} and forms voltage V_{COMP}, which is then compared with the sawtooth ramp to generate PWM signal.

The first step of compensator design is to calculate the dc gain of the PWM modulator. Figure 8 shows the PWM modulator, which is composed of the PWM comparator, high-side MOSFET, low-side MOSFET and the drivers. The dc gain of the modulator is the input voltage of the regulator, V_{IN}, divided by the peak-to-peak ramp amplitude of the oscillator, ΔV_{OSC}.

$$Gain_{modulator} = \frac{V_{IN}}{\Delta V_{OSC}}$$

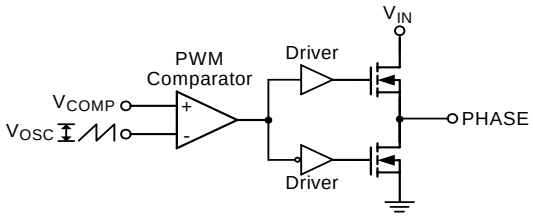


Figure 8. PWM Modulator

As shown in Figure 9, the inductor and the output capacitor form a low-pass L-C output filter. The input to the L-C output filter is the PHASE node and the output is the voltage across the output capacitor. The ESR of the output capacitor plays an important role in the compensator design. The L-C filter introduces a double pole to the system transfer function with a slope of -40dB/dec above its corner frequency and a 180 degree phase lag. The ESR of the output capacitor introduces a zero to the system transfer function with a 90 degree phase shift.

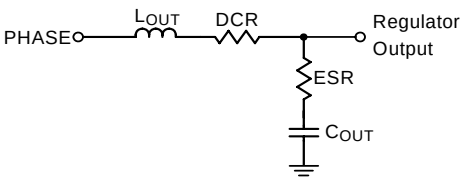


Figure 9. Inductor and Output Capacitor

The second step comes to calculate the frequencies of pole and zero. The frequency of double pole is determined as follows.

$$F_{P(LC)} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

The frequency of the zero is determined as follows.

$$F_{Z(ESR)} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

Note that the output capacitor(s) should have enough ESR to satisfy the stability requirement.

The third step is to design the compensation network. There are two kinds of compensation network : Type II and Type III. Figure 10 shows the Type II compensator.

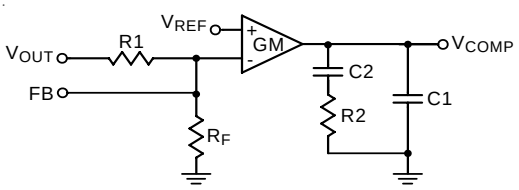


Figure 10. Type II Compensator

Figure 11 shows the Bode plot of the Type II compensator. The frequencies of the single zero and the two poles are determined as follows.

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R2 \times \left(\frac{C1 \times C2}{C1+C2}\right)}$$

$$F_{Z1} = \frac{1}{2\pi \times R2 \times C2}$$

The voltage divider resistors and the transconductance determine the mid-frequency gain of the compensator G_{mid}, which can be calculated as follows.

$$G_{mid} = GM\frac{R_F}{R1+R_F}$$

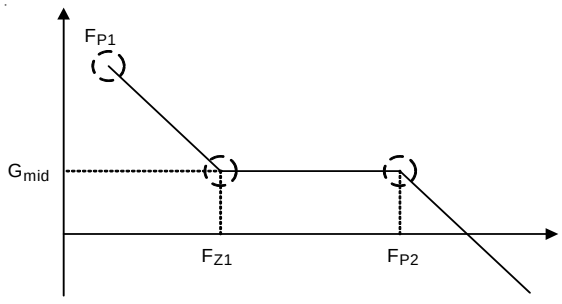


Figure 11. Gain Curve of Type II Compensator

Figure 12 shows the Bode plot of the converter's gain vs. frequency with Type II compensator. The compensator helps to shape the profile of the gain curve with respect to frequency. The zero gives a 90° phase boost to counteract the phase delay contributed by the L-C double pole. The first pole, F_{P1}, gives a shift to the gain curve at low frequency range while the second pole, F_{P2}, provides further attenuation at high frequency range.

In general, a control loop with high bandwidth can achieve fast transient response but usually tends to lose stability. Therefore, it is always a trade-off between the bandwidth and the stability. Empirically, F_{Z1} is placed at about 10% lower than the double pole frequency of the L-C filter to obtain enough phase margin. The bandwidth should be less than 1/5 of the switching frequency. The F_{P2} is placed at half of the switching frequency.

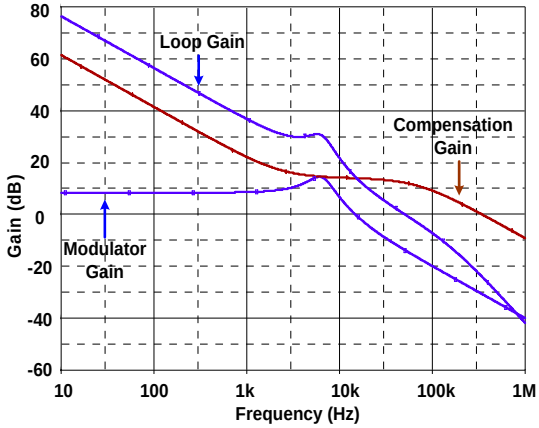


Figure 12. System Bode Plot with Type II Compensator

For the system with low DCR and ESR, the phase curve will have a very sharp slope downward at the double pole that makes the system more difficult to obtain sufficient phase margin using Type II compensator. The Type III compensator has two zeros to create a total of 180° phase boost, and is usually used to compensate a system with low ESR to obtain the necessary phase margin.

Figure 13 shows the Type III compensator, which introduces an extra pole-zero pair by inserting a series R-C circuit between V_{OUT} and FB.

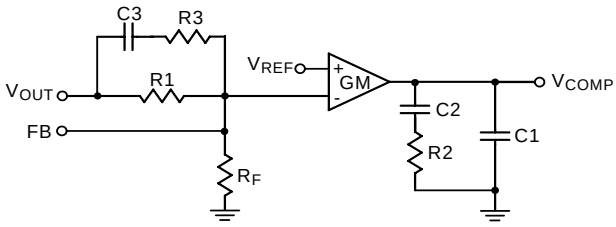


Figure 13. Type III Compensator

Figure 14 shows the Bode plot of the Type III compensator. The frequencies of the three poles and two zeros are determined as follows.

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R2 \times \left(\frac{C1 \times C2}{C1+C2}\right)}$$

$$F_{P3} = \frac{1}{2\pi \times R3 \times C3}$$

$$F_{Z1} = \frac{1}{2\pi \times R2 \times C2}$$

$$F_{Z2} = \frac{1}{2\pi \times (R1+R3) \times C3}$$

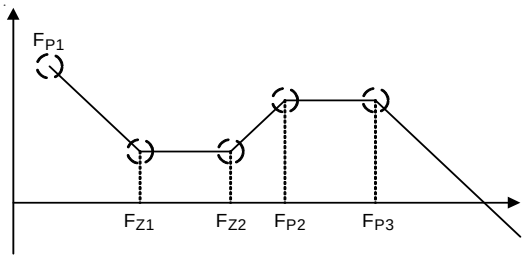


Figure 14. Gain Curve of Type III Compensator

Figure 15 shows the Bode diagram of the converter's gain vs. frequency with Type III compensator. It is recommended that F_{Z1} is placed at half of the L-C double pole, F_{Z2} is placed at the LC double pole, F_{P1} is placed at the ESR zero and F_{P2} is placed at half of the switching frequency.

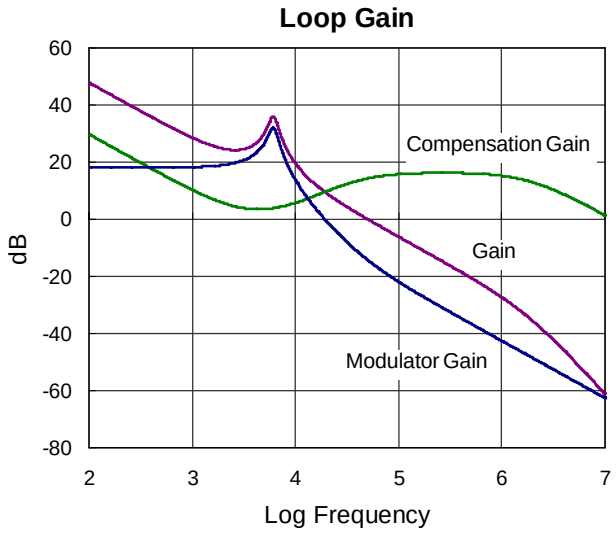


Figure 15. Converter System Bode Plot with Type III Compensator

General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multi-phase buck converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced below.

Power Stages

One of the most important concerns in designing a multi-phase converter is to determine the number of phases. Determining the number of phases highly depends on the overall cost, the system constraints, and usually differs case by case. The main concerns of the circuit designer include the total available board space, the type of component that can be used (through-hole/surface mount device), the maximum load current, and of the most importance, total cost.

In general, the most economical solutions are those in which each phase handles current ranging from 20A to 25A (using one high-side MOSFET and one low-side MOSFET). If each phase have to handle higher current, it is recommended to use two low-side MOSFETs in parallel. However, all the designs are highly depends on whether the large amount of heat can be appropriately removed or not (heat sink, fan cooling, etc).

MOSFET Selection

The majority of power loss in the buck converter is the loss from the low-side power MOSFETs. In the low-voltage high-current applications, the duty cycle of the high-side MOSFET is small. Therefore, the switching loss of the high-side MOSFET is of concern. Power MOSFETs with lower total gate charge are preferred in choosing the high-side power devices.

However, the small duty cycle means the low-side MOSFET is on for most of the switching cycle. Therefore, the conduction loss tends to dominate the total power loss of the converter at heavy load. To improve efficiency, the MOSFETs with low $R_{DS(ON)}$ are preferred.

It is common to use two MOSFETs connected in parallel to decrease the total $R_{DS(ON)}$ in high-current applications. However, this depends on the low-side MOSFET driver capability and the budget.

Package Power Dissipation

It is also important to consider the amount of power being dissipated in the two embedded MOSFET drivers when choosing power MOSFETs. Since there are two drives in the same package, the total power dissipation must not exceed the maximum allowable power dissipation for the WQFN package. Calculating the power dissipation in the drivers is crucial to ensure a safe operation of the controller. Exceeding the maximum allowable power dissipation will let the IC to be operated beyond the recommended maximum junction temperature of 125°C.

The maximum power dissipation for the 4X4 WQFN package is approximately equal to 1.9W at room temperature. The following equations provide the estimation of power dissipation of the integrated drivers.

$$P_D = (C_{UGATE} \times V_{BOOT-PHASE}^2 \times f_{SW}) + (C_{LGATE} \times V_{CC}^2 \times f_{SW})$$

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where the C_{UGATE} and the C_{LGATE} represent the C_{ISS} of the high-side MOSFET and the low-side MOSFET, respectively. From the above equations, it is clear that the junction temperature is directly proportional to the total C_{ISS} of all the external MOSFETs.

For instance, if C_{UGATE}=1nF, C_{LGATE}=5nF (two MOSFETs in parallel, total C_{LGATE} =2 x 5nF), $V_{BOOT-PHASE}$ = 12V, V_{CC} = 12V, switching frequency f_{sw} = 300kHz, the power dissipation in the driver per phase can be obtained :

$P_D \cong 1n \times 12^2 \times 300k + (2 \times 5n) \times 12^2 \times 300k = 475mW$ per phase

Assuming the room temperature is equal to 30°C, the junction temperature for two-phase operation is :

$T_J = 30°C + (52°C/W) \times (0.475W \times 2) = 74.4°C < 125°C$,

, which means the junction temperature is below the maximum recommended value for a safe operation.

Layout Considerations

Layout plays a critical role in switching converter design. Circuit board with careful layout can help the IC to function properly and achieve low losses, low switching noise, and stable operation with better performance. Or the PCB could radiate excessive noise, causing noise-induced IC problems and then contribute to instability. The following guidelines can be used to achieve better performance.

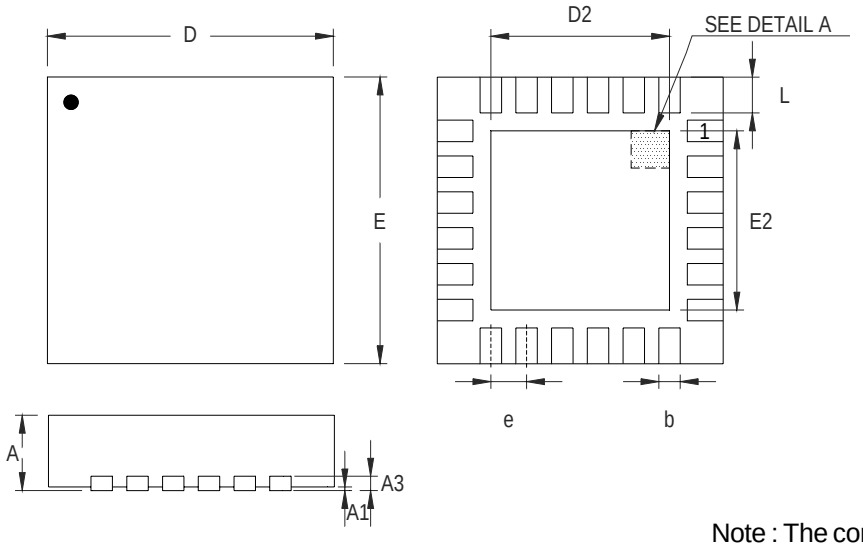
- Power components should be placed first. Place the input capacitors close to the power MOSFETs, then locate the filter inductors and output capacitors between the power MOSFETs and the load.
- Place both the ceramic and bulk input capacitor close to the drain pin of the high-side MOSFET. This can reduce the impedance presented by the input bulk capacitance at high switching frequency. If there is more than one high-side MOSFET in parallel, each should have its own individual ceramic capacitor.
- Keep the power loops as short as possible. For low-voltage high-current applications, power components are the most critical part in the layout because they switch a large amount of current. The current transition from one device to another at high speed causes voltage spikes due to the parasitic components on the circuit board. Therefore, all the high-current switching loops should be kept as short as possible with large and thick copper traces to minimize the parasitic components.
- Minimize the trace length between the power MOSFETs and its drivers.

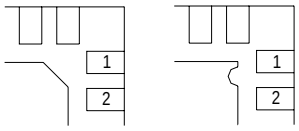
Since the drivers use short, high-current pulses to drive the power MOSFETs, the driving traces should be sized as short and large as possible to reduce the trace inductance. This is especially important to the low-side MOSFET, because this can reduce the possibility of the shoot-through.

- Provide enough copper area around the power MOSFETs and the inductors to aid in heat sinking. Using thick copper PCB also reduces the resistance and inductance to have improved efficiency.
- Output capacitor bank should be placed physically close to the load. This can minimize the impedance seen by the load, and then improves the transient response.
- Place all the high-frequency decoupling ceramic capacitors close to their decoupling targets.
- Small signal components should be located as close as possible to the IC. The small signal components include the feedback components, current sensing components, the compensation components, function setting components and any bypass capacitors. These components belong to the high-impedance circuit loop and are inherently sensitive to noise pick-up. Therefore, they must be located close to their respective controller pins and away from the noisy switching nodes.

  Therefore, R_{RT} and R_{IMAX} resistors should be placed close to IC, and their GND return should be short and away from the noisy MOSFET GND.
- A multi-layer PCB design is recommended. Use one single layer as the power ground and have a separate control signal ground as the reference of all signals.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.950	4.050	0.156	0.159
D2	2.300	2.750	0.091	0.108
E	3.950	4.050	0.156	0.159
E2	2.300	2.750	0.091	0.108
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 24L QFN 4x4 Package

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