General Description

The RT8813C is a 3/2/1 phase synchronous Buck PWM controller which is optimized for high performance graphic microprocessor and computer applications. The IC integrates a Constant-On-Time (COT) PWM controller, two MOSFET drivers with internal bootstrap diodes, as well as channel current balance and protection functions including Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), current limit, and thermal shutdown into the WQFN-24L 4x4 package.

The RT8813C adopts RDS(ON) current sensing technique. Current limit is accomplished through continuous inductor-current-sense, while RDS(ON) current sensing is used for accurate channel current balance. Using the method of current sampling utilizes the best advantages of each technique.

The RT8813C features external reference input and PWM-VID dynamic output voltage control, in which the feedback voltage is regulated and tracks external input reference voltage. Other features include adjustable switching frequency, dynamic phase number control, internal/external soft-start, power good indicator, and enable functions.

Features

- Multi-Phase PWM Controller
- Two Embedded MOSFET Drivers and Embedded Switching Boot Diode
- External Reference Input Control
- PWM-VID Dynamic Voltage Control
- Dynamic Phase Number Control
- Lossless RDS(ON) Current Sensing for Current Balance
- Internal Fixed and External Adjustable Soft-Start
- Adjustable Current Limit Threshold
- Adjustable Switching Frequency
- UVP/OVP Protection
- Shoot Through Protection and Short Pulse Free Technology
- Support an Ultra-Low Output Voltage as Standby Voltage
- Thermal Alert Indicator in 2/1 Active Phase Application
- Thermal Shutdown
- Power Good Indicator
- RoHS Compliant and Halogen Free

Simplified Application Circuit
Applications

- CPU/GPU Core Power Supply
- Notebook PC Memory Power Supply
- Chipset/RAM Power Supply
- Generic DC/DC Power Regulator

Ordering Information

RT8813C

Pin No. | Pin Name | Pin Function
--- | --- | ---
1 | BOOT1 | Bootstrap Supply for PWM 1. This pin powers the high-side MOSFET driver.
2 | UGATE1 | High-side Gate Driver of PWM 1. This pin provides the gate drive for the converter's high-side MOSFET. Connect this pin to the Gate of high-side MOSFET.
3 | EN | Enable Control Input. Active high input.
4 | PSI | Power Saving Interface. When the voltage is pulled below 0.8V, the device will operate into 1 phase DEM. When the voltage is between 1.2V to 1.8V, the device will operate into 1 phase force CCM. When the voltage is between 2.4V to 5.5V, the device will operate into active phase force CCM (only for 2 or 3 phase).
5 | VID | Programming Output Voltage Control Input. Refer to PWM-VID Dynamic Voltage Control.
6 | REFADJ | Reference Adjustment Output. Refer to PWM-VID Dynamic Voltage Control.
7 | REFIN | External Reference Input.
8 | VREF | Reference Voltage Output. This is a high precision voltage reference (2V) from VREF pin to RGND pin.
9 | TON | On-Time/Switching Frequency Adjustment Input. Connect a 100pF capacitor between C_{TON} and ground is optional for noise immunity enhancement.
10 | RGND | Negative Remote Sense Input. Connect this pin to the ground of output load.
11 | VSNS | Positive Remote Sense Input. Connect this pin to the positive terminal of output load.
12 | SS | Soft-Start Time Setting. Connect an external capacitor to adjust soft-start time. When the external capacitor is removed, the internal soft-start function will be chose.
13 | TSNS | Temperature Sensing Input for 2/1 Phase Operation.
14 | ISEN3 | Phase 3 Current Sense Input for 3-Phase Operation.
<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
<td>TALERT</td>
<td>Thermal Alert. Active low open drain output for 2/1 Phase Operation.</td>
</tr>
<tr>
<td></td>
<td>ISEN2</td>
<td>Phase 2 Current Sense Input for 3-Phase Operation.</td>
</tr>
<tr>
<td>15</td>
<td>VCC</td>
<td>Supply Voltage Input for 2/1 Phase Operation. (Connect to PVCC)</td>
</tr>
<tr>
<td></td>
<td>ISEN1</td>
<td>Phase 1 Current Sense Input for 3-Phase Operation. (Connect to PHASE1)</td>
</tr>
<tr>
<td>16</td>
<td>PGOOD</td>
<td>Power Good Indicator Output. Active high open-drain output.</td>
</tr>
<tr>
<td>17</td>
<td>UGATE2</td>
<td>High-side Gate Driver of PWM 2. This pin provides the gate drive for the</td>
</tr>
<tr>
<td></td>
<td></td>
<td>converter's high-side MOSFET. Connect this pin to the Gate of high-side</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MOSFET.</td>
</tr>
<tr>
<td>18</td>
<td>BOOT2</td>
<td>Bootstrap Supply for of PWM 2. This pin powers the high-side MOSFET driver.</td>
</tr>
<tr>
<td>19</td>
<td>PHASE2</td>
<td>Switch Node for PWM2. This pin is return node of the high-side driver of PWM</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. Connect this pin to the Source of high-side MOSFET together with the</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Drain of low-side MOSFET and the inductor.</td>
</tr>
<tr>
<td>20</td>
<td>LGATE2</td>
<td>Low-Side Gate Driver of PWM 2. This pin provides the gate drive for the</td>
</tr>
<tr>
<td></td>
<td></td>
<td>converter's low-side MOSFET. Connect this pin to the Gate of low-side</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MOSFET.</td>
</tr>
<tr>
<td>21</td>
<td>PVCC</td>
<td>Supply Voltage Input. Connect this pin to a 5V bias supply. Place a high</td>
</tr>
<tr>
<td></td>
<td></td>
<td>quality bypass capacitor from this pin to GND.</td>
</tr>
<tr>
<td>22</td>
<td>PWM3</td>
<td>Third Phase PWM Control Signal Output to Driver for 3-Phase Operation. In 2/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Phase Operation, this pin is high impedance.</td>
</tr>
<tr>
<td>23</td>
<td>LGATE1</td>
<td>Low-Side Gate Driver of PWM 1. This pin provides the gate drive for the</td>
</tr>
<tr>
<td></td>
<td></td>
<td>converter's low-side MOSFET. Connect this pin to the Gate of low-side</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MOSFET.</td>
</tr>
<tr>
<td>24</td>
<td>PHASE1</td>
<td>Switch Node for PWM1. This pin is return node of the high-side driver of PWM</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1. Connect this pin to the Source of high-side MOSFET together with the</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Drain of low-side MOSFET and the inductor.</td>
</tr>
<tr>
<td>25</td>
<td>GND</td>
<td>Ground. The Exposed pad should be soldered to a large PCB and connected to</td>
</tr>
<tr>
<td>(Exposed Pad)</td>
<td></td>
<td>GND for maximum thermal dissipation.</td>
</tr>
</tbody>
</table>
Function Block Diagram

Reference Output Gen.

Power On Reset & Central Logic

Control & Protection Logic

Driver Logic

Logic

Boot-Phase Detection 2

Boot-Phase Detection 1

PWM1

PWM2

PWM3

To Protection Logic

To Driver Logic

Current Limit

Soft-Start & Slew Rate Control

OV Threshold Select

40% REF

PWM CMP

TON Gen 1

TON Gen 2 & TON Gen 3

Current Balance

UV

Enable Logic

To Driver Logic

To Power On Reset

To Central Logic

To Protection Logic

Internal OTP

1V

ZCD

To Driver Logic

PHASE1

RGND

Phase Select

VREF

VID

REFADJ

PSI

REFIN

SS

VSNS

RGND

EN

TON

VCC/ISEN1

TALERT/ISEN2

TSNS/ISEN3

Internal OTP

To Central Logic

To Protection Logic

PHASE1

ZCD

To Driver Logic

PHASE1
Operation

The RT8813C is a 3/2/1 phase synchronous Buck PWM controller with integrated drivers which are optimized for high performance graphic microprocessor and computer applications. The IC integrates a COT (Constant-On-Time) PWM controller with two MOSFET drivers, as well as output current monitoring and protection functions. Referring to the function block diagram of TON Genx, the synchronous UGATE driver is turned on at the beginning of each cycle. After the internal one-shot timer expires, the UGATE driver will be turned off. The pulse width of this one-shot is determined by the converter’s input voltage and the output voltage to keep the frequency fairly constant over the input voltage range and output voltage. Another one-shot sets a minimum off-time.

The RT8813C also features a PWM-VID dynamic voltage control circuit driven by the pulse width modulation method. This circuit reduces the device pin count and enables a wide dynamic voltage range.

Soft-Start (SS)

For internal soft-start function, an internal current source charges an internal capacitor to build the soft-start ramp voltage. The output voltage will track the internal ramp voltage during soft-start interval. For external soft-start function, an additional capacitor connected from SS to the GND will be charged by a current source and determines the soft-start time.

PGOOD

The power good output is an open-drain architecture.

When the soft-start is finished, the PGOOD open-drain output will be high impedance.

Current Limit

The current limit circuit employs a unique “valley” current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current limit threshold, the PWM is not allowed to initiate a new cycle. Thus, the current to the load exceeds the average output inductor current, the output voltage falls and eventually crosses the under-voltage protection threshold, inducing IC shutdown.

Over-Voltage Protection (OVP) & Under-Voltage Protection (UVP)

The output voltage is continuously monitored for over-voltage and under-voltage protection. When the output voltage exceeds its set voltage threshold (If \( V_{\text{REFIN}} \leq 1.33V, \text{OV} = 2V \), or \( V_{\text{REFIN}} > 1.33V, \text{OV} = 1.5 \times V_{\text{REFIN}} \)), UGATE goes low and LGATE is forced high; when it is less than 40% of its set voltage, under-voltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. The controller is latched until PVCC is re-supplied and exceeds the POR rising threshold voltage or EN is reset.
Absolute Maximum Ratings (Note 1)

- TON to GND
  - DC: −0.3V to 30V
  - <20ns: −8V to 36V
- RGND to GND
  - DC: −0.7V to 0.7V
- BOOTx to PHASEx
  - DC: −0.3V to 6V
  - <20ns: −5V to 7.5V
- PHASEx to GND
  - DC: −0.3V to 30V
- UGATEx to PHASEx
  - DC: −0.3V to 6V
  - <20ns: −5V to 7.5V
- LGATEx to GND
  - DC: −0.3V to 6V
  - <20ns: −2.5V to 7.5V
- Other Pins
  - DC: −0.3V to 6V
- Power Dissipation, PD @ TA = 25°C
  - WQFN-24L 4x4: 3.57W
- Package Thermal Resistance (Note 2)
  - WQFN-24L 4x4, θJA: 28°C/W
  - WQFN-24L 4x4, θJC: 7°C/W
- Lead Temperature (Soldering, 10 sec.)
  - 260°C
- Junction Temperature
  - 150°C
- Storage Temperature Range
  - −65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model): 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage, V_IN
  - 7V to 26V
- Supply Voltage, V_PVCC
  - 4.5V to 5.5V
- Junction Temperature Range
  - −40°C to 125°C
- Ambient Temperature Range
  - −40°C to 85°C

Electrical Characteristics

(ТА = 25°C unless otherwise specified)

<table>
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<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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<td>PWM Controller</td>
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<td>PVCC Supply Voltage</td>
<td>VPVCC</td>
<td></td>
<td>4.5</td>
<td>--</td>
<td>5.5</td>
<td>V</td>
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<tr>
<td>PVCC Supply Current</td>
<td>ISUPPLY</td>
<td>EN = 3.3V, Not Switching</td>
<td>--</td>
<td>1.5</td>
<td>2</td>
<td>mA</td>
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<tr>
<td>PVCC Shutdown Current</td>
<td>ISHDN</td>
<td>EN = 0V</td>
<td>--</td>
<td>--</td>
<td>10</td>
<td>μA</td>
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<tr>
<td>PVCC POR Threshold</td>
<td></td>
<td></td>
<td>3.8</td>
<td>4.1</td>
<td>4.4</td>
<td>V</td>
</tr>
<tr>
<td>POR Hysteresis</td>
<td></td>
<td></td>
<td>--</td>
<td>0.3</td>
<td>--</td>
<td>V</td>
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</table>

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<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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<tbody>
<tr>
<td>Switching Frequency</td>
<td>( f_{SW} )</td>
<td>( R_{TON} = 500k\Omega ) (Note 5)</td>
<td>270</td>
<td>300</td>
<td>330</td>
<td>kHz</td>
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<tr>
<td>Minimum On-Time</td>
<td>( t_{ON(MIN)} )</td>
<td>--</td>
<td>70</td>
<td>--</td>
<td>--</td>
<td>ns</td>
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<tr>
<td>Minimum Off-Time</td>
<td>( t_{OFF(MIN)} )</td>
<td>--</td>
<td>300</td>
<td>--</td>
<td>--</td>
<td>ns</td>
</tr>
<tr>
<td>EN Threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN Input Voltage</td>
<td>Logic-High</td>
<td>( V_{ENH} )</td>
<td>1.6</td>
<td>--</td>
<td>--</td>
<td>V</td>
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<tr>
<td></td>
<td>Logic-Low</td>
<td>( V_{ENL} )</td>
<td>--</td>
<td>--</td>
<td>0.8</td>
<td>V</td>
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<tr>
<td>Mode Decision</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>PSI High Threshold</td>
<td>( V_{PSIH} )</td>
<td>Enables Two Phases with FCCM</td>
<td>2.4</td>
<td>--</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>PSI Intermediate Threshold</td>
<td>( V_{PSIM} )</td>
<td>Enables One Phases with FCCM</td>
<td>1.2</td>
<td>--</td>
<td>1.8</td>
<td>V</td>
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<tr>
<td>PSI Low Threshold</td>
<td>( V_{PSIL} )</td>
<td>Enables One Phases with DEM</td>
<td>--</td>
<td>--</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>VID Input Voltage</td>
<td>Logic-High</td>
<td>( V_{VIDH} )</td>
<td>2</td>
<td>--</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Logic-Low</td>
<td>( V_{VIDL} )</td>
<td>--</td>
<td>--</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td>Protection Function</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Zero Current Crossing</td>
<td></td>
<td>--</td>
<td>--</td>
<td>8</td>
<td>--</td>
<td>mV</td>
</tr>
<tr>
<td>Threshold</td>
<td>( I_{OCSET} )</td>
<td></td>
<td>9</td>
<td>10</td>
<td>11</td>
<td>( \mu ) A</td>
</tr>
<tr>
<td>Current Limit Setting</td>
<td>( I_{OCSET} )</td>
<td></td>
<td>6300</td>
<td>--</td>
<td>--</td>
<td>ppm/( ^\circ ) C</td>
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<td>Temperature Coefficient</td>
<td>( I_{OCSET_TC} )</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Current Limit Threshold</td>
<td>( R_{OCSET} )</td>
<td>10k</td>
<td>--</td>
<td>60</td>
<td>--</td>
<td>mV</td>
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<tr>
<td>Absolute Over-Voltage</td>
<td>( V_{OVP,_Absolute} )</td>
<td>( V_{REFIN} \leq 1.33V )</td>
<td>1.9</td>
<td>2</td>
<td>2.1</td>
<td>V</td>
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<tr>
<td>Protection Threshold</td>
<td>( V_{OVP,_Relative} )</td>
<td>( V_{REFIN} &gt; 1.33V )</td>
<td>145</td>
<td>150</td>
<td>155</td>
<td>%</td>
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<tr>
<td>OV Fault Delay</td>
<td></td>
<td>FB forced above OV threshold</td>
<td>--</td>
<td>5</td>
<td>--</td>
<td>( \mu ) s</td>
</tr>
<tr>
<td>Relative Under-Voltage</td>
<td>( V_{UVP} )</td>
<td>UVP</td>
<td>35</td>
<td>40</td>
<td>45</td>
<td>%</td>
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<tr>
<td>Protection Threshold</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>UV Fault Delay</td>
<td></td>
<td>FB forced above UV threshold</td>
<td>--</td>
<td>3</td>
<td>--</td>
<td>( \mu ) s</td>
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<tr>
<td>Thermal Shutdown Threshold</td>
<td>( T_{SD} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Minimum TM Threshold</td>
<td>( V_{TSEN} )</td>
<td>(No Shutting Down)</td>
<td>0.98</td>
<td>1</td>
<td>1.02</td>
<td>V</td>
</tr>
<tr>
<td>PGOOD Blanking Time</td>
<td></td>
<td>From EN = high to PGOOD = high with VSNS within regulation point</td>
<td></td>
<td>2.5</td>
<td>--</td>
<td>ms</td>
</tr>
<tr>
<td>(Internal)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VSNS Soft-Start (Internal)</td>
<td></td>
<td>From first UGATE to VSNS regulation point, ( V_{REFIN} = 1V ) and VSNS initial = 0V</td>
<td></td>
<td>0.7</td>
<td>--</td>
<td>ms</td>
</tr>
<tr>
<td>Soft-Start Current Source</td>
<td>( I_{SS} )</td>
<td></td>
<td>--</td>
<td>5</td>
<td>--</td>
<td>( \mu ) A</td>
</tr>
<tr>
<td>Error Amplifier</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VSNS Error Comparator</td>
<td></td>
<td>( V_{REFIN} = 1V )</td>
<td></td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
</tbody>
</table>

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### Reference

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<tr>
<th>Parameter</th>
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<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference Voltage</td>
<td>VREF</td>
<td>Sourcing Current = 1mA, VID no Switching</td>
<td>1.98</td>
<td>2</td>
<td>2.02</td>
<td>V</td>
</tr>
</tbody>
</table>

### Driver On-Resistance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>UGATE Driver Source</td>
<td>R(_{UGATEsr})</td>
<td>BOOTx – PHASEx Forced to 5V</td>
<td>--</td>
<td>2</td>
<td>4</td>
<td>Ω</td>
</tr>
<tr>
<td>UGATE Driver Sink</td>
<td>R(_{UGATEsk})</td>
<td>BOOTx – PHASEx Forced to 5V</td>
<td>--</td>
<td>1</td>
<td>2</td>
<td>Ω</td>
</tr>
<tr>
<td>LGATE Driver Source</td>
<td>R(_{LGATEGy})</td>
<td>LGATEx, High State</td>
<td>--</td>
<td>1.5</td>
<td>3</td>
<td>Ω</td>
</tr>
<tr>
<td>LGATE Driver Sink</td>
<td>R(_{LGATEsk})</td>
<td>LGATEx, Low State</td>
<td>--</td>
<td>0.7</td>
<td>1.5</td>
<td>Ω</td>
</tr>
</tbody>
</table>

| Dead-Time                  |          | From LGATE Falling to UGATE Rising     | --  | 30  | --  | ns   |
|                            |          | From UGATE Falling to LGATE Rising     | --  | 20  | --  | ns   |

| Internal Boost Charging    | R\(_{BOOT}\) | PVCC to BOOTx, I\(_{BOOT}\) = 10mA     | --  | 40  | 80  | Ω    |

**Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** \(\theta\)\(_{JA}\) is measured at \(T_A = 25°C\) on a high effective thermal conductivity four-layer test board per JEDEC 51-7. \(\theta\)\(_{JC}\) is measured at the exposed pad of the package.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Note 5.** Not production tested. Test condition is \(V_{IN} = 8V, V_{OUT} = 1V, I_{OUT} = 20A\) using application circuit.
Typical Application Circuit

**Figure 1.** 3 Active Phase Configuration

**Figure 2.** 2 Active Phase Configuration
Figure 3.1 Active Phase Configuration
Typical Operating Characteristics

Efficiency vs. Load Current

- **VIN = 19V, VPVCC = 5V, VOUT = 0.9V, 2 Phase Operation**

- **VIN = 19V, VPVCC = 5V, VOUT = 0.9V, 1 Phase with DEM Operation**

**TON vs. Temperature**

- **VIN = 19V, VPVCC = 5V, No Load**

**VREF vs. Temperature**

- **VIN = 19V, VPVCC = 5V, No Load**

**Inductor Current vs. Output Current**

- **VIN = 19V, VPVCC = 5V**

**Power On from EN**

- **EN (5V/Div)**
- **VOUT (1V/Div)**
- **UGATE1 (50V/Div)**
- **UGATE2 (50V/Div)**

VIN = 19V, VPVCC = 5V, IOUT = 50A
Load Transient Response

OVP

UVP

OCP
Application Information

The RT8813C is a multi-phase synchronous Buck PWM controller with integrated drivers which is optimized for high-performance graphic microprocessor and computer applications. A COT (Constant-On-Time) PWM controller and two MOSFET drivers with internal bootstrap diodes are integrated so that the external circuit can be easily designed and the number of component is reduced.

The topology solves the poor load transient response timing problems of fixed-frequency mode PWM and avoids the problems caused by widely varying switching frequencies in conventional constant on-time and constant off-time PWM schemes.

The IC supports dynamic mode transition function with various operating states, which include multi-phase with CCM operation and single phase with diode emulation mode. These different operating states make the system efficiency as high as possible.

The RT8813C provides a PWM-VID dynamic control operation in which the feedback voltage is regulated and tracks external input reference voltage. It also features complete fault protection functions including over voltage, under voltage and current limit.

Remote Sense

The RT8813C uses the remote sense path (VSNS and RGND) to overcome voltage drops in the power lines by sensing the voltage directly at the end of GPU. Normally, to protect remote sense path disconnecting, there are two resistors (R_{Local}) connecting between local sense path and remote sense path. That is, in application with remote sense, the R_{Local} is recommended to be 10Ω to 100Ω. If no need of remote sense, the R_{Local} is recommended to be 0Ω.

PWM Operation

The RT8813C integrates a Constant-On-Time (COT) PWM controller, and the controller provides the PWM signal which relies on the output ripple voltage comparing with internal reference voltage as shown in Figure 5. Referring to the function block diagram of TON Genx, the synchronous UGATE driver is turned on at the beginning of each cycle. After the internal one-shot timer expires, the UGATE driver will be turned off. The pulse width of this one-shot is determined by the converter's input voltage and the output voltage to keep the frequency fairly constant over the input voltage and output voltage range. Another one-shot sets a minimum off-time.

On-Time Control

The on-time one-shot comparator has two inputs. One input monitors the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to V_{OUT}, thereby making the on-time of the high side switch directly proportional to output voltage and inversely proportional to input voltage. The implementation results in a nearly constant switching frequency without the need for a clock generator.

\[
T_{ON} = \frac{2 \times V_{OUT} \times 3.2p}{V_{IN} - 0.5} \times R_{TON}
\]

and then the switching frequency F_S is:

\[
F_S = \frac{V_{OUT}}{(V_{IN} \times T_{ON})}
\]

R_{TON} is a resistor connected from the \( V_{IN} \) to TON pin. The value of R_{TON} can be selected according to Figure 6.

The recommend operation frequency range is 150kHz to 600kHz.
The RT8813C can operate in 3/2/1 phase. When PVCC is higher than POR threshold and EN is higher than logical-high level, the RT8813C will detect the VCC/ISEN1 pin to determine how many phases should be active. For three phases operation, the VCC/ISEN1 pin is connected to PHASE1, the TALERT/ISEN2 pin is connected to PHASE2, the TSNS/ISEN3 pin is connected to PHASE3, and external MOSFET driver’s PWM pin is connected to PWM3. For two phases operation, the VCC/ISEN1 pin is connected to PVCC, the TALERT/ISEN2 pin is connected to TALERT signal, the TSNS/ISEN3 pin is connected to TSNS signal, and the PWM3 pin is connected to GND. For one phase operation, the VCC/ISEN1 pin is connected to PVCC, TALERT/ISEN2 pin is connected to TALERT signal, the TSNS/ISEN3 pin is connected to TSNS signal, the PWM3 pin is connected to GND, and UGATE2, BOOT2, PHASE2, and LGATE 2 pins are floating. The voltage setting at PSI pin can’t higher than 1.8V.

Mode Selection
The RT8813C can operate in 3 phases or 2 phases with force CCM, 1 phase with force CCM, and 1 phase with DEM according to PSI voltage setting. If PSI voltage is pulled below 0.8V, the controller will operate into 1 phase with DEM. In DEM operation, the RT8813C automatically reduces the operation frequency at light load conditions for saving power loss. If PSI voltage is pulled between 1.2V to 1.8V, the controller will switch operation into 1-phase with force CCM. If PSI voltage is pulled between 2.4V to 5.5V, the controller will switch operation into active phase (only for 2 or 3 phases). The operation mode is summarized in Table 1. Moreover, the PSI pin is valid after POR of VR.

<table>
<thead>
<tr>
<th>Operation Phase Number</th>
<th>PSI Voltage Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 phase with DEM</td>
<td>0V to 0.8V</td>
</tr>
<tr>
<td>1 phase with CCM</td>
<td>1.2V to 1.8V</td>
</tr>
<tr>
<td>Active phase with CCM</td>
<td>2.4V to 5.5V</td>
</tr>
</tbody>
</table>

Diode-Emulation Mode
In diode-emulation mode, the RT8813C automatically reduces switching frequency at light-load conditions to maintain high efficiency. As the output current decreases from heavy-load condition, the inductor current is also reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low-side MOSFET allows only partial of negative current when the inductor freewheeling current reaches negative value. As the load current is further decreased, it takes a longer time to discharge the output capacitor to the level that requires the next “ON” cycle. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction condition. The transition load point to the light load operation is shown in Figure 7 and can be calculated as follows:

\[ I_{LOAD(SKIP)} = \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON} \]

where \( t_{ON} \) is on-time.

![Figure 6. Frequency vs. R_{TON}](image)

![Figure 7. Boundary condition of CCM/DEM](image)
The switching waveforms may be noisy and asynchronous in light loading diode-emulation operation condition, but this is a normal operating condition that results in high light-load efficiency. Trade-off in DEM noise vs. light-load efficiency is made by varying the inductor value. Generally, low inductor values produce a broad high efficiency range vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. The disadvantages for using higher inductor values include larger physical size and degraded load-transient response (especially at low input voltage levels).

**Forced-CCM Mode**
The low noise, forced-CCM mode disables the zero-crossing comparator, which controls the low-side switch on-time. This causes the low-side gate drive waveform to be the complement of the high-side gate drive waveform. This in turn causes the inductor current to reverse at light loads as the PWM loop to maintain a duty ratio $V_{OUT}/V_{IN}$. The benefit of forced-CCM mode is to keep the switching frequency fairly constant.

**Enable and Disable**
The EN pin is a high impedance input that allows power sequencing between the controller bias voltage and another voltage rail. The RT8813C remains in shutdown if the EN pin is lower than 800mV. When the EN voltage rises above the 1.6V high level threshold, the RT8813C will begin a new initialization and soft-start cycle.

**Power On Reset (POR), UVLO**
Power On Reset (POR) occurs when $V_{PVCC}$ rises above to approximately 4.1V (typical), the RT8813C will reset the fault latch circuit and prepare for PWM operation. When the $V_{PVCC}$ is lower than 3.8V (typical), the Under Voltage Lockout (UVLO) circuitry inhibits switching by keeping UGATE and LGATE low.

**Soft-Start**
The RT8813C provides both internal soft-start function and external soft-start function. The soft-start function is used to prevent large inrush current and output voltage overshoot while the converter is being powered-up. The soft-start function automatically begins once the chip is enabled. There is a delay time around 1.1ms from EN goes high to $V_{OUT}$ begins to ramp-up.

If the external capacitor between the SS pin and ground is removed, the internal soft-start function will be chosen. An internal current source charges the internal soft-start capacitor so that the internal soft-start voltage ramps up linearly. The output voltage will track the internal soft-start voltage during the soft-start interval. After the internal soft-start voltage exceeds the REFIN voltage, the output voltage no longer tracks the internal soft-start voltage but follows the REFIN voltage. Therefore, the duty cycle of the UGATE signal as well as the input current at power up are limited. The soft-start process is finished until both the single internal SSOK and external SSOK go high and protection is not triggered. Figure 8 shows the internal soft-start sequence.
The RT8813C also provides an external soft-start function, and the external soft-start sequence is shown in Figure 9. The external capacitor connected from SS pin to GND is charged by a 5μA current source to build a soft-start voltage ramp. If the external soft-start function is chosen, the external soft-start time should be set longer than internal soft-start time to avoid output voltage tracking the internal soft-start ramp. The recommended external soft-start slew rate is from 0.1V/ms to 0.4V/ms.

Power Good Output (PGOOD)
The PGOOD pin is an open-drain output, and it requires a pull-up resistor. During soft-start, the PGOOD is held low and is allowed to be pulled high after VOUT achieved over UVP threshold and under OVP threshold. In additional, if any protection is triggered during operation, the PGOOD will be pulled low immediately.

PWM VID and Dynamic Output Voltage Control
The RT8813C features a PWM VID input for dynamic output voltage control as shown in Figure 11, which reduces the number of device pin and enables a wide dynamic voltage range. The output voltage is determined by the applied voltage on the REFIN pin. The PWM duty cycle determines the variable output voltage at REFIN.

With the external circuit and VID control signal, the controller provides three operation modes shown as Figure 12.
Boot Mode

VID is not driven, and the buffer output is tri-state. At this time, turn off the switch Q1 and connect a resistor divider as shown in Figure 11 that can set the REFIN voltage to be VBoot as the following equation:

\[ V_{\text{Boot}} = V_{\text{REF}} \times \left( \frac{R_{\text{REF2}}}{R_{\text{REF1}} + R_{\text{REF2}} + R_{\text{BOOT}}} \right) \]

where \( V_{\text{REF}} \) = 2V (typ.)

Choose \( R_{\text{REF2}} \) to be approximately 10kΩ, and the \( R_{\text{REF1}} \) and \( R_{\text{BOOT}} \) can be calculated by the following equations:

\[ R_{\text{REF1}} = \frac{R_{\text{REF2}} \times (V_{\text{REF}} - V_{\text{Boot}})}{V_{\text{Boot}}} \]
\[ R_{\text{BOOT}} = \frac{R_{\text{REF2}} \times (V_{\text{REF}} - V_{\text{Boot}})}{V_{\text{Boot}}} - R_{\text{REF1}} \]

Standby Mode

An external control can provide a very low voltage to meet \( V_{\text{OUT}} \) operating in standby mode. If the VID pin is floating and switch Q1 is enabled as shown in Figure 11, the REFIN pin can be set for standby voltage according to the calculation below:

\[ V_{\text{STANDBY}} = V_{\text{REF}} \times \left( \frac{R_{\text{REF2}} / R_{\text{STANDBY}}}{R_{\text{REF1}} + R_{\text{BOOT}} + (R_{\text{REF2}} / R_{\text{STANDBY}})} \right) \]

By choosing \( R_{\text{REF1}}, R_{\text{REF2}}, \) and \( R_{\text{BOOT}}, \) the \( R_{\text{STANDBY}} \) can be calculated by the following equation:

\[ R_{\text{STANDBY}} = \left( \frac{R_{\text{REF2}} \times (R_{\text{REF1}} + R_{\text{BOOT}}) \times V_{\text{STANDBY}}}{R_{\text{REF2}} \times V_{\text{REF}} - V_{\text{STANDBY}} \times (R_{\text{REF1}} + R_{\text{REF2}} + R_{\text{BOOT}})} - R_{\text{REF1}} \right) \]

Normal Mode

If the VID pin is driven by a PWM signal and switch Q1 is disabled as shown in Figure 11, the \( V_{\text{REFIN}} \) can be adjusted from \( V_{\text{min}} \) to \( V_{\text{max}} \), where \( V_{\text{min}} \) is the voltage at zero percent PWM duty cycle and \( V_{\text{max}} \) is the voltage at one hundred percent PWM duty cycle. The \( V_{\text{min}} \) and \( V_{\text{max}} \) can be set by the following equations:

\[ V_{\text{min}} = V_{\text{REF}} \times \left( \frac{R_{\text{REF2}}}{R_{\text{REF1}} + R_{\text{REF2}} + R_{\text{BOOT}}} \times \frac{R_{\text{REFADJ ADJ}} / (R_{\text{BOOT}} + R_{\text{REF2}})}{R_{\text{REF1}} + \left( R_{\text{REFADJ ADJ}} / (R_{\text{BOOT}} + R_{\text{REF2}}) \right)} \right) \]
\[ V_{\text{max}} = V_{\text{REF}} \times \left( \frac{R_{\text{REF2}}}{R_{\text{REF1}} + R_{\text{REF2}}} \right) \]

By choosing \( R_{\text{REF1}}, R_{\text{REF2}}, \) and \( R_{\text{BOOT}}, \) the \( R_{\text{REFADJ ADJ}} \) can be calculated by the following equation:

\[ R_{\text{REFADJ}} = \frac{R_{\text{REF1}} \times V_{\text{min}}}{V_{\text{max}} - V_{\text{min}}} \]

The relationship between VID duty and \( V_{\text{REFIN}} \) is shown in Figure 13, and \( V_{\text{OUT}} \) can be set according to the calculation below:

\[ V_{\text{OUT}} = V_{\text{min}} + N \times V_{\text{STEP}} \]

where \( V_{\text{STEP}} \) is the resolution of each voltage step 1.

\[ V_{\text{STEP}} = \left( \frac{V_{\text{max}} - V_{\text{min}}}{N_{\text{max}}} \right) \]

where \( N_{\text{max}} \) is the number of total available voltage steps and \( N \) is the number of step at a specific \( V_{\text{OUT}} \). The dynamic voltage VID period (\( T_{\text{vid}} = T_{u} \times N_{\text{max}} \)) is determined by the unit pulse width (\( T_{u} \)) and the available step number (\( N_{\text{max}} \)). The recommended \( T_{u} \) is 27ns.
VID Slew Rate Control

In RT8813C, the \( V_{\text{REFIN}} \) slew rate is proportional to PWM VID duty. The rising time and falling time are the same because the voltage of REFIN pin traveling is the same. In normal mode, the \( V_{\text{REFIN}} \) slew rate SR can be estimated by \( C_{\text{REFADJ}} \) or \( C_{\text{REFIN}} \) as the following equation:

\[
\text{When choose } C_{\text{REFADJ}}: \\
SR = \frac{(V_{\text{REFIN,final}} - V_{\text{REFIN,initial}}) \times 80\%}{2.2R_{\text{SR}}C_{\text{REFADJ}}} \\
R_{\text{SR}} = \left[\frac{(R_{\text{REF1}} \parallel R_{\text{REFADJ}})}{R_{\text{BOOT}} + R_{\text{REF2}}}\right] \\
\text{When choose } C_{\text{REFIN}}: \\
SR = \frac{(V_{\text{REFIN,final}} - V_{\text{REFIN,initial}}) \times 80\%}{2.2R_{\text{SR}}C_{\text{REFIN}}} \\
R_{\text{SR}} = \left[\frac{(R_{\text{REF1}} \parallel R_{\text{REFADJ}} + R_{\text{BOOT}})}{R_{\text{REF2}}}\right]
\]

The recommend SR is estimated by \( C_{\text{REFADJ}} \).

Current limit

The RT8813C provides cycle-by-cycle current limit control by detecting the PHASE voltage drop across the low-side MOSFET when it is turned on. The current limit circuit employs a unique “valley” current sensing algorithm as shown in Figure 14. If the magnitude of the current sense signal at PHASE is above the current limit threshold, the PWM is not allowed to initiate a new cycle.

![Figure 14. “Valley” Current Limit](image)

In order to provide both good accuracy and a cost effective solution, the RT8813C supports temperature compensated MOSFET \( R_{\text{DS(ON)}} \) sensing.

In an over-current condition, the current to the load exceeds the average output inductor current. Thus, the output voltage falls and eventually crosses the under-voltage protection threshold, inducing IC shutdown.

Current Limit Setting

Current limit threshold can be set by a resistor \( (R_{\text{OCSET}}) \) between LGATE1 and GND. Once PVCC exceeds the POR threshold and chip is enabled, an internal current source \( I_{\text{OCSET}} \) flows through \( R_{\text{OCSET}} \). The voltage across \( R_{\text{OCSET}} \) is stored as the current limit protection threshold \( V_{\text{OCSET}} \). The threshold range of \( V_{\text{OCSET}} \) is 50mV to 400mV. After that, the current source is switched off.

\( R_{\text{OCSET}} \) can be determined using the following equation:

\[
R_{\text{OCSET}} = \left(\frac{I_{\text{VALLEY}} \times R_{\text{LGS(ON)}}}{I_{\text{OCSET}}}\right) + 40\text{mV}
\]

where \( I_{\text{VALLEY}} \) represents the desired inductor limit current (valley inductor current) and \( I_{\text{OCSET}} \) is current limit setting current which has a temperature coefficient to compensate the temperature dependency of the \( R_{\text{DS(ON)}} \).

If \( R_{\text{OCSET}} \) is not present, there is no current path for \( I_{\text{OCSET}} \) to build the current limit threshold. In this situation, the current limit threshold is internally preset to 400mV (typical).

Negative Current Limit

The RT8813C supports cycle-by-cycle negative current limit. The absolute value of negative current limiting threshold is the same with the positive current limit threshold. If negative inductor current is rising to trigger negative current limit, the low-side MOSFET will be turned off and the current will flow to input side through the body diode of the high-side MOSFET. At this time, output voltage tends to rise because this protection limits current to discharge the output capacitor. In order to prevent shutdown because of over-voltage protection, the low-side MOSFET is turned on again 400ns after it is turned off. If the device hits the negative current limit threshold again before output voltage is discharged to the target level, the low-side MOSFET is turned off and process repeats. It ensures maximum allowable discharge capability when output voltage continues to rise. On the other hand, if the output voltage is discharged to the target level before negative current limit threshold is reached, the low-side MOSFET is turned off, the high-side MOSFET is then turned on, and the device keeps normal operation.
Current Balance
The RT8813C implements current balance mechanism in the current loop. The RT8813C senses per phase current signal and compares it with the average current. If the sensed current of any particular phase is higher than the average current, the on-time of this phase will be decreased.

The current balance accuracy is major related with on-resistance of low side MOSFET ($R_{\text{LGS(ON)}}$). That is, in practical application, using lower $R_{\text{LGS(ON)}}$ will reduce the current balance accuracy.

Output Over-Voltage Protection (OVP)
The output voltage can be continuously monitored for over-voltage protection. If REFIN voltage is lower than 1.33V, the over voltage threshold follows to absolute over voltage 2V. If REFIN voltage is higher than 1.33V, the over voltage threshold follows relative over voltage 1.5 x VREFIN. When OVP is triggered, UGATE goes low and LGATE is forced high. The RT8813C is latched once OVP is triggered and can only be released by PVCC or EN power on reset. A 5μs delay is used in OVP detection circuit to prevent false trigger.

Output Under-Voltage Protection (UVP)
The output voltage can be continuously monitored for under-voltage protection. When the output voltage is less than 40% of its set voltage, under-voltage protection is triggered and then all UGATEx and LGATEx gate drivers are forced low. There is a 3μs delay built in the UVP circuit to prevent false transitions. During soft-start, the UVP blanking time is equal to PGOOD blanking time.

Thermal Monitoring and Temperature Reporting
The RT8813C provides thermal monitoring function in 2/1 phase operation via sensing the TSNS pin voltage, and which can indicate ambient temperature through the voltage divider $R_{\text{OTSET}}$ and $R_{\text{NTC}}$ shown in Figure 15. The voltage of $V_{\text{TSNS}}$ is typically set to be higher than 1V. When ambient temperature rises, $V_{\text{TSNS}}$ will fall and the $\overline{\text{TALERT}}$ signal will be pulled to low level if TSNS voltage drops below 1V.

$$R_{\text{OTSET}}\text{ can be determined using the following equation : } R_{\text{OTSET}} = R_{\text{NTC,T-250C}} (V_X - 1)$$

where $R_{\text{NTC,T-250C}}$ is the thermistor’s resistance at OTP trigger temperature.

The standard formula for the resistance of the NTC thermistor as a function of temperature is given by:

$$R_{\text{NTC,T-250C}} = R_{250C} \times \left( \frac{1}{T+273} \right) \left( \frac{1}{298} \right)$$

where $R_{250C}$ is the thermistor’s nominal resistance at room temperature 25°C, $\beta$ (beta) is the thermistor’s material constant in Kelvins, and $T$ is the thermistor’s actual temperature in Celsius.

MOSFET Gate Driver
The RT8813C integrates high current gate drivers for the MOSFETs to obtain high efficiency power conversion in synchronous Buck topology. A dead-time is used to prevent the crossover conduction for high-side and low-side MOSFETs. Because both the two gate signals are off during the dead-time, the inductor current freewheels through the body diode of the low-side MOSFET. The freewheeling current and the forward voltage of the body diode contribute power losses to the converter. The RT8813C employs adaptive dead-time control scheme to ensure safe operation without sacrificing efficiency. Furthermore, elaborate logic circuit is implemented to prevent cross conduction. For high output current applications, two power MOSFETs are usually paralleled to reduce $R_{\text{DS(ON)}}$. The gate driver needs to provide more current to switch on/off these paralleled MOSFETs. Gate driver with lower source/sink current capability results in longer rising/falling time in gate signals and higher switching loss. The RT8813C embeds high current gate drivers to obtain high efficiency power conversion.
Inductor Selection

Inductor plays an importance role in step-down converters because the energy from the input power rail is stored in it and then released to the load. From the viewpoint of efficiency, the DC Resistance (DCR) of inductor should be as small as possible to minimize the copper loss. In addition, the inductor occupies most of the board space so the size of it is important. Low profile inductors can save board space especially when the height is limited. However, low DCR and low profile inductors are usually not cost effective.

Additionally, higher inductance results in lower ripple current, which means the lower power loss. However, the inductor current rising time increases with inductance value. This means the transient response will be slower. Therefore, the inductor design is a trade-off between performance, size and cost.

In general, inductance is designed to let the ripple current ranges between 20% to 40% of full load current. The inductance can be calculated using the following equation:

\[ L_{\text{min}} = \frac{V_{\text{IN}} - V_{\text{OUT}}}{F_{\text{SW}} \times k \times I_{\text{OUT \_ rated}}} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}} \]

where \( k \) is the ratio between inductor ripple current and rated output current.

Input Capacitor Selection

Voltage rating and current rating are the key parameters in selecting input capacitor. Generally, input capacitor has a voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation:

\[ I_{\text{RMS}} = I_{\text{OUT}} \times \sqrt{\frac{V_{\text{OUT}}}{V_{\text{IN}}} \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}} \right)} \]

The next step is to select proper capacitor for RMS current rating. Use more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank is a good design. Besides, placing ceramic capacitor close to the Drain of the high-side MOSFET is helpful in reducing the input voltage ripple at heavy load.

Output Capacitor Selection

The output filter capacitor must have ESR low enough to meet output ripple and load transient requirement, yet have high enough ESR to satisfy stability requirements. Also, the capacitance must be high enough to absorb the inductor energy going from a full load to no load condition without tripping the OVP circuit. Organic semiconductor capacitor(s) or special polymer capacitor(s) are recommended.

MOSFET Selection

The majority of power loss in the step-down power conversion is due to the loss in the power MOSFETs. For low voltage high current applications, the duty cycle of the high-side MOSFET is small. Therefore, the switching loss of the high-side MOSFET is of concern. Power MOSFETs with lower total gate charge are preferred in such kind of application.

However, the small duty cycle means the low-side MOSFET is on for most of the switching cycle. Therefore, the conduction loss tends to dominate the total power loss of the converter. To improve the overall efficiency, the MOSFETs with low \( R_{DS(ON)} \) are preferred in the circuit design. In some cases, more than one MOSFET are connected in parallel to further decrease the on-state resistance. However, this depends on the low-side MOSFET driver capability and the budget.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

\[ P_{D(\text{MAX})} = \frac{(T_{J(\text{MAX})} - T_A)}{\theta_{JA}} \]

where \( T_{J(\text{MAX})} \) is the maximum junction temperature, \( T_A \) is the ambient temperature, and \( \theta_{JA} \) is the junction to ambient thermal resistance.
For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, $\theta_{JA}$, is layout dependent. For WQFN-24L 4x4 package, the thermal resistance, $\theta_{JA}$, is 28°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at $T_A = 25^\circ$C can be calculated by the following formula:

$$ P_{D(MAX)} = (125^\circ°C - 25^\circ°C) / (28^\circ°C/W) = 3.57W $$ for WQFN-24L 4x4 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, $\theta_{JA}$. The derating curve in Figure 16 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

### Layout Considerations

Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. Following layout guidelines must be considered before starting a layout for RT8813C.

- Place the RC filter as close as possible to the PVCC pin.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching node.
- Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components such as VSNS, RGND, EN, PSI, VID, PGOOD, VREF, TON VREFADJ, VREFIN and TSNS should be placed away from high voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Power sections should connect directly to ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses.
Outline Dimension

Note: The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Dimensions In Millimeters</th>
<th>Dimensions In Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Min 0.700, Max 0.800</td>
<td>Min 0.028, Max 0.031</td>
</tr>
<tr>
<td>A1</td>
<td>Min 0.000, Max 0.050</td>
<td>Min 0.000, Max 0.002</td>
</tr>
<tr>
<td>A3</td>
<td>Min 0.175, Max 0.250</td>
<td>Min 0.007, Max 0.010</td>
</tr>
<tr>
<td>b</td>
<td>Min 0.180, Max 0.300</td>
<td>Min 0.007, Max 0.012</td>
</tr>
<tr>
<td>D</td>
<td>Min 3.950, Max 4.050</td>
<td>Min 0.156, Max 0.159</td>
</tr>
<tr>
<td>D2</td>
<td>Option 1 Min 2.400, Max 2.500, Option 2 Min 2.650, Max 2.750</td>
<td>Option 1 Min 0.094, Max 0.098, Option 2 Min 0.104, Max 0.108</td>
</tr>
<tr>
<td>E</td>
<td>Min 3.950, Max 4.050</td>
<td>Min 0.156, Max 0.159</td>
</tr>
<tr>
<td>E2</td>
<td>Option 1 Min 2.400, Max 2.500, Option 2 Min 2.650, Max 2.750</td>
<td>Option 1 Min 0.094, Max 0.098, Option 2 Min 0.104, Max 0.108</td>
</tr>
<tr>
<td>e</td>
<td>Min 0.500</td>
<td>Min 0.020</td>
</tr>
<tr>
<td>L</td>
<td>Min 0.350, Max 0.450</td>
<td>Min 0.014, Max 0.018</td>
</tr>
</tbody>
</table>

W-Type 24L QFN 4x4 Package

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