

Multi-Phase PWM Controller with PWM-VID Reference

General Description

The RT8843B is a 3/2/1 multi-phase synchronous Buck controller which is optimized for high performance graphic microprocessor and support nVidia OVR3i+ spec with PWM-VID interface. It can support both DrMOS with current output and DCR current sensing. The RT8843B adopts AC G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of internal GM amplifier with current mode control. By utilizing the AC G-NAVP™ topology, the operating frequency of the RT8843B varies with VID, load and input voltage to further enhance the efficiency even in CCM. Moreover, the AC G-NAVP™ with CCRCOT (Constant Current Ripple COT) technology provides superior output voltage ripple over the entire input/output range.

The RT8843B features external reference input and PWM-VID dynamic output voltage control, in which the output voltage is regulated and tracks external input reference voltage. The RT8843B can set internal RAMP amplitude through PINSETx pin and this can optimize stability and load transient performance. The RT8843B also provides complete fault protection functions including Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), Over-Current Limit (OCL) and Over-Temperature Protection (OTP).

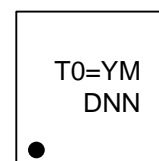
Features

- Multi-Phase PWM Controller
- PWM-VID Dynamic Voltage Control
- Support 1.8V PWM-VID Interface
- Power State Indicator
 - ▶ 1Phase-DEM/Full Phase-DEM/ Full Phase -CCM
- External Reference Input Control
- 3/2/1 Phase Hardware Setting
- Adjustable Soft-Start time
- Adjustable Current Limit Threshold
- Adjustable Switching Frequency
- UVP/OVP/OTP Protection
- Power Good Indicator
- RoHS Compliant and Halogen Free

Applications

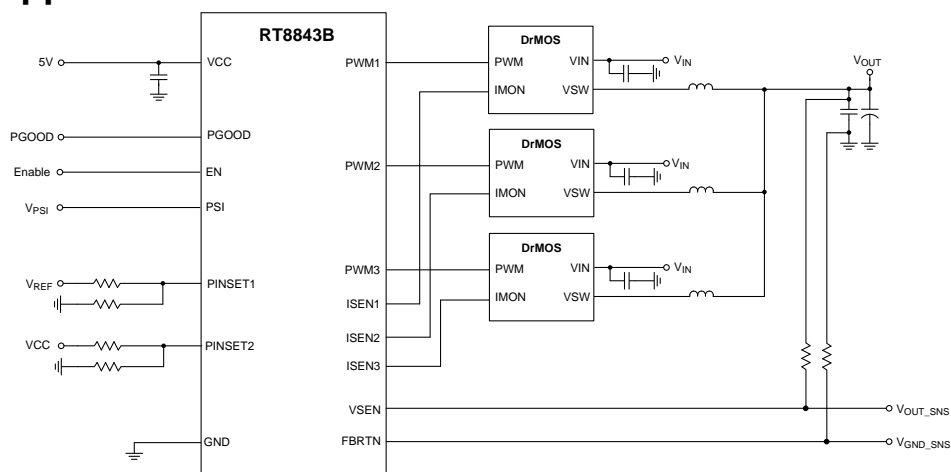
- GPU Core Power for OVR3i+ Spec

Marking Information



T0 = : Product Code
YMDNN : Date Code

Simplified Application Circuit



Ordering Information

RT8843B □ □

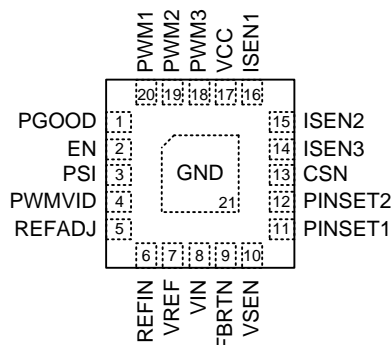
- Package Type
QW : WQFN-20L 3x3 (W-Type)
- Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

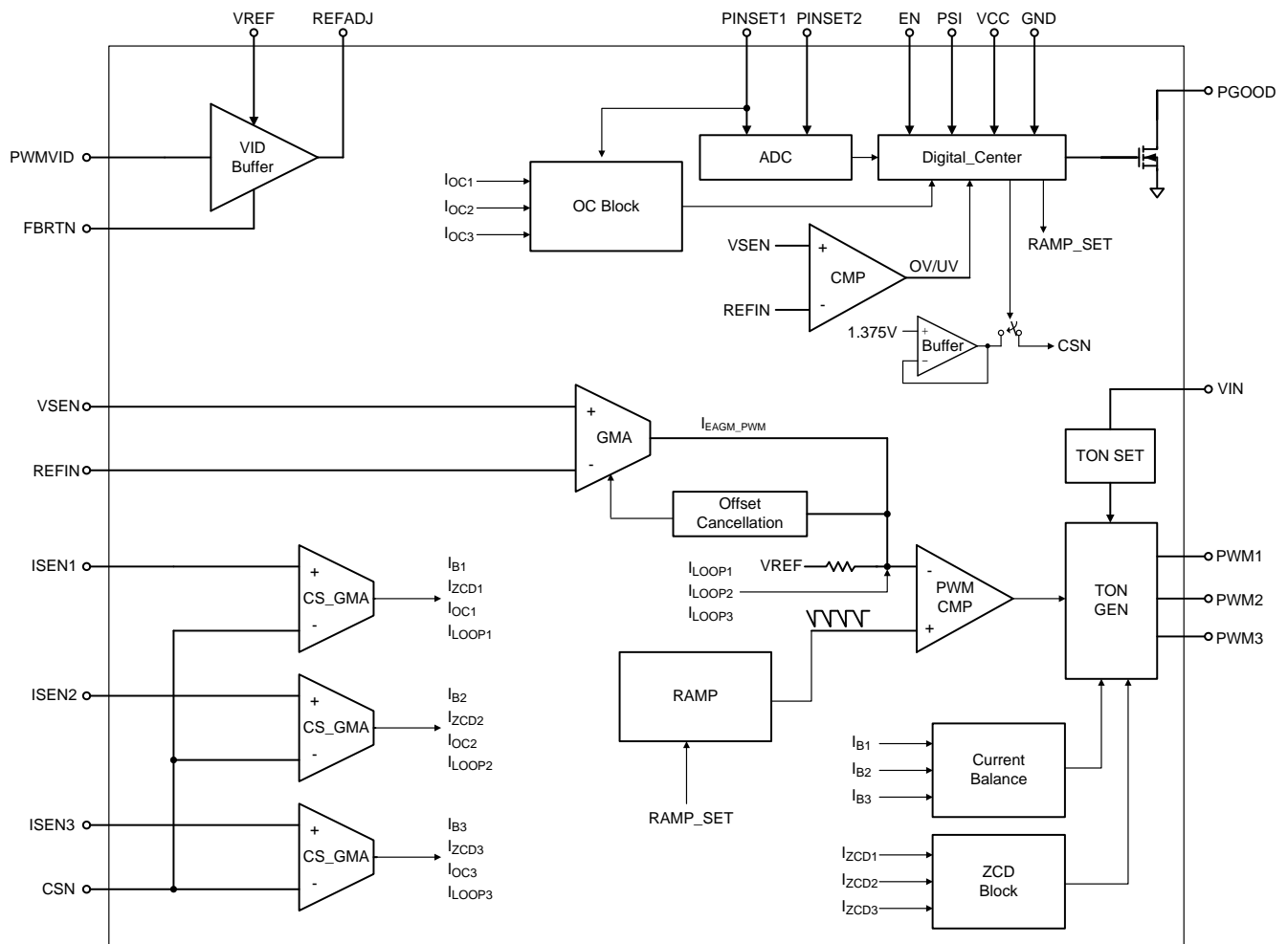


WQFN-20L 3x3

Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|------------------|-----------|--|
| 1 | PGOOD | Power good indicator output. Active high open-drain output. A 10k pull high resistor is needed. |
| 2 | EN | Enable control input. Active high input. |
| 3 | PSI | Controller power state setting input. H: full phase CCM. MID: full phase DEM. L: 1 phase DEM |
| 4 | PWMVID | Programming output voltage control input. Refer to PWM-VID dynamic voltage control. |
| 5 | REFADJ | Reference adjustment output. Refer to PWM-VID dynamic voltage control. |
| 6 | REFIN | External reference input |
| 7 | VREF | Reference voltage output. This is a high precision voltage reference (2V) from the VREF pin to FBRTN pin. |
| 8 | VIN | Connecting a R _{TON} resistor from this pin to input voltage to set frequency. This pin can't place a decoupling capacitor. |
| 9 | FBRTN | Return ground. This pin is the negative input of output voltage differential remote sense. |
| 10 | VSEN | Voltage sense input. This pin is connected to the terminal of output voltage. |
| 11 | PINSET1 | Soft-start, internal ramp, and OCSET setting input. This pin can't place a decoupling capacitor. |
| 12 | PINSET2 | DrMOS IMON function, Auto-ZCD function, and Internal compensation setting input. This pin can't place a decoupling capacitor. |
| 13 | CSN | Output 1.36V when enable DrMOS IMON function. |
| 14, 15, 16 | ISEN[3:1] | Current sense inputs of phase1, 2 and 3. |
| 17 | VCC | Supply voltage input. Connect this pin to a 5V bias supply. Place a high quality bypass capacitor from this pin to GND. |
| 18, 19, 20 | PWM[3:1] | PWM outputs. |
| 21 (Exposed Pad) | GND | Ground. The Exposed pad should be soldered to a large PCB and connected to GND for maximum thermal dissipation. |

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- VIN to GND ----- -0.3 to 28V
- VCC to GND ----- -0.3 to 6V
- FBRTN to GND ----- -0.3 to 0.3V
- Other Pins ----- -0.3 to 6V
- Power Dissipation, PD @ TA = 25°C
WQFN-20L 3x3----- 2.67W
- Package Thermal Resistance (Note 2)
WQFN-20L 3x3, θ_{JA} ----- 30°C/W
WQFN-20L 3x3, θ_{JC} ----- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range----- -65°C to 150°C
- ESD Susceptibility (Note 3)
HBM ----- 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage, VIN ----- 2.7 to 25V
- Supply Voltage, VVCC ----- 4.5 to 5.5V
- Junction Temperature Range----- -40°C to 125°C

Electrical Characteristics

(VVCC = 5V, typical values are referenced to TA = TJ = 25°C, Min and Max values are referenced to TA = TJ from -10°C to 105°C, unless other noted.)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---------------------------------|-----------|--------------------------|------|-------|------|------|
| PWM Controller | | | | | | |
| VCC Supply Voltage | VVCC | | 4.5 | 5 | 5.5 | V |
| VCC Supply Current | IVCC | EN = high, not switching | -- | 6 | -- | mA |
| VCC Shutdown Current | ISHDN | EN = 0V | -- | -- | 10 | μA |
| VCC POR Threshold | | VCC rising voltage | -- | 4.3 | -- | V |
| VCC UVLO Threshold | | VCC falling voltage | -- | 4.1 | -- | V |
| POR Hysteresis | | | -- | 200 | -- | mV |
| Reference Voltage | | | | | | |
| Reference Voltage | VREF | | 1.98 | 2 | 2.02 | V |
| CSN Output Voltage | VCSN_OUT | | 1.3 | 1.375 | 1.45 | V |
| PWMVID Input Voltage | | | | | | |
| PWMVID Input Voltage Logic-High | VPWMVID_H | | 1.2 | -- | -- | V |
| PWMVID Input Voltage Logic-Low | VPWMVID_L | | -- | -- | 0.6 | V |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|----------|--|-------|-----|-------|--------------|
| Soft-Start | | | | | | |
| Soft-Start Ramp Up Slew Rate | | Slew rate set to 1mV/ μ s | 0.9 | 1 | 1.1 | mV/ μ s |
| PGOOD Blanking Time | tPGOOD | From EN go high to PGOOD go high | -- | -- | 2 | ms |
| EN and Logic Input | | | | | | |
| EN Threshold | VEN_H | | 0.7 | -- | -- | V |
| | VEN_L | | -- | -- | 0.3 | |
| Leakage Current of EN, PGOOD, PSI | | | -1 | -- | 1 | μ A |
| PSI Input Voltage | | | | | | |
| PSI Logic High Threshold | VPSI_IH | | 1.6 | -- | -- | V |
| PSI Logic Tri-State Threshold | VPSI_HIZ | | 0.8 | -- | 1.2 | V |
| PSI Logic Low Threshold | VPSI_IL | | -- | -- | 0.4 | V |
| TON Setting | | | | | | |
| ON-Time Setting | ton | ITON = 40 μ A, VREFIN = 1V | 190 | 210 | 230 | ns |
| IPINSET | | | | | | |
| PIN SET Current | IPINSET | VPINSET = 1V | 79.2 | 80 | 80.8 | μ A |
| EA/GM Amplifier | | | | | | |
| Input Offset | VEAOFS | | -3 | -- | 3 | mV |
| CS Amplifier | | | | | | |
| Input Offset | VEAOFS | | -0.6 | -- | 0.6 | mV |
| Protection Function | | | | | | |
| Relative Over Voltage Protection Threshold | VROVP | VREFIN \geq 1.33V | 142.5 | 150 | 157.5 | % |
| Absolute Over-Voltage Protection Threshold | VABOVP | VREFIN < 1.33V, | 1.9 | 2 | 2.1 | V |
| OV Fault Delay | | FB forced above OV threshold | -- | 5 | -- | μ s |
| Relative Under Voltage Protection Threshold | VRUVP | | 35 | 40 | 45 | % |
| UV Fault Delay | | FB forced above UV threshold | -- | 3 | -- | μ s |
| Thermal Shutdown Threshold | TSD | | -- | 150 | -- | $^{\circ}$ C |
| Per Phase OC Current | VOCp | VOCSET = 800mV, ISNEX – CSN, for DCR DRMos Application | 21 | 25 | 29 | mV |
| | | VOCSET = 800mV, ISENx – CSN, for SPS DRMos Application | 70 | 77 | 84 | mV |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|-------------------------------|----------|--------------------|-----|------|-----|----------|
| PWM Driving Capability | | | | | | |
| PWM Source Resistance | RPWM_SRC | | -- | 30 | -- | Ω |
| PWM Sink Resistance | RPWM_SNK | | -- | 10 | -- | Ω |
| PWM Tri-state Voltage | VPWM_Tri | VCC = 5 V (Note 5) | 1.4 | 1.65 | 1.9 | V |

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at $T_A = 25^\circ\text{C}$ with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Pull PWM to HIZ voltage 200ns when PWM enter HIZ.

Typical Application Circuit

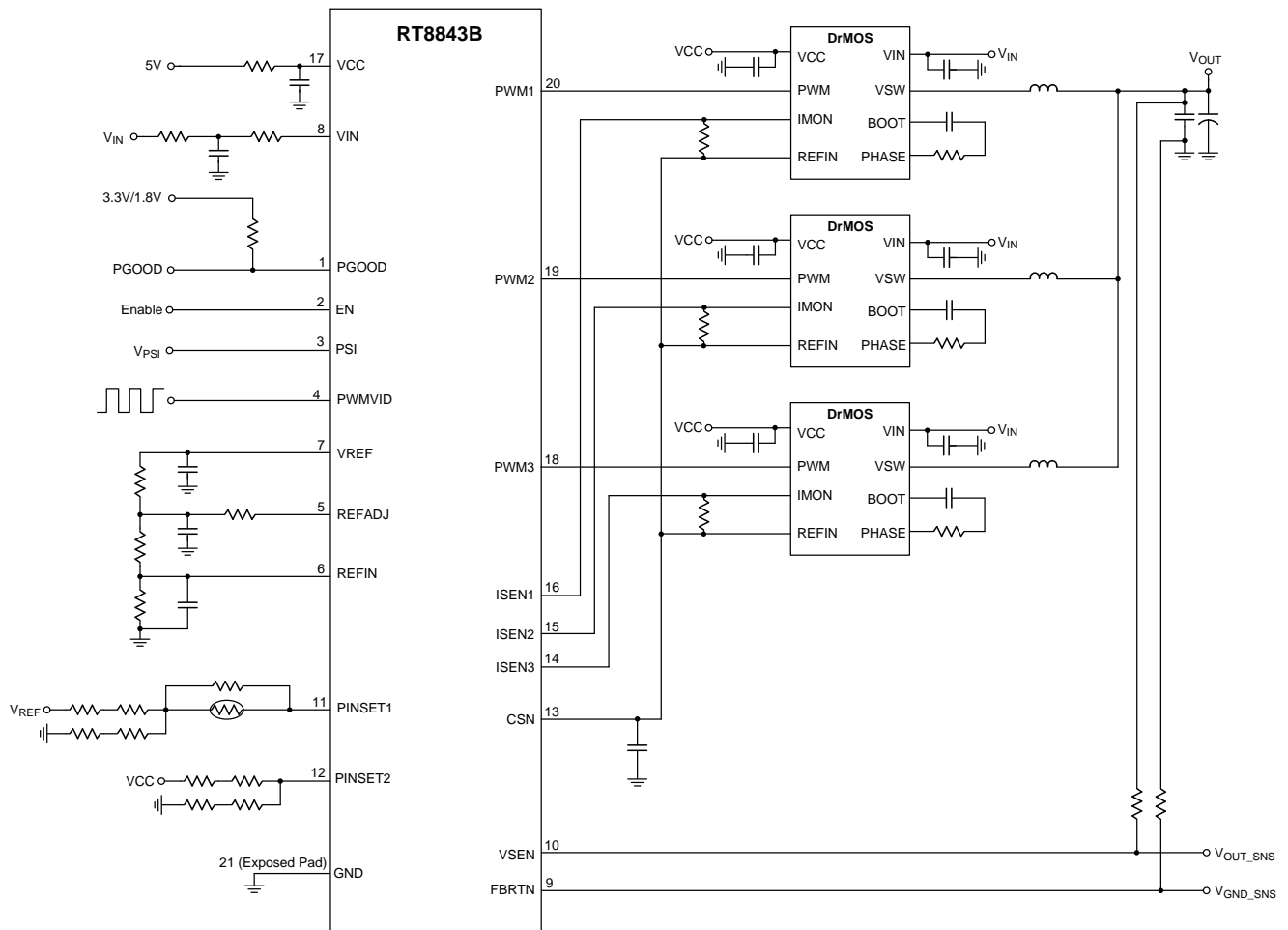


Figure 1. 3 Active Phase IMON Configuration

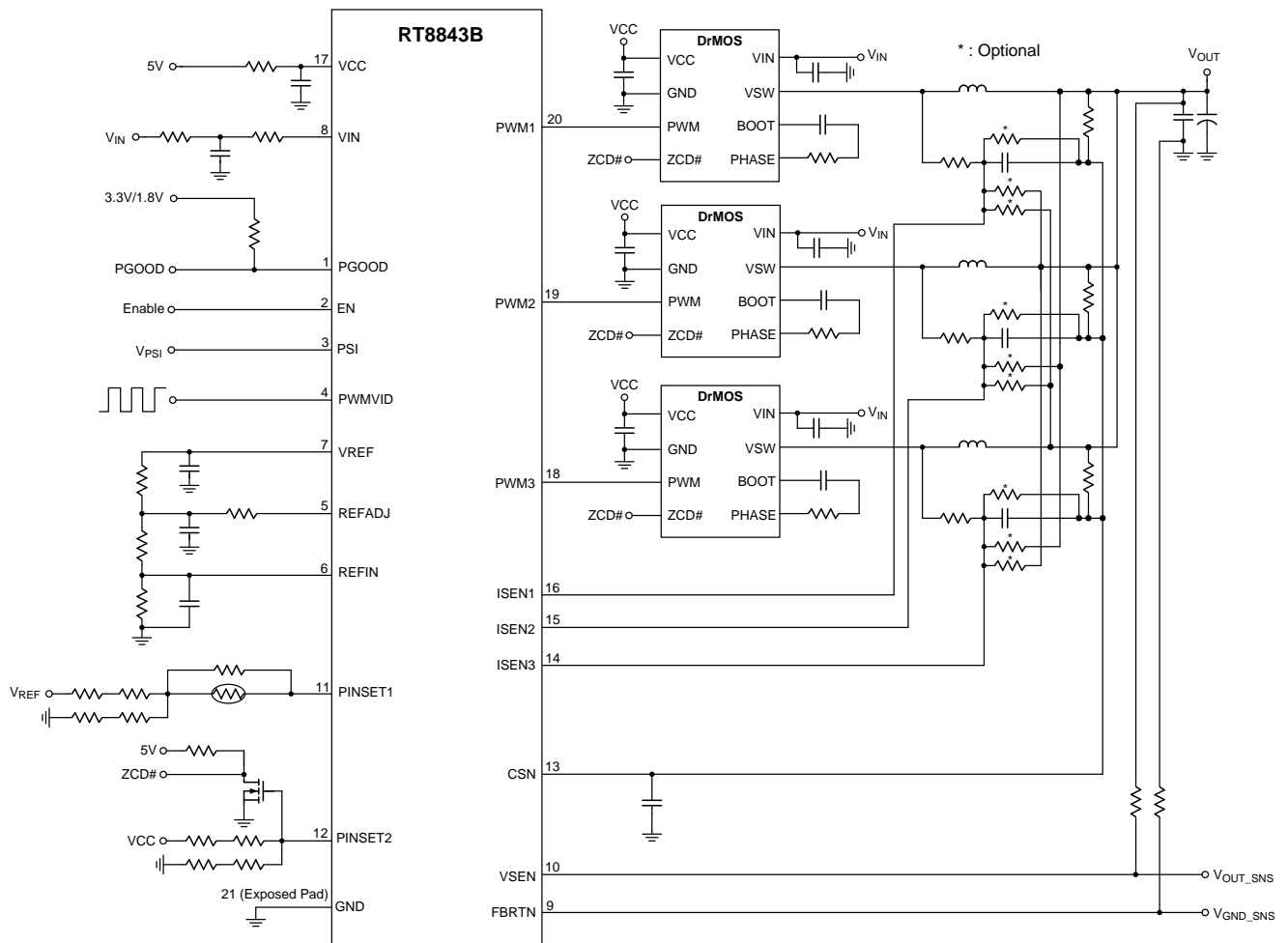
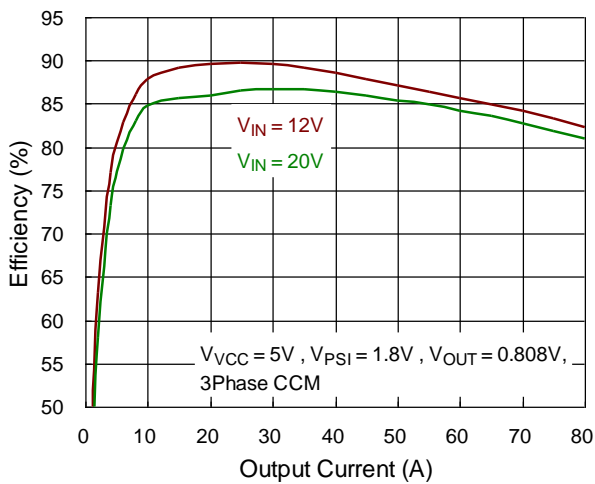


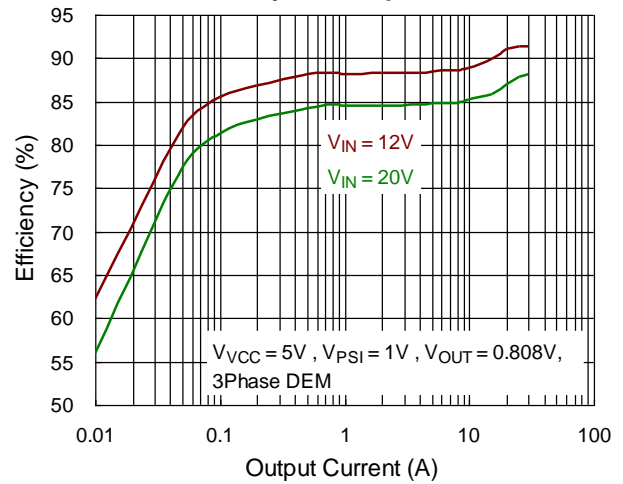
Figure 2. 3 Active Phase DCR Configuration

Typical Operating Characteristics

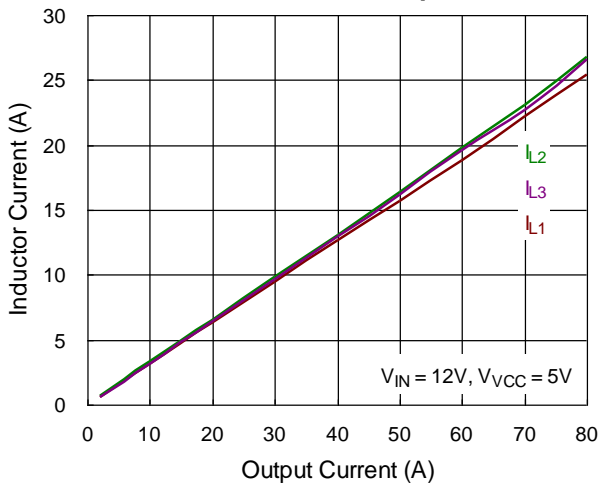
Efficiency vs. Output Current



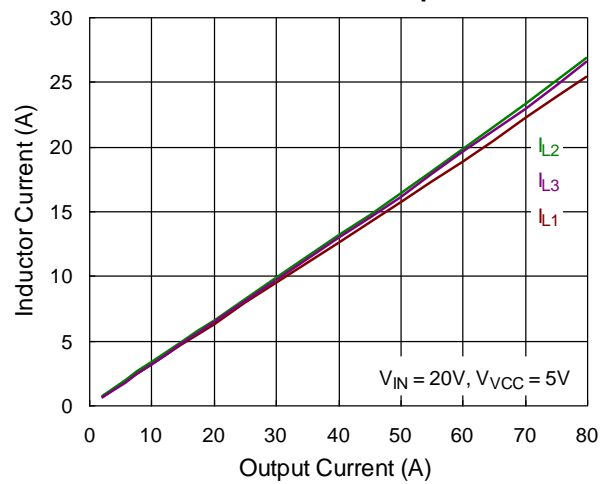
Efficiency vs. Output Current



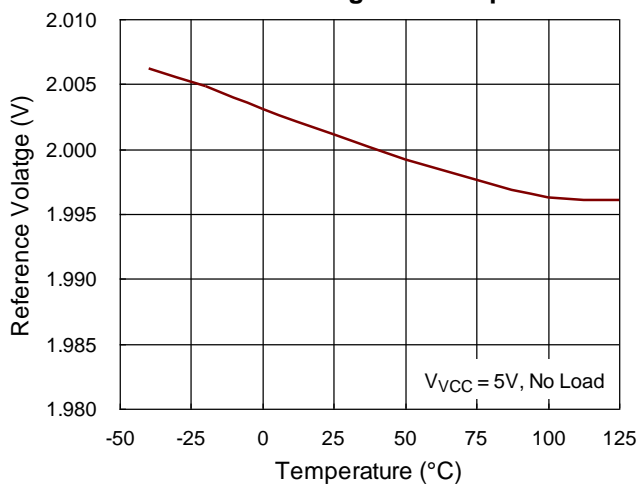
Inductor Current vs. Output Current



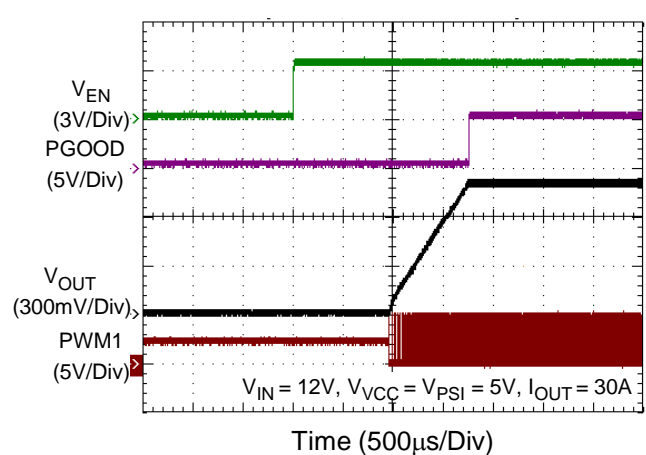
Inductor Current vs. Output Current



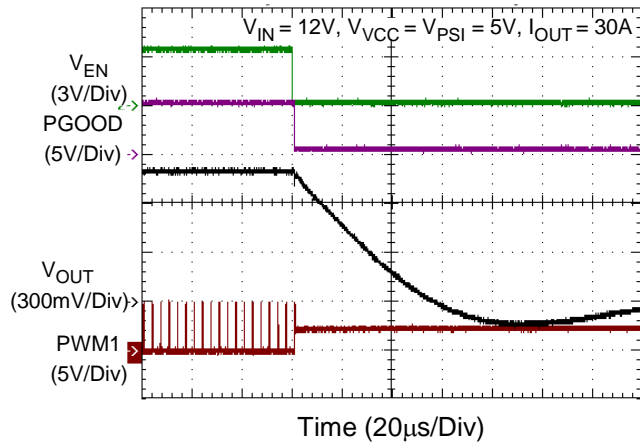
Reference Voltage vs. Temperature



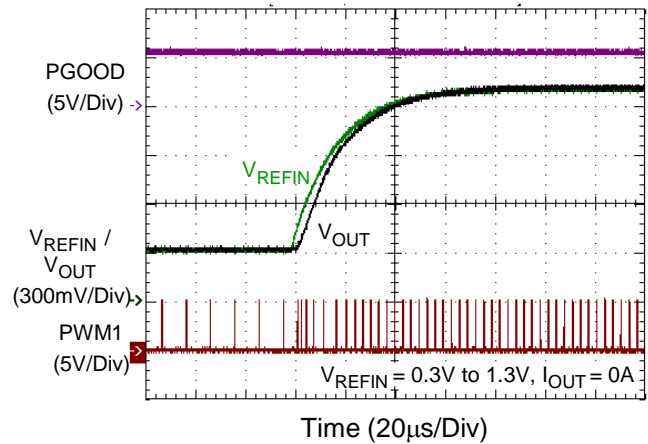
Power On from EN



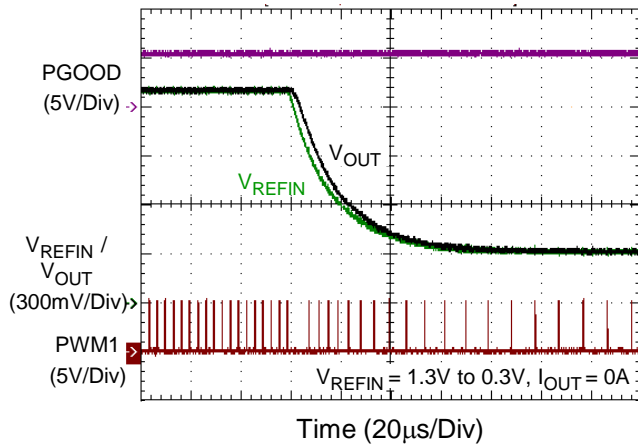
Power Off from EN



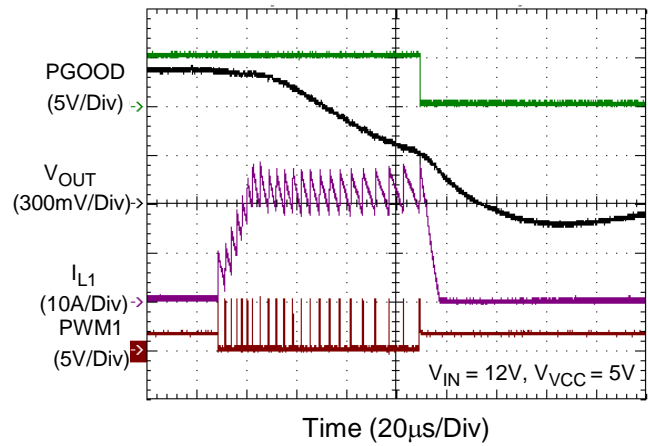
Dynamic Output Voltage Control



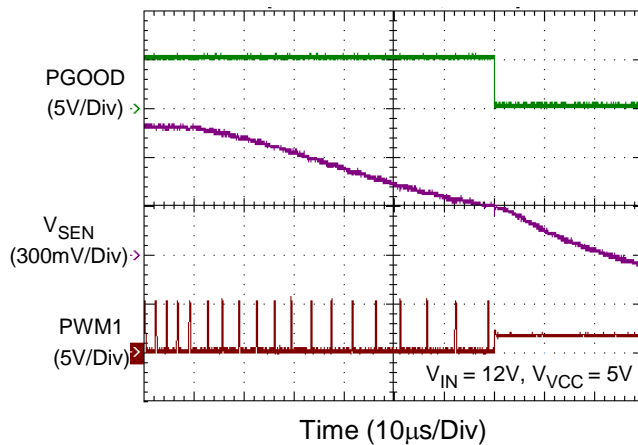
Dynamic Output Voltage Control



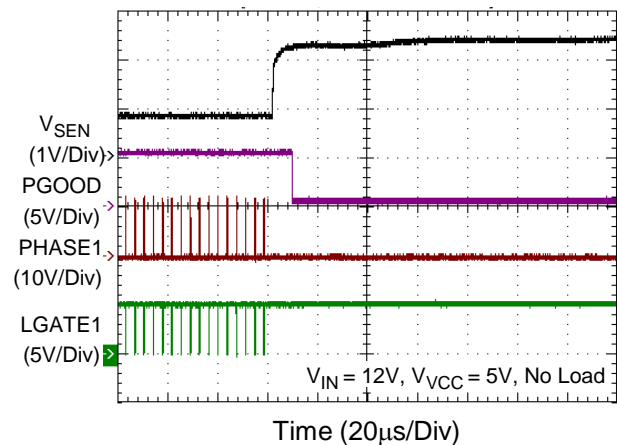
Per Phase Current Limit



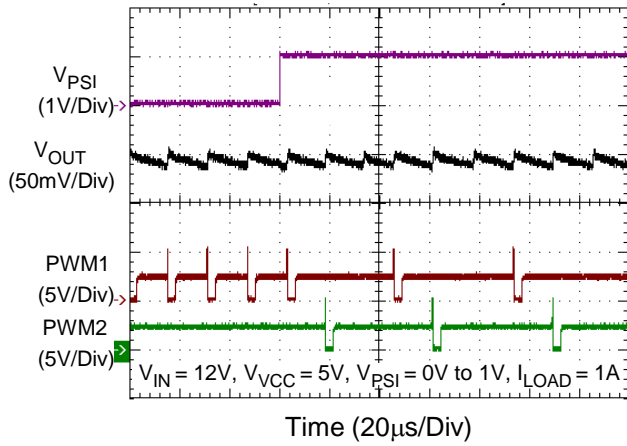
UVP



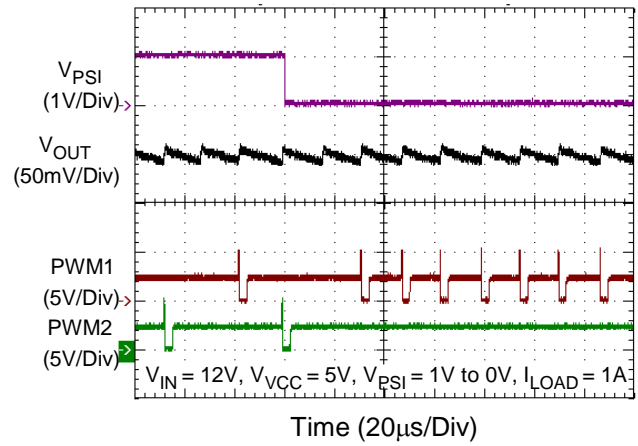
OVP



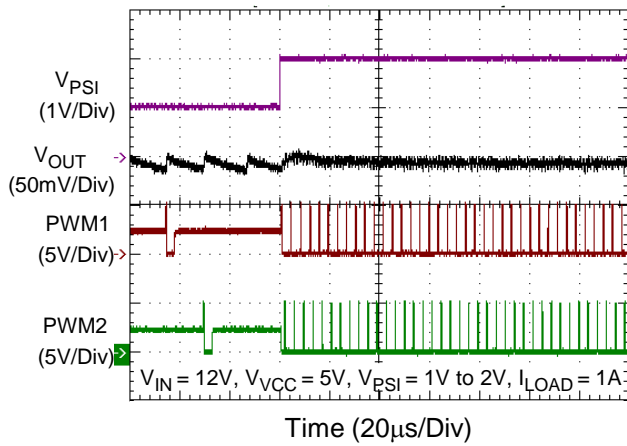
Mode Transition



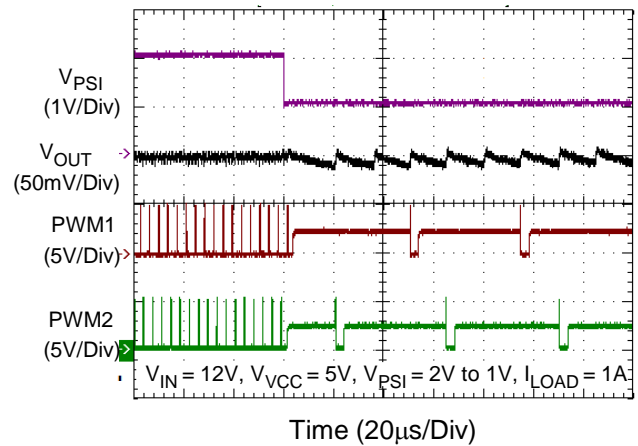
Mode Transition



Mode Transition



Mode Transition



Application Information

The RT8843B is a three-phase synchronous Buck controller which is optimized for high performance graphic microprocessor and computer applications.

The RT8843B adopts AC G-NAVP™ (Green Native Adaptive Voltage Positioning) which is Richtek's proprietary topology derived from finite DC gain of internal GM amplifier with current mode control. By utilizing the AC G-NAVP™ topology, the operating frequency of the RT8843B varies with VID, load and input voltage to further enhance the efficiency even in CCM. Moreover, the AC G-NAVP™ with CCRCOT (Constant Current Ripple COT) technology provides superior output voltage ripple over the entire input/output range.

The RT8843B features external reference input and PWM-VID dynamic output voltage control, in which the output voltage is regulated by tracking external input reference voltage. In addition, the RT8843B integrates multiple functions including Internal-Ramp-Setting, AI Gain Selection, Soft-Start Time Setting, SPS Current Sensing, Auto-Zero-Current Detection, and Over-Current Limiting. These functions can be achieved through PINSET voltage setting. The RT8843B also provides comprehensive protection, not only Over-Current Limiting (OCL), but also Over-Voltage Protection (OVP), Under-Voltage Protection (UVP) and Over-Temperature Protection (OTP).

Power On Reset (POR), UVLO

Power On Reset (POR) occurs as VVCC rising above to approximately 4.3V (typical), and the RT8843B resets the fault latch circuit and prepares for PWM operation.

When the VVCC is lower than 4.1V (typical), PWMx signal is kept low to inhibit any switching through Under Voltage Lockout (UVLO).

Enable and Disable

The EN pin is a high impedance input that allows power sequencing between the controller bias voltage and another voltage rail. The RT8843B remains in shutdown if the EN pin is lower than 300mV. When the

EN voltage rises above the 700mV high level threshold, the RT8843B begins a new initialization and soft-start cycle. EN timing must be later than VCC POR in order to ensure that the PINSET function can be set normally.

Power Good Indicator (PGOOD)

The PGOOD pin is an open-drain output, and requires a pull-up resistor. During soft-start time period, the PGOOD remains low. When the output voltage reach to REFIN voltage, PGOOD is pulled high and latched. If OVP/UVP is triggered or EN goes low during operation, the PGOOD will be pulled low immediately.

Operation Mode Setting

The RT8843B provides three operation modes, 1Phase with DEM, multi-Phase with DEM and multi-Phase with CCM. In DEM operation, the RT8843B automatically reduces the operation frequency at light load conditions for saving power loss. The operating mode can be set by the voltage of the PSI pin as listed in Table 1. Moreover, the PSI pin is valid after POR of VR.

Table 1.

| Operation Mode | PSI Voltage Setting |
|------------------------|---------------------|
| 1Phase with DEM | 0V to 0.4V |
| Multi-Phase with DEM*1 | 0.8V to 1.2V |
| Multi-Phase with CCM*1 | 1.6V to 5.5V |

*1: multi-phase number by hardware setting

PWM VID and Dynamic Output Voltage Control

The RT8843B features a PWM VID input for dynamic output voltage control as shown in Figure 3, which reduces the number of device pin and enables a wide dynamic voltage range. The output voltage is determined by the applied voltage on the REFIN pin and duty cycle of PWMVID.

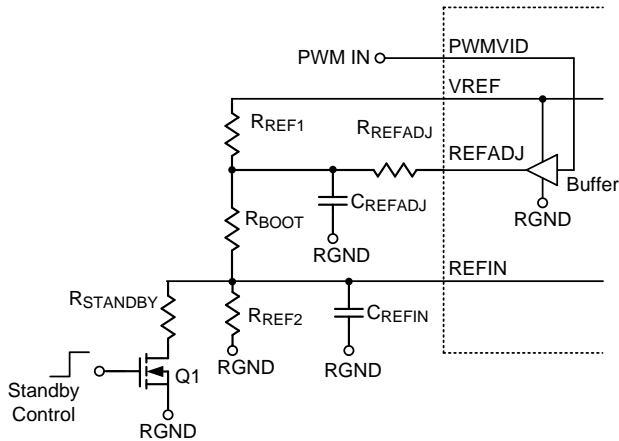


Figure 3. PWM VID Analog Circuit Diagram

Through utilizing the external circuit and VID control signal, the controller provides three operation modes as shown in Figure 4.

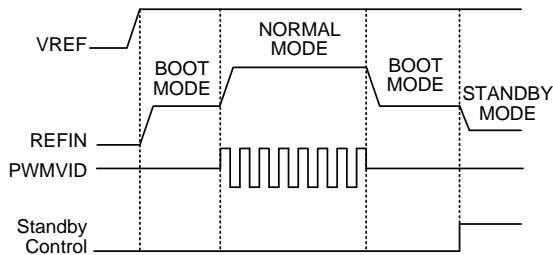


Figure 4. PWM VID Time Diagram

BOOT Mode

When the PWMVID is not driven, the buffer output is in tri-stated. At this time, PWM-VID circuit is working in BOOT mode and Q1 is turned off. Further, REFIN is connected to a resistor divider as shown in Figure 3. The following equation expresses VBOOT equation from REFIN and divider resistors.

$$V_{BOOT} = V_{VREF} \times \left(\frac{R_{REF2}}{R_{REF1} + R_{REF2} + R_{BOOT}} \right)$$

where $V_{VREF} = 2V$ (typ.)

Choose R_{REF2} to be approximately $10k\Omega$, and the R_{REF1} and R_{BOOT} can be calculated by the following equations :

$$R_{REF1} + R_{BOOT} = \frac{R_{REF2} \times (V_{VREF} - V_{BOOT})}{V_{BOOT}}$$

$$R_{REF1} = \frac{R_{REF2} \times (V_{VREF} - V_{BOOT})}{V_{BOOT}} - R_{BOOT}$$

$$R_{BOOT} = \frac{R_{REF2} \times (V_{VREF} - V_{BOOT})}{V_{BOOT}} - R_{REF1}$$

Standby Mode

When the PWMVID control is to enter the standby mode, the standby voltage can be set via $R_{STANDBY}$ and Q1 as shown in Figure 3. The standby voltage is set by a voltage that is lower than the PWMVID operating range. Assuming the PWMVID operating range is $0.3V$ to $1.3V$, then the standby voltage will be set below than $0.3V$. However, as the REFIN voltage is lower than $0.2V$, the controller will pull the PWM into tri-state. Therefore, the standby voltage setting range is recommended from $0.2V$ to the lowest voltage of PWMVID operation voltage.

The following conditions must be met when entering standby mode. 1. PWMVID pin is floating, 2. Q1 is enabled. Further, the desired value can be set by the following equation :

$$V_{STANDBY} = V_{VREF} \times \frac{R_{REF2} // R_{STANDBY}}{R_{REF1} + R_{BOOT} + (R_{REF2} // R_{STANDBY})}$$

By choosing R_{REF1} , R_{REF2} , and R_{BOOT} , the $R_{STANDBY}$ can be calculated by the following equation :

$$R_{STANDBY} =$$

$$\frac{V_{STANDBY} \times R_{REF2} \times (R_{REF1} + R_{BOOT})}{V_{VREF} \times R_{REF2} - V_{STANDBY} \times (R_{REF1} + R_{REF2} + R_{BOOT})}$$

Normal Mode

If the PWMVID pin is driven by a PWM signal and switch Q1 is disabled as shown in Figure 3. The V_{REFIN} can be adjusted from V_{min} to V_{max} , where V_{min} is the voltage at zero percent PWM duty cycle and V_{max} is the voltage at one hundred percent PWM duty cycle. The V_{min} and V_{max} can be set by the following equations :

$$V_{min} = V_{VREF} \times \frac{R_{REF2}}{R_{REF2} + R_{BOOT}} \times \frac{R_{REFADJ} // (R_{BOOT} + R_{REF2})}{R_{REF1} + [(R_{REFADJ} // (R_{BOOT} + R_{REF2}))]}$$

$$V_{max} = V_{VREF} \times \frac{R_{REF2}}{(R_{REF1} // R_{REFADJ}) + R_{BOOT} + R_{REF2}}$$

By choosing R_{REF1} , R_{REF2} , and R_{BOOT} , the R_{REFADJ} can be calculated by the following equation :

$$R_{REFADJ} = \frac{R_{REF1} \times V_{min}}{V_{max} - V_{min}}$$

The relationship between PWMVID duty and V_{REFIN} is shown in Figure 5, and V_{OUT} can be set according to the following equation.

$$V_{OUT} = V_{min} + N \times V_{STEP}$$

where the V_{STEP} is the resolution of each voltage step :

$$V_{STEP} = \frac{V_{max} - V_{min}}{N_{max}}$$

where N_{max} is the number of total available voltage steps and N is the number of step at a specific V_{OUT} . The dynamic voltage VID period ($T_{vid} = T_u \times N_{max}$) is determined by the unit pulse width (T_u), and the available step number (N_{max}). The recommended T_u is 27ns.

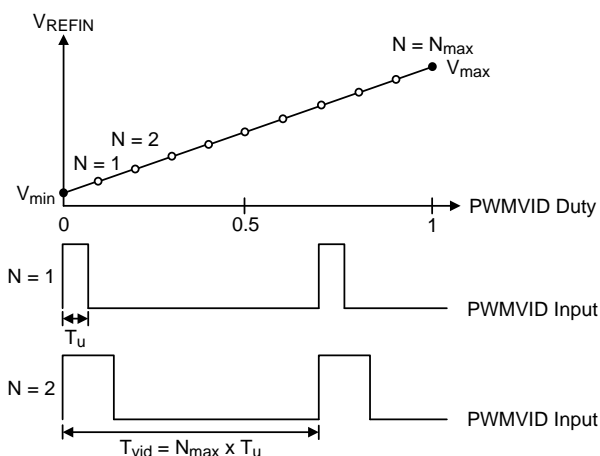


Figure 5. PWM VID Analog Output

VID Slew Rate Control

In the RT8843B, the V_{REFIN} slew rate is proportional to PWM VID duty and, the rising time and falling time are the same. In normal mode, the V_{REFIN} slew rate SR can be estimated by C_{REFADJ} as expressed in the following equation :

$$SR = \frac{(V_{REFIN_Final} - V_{REFIN_Initial}) \times 80\%}{2.2 \times R_{SR} \times C_{REFADJ}}$$

$$R_{SR} = [(R_{REF1} // R_{REFADJ})] // (R_{BOOT} + R_{REF2})$$

Remote Sense Setting

In order to allow the load voltage to be accurately detected to avoid the voltage drop from output to load, the RT8843B uses a high-accuracy differential amplifier to directly detect the voltage at the end of GPU through the V_{SEN} and $FBRTN$ pins. The V_{OUT} sensing network from controller to the load and output needs to be specially designed according to different load conditions. The output voltage detection circuit has two loops, the remote sense path (from the controller to the load end of GPU) and the local sense path (from the controller to the output capacitor) as shown in Figure 6. When the load is GPU, in order to make the GPU voltage consistent with V_{REFIN} , the R_{Remote} must be set to 0Ω . At this time, the purpose of local sense path is to avoid the output overvoltage caused by the GPU open. Therefore, the R_{Local} must be placed a 10Ω to 100Ω resistor. If the GPU is not used and load from the end of V_{OUT} , the R_{Local} must be set to 0Ω to avoid PWM jitter caused by delayed output voltage signal. Considering the components placement, it is recommended to place all the detecting resistors on the controller side. This setting can minimizes the path of local sense, and make the system debug easier as any noise coupling occurring on the sensing path.

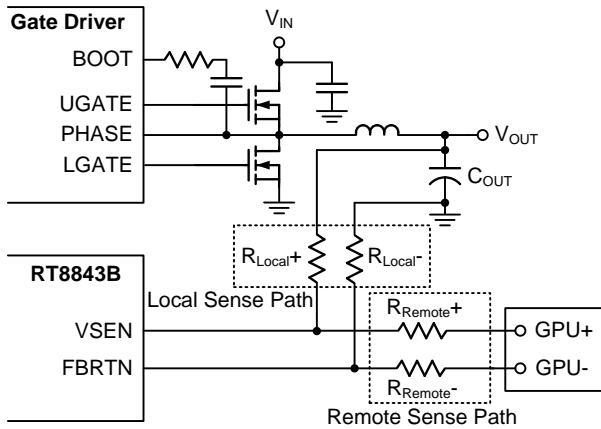


Figure 6. Output Voltage Sensing

Multi-Function Pin Setting

For reducing total pin number of package, PINSET1 and PINSET2 pins adopt the multi-function pin setting mechanism in the RT8843B. Table 2 summarizes the overall pin setting function. Figure 7 shows the Pin Setting Circuit. The voltage divider of each PINSET pin is used to set desired function. The setting voltage of each PINSET pin can be represented as

$$V_{PINSET1} = V_{REF}(2V) \times \frac{R3 + R4}{R1 + R2 + R3 + R4}$$

$$V_{PINSET2_V} = V_{VCC}(5V) \times \frac{R3 + R4}{R1 + R2 + R3 + R4}$$

$$V_{PINSET2_I} = 80\mu \times \frac{(R1 + R2) \times (R3 + R4)}{R1 + R2 + R3 + R4}$$

Table 3, Table 4 and Table 5 show the pin setting function table. The ramp example for a typical 300kHz application is also shown on Table 6.

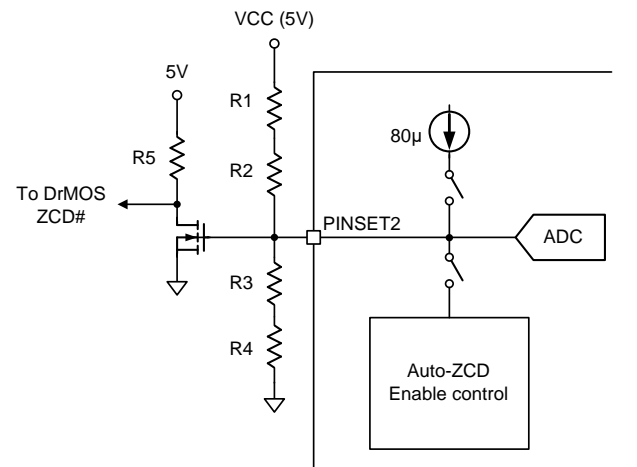
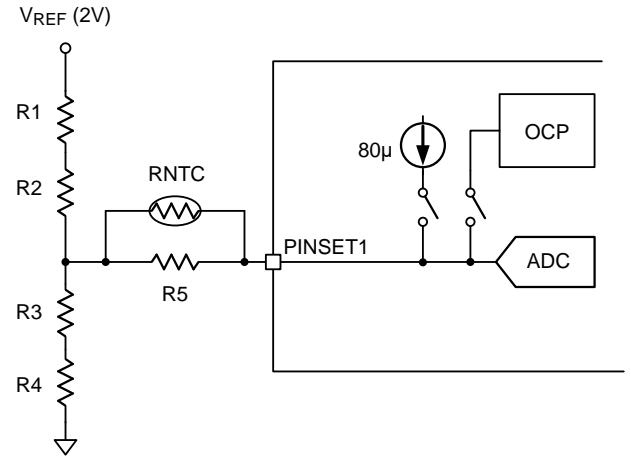


Figure 7. Multi-Function Pin Setting Circuit

Table 2. Pin Set Table

| | Function1 | Function2 | Function2 | Function3 | Function4 |
|---------|----------------------|----------------------|---------------------------|----------------------------|-----------|
| PINSET1 | Soft-Start Slew Rate | Ramp Amplitude <2:0> | N/A | N/A | N/A |
| PINSET2 | Ramp Valley | Ramp Amplitude <3> | Dr.IMON Enable/Disable | Auto-ZCD Enable/Disable | AI Gain |

Table 3. PINSET1 Pin Setting for Soft-Start Slew Rate and Ramp Amplitude

| SS Slew Rate (mV/μs) | RAMP Amplitude <2:0> (mV) $V_{\text{RAMP_AMP}} = \frac{30000 \times (16 - \text{RAMP} \langle 3:0 \rangle)}{f_s}$ | | | $V_{\text{PINSET1}} = V_{\text{REF}}(2V) \times \frac{R3 + R4}{R1 + R2 + R3 + R4}$ | | | |
|-------------------------|---|---|---|--|---------|---------|------|
| | | | | Min | Typ | Max | Unit |
| 1 | 0 | 0 | 0 | 0 | 15.625 | 18.125 | mV |
| | 0 | 0 | 1 | 44.375 | 46.875 | 49.375 | mV |
| | 0 | 1 | 0 | 75.625 | 78.125 | 80.625 | mV |
| | 0 | 1 | 1 | 106.875 | 109.375 | 111.875 | mV |
| | 1 | 0 | 0 | 138.125 | 140.625 | 143.125 | mV |
| | 1 | 0 | 1 | 169.375 | 171.875 | 174.375 | mV |
| | 1 | 1 | 0 | 200.625 | 203.125 | 205.625 | mV |
| | 1 | 1 | 1 | 231.875 | 234.375 | 236.875 | mV |
| 2 | 0 | 0 | 0 | 263.125 | 265.625 | 268.125 | mV |
| | 0 | 0 | 1 | 294.375 | 296.875 | 299.375 | mV |
| | 0 | 1 | 0 | 325.625 | 328.125 | 330.625 | mV |
| | 0 | 1 | 1 | 356.875 | 359.375 | 361.875 | mV |
| | 1 | 0 | 0 | 388.125 | 390.625 | 393.125 | mV |
| | 1 | 0 | 1 | 419.375 | 421.875 | 424.375 | mV |
| | 1 | 1 | 0 | 450.625 | 453.125 | 455.625 | mV |
| | 1 | 1 | 1 | 481.875 | 484.375 | 486.875 | mV |
| 6 | 0 | 0 | 0 | 513.125 | 515.625 | 518.125 | mV |
| | 0 | 0 | 1 | 544.375 | 546.875 | 549.375 | mV |
| | 0 | 1 | 0 | 575.625 | 578.125 | 580.625 | mV |
| | 0 | 1 | 1 | 606.875 | 609.375 | 611.875 | mV |
| | 1 | 0 | 0 | 638.125 | 640.625 | 643.125 | mV |
| | 1 | 0 | 1 | 669.375 | 671.875 | 674.375 | mV |
| | 1 | 1 | 0 | 700.625 | 703.125 | 705.625 | mV |
| | 1 | 1 | 1 | 731.875 | 734.375 | 736.875 | mV |

Table 4. PINSET2_V Pin Setting for Ramp Amplitude and Ramp Valley

| RAMP Valley (mV) | RAMP Amplitude <3> (mV) $V_{\text{RAMP_AMP}} = \frac{30000 \times (16 - \text{RAMP} \langle 3:0 \rangle)}{f_s}$ | $V_{\text{PINSET2_V}} = V_{\text{VCC}}(5V) \times \frac{R3 + R4}{R1 + R2 + R3 + R4}$ | | | |
|------------------|---|---|------|--------|------|
| | | Min | Typ | Max | Unit |
| 100 | 0 | 0 | 25 | 27.5 | mV |
| 100 | 1 | 72.5 | 75 | 77.5 | mV |
| 150 | 0 | 122.5 | 125 | 127.5 | mV |
| 150 | 1 | 172.5 | 175 | 177.5 | mV |
| 200 | 0 | 222.5 | 225 | 227.5 | mV |
| 200 | 1 | 272.5 | 275 | 277.5 | mV |
| 250 | 0 | 322.5 | 325 | 327.5 | mV |
| 250 | 1 | 372.5 | 375 | 377.5 | mV |
| 300 | 0 | 422.5 | 425 | 427.5 | mV |
| 300 | 1 | 472.5 | 475 | 477.5 | mV |
| 350 | 0 | 522.5 | 525 | 527.5 | mV |
| 350 | 1 | 572.5 | 575 | 577.5 | mV |
| 400 | 0 | 622.5 | 625 | 627.5 | mV |
| 400 | 1 | 672.5 | 675 | 677.5 | mV |
| 450 | 0 | 722.5 | 725 | 727.5 | mV |
| 450 | 1 | 772.5 | 775 | 777.5 | mV |
| 500 | 0 | 822.5 | 825 | 827.5 | mV |
| 500 | 1 | 872.5 | 875 | 877.5 | mV |
| 550 | 0 | 922.5 | 925 | 927.5 | mV |
| 550 | 1 | 972.5 | 975 | 977.5 | mV |
| 600 | 0 | 1022.5 | 1025 | 1027.5 | mV |
| 600 | 1 | 1072.5 | 1075 | 1077.5 | mV |
| 650 | 0 | 1122.5 | 1125 | 1127.5 | mV |
| 650 | 1 | 1172.5 | 1175 | 1177.5 | mV |
| 700 | 0 | 1222.5 | 1225 | 1227.5 | mV |
| 700 | 1 | 1272.5 | 1275 | 1277.5 | mV |
| 750 | 0 | 1322.5 | 1325 | 1327.5 | mV |
| 750 | 1 | 1372.5 | 1375 | 1377.5 | mV |
| 800 | 0 | 1422.5 | 1425 | 1427.5 | mV |
| 800 | 1 | 1472.5 | 1475 | 1477.5 | mV |
| 850 | 0 | 1522.5 | 1525 | 1527.5 | mV |
| 850 | 1 | 1572.5 | 1575 | 1577.5 | mV |

Table 5. PINSET2_I Pin Setting for Enable Dr.IMON, Enable Auto-ZCD and AI Gain Selection

| Dr.IMON | Auto_ZCD# | AI Gain | $V_{PINSET2_I} = 80\mu \times \frac{(R1 + R2) \times (R3 + R4)}{R1 + R2 + R3 + R4}$ | | | |
|---------|-----------|---------|--|------|------|------|
| | | | Min | Typ | Max | Unit |
| Disable | Disable | Disable | 0 | 50 | 55 | mV |
| | | 1X | 145 | 150 | 155 | mV |
| | | 2X | 245 | 250 | 255 | mV |
| | | 4X | 345 | 350 | 355 | mV |
| Disable | Enable | Disable | 445 | 450 | 455 | mV |
| | | 1X | 545 | 550 | 555 | mV |
| | | 2X | 645 | 650 | 655 | mV |
| | | 4X | 745 | 750 | 755 | mV |
| Enable | Disable | Disable | 845 | 850 | 855 | mV |
| | | 1X | 945 | 950 | 955 | mV |
| | | 2X | 1045 | 1050 | 1055 | mV |
| | | 4X | 1145 | 1150 | 1155 | mV |
| Enable | Enable | Disable | 1245 | 1250 | 1255 | mV |
| | | 1X | 1345 | 1350 | 1355 | mV |
| | | 2X | 1445 | 1450 | 1455 | mV |
| | | 4X | 1545 | 1550 | 1555 | mV |

Table 6. Ramp Amplitude Example for 300kHz Frequency

| Code <3:0> | | | | | Ramp Amplitude (mV) |
|-------------|---|---|---|-----|---------------------|
| 3 (PINSET2) | 2 | 1 | 0 | DEC | |
| 0 | 0 | 0 | 0 | 0 | 1600 |
| 0 | 0 | 0 | 1 | 1 | 1500 |
| 0 | 0 | 1 | 0 | 2 | 1400 |
| 0 | 0 | 1 | 1 | 3 | 1300 |
| 0 | 1 | 0 | 0 | 4 | 1200 |
| 0 | 1 | 0 | 1 | 5 | 1100 |
| 0 | 1 | 1 | 0 | 6 | 1000 |
| 0 | 1 | 1 | 1 | 7 | 900 |
| 1 | 0 | 0 | 0 | 8 | 800 |
| 1 | 0 | 0 | 1 | 9 | 700 |
| 1 | 0 | 1 | 0 | 10 | 600 |
| 1 | 0 | 1 | 1 | 11 | 500 |
| 1 | 1 | 0 | 0 | 12 | 400 |
| 1 | 1 | 0 | 1 | 13 | 300 |
| 1 | 1 | 1 | 0 | 14 | 200 |
| 1 | 1 | 1 | 1 | 15 | 100 |

Soft-Start

The RT8843B provides the soft-start function that is used to prevent large inrush current and output voltage overshoot while the converter is being powered up. The soft-start sequence as shown in Figure 8. When EN goes high, the RT8843B enters the internal circuit initialization and pinset function setting. The soft start circuit starts after the IC initialization is completed. During soft-start period, the output voltage follows the internal soft-start ramp up. The soft start slew rate has 3 stages that can be adjusted through PINSET1 pin as shown in the Table3. And the soft-start time can be calculated as:

$$T_{SS} = 900\mu s + \frac{V_{OUT}}{SR}$$

where the V_{OUT} is the target output voltage and SR is the soft-start slew rate.

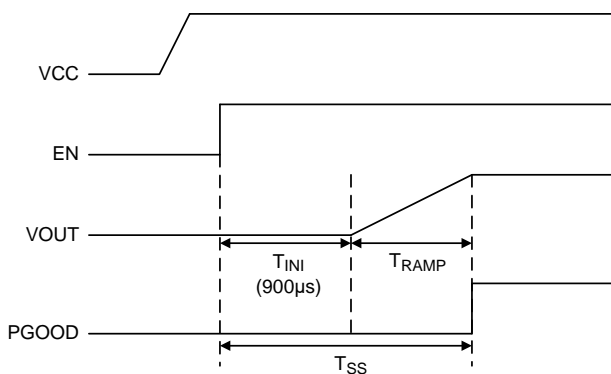


Figure 8. Soft-Start Sequence

Switching Frequency Setting

Connecting a resistor R_{TON} between input terminal and VIN pin to set the on-time width. The R_{TON} can be calculated according to the following formula :

$$R_{TON} = \frac{V_{IN}-0.9}{8.8 \times 10^{-12} \times V_{IN} \times f_s} \quad (V_{OUT} > 0.9V)$$

$$R_{TON} = \frac{V_{OUT}}{V_{IN}} \times \frac{V_{IN}-V_{OUT}}{7.9 \times 10^{-12} \times f_s} \quad (0.9V < V_{OUT} < 0.5V)$$

$$R_{TON} = \frac{V_{OUT}}{V_{IN}} \times \frac{V_{IN}-0.5}{7.9 \times 10^{-12} \times f_s} \quad (V_{OUT} < 0.5V)$$

When load increases, on-time keeps constant. The off-time width will be reduced so that input terminal can provide more power to output to regulate output voltage. Hence the higher load current will result in higher switching frequency.

Higher switching frequency operation can reduce power components' size and PCB space, but the high switching frequency will increase the switching loss, so the frequency setting must be traded off between the component size and overall efficiency.

The recommended frequency setting range is 150kHz to 1.5MHz. And the minimum T_{ON} cannot be less than 70ns, otherwise the frequency will be less than the desired value.

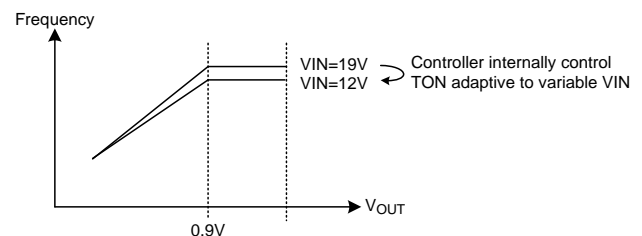


Figure 9. Switching Frequency with Different VOUT

Ramp Setting

The RT8843B provides an internal ramp that effectively suppresses PWM signal jitter in small output ripple applications. The ramp amplitude and valley can be set through PINSET1 and PINSET2 pins as shown in Table 3 and Table 4. The ramp amplitude can be set in total 16 steps. Further, the value according to different switching frequency can be calculated by the following formula:

$$V_{RAMP_AMP} = \frac{30000 \times (16 - RAMP(3:0))}{f_s}$$

Table 6 is an calculation example of a ramp amplitude with a switching frequency of 300kHz. Higher amplitude has better suppression of jitter, but it will reflect poor load transient performance. Therefore, the design of the ramp amplitude need to be traded-off between stability and transient performance. To ensure that the PWM jitter rate is below 15% and load transient response can meet $V_{OUT} -10\% / +20\%$ of system specifications, the default setting of ramp amplitude is recommended to choose approximately 300mV. In

addition, in order to ensure the stability at DEM (the multi-pulse phenomenon does not occur), the ramp valley is recommended to choose 50mV larger than ramp amplitude.

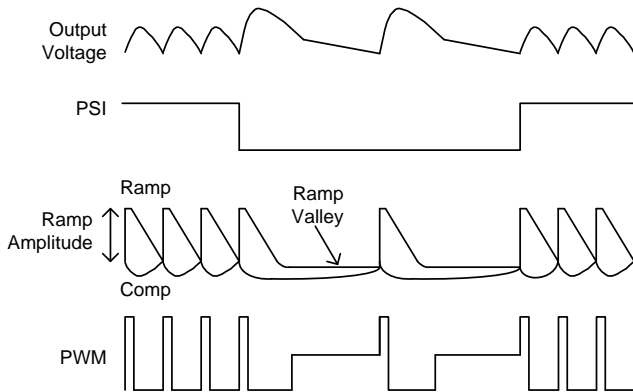


Figure 10. Mode Transition Behavior

Current Sensing

The RT8843B provides per phase current sensing amplifier for different current sensing topology including DCR current sensing and SPS current sensing. This current signal is used for loop control, zero current detection, current balance and per-phase current limit.

DCR Current Sensing

The RT8843B can support inductor DCR current sensing to get each phase current signal, as illustrated in Figure 11. An external low-pass filter R_{X1} and C_X reconstruct the current signal. The low-pass filter time constant $R_{X1} \times C_X$ should match time constant L/DCR of Inductance and DCR. The R_X and C_X can be fine-tuned for transient performance. If RC network time constant is smaller than inductor time constant L/DCR , V_{CS} current signal leads the inductor current signal, and early trigger per-phase current limit during load transient. If RC network time constant is larger than inductor time constant L/DCR , V_{CS} current signal has a sluggish rise and delay trigger per-phase current limit during load transient. If RC network time constant matches inductor time constant L/DCR , the trigger level of per-phase current limit will meet desired value. R_{X1} is highly recommended as two 0603 size resistors in series to enhance the current signal accuracy. X7R type capacitor is suggested for C_X in the application. R_{X2} is optional for preventing V_{CS} exceeding current sense amplifier input range ($-10mV$ to $90mV$). The time constant of $(R_{X1} \parallel R_{X2}) \times C_X$ should be match L/DCR .

The current sense lines must be routed as differential pair from the inductor to the controller on the same layer. When the DCR current sensing circuit is selected, the DrIMON enable/disable of PINSET2 function must be set to Disable.

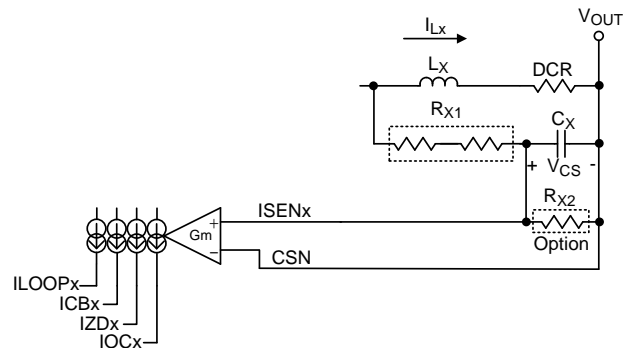


Figure 11. Inductor DCR Current Sensing Method

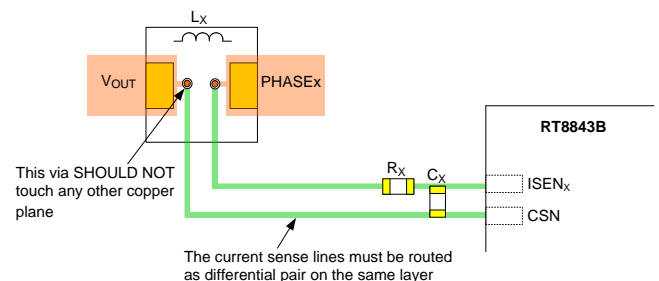


Figure 12. PCB Layout of DCR Current Sensing

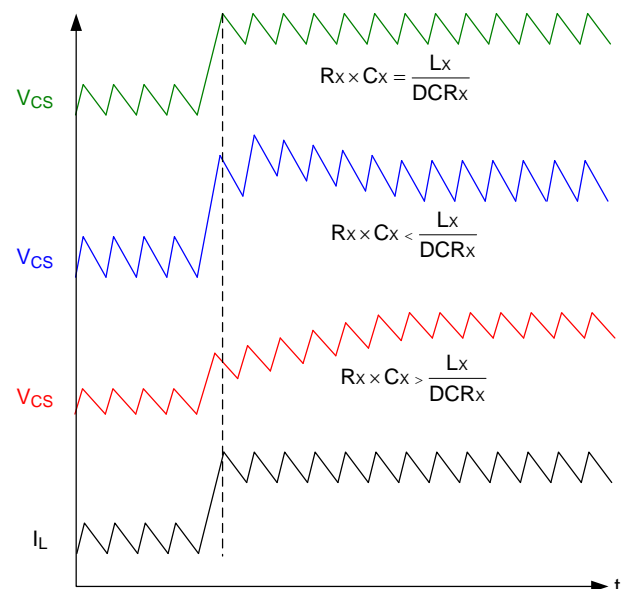


Figure 13. All Kinds of RC Network Time Constant

Table 7. Pin Setting of DrIMON

| DrIMON [0] | Enable/Disable |
|------------|----------------|
| 0 | Disable |
| 1 | Enable |

SPS Current Sensing

The RT8843B current sensing circuit can also support SPS current sensing. SPS (Smart Power Stage) can accurately detect the internal MOSFET current for a reference of PWM controller, SPS current sensing circuit simplifies the quantity of components on the external circuit and provides a more accurate current signal unlike DCR detection circuit. SPS has two kinds of current signal, current output and voltage output. Figure 14 shows the current reporting circuit of different current signals respectively. When the SPS current sensing is used, the DrIMON enable/disable of PINSET2 function must be set to enable. After DrIMON enable is set, the inverting input of the current-sense amplifier generates a 1.375V reference voltage for SPS current sensing circuit. The current is reported to the controller as a differential voltage between the ISENx and CSN pins with a conversion gain to represent the inductor current I_L , as shown in below equations.

$$V_{ISENx-CSN} = \text{gain}(A/A) \times I_L \times R_{IMON}$$

...(Current Type Signal)

$$V_{ISENx-CSN} = \text{gain}(V/A) \times I_L \times \frac{R_{IMON2}}{R_{IMON1} + R_{IMON2}}$$

...(Voltage Type Signal)

For larger current sense gain as voltage type, it is recommended to place a voltage divider resistor between IOUT and REFIN pins to avoid the controller's current amplifier input voltage range exceeding -10mV to 90mV .

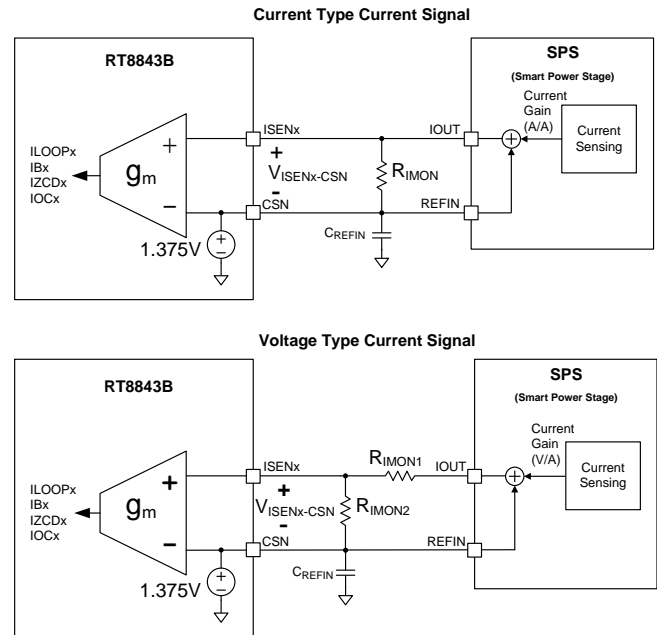


Figure 14. SPS Current Sensing

Auto-Zero Crossing Detection (Auto-ZCD)

The RT8843B can support the system to use ZCD threshold of DrMOS at light load condition. The ZCD function of DrMOS can be enabled by pulled down the ZCD# pin of DrMOS. When using the Auto-ZCD function, the Auto-ZCD# function of PINSET2 must be set to enable. Once the Auto-ZCD function is enabled, PINSET2 turns on the external NMOS and pulls the ZCD# voltage of DrMOS low as shown in Figure 7. The Auto-ZCD function only works at the status of ZCD# = L, PWM = L and GH = L. At this status, if the inductor current $I_L > 0\text{A}$, then $GL = H$. Conversely, if the inductor current $I_L < 0\text{A}$, then $GL = L$. In addition, once Auto-ZCD is enabled, controller only operates in FCCM regardless of PSI setting voltage.

Current Balance

The Per-phase current sense signal of the RT8843B is compared with sensed average current. The comparison result adjusts each phase PWM width to optimize current and thermal balance. When the PCB layout makes the parasitic impedance inconsistent from the inductor to the output, that will affect the performance of the current balance. Figure 15 shows a method to eliminate the parasitic impedance. Place two RCB resistors in each phase of the DCR sensing circuit to cancel the R_{PCB} effect and improve current balance.

The R_{CBx} value can be calculated by following equation.

$$R_{CBx} = R_{Xx} \times N$$

Where N is the phase number.

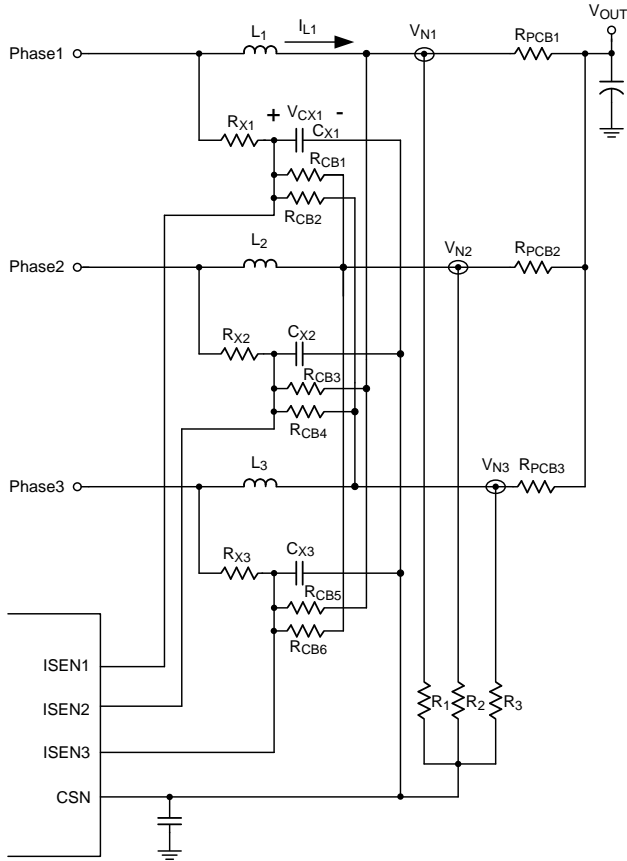


Figure 15. Current Balance Improving

Per-phase Current Limit

The RT8843B incorporates per phase current limit mechanism to prevent over current event. The per phase current limit circuit employs a unique “valley” current sensing algorithm. If the magnitude of the current sense signal is above the current limit threshold, the PWM is not allowed to initiate a new cycle. The per phase current limit threshold can be set by PINSET1 pin. When the DCR sensing circuit is selected, in order to ensure the accuracy of the current signal over a wide range temperature, it is recommended to use the NTC compensation circuit as shown in Figure 7. The current limit threshold can be calculated according to the following equation :

$$V_{OCSET} = V_{REF} - \left[\frac{V_{REF} \times \frac{R_3 + R_4}{R_1 + R_2 + R_3 + R_4} + 80\mu}{\times \left[\frac{R_5}{R_{NTC}} + (R_1 + R_2) // (R_3 + R_4) \right]} \right]$$

$$= V_{ISEN} \times CSN \times 32 = DCR \times I_{L_OC} \times 32$$

Where the I_{L_OC} is the desired current limit threshold.

On the other hand, when the SPS current sensing is selected, as shown in Figure 16, and the current limit threshold can be calculated as the following equation.

$$V_{OCSET} = V_{REF} - \left[\frac{V_{REF} \times \frac{R_3 + R_4}{R_1 + R_2 + R_3 + R_4} + 80\mu}{\times \left[(R_1 + R_2) // (R_3 + R_4) \right]} \right]$$

$$= V_{ISEN} - CSN \times 32 / 3.08$$

$$= I_{MON_SLOPE} \times R_{IMON} \times I_{L_OC} \times 32 / 3.08 \text{ (Current Type DR MOS)}$$

$$= V_{MON_SLOPE} \times R_{IMON2} / (R_{IMON1} + R_{IMON2}) \times I_{L_OC} \times 32 / 3.08 \text{ (Voltage Type DR MOS)}$$

Richtek provides a Microsoft Excel-based design tool to help design desired per-phase current limit threshold.

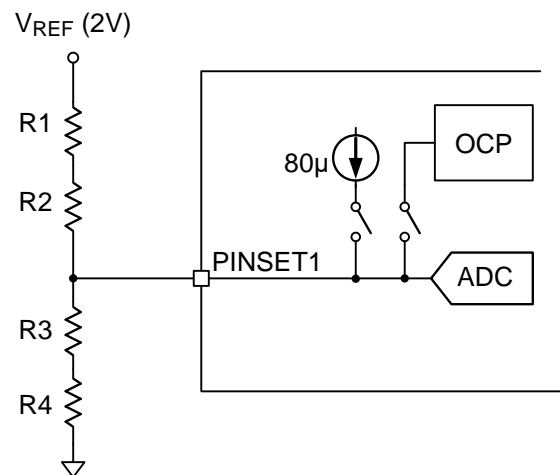


Figure 16. PINSET1 without NTC Network

AC Droop

The RT8843B adopts a new feature, i.e. AC-droop, to effectively suppress load transient ring back and to control overshoot well for zero loadline application. Figure 17 shows the condition without AC-droop control. The output voltage without AC-droop control has extra ring back ΔV_2 due to C area charge.

Figure 18 shows the condition with AC-droop control. While loading occurs, controller temporarily changes VID target to short-term voltage target. Short-term voltage target is related to transient loading current ΔI_{CC} and can be represented as the following :

Short_Term_Voltage_Target = $V_{CS} \times 9 \times AI$

Where the V_{CS} is the current sensing signal from DCR sensing or SPS current sensing. For DCR sensing, the $V_{CS} = I_{CC_MAX} \times DCR$. The current gain (AI) can be set by Pin Setting of AI Gain. User can select AI gain according to Table 8 to set desired short term voltage target. The short-term voltage target reverts to VID target slowly after approximately 100 μ s. The short-term voltage target can help inductor current not to exceed loading current too much and then the ring back can be suppressed. Referring to Figure 18, the overshoot amplitude is reduced to only ΔV_3 .

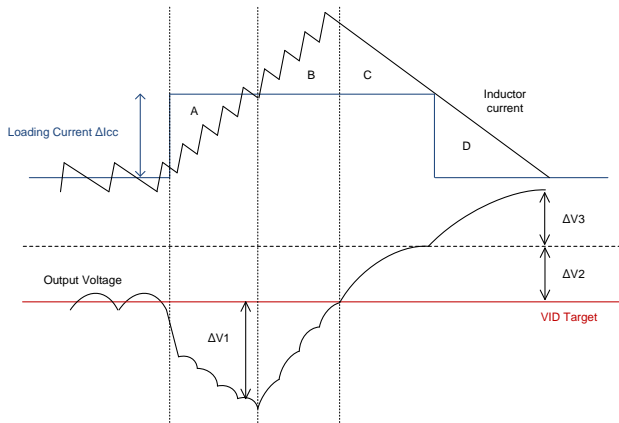


Figure 17. Zero Loadline without AC-Droop Control

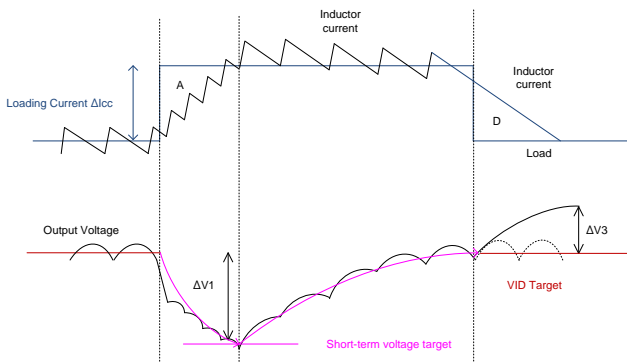


Figure 18. Zero Loadline with AC-Droop Control

Table 8. Pin Setting of AI Gain

| AI Gain [1:0] | Gain Value |
|---------------|------------|
| 00 | Disable |
| 01 | 1/16 |
| 10 | 2/16 |
| 11 | 4/16 |

Over Voltage Protection

The output voltage can be continuously monitored through VSEN pin for over-voltage protection. If REFIN voltage is lower than 1.33V, the over voltage threshold follows to absolute over voltage 2V. If REFIN voltage is higher than 1.33V, the over voltage threshold follows relative over voltage $1.5 \times V_{REFIN}$. The OV protection mechanism is illustrated in Figure 19. When OVP is triggered with 5 μ s filter time, controller de-asserts PGOOD and starts NVP function. After NVP is enabled, controller controls PWM as low when VSEN is higher than VID. When VSEN is lower than VID, PWM is controlled in tri-state to prevent large negative inductor current that may damage MOSFETs or driver. After 45 μ s from OVP trigger, VID starts to ramp down to 0V with slow slew rate. During the period, PWMx is not allowed to turn on. Controller controls PWMx to be low or tri-state to pull down the output voltage with VID. The OVP is latch mode protection, and it can be released by VCC or EN power on reset.

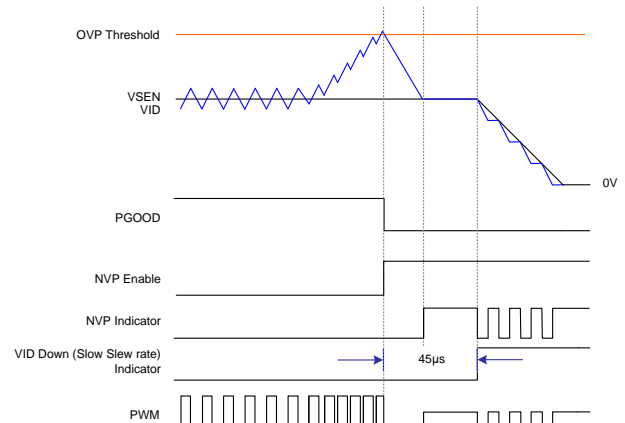


Figure 19. Over Voltage Protection Mechanism

The RT8843B reduces the on-time by pulling the PWM low when VSEN is higher than REFIN + 28mV to prevent overcharging of the output capacitor. Therefore, output voltage overshoot is reduced. When zero current (ZC) is detected, the on-time reduction threshold increases to REFIN + 36mV.

Under Voltage Protection

The output voltage can be continuously monitored through VSEN pin for under-voltage protection. When the output voltage is less than UVP threshold with 3 μ s filter time, controller de-asserts PGOOD and controls all PWMs to tri-state to turn off high-side and low-side

power MOSFETs. During soft-start, the UVP blanking time is equal to PGOOD blanking time.

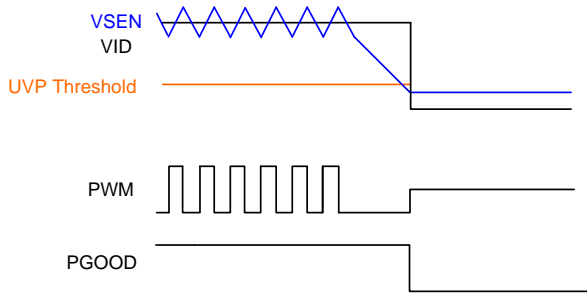


Figure 20. Under Voltage Protection Mechanism

Inductor Selection

The switching frequency and ripple current determine the inductor value as follows :

$$L_{(MIN)} = \frac{V_{IN} - V_{OUT}}{I_{RIPPLE(MAX)}} \times T_{ON}$$

where T_{ON} is the UGATE turn on period.

Higher inductance results in lower ripple current, which means the lower power loss. However, the inductor current rising time increases with inductance value. This means the transient response will be slower. Therefore, the inductor design is a trade-off between performance, size and cost.

The RT8843B supports inductor DCR sensing for loop control, zero-current-detection, current balance and per-phase current limiting. For ensuring the accuracy of DCR sensing signal, the minimum DC resistance of inductor must be greater than 0.2mΩ. The core must be large enough to prevent inductor saturation at heavy load condition.

Output Capacitor Selection

The selection of C_{OUT} is determined by considering to satisfy the voltage ripple, the transient loads and to ensure that control loop is stable. Loop stability can be checked by viewing the load transient response. The peak-to-peak output ripple, ΔV_{OUT} , is characterized by two components, which are ESR ripple ΔV_{P-P_ESR} and capacitive ripple ΔV_{P-P_C} , can be expressed as below :

$$\Delta V_{OUT} = \Delta V_{P-P_ESR} + \Delta V_{P-P_C}$$

$$\Delta V_{P-P_ESR} = \Delta I_L \times R_{ESR}$$

$$\Delta V_{P-P_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Where the ΔI_L is the peak-to-peak inductor ripple current and R_{ESR} is the equivalent series resistance of C_{OUT} . The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding to the transient loads, the V_{SAG} and V_{SOAR} requirement should be taken into consideration for choosing the output capacitance value. The amount of output sag is a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF_MIN}}$$

The worst-case output sag voltage can be determined by :

$$\Delta V_{OUT_SAG} = \frac{L \times (I_{L_PEAK})^2}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})}$$

The amount of overshoot due to stored inductor energy when the load is removed can be calculated as :

$$\Delta V_{OUT_SOAR} = \frac{L \times (I_{L_PEAK})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. Choose X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 105°C. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a WQFN-20L 3x3 package, the thermal resistance, θ_{JA} , is 30°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as below :

$$P_{D(MAX)} = (105^\circ\text{C} - 25^\circ\text{C}) / (30^\circ\text{C/W}) = 2.67\text{W for a WQFN-20L 3x3 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curves in Figure 21 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

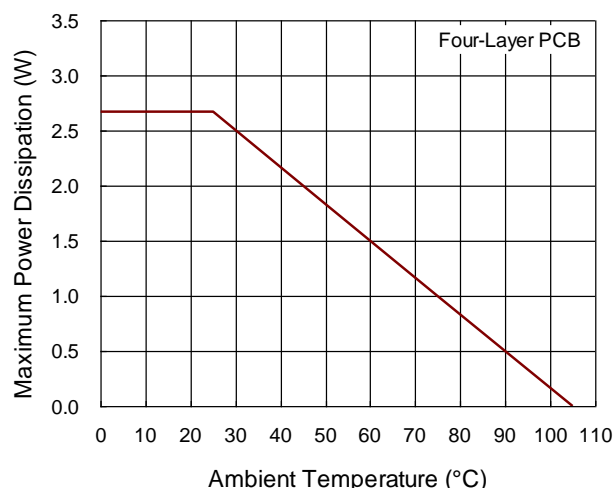


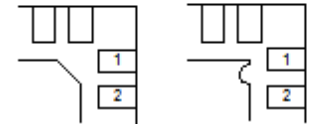
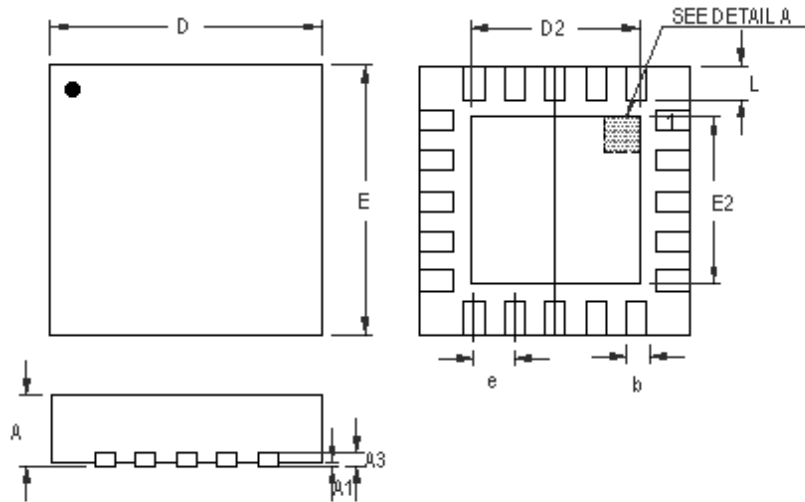
Figure 21. Derating Curve of Maximum Power Dissipation

Layout Considerations

Careful PCB layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all of the power components on the top side of the board with their ground terminals flushed against one another. Follow these guidelines for optimum PCB layout :

- ▶ Keep the high current paths short, especially at the ground terminals.
- ▶ Keep the power traces and load connections short. This is essential for high efficiency.
- ▶ When trade-offs in trace lengths must be made, it's preferable to allow the inductor charging path to be made longer than the discharging path.
- ▶ Place the current sense components close to the controller. ISENx and CSN connections for current limit and voltage positioning must be made by using Kelvin sense connections to guarantee the current sense accuracy. The PCB trace from the sense nodes should be paralleled back to the controller.
- ▶ Route high speed switching nodes away from sensitive analog areas (PINSETx, ISENx, CSN, VSEN, FBRTN, etc.)

Outline Dimension



DETAIL A

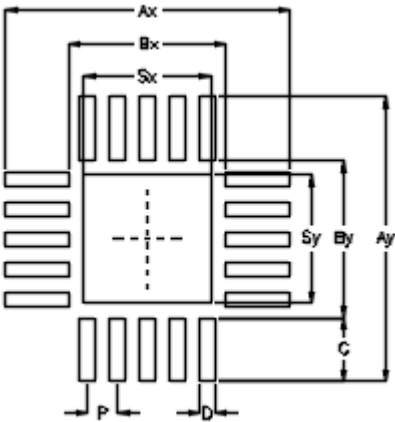
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| D2 | 1.650 | 1.750 | 0.065 | 0.069 |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| E2 | 1.650 | 1.750 | 0.065 | 0.069 |
| e | 0.400 | | 0.016 | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |

W-Type 20L QFN 3x3 Package

Footprint Information



| Package | Number of Pin | Footprint Dimension (mm) | | | | | | | | | Tolerance |
|------------------|---------------|--------------------------|------|------|------|------|------|------|------|------|-----------|
| | | P | Ax | Ay | Bx | By | C | D | Sx | Sy | |
| V/W/U/XQFN3*3-20 | 20 | 0.40 | 3.80 | 3.80 | 2.10 | 2.10 | 0.85 | 0.20 | 1.70 | 1.70 | ±0.05 |

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