Multi-Phase PWM Controller with PWM-VID Reference

1 General Description

The RT8848C is a 8/7/6/5/4/3/2/1 multi-phase synchronous Buck controller which is optimized for high-performance graphic microprocessor and supports nVidia OVR4i+ spec with PWM-VID interface. The RT8848C adopts AC G-NAVP™ (Green Native AVP), which is Richtek's proprietary topology derived from finite DC gain of internal GM amplifier with current mode control. By utilizing the AC G-NAVP™ topology, the operating frequency of the RT8848C varies with VID, load and input voltage to further enhance the efficiency even in CCM. Besides, for current sensing application, the RT8848C can support either a traditional DCR network current sensing from inductor or a smart power stage (SPS) which can directly provide a current monitor signal (IMON).

The RT8848C features external reference input and PWM-VID dynamic output voltage control, in which the output voltage is regulated and tracks external input reference voltage. The RT8848C can set internal RAMP amplitude through PINSETx pin and this can optimize stability and load transient performance. The RT8848C also provides complete fault protection functions including overvoltage protection (OVP), undervoltage protection (UVP), channel overcurrent limit (CH_OC), sum output current protection (SOC) and over-temperature protection (OTP). The recommended junction temperature is –40°C to 125°C.

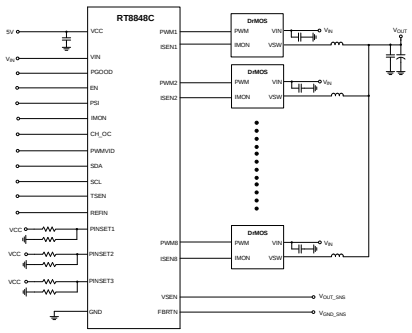
2 Features

- **Multi-Phase PWM Controller**
- **PWM-VID Dynamic Voltage Control**
- **Support 1.8V PWM-VID Interface**
- **Power State Indicator**
  - **LPC (Low Phase Count), PSI = Low**
  - **APS (Auto Phase Shedding), PSI = Mid**
  - **HPC (High Phase Count), PSI = High**
- **External Reference Input Control**
- **8/7/6/5/4/3/2/1 Phase Hardware Setting**
- **Adjustable Soft-Start Time**
- **Adjustable Switching Frequency**
- **Adjustable Phase Current Balance**
- **Support Standby Mode**
- **UVP/OVP/OTP/SOC/CH_OC/TSEN Protection**
- **Adjustable Protection Thresholds**
- **Power Good Indicator**
- **ADC Reporting for IMON, TSEN and VSEN**
- **Support I²C Interface for Programming**

3 Applications

- GPU Core Power for OVR4i+ Spec

4 Simplified Application Circuit



5 Ordering Information

RT8848C □□

Package Type
QW: WQFN-40L 5x5 (W-Type)

Lead Plating System
G: Richtek Green Policy Compliant

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information

RT8848CGQW: Product Code
YMDNN: Date Code

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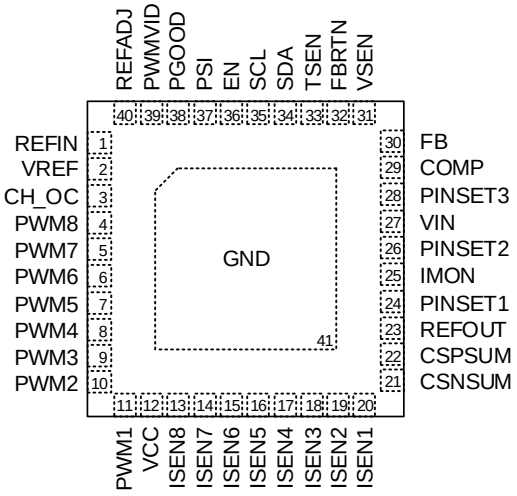
7 Pin Configuration

(TOP VIEW)



WQFN-40L 5x5

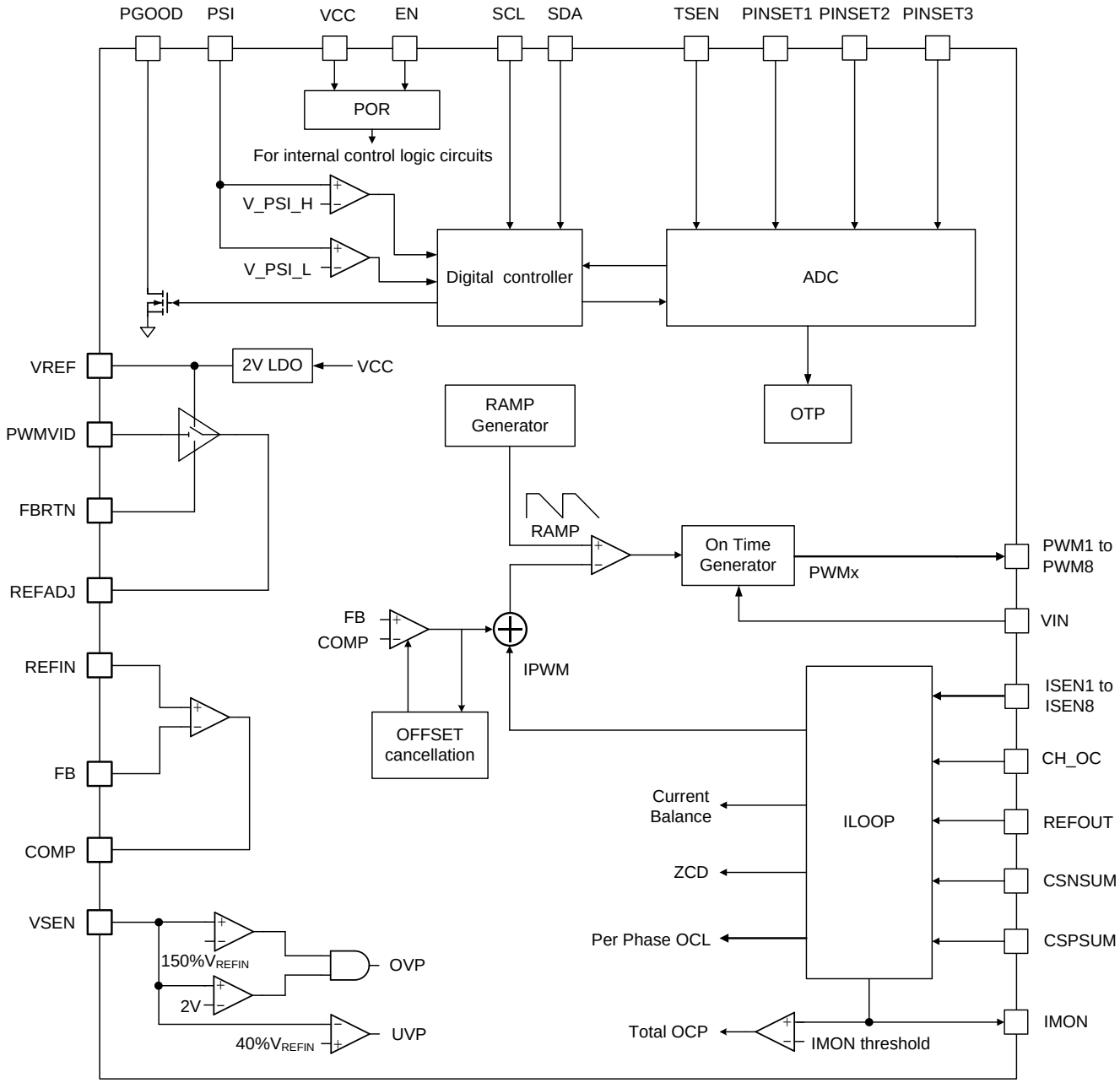
8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	REFIN	External reference input. Connect this pin to an external voltage source through a RC filter (R = 2.2Ω/0603 and C = 1μF/0603) or connect to the output of REFADJ circuit.
2	VREF	Reference voltage output. Connect a 0.1μF/0603 decoupling capacitor between VREF and GND. The reference voltage is 2V.
3	CH_OC	Channel current limit. Connect a resistor from CH_OC to GND to adjust the per-phase current-limit threshold. The resistor setup for current-limit threshold is detailed in Application Information section. Besides, if CH_OC is left floating, voltage of CH_OC is fixed at 5V for maximum current limit level.
4 to 11	PWM8 to PWM1	PWM control output for phase 8 to phase 1 driver circuit. As PWM output is high (pulled up to VCC), high-side MOSFET is turned on. As PWM output is in tri-state level (1.65V or 1.9V), both MOSFETs are turned off. As PWM output is low (pull down to GND), low-side MOSFET is turned on. In addition, the parasitic capacitor on the PWM pin should be smaller than 100pF. Leave pin floating if the operating phase is disabled.
12	VCC	Bias voltage for control logic. The required bias voltage for VCC is 5V typ. For avoiding noise disturbance, the supplied bias voltage must be stable. Besides, a RC filter (R = 2.2Ω/0603 and C = 1μF/0603) from bias voltage to VCC pin is necessary, and should be placed as close as physically possible to VCC pin. There is around 50mA sink current during POR duration, the maximum resistance of RC filter should be smaller than 2.2Ω.

Pin No.	Pin Name	Pin Function
13 to 20	ISEN8 to ISEN1	Current sense inputs of phase 1 to phase 8. These pins can be used for differentially sensing output current from DCR current sensing network or connecting to IMON output pin of SPS (Smart Power Stage) for each phase. DO NOT add additional RC filter. Besides, the ISENx pins can also be used for hardware setting of maximum phase number. When ISENx pin is pulled up to VCC with a 100kΩ resistor, the PHASEx is disabled and the maximum phase number reduces to X-1. For example, if ISEN7 pin is pulled up to VCC, the maximum phase number is 6. Both PHASE7 and PHASE8 are disabled.
21	CSNSUM	Inverting input of total current sense amplifier. DO NOT add RC filter on this pin. Only add a decoupling cap. (10nF/0603) to GND.
22	CSPSUM	Non-inverting input of total current sense amplifier. DO NOT add additional RC filter on this pin.
23	REFOUT	Reference output pin. As for SPS application by setting the PINSET1 to SPS mode, REFOUT outputs 1.38V (typ.) to the REFIN pin of SPS. Connect a 0.47μF/0603 decoupling capacitor near this pin, and the equivalent capacitance on this pin should be limited at ±10% of 0.47μF. Besides, as for DCR current sensing application by setting the PINSET1 to DCR mode, REFOUT is regarded as an input pin and it should be connected to the positive terminal of output capacitor. A small decoupling capacitor (10nF/0603) to GND is necessary.
24	PINSET1	PINSET 1 I/O pin. Connect a pair of voltage divider to adjust the internal function setting for “internal ramp amplitude”, “soft-start slew rate”, “PWM high-Z level”, “AI gain” and “SPS selection”. The design value of resistors is detailed in Application Information section. Moreover, DO NOT put any decoupling capacitor near this pin.
25	IMON	Output current monitor. The output current of this pin is proportional to the total load current. The total load current is sensed and flows out of this pin, and a resistor from this pin to GND makes the IMON voltage proportional to the total output current. The IMON resistor selection should follow the application type (SPS or DCR). The guide is introduced in Application Information section. Do not put any decoupling capacitor near this pin since it affects the accuracy of IMON reporting.
26	PINSET2	PINSET 2 I/O pin. Connect a pair of voltage divider to adjust the internal function setting for “per-phase switching frequency”, “slave device address code”, “middle drive control” and “operation phase number as PSI = L”. The design value of resistors is detailed in Application Information section. Moreover, DO NOT put any decoupling capacitor near this pin.
27	VIN	VIN monitor pin. It is recommended to place a RC filter before VIN pin for stable operation. The suggested design value of RC filter is R = 2.2Ω/0603 and C = 1μF/0603.
28	PINSET3	PINSET 3 I/O pin. Connect a pair of voltage divider to adjust the internal function setting for “auto phase shedding current threshold” and “soft-start phase number during cold-boot and warm-boot”. The design value of resistors is detailed in Application Information section. Moreover, DO NOT put any decoupling capacitor near this pin. If PISET3 is not used, please leave this pin floating and DO NOT short this pin to GND.
29	COMP	Output of control loop error amplifier.

Pin No.	Pin Name	Pin Function
30	FB	Inverting input of the error amplifier.
31	VSEN	Output voltage sensing input. This pin is the positive input from differential output voltage remote sense. Connect to the positive terminal of output capacitors at GPU side with a resistor (0Ω/0603) for OVP and UVP detection. Besides, to prevent output overvoltage when GPU is disconnected, connect to positive terminal of output capacitors at local side with a resistor (100Ω/0603).
32	FBRTN	Output voltage feedback return. This pin is the negative input from differential output voltage remote sense. Connect to the remote sensing ground at GPU side with a resistor (0Ω/0603). Besides, to prevent output overvoltage when GPU is disconnected, connect to output capacitors' ground at local side with a resistor (100Ω/0603).
33	TSEN	Thermal monitor input. Connect a voltage divider with a NTC thermistor for VR temperature sensing or connect to the DrMOS's temperature monitor output.
34	SDA	I^2C data pin. This pin is the input and output of serial bus data signal.
35	SCL	I^2C clock pin. This pin is the input of serial bus clock signal.
36	EN	Enable control input. Connect a resistor (R = 60kΩ/0603) to GND in parallel with a NMOS switch. As EN voltage is lower than 0.3V, RT8848C is in shutdown mode and all power rails are disabled. As EN is higher than 1.8V, RT8848C wakes up.
37	PSI	Power state input. Depending on different input voltage levels of PSI, the controller can be operated in full phase mode (PSI > 1.6V), auto-phase shedding mode (0.8V < PSI < 1.2V) or low phase count mode (PSI < 0.4V) separately.
38	PGOOD	Power good indicator. This open-drain is pulled low as UVP, OVP, OTP, EN low and output voltage is not regulated (such as before soft-start). An external pull-up resistor to VCC or other external rail is required, and a 10kΩ pull-up resistor is recommended.
39	PWMVID	PWMVID input pin. The reference of output voltage can be programmed by adjusting the PWMVID input signal.
40	REFADJ	PWMVID output pin for output reference adjustment. Connect this pin with a RC filter to generate REFIN voltage. The recommended RC value is R = 6.19kΩ (0603) and C = 4.7nF(0603). Please refer to Application Information section for further information about RC filter.
41 (Exposed Pad)	GND	Ground. The exposed pad is the ground of logic control circuits. For better power dissipation, it should be soldered to a large ground plane with enough thermal vias.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 1)

- VIN to GND ---------- –0.3 to 28V
- VCC to GND ---------- –0.3 to 6V
- FBRTN to GND ---------- –0.3 to 0.3V
- Other Pins ---------- –0.3 to 6V
- Power Dissipation, P_D @ T_A = 25°C

  WQFN-40L 5x5 ---------- 3.63W
- Package Thermal Resistance (Note 2)

  WQFN-40L 5x5, θ_{JA} ---------- 27.5°C/W

  WQFN-40L 5x5, θ_{JC} ---------- 6°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM ---------- 2kV

11 Recommended Operating Conditions

(Note 4)

- Input Voltage, V_{IN} ---------- 2.8 to 24V
- Supply Voltage, V_{VCC} ---------- 4.5 to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

12 Electrical Characteristics

(V_{VCC} = 5V, typical values are referenced to T_A =T_J = 25°C, Min and Max Values are referenced to T_A =T_J from –10°C to 105°C, unless other noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller						
VCC Supply Voltage	V_{VCC}		4.5	5	5.5	V
VCC Supply Current	I_{VCC}	EN = high, not switching	--	10	15	mA
VCC Shutdown Current	I_{SHDN}	EN = 0V	--	--	200	μA
VCC POR Threshold		VCC rising voltage	4.1	4.3	4.5	V
VCC UVLO Threshold		VCC falling voltage	3.9	4.1	4.3	V
POR Hysteresis			90	200	310	mV
Reference Voltage						
Reference Voltage	V_{REF}		1.98	2	2.02	V
REFOUT Output Voltage	V_{REFOUT}		1.3	1.38	1.45	V
REFIN Standby Voltage	V_{REFIN_STD}	V_{REFIN} < 0.15V	--	--	0.15	V
External REFIN Voltage	V_{REFIN}		0.25	--	2	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWMVID Input Voltage						
PWMVID Input Voltage Logic-High	V_{PWMVID_H}		1.2	--	--	V
PWMVID Input Voltage Logic-Low	V_{PWMVID_L}		--	--	0.6	V
PWMVID Tri-state Voltage	V_{PWMVID_TRI}		0.8	--	1	V
Soft-Start						
Soft-Start Ramp Up Slew Rate		Slew rate set to 3mV/μs	2.5	3	3.5	mV/μs
PGOOD Blanking Time	t_{PGOOD}	From EN go high to PGOOD go high	--	--	2	ms
EN and Logic Input						
EN Threshold	V_{EN1_H}	R_{EN} = 60kΩ, I_{SOURCE_EN} = 10μA	0.5	--	--	V
	V_{EN1_L}		--	--	0.3	
	V_{EN2_H}	R_{EN} = 60kΩ, I_{SOURCE_EN} = 90μA	1.8	--	--	
	V_{EN2_L}		--	--	1.6	
EN Deglitch Time		V_{EN} is higher than high threshold or lower than low threshold	--	1.6	--	μs
Leakage Current of PGOOD, PSI			–1	--	1	μA
PSI Input Voltage						
PSI Logic High Threshold	V_{PSI_H}		1.6	--	--	V
PSI Logic Tri-State Threshold	V_{PSI_HIZ}		0.8	--	1.2	V
PSI Logic Low Threshold	V_{PSI_L}		--	--	0.4	V
Frequency Setting						
Frequency Setting	f_{SW}	f_{SW} = 300kHz, I_{LOAD} = 0A	270	300	330	kHz
Minimum PWM Pulse Width	t_{PWM_MIN}		--	50	--	ns
I_{PINSET} (For PINSET1, PINSET2 and PINSET3)						
PIN SET Current	I_{PINSET}	$V_{PINSETx}$ = 1V, V_{VCC} = 5V	79.2	80	80.8	μA
EA/GM Amplifier						
Input Offset	V_{EAOFS}		–3	--	3	mV
CS Amplifier						
Input Offset	V_{EAOFS}		–1	--	1	mV
Protection Function						
Relative Overvoltage Protection Threshold	V_{ROVP}	V_{REFIN} ≥ 1.33V	142.5	150	157.5	%
Absolute Overvoltage Protection Threshold	V_{ABOVP}	V_{REFIN} < 1.33V,	1.9	2	2.1	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OV Fault Delay		FB forced above OV threshold	--	1	2	µs
Relative Undervoltage Protection Threshold	V_{RUVP}		35	40	45	%
UV Fault Delay		FB forced above UV threshold	2	4	6	µs
Thermal Shutdown Threshold	T_{SD}		--	150	--	°C
Per Phase OC Threshold	V_{CS_PH}	(V_{ISENPx} – V_{CSNSUM}) when $V_{CH\_OC\_SET}$ = 1.6V	56	62.5	69	mV
Channel OC Source Current	I_{CH_OC}	V_{VCC} = 5V	19.6	20	20.4	µA
Sum OC Protection Threshold	$V_{IMON\_SOC\_TH}$	V_{VCC} = 5V, 0x24[5:0] = 0x00	2.1	2.2	2.3	V
TSEN Protection Threshold Voltage	V_{TSEN_TH}	V_{VCC} = 5V, PTC Application	0.72	0.8	0.88	V
PWM Driving Capability						
PWM Source Resistance	R_{PWM_SRC}	Pull up to VCC	15	25	35	Ω
PWM Sink Resistance	R_{PWM_SNK}	Pull down to GND	--	7	12	Ω
PWM Tri-state Voltage	V_{PWM_Tri}	V_{VCC} = 5V, 0x40[0] = 0	1.65	1.9	2.15	V
		V_{VCC} = 5V, 0x40[0] = 1	1.4	1.65	1.9	
Power Good Indicator						
PGOOD Output Low Level	V_{PGOOD}	I_{SINK} = 4mA	--	--	0.3	V
PGOOD Leakage Current	I_{PGOOD_Leak}	V_{PGOOD} = 5V	--	--	1	µA
I^2C Interface (SDA&SCL)						
Input High Level	V_{IH_I2C}		1	--	--	V
Input Low Level	V_{IL_I2C}		--	--	0.6	V
SDA Pull Down Resistance	R_{DOWN_I2C}		--	7	12	Ω
Leakage Current	I_{LEAK_I2C}		--	--	1	µA
ADC Voltage Range						
TSEN ADC	V_{TSEN_ADC}	ADC = 12.5mV/step	0	--	3.2	V
IMON ADC	V_{IMON_ADC}	ADC = 6.25mV/step	0.6	--	2.2	V
VSEN ADC	V_{VSEN_ADC}	ADC = 6.25mV/step	0	--	1.6	V

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Typical Application Circuit

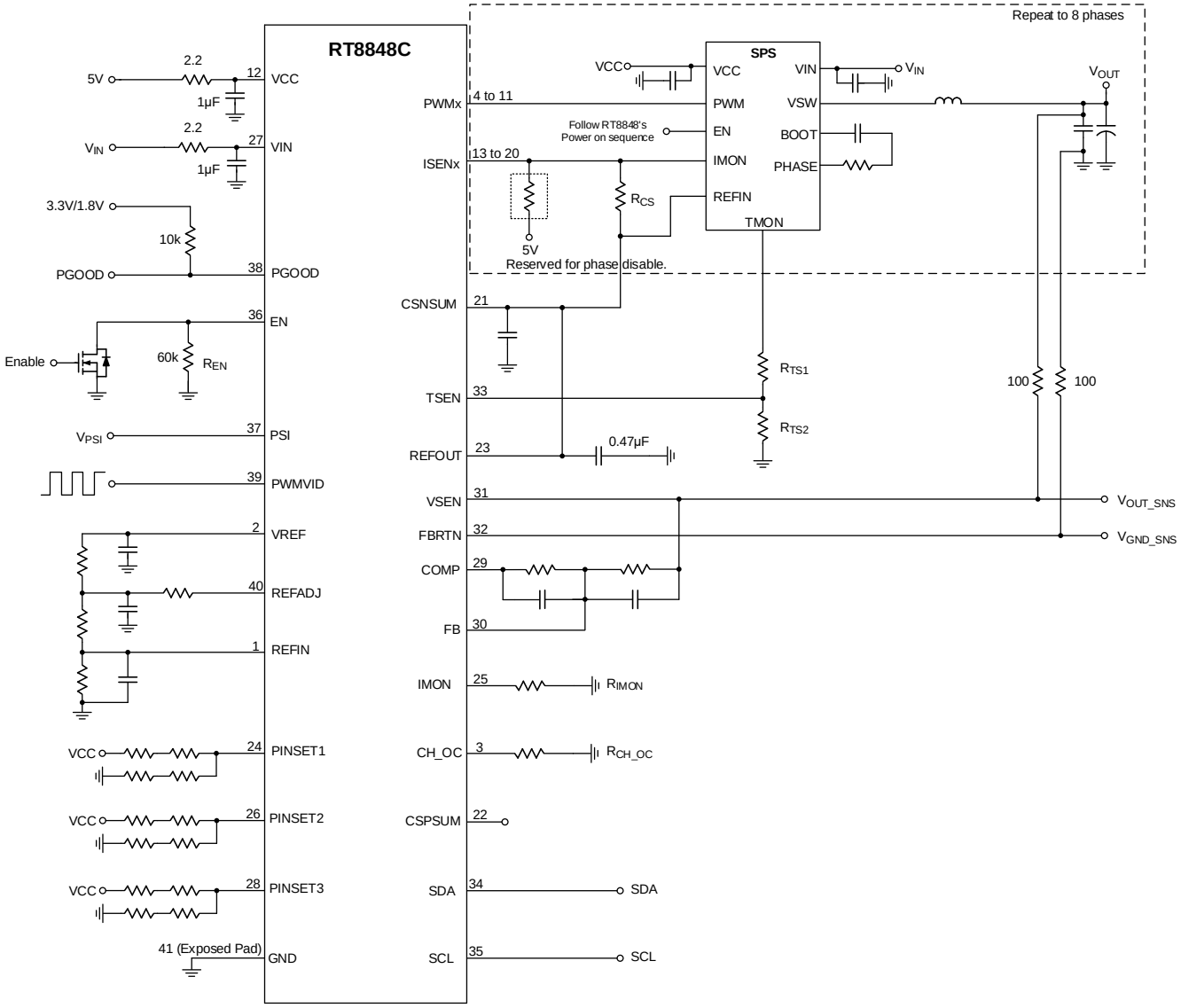


Figure 1. Typical Application Circuit for RT8848C with SPS's IMON Configuration

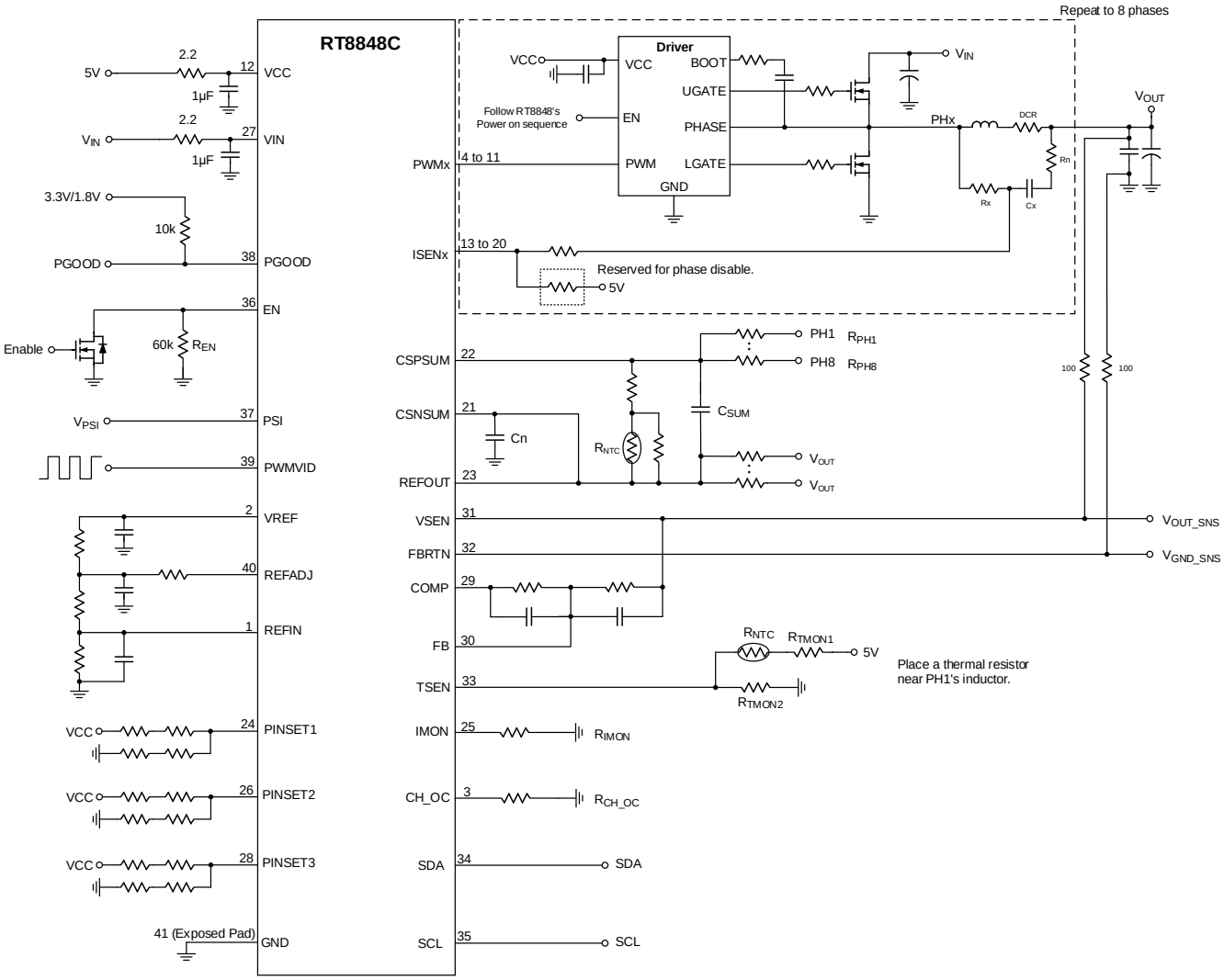
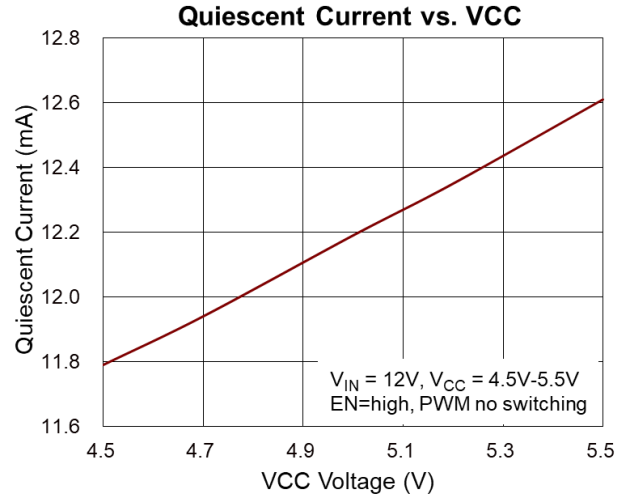
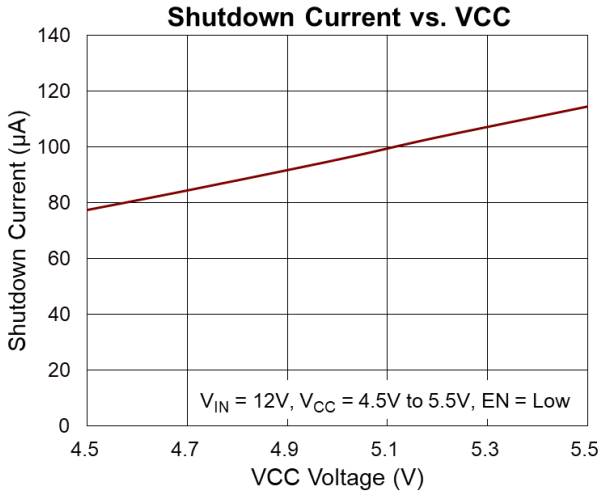


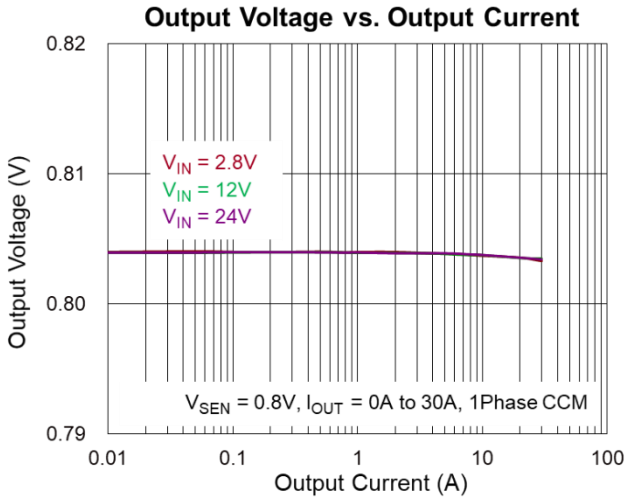
Figure 2. Typical Application Circuit for RT8848C with DCR Current Sense Configuration

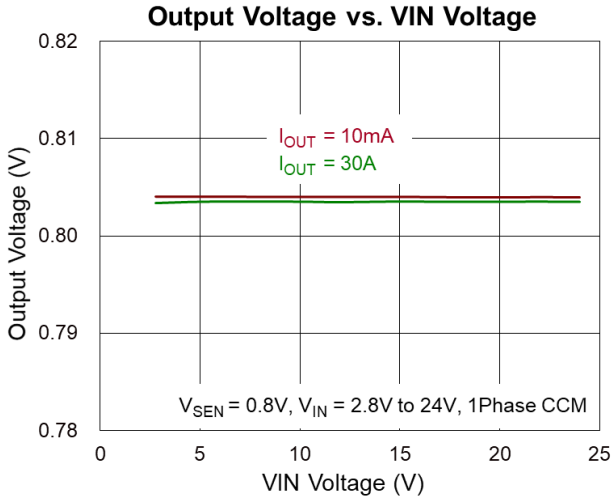
14 Typical Operating Characteristics

Performance waveforms are tested on the evaluation board of the Typical Application Circuit, V_{IN} = 12V, V_{SEN} = 0.8V, f_{SW} = 300kHz, L = 0.22µH, C_{OUT} = 330µF/2V POSCAP x 8pcs + 22µF/6.3V/X5R/0805 x 48pcs + 22µF/6.3V/X5R/0603 x 80pcs, T_C = 25°C, unless otherwise noted.

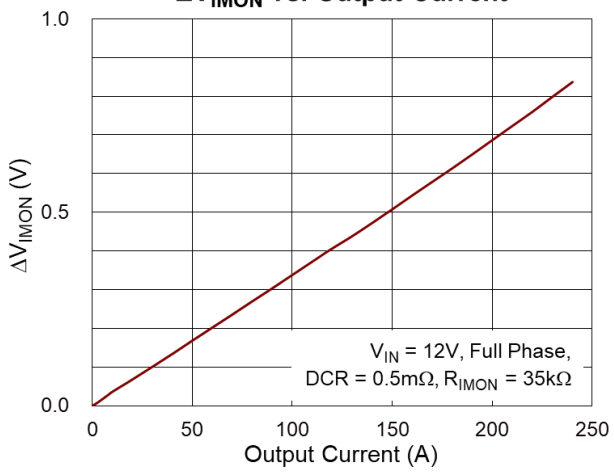




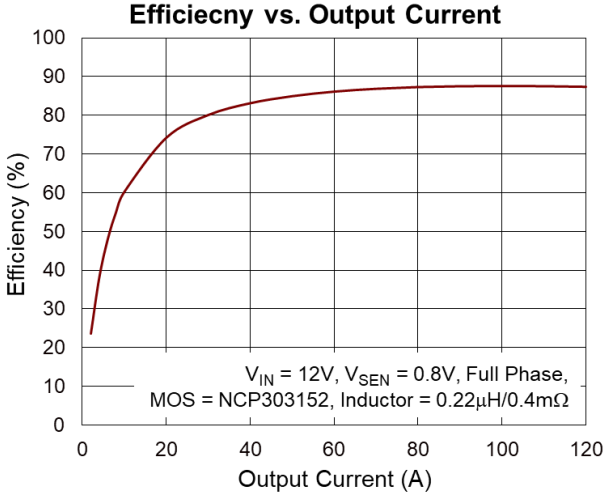




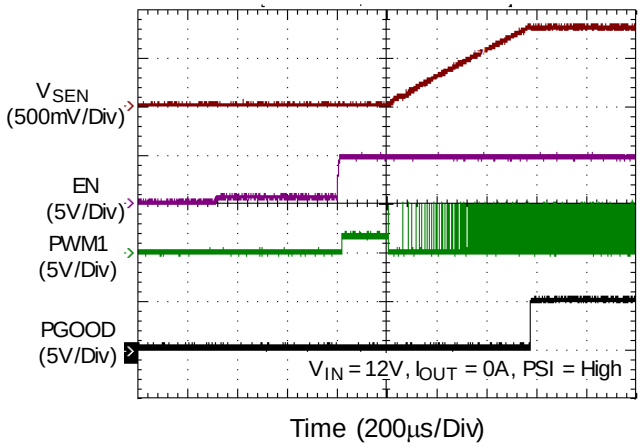
ΔV_{IMON} vs. Output Current



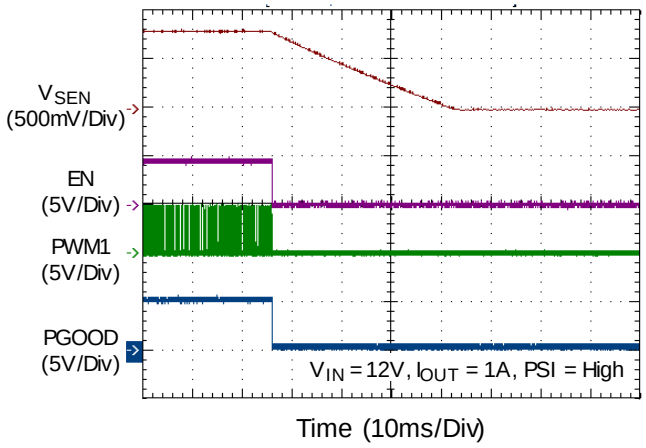
Efficiecny vs. Output Current



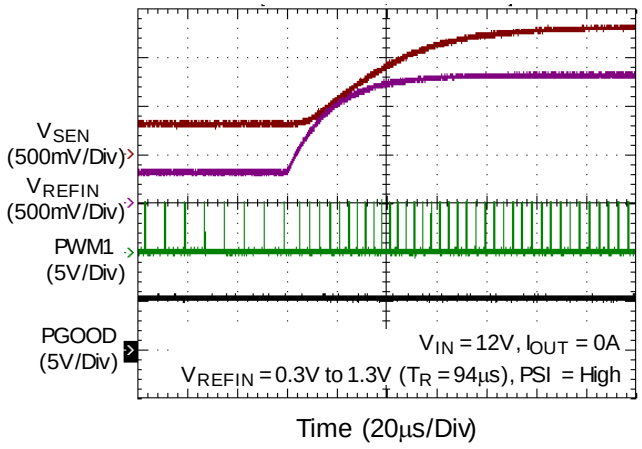
Power On from EN



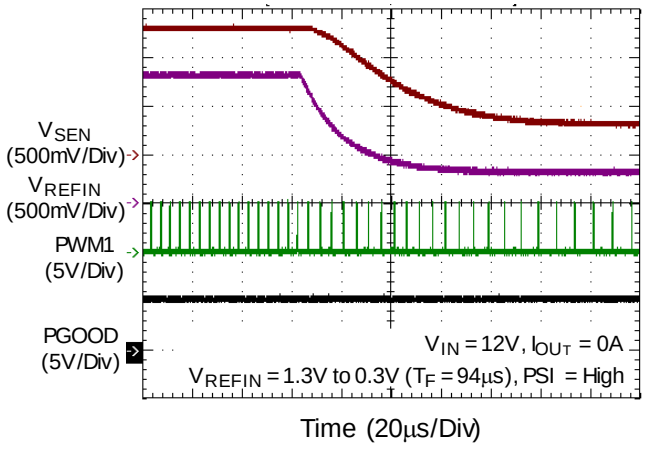
Power Off from EN



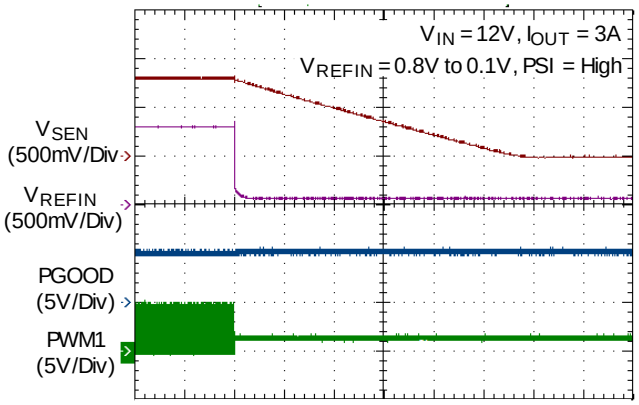
DVID Up



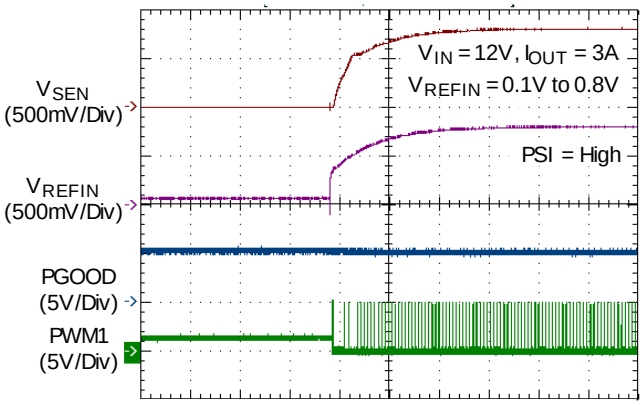
DVID Down



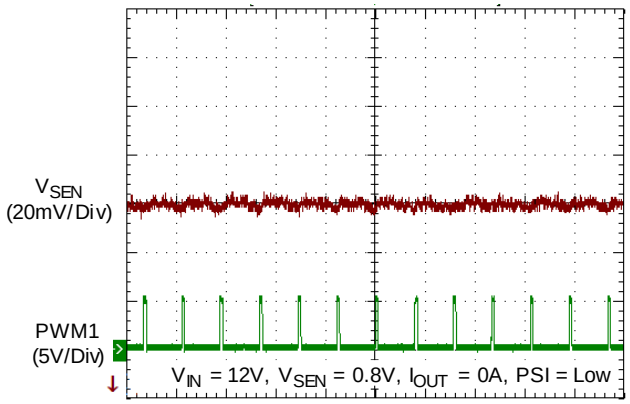
Enter Standby Mode



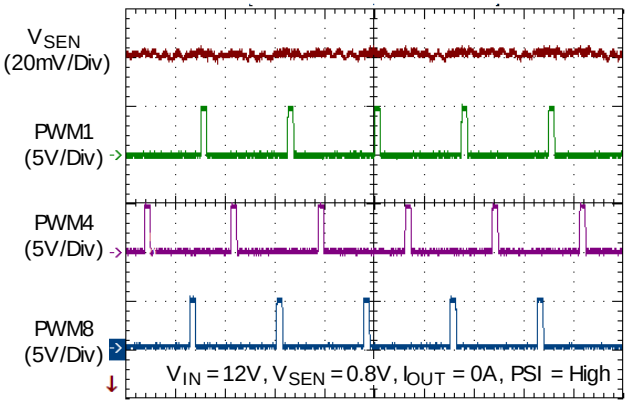
Exit Standby Mode



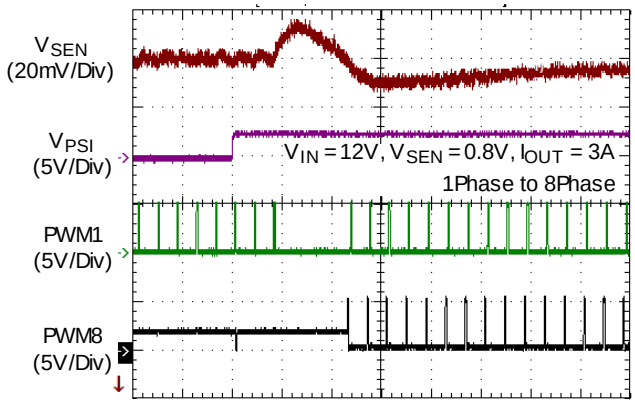
Stability 1Phase DEM



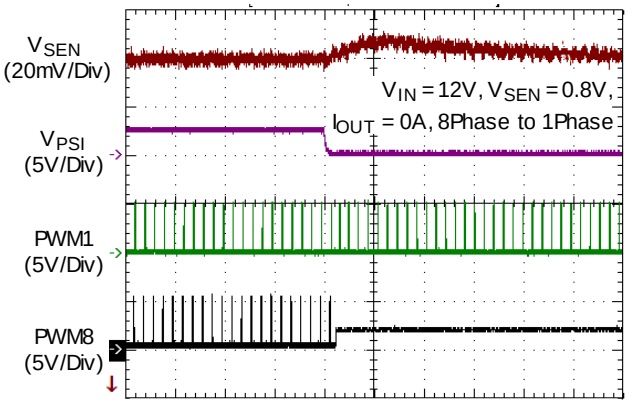
Stability 8Phase CCM



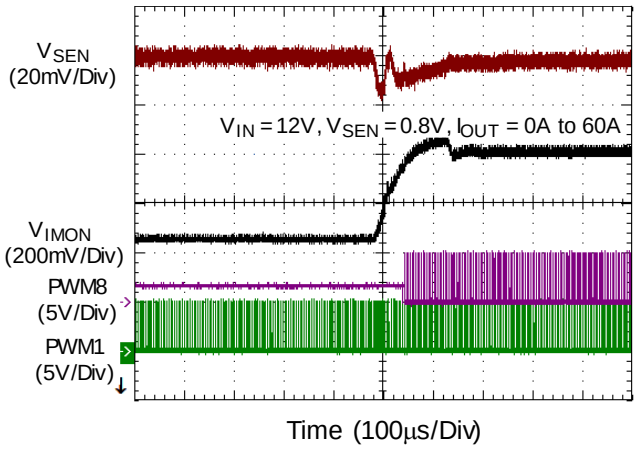
PSI Transition from Low to High



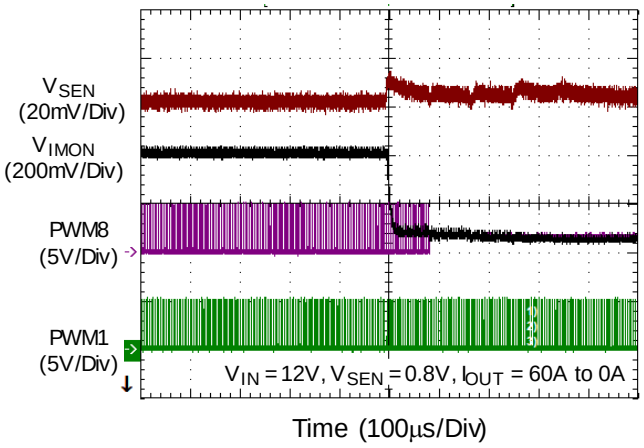
PSI Transition from High to Low



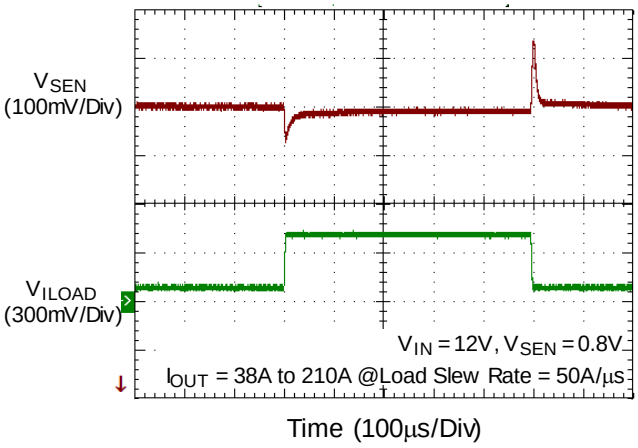
APS Phase Adding



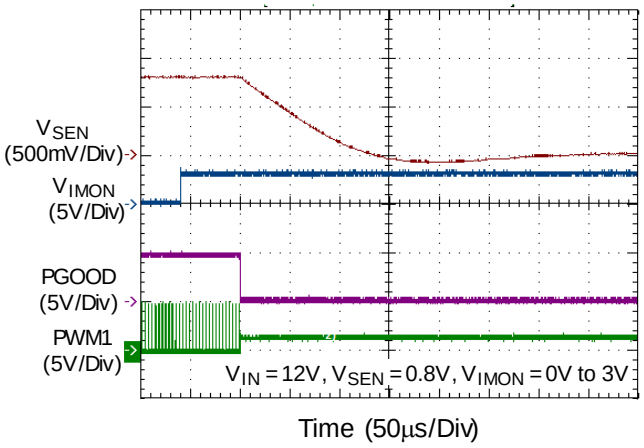
APS Phase Shedding



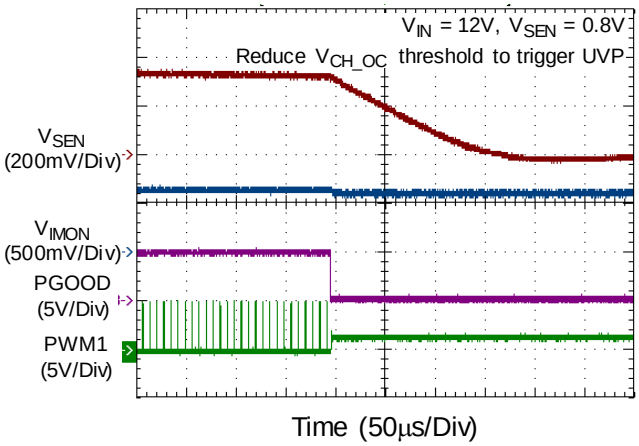
Load Transient



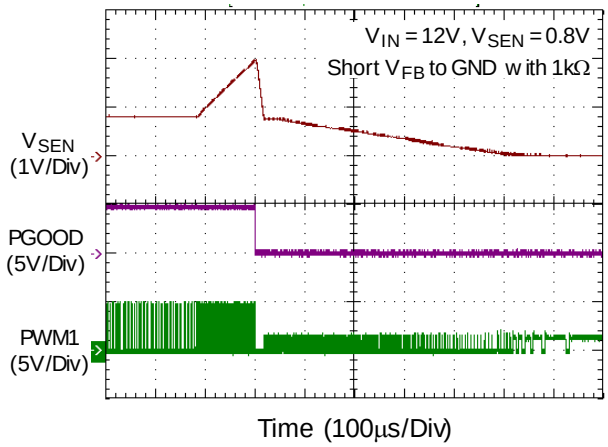
Sum OCP Behavior (8Phase)



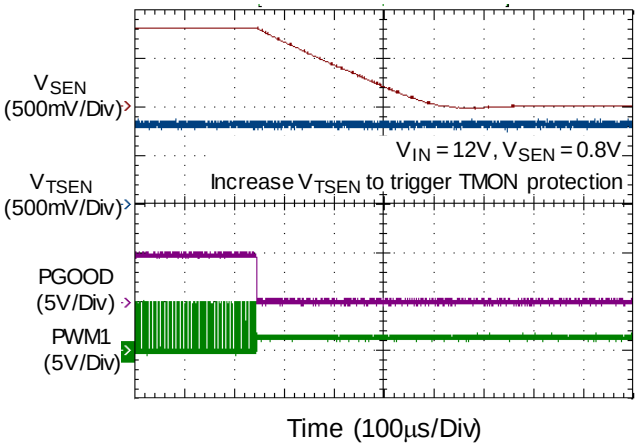
UVP Behavior (1Phase)



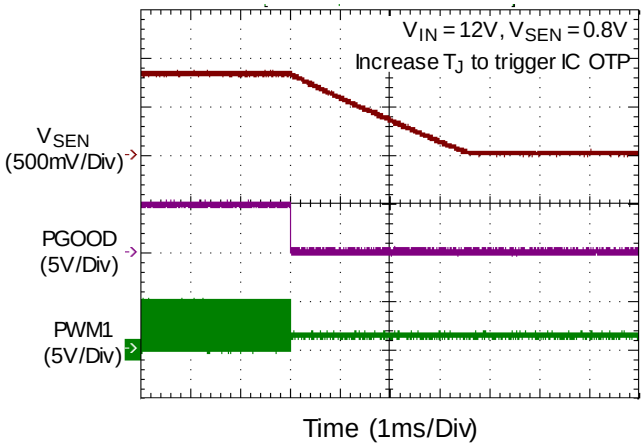
OVP Behavior (1Phase)



TMON Protection Behavior (1Phase)



OTP Behavior (8Phase)



15 Operations

15.1 VCC Power-On Reset (POR), UVLO

The power ready detection circuit is shown in Figure 3. The VCC voltage is monitored for power-on reset with typically 4.3V rising edge threshold. There is around 200mV hysteresis voltage for the comparator. When VCC is above POR threshold, the controller starts up after EN is higher than 1.8V. In contrast, as EN pin is driven below 0.3V, the controller will be turned off, and all fault states are cleared. Moreover, for avoiding noise disturbance, the supplied bias voltage must be stable. A RC filter (R = 2.2Ω/0603 and C = 1μF/0603) from bias voltage to VCC pin is necessary, and should be placed as close as possible to VCC pin. There is around 50mA sink current during POR duration, the maximum resistance of RC filter should be smaller than 2.2Ω.

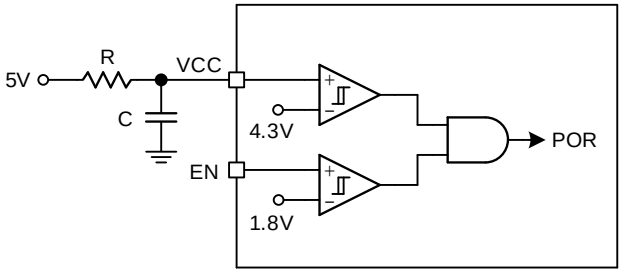


Figure 3. Circuit of Power Ready Detection

15.2 EN Control Circuit

As PWM controller's VCC is higher than POR threshold (typically 4.3V), an internal I_{SOURCE_EN} current is generated. A simplified enable sequence control circuit is shown in Figure 4. There is a MOSFET, Q1, in parallel with R_{EN} to control the high/low status of EN. For first power-on, as Q1 is open, a source current (I_{SOURCE_EN}) flows through R_{EN} to GND to enable the controller, and the initial value of I_{SOURCE_EN} is 10μA during pin setting detection process. At the end of pin setting process, the I_{SOURCE_EN} increases to 90μA and V_{EN} is clamped by VCC at 4.5V. The controller will follow the power-on sequence setting to ramp up the output voltage with a determined ramp up slope (Please refer to the Power-On Sequence section). The recommended design value of R_{EN} is 60kΩ.

Besides, the RT8848C also offers a special Middle drive function to drive the PWM voltage at tri-state level to turn off both high-side and low-side MOSFETs. This function can be enabled or disabled by I^2C register 0x43[3] or PINSET2. For most of drivers or DrMOSs in the market, they have built-in pull high and pull low resistors connected to PWM pins, therefore, the Middle drive function is not necessary. For some special products without internal driving capability for tri-state voltage, the Middle drive function can help to drive PWM pin at correct voltage level for normal operation. However, there is one important thing to be noticed for applying Middle drive function to DrMOS. Because of Middle drive function is disabled when controller EN logic is low, it requires around 50μs to reboot for normal operation. Therefore, the driver enable (EN_D) and the controller EN should be synchronized to prevent the unknown operation during Middle drive reboot duration. The sequence of EN and EN_D should follow the sequence as depicted in Figure 5. The delay time (T_{EN_D1}) from EN high to EN_D high should be larger than 60μs and smaller than 100μs to prevent abnormal operation. On the other hand, for the applications without Middle drive function, the only sequence requirement between driver and controller is that the EN_D of driver should be high 100μs (T_{EN_D2}) before controller EN logic goes high as shown in Figure 6.

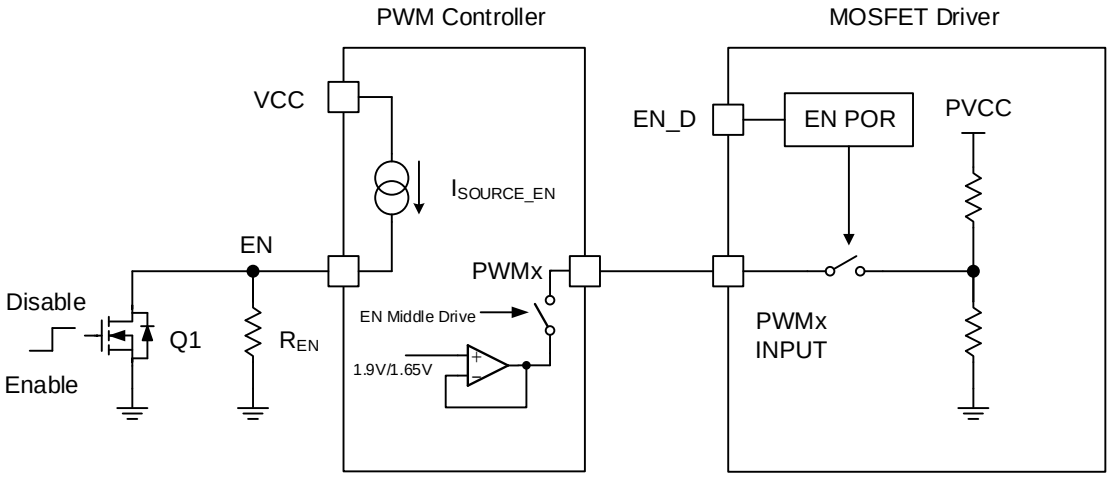


Figure 4. Enable Sequence Control Circuit

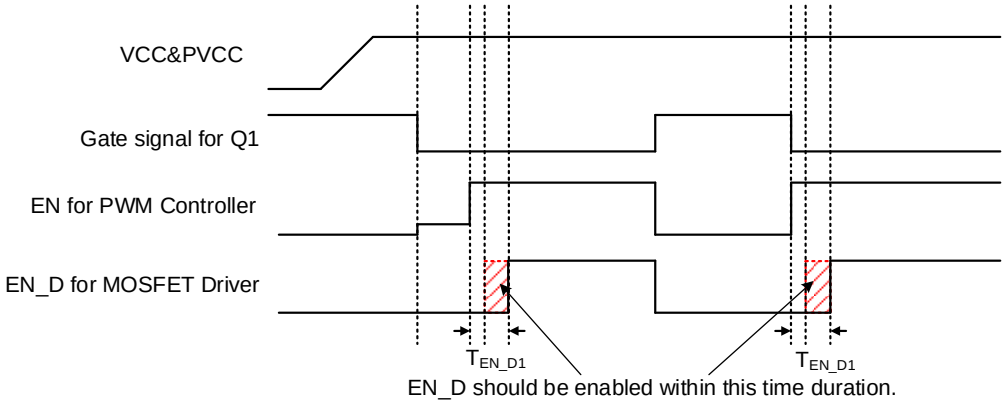


Figure 5. EN Sequence Control Diagram when Middle Drive Function is Enabled

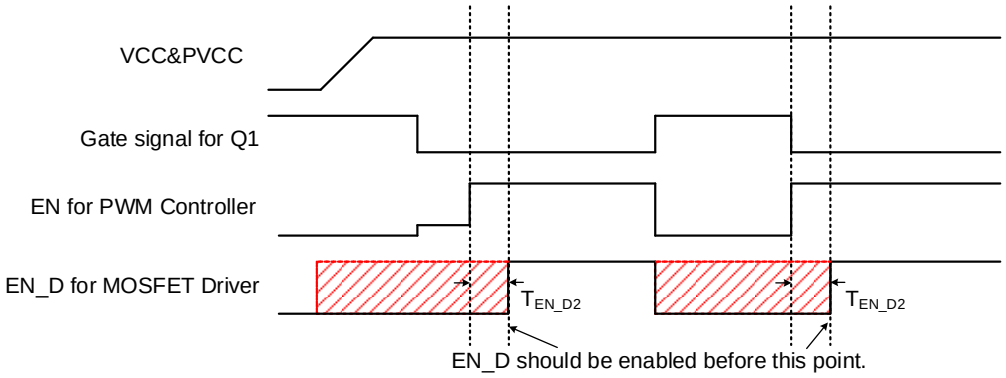


Figure 6. EN Sequence Control Diagram when Middle Drive Function is Disabled

15.3 Power-On and Power-Off Sequence

The RT8848C features a programmable soft-start function to limit the inrush current from power supply input. During the first power-on, the controller starts pin setting process when V_{EN} > 0.5V within typical 0.5ms initialization time (T_{INIT1}), where V_{EN} is established by a sourcing current I_{SOURCE_EN} = 10μA flowing through R_{EN}. After the end of pin setting process, the I_{SOURCE_EN} increases to 90μA and the V_{EN} is clamped by VCC at 4.5V. When V_{EN} >1.8V, there is an around 200μs delay time (T_{INIT2}) before the controller starts soft-start process. In the 200μs delay time, the controller keeps the PWM pins in high-impedance status and REFOUT outputs to 1.38V (typ.) if SPS mode is applied. The ramping up slew rate (SR_{RAMP}) of output voltage during soft-start process is determined by PINSET1 and can be modified by I^2C register 0x40[1]. The recommended soft-start slew rate is 1.5mV/μs for reducing inrush current during power-on. As output voltage reaches to V_{REFIN} after soft-start process, PGOOD will be pulled high by external voltage source with a resistor. The power-on sequence of RT8848C at first power-on is shown in Figure 7. Generally, the duration of power-on sequence from EN goes high to PGOOD goes high is less than 1.5ms. Besides, the I^2C R/W access can only work after the end of VR power-on sequence. It should be noticed that the Middle drive function is default disabled at first power-on. The Middle drive function will be activated after finishing pin setting process and provide driving capability for PWM pins.

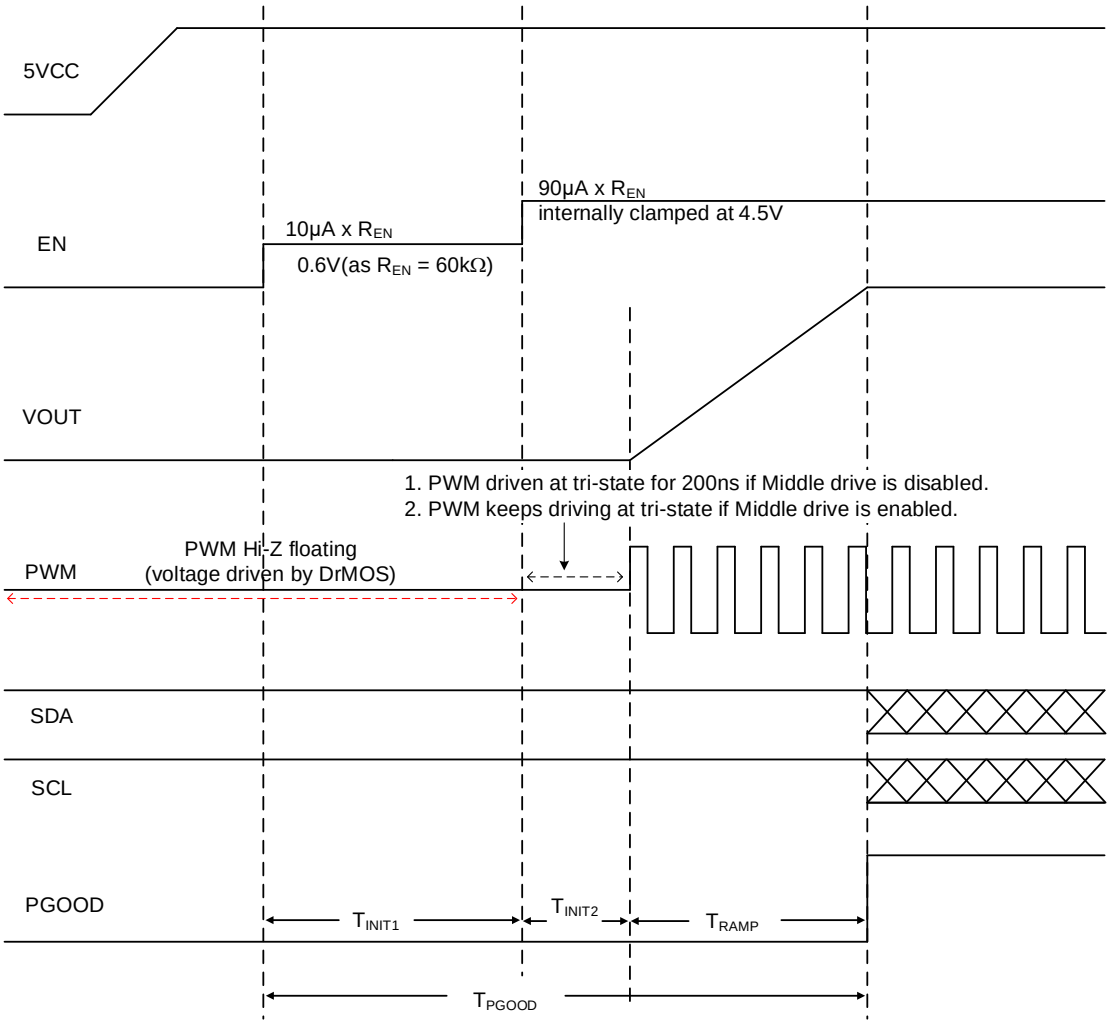


Figure 7. Power-On Sequence of RT8848C at First Power-On

Moreover, if RT8848C is powered up through EN re-toggle after first power-on, there is no pin setting process during power-on sequence. V_{EN} is directly established by a sourcing current I_{SOURCE_EN} = 90μA flowing through R_{EN}. When V_{EN} > 1.8V, there is an around 200μs delay time (T_{INIT2}) before the controller starts soft-start process. In the 200μs delay time, the controller keeps the PWM pins in tri-state status and REFOUT outputs to 1.38V (typ.) if SPS mode is applied. The ramping up slew rate (SR_{RAMP}) of output voltage during soft-start process follows the PINSET1 setting, which is detected at first power-on. The power-on sequence of RT8848C by EN re-toggle after first power-on is shown in Figure 8. It should be noticed that the I^2C registers keep the data unless VCC power recycle and I^2C R/W access only works after VR power-on sequence. It should also be noticed that the EN control sequence between the controller and driver should follow EN signal control diagram as shown in Figure 5 if Middle drive function is necessary.

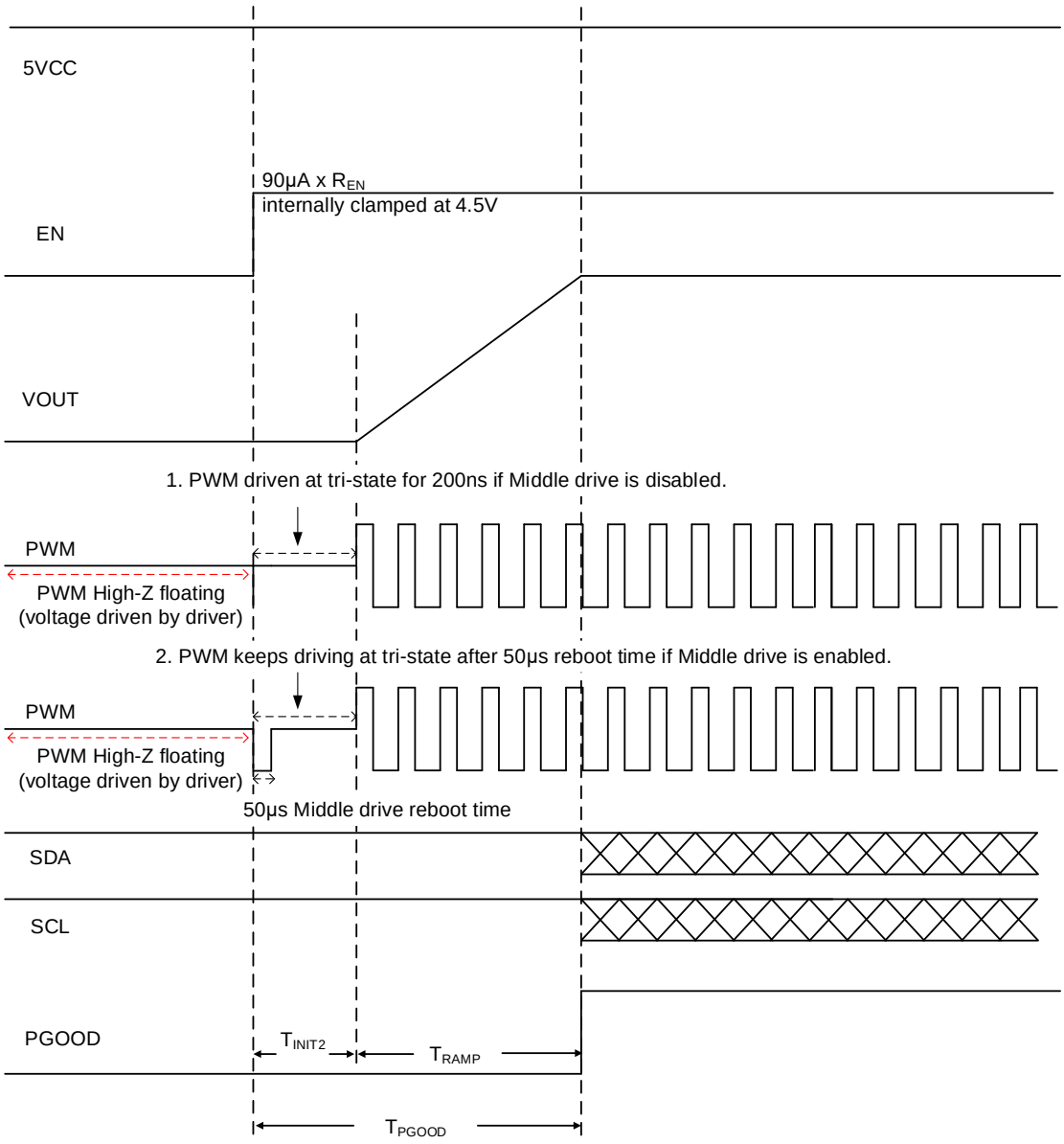


Figure 8. Power-On Sequence of RT8848C by EN re-toggle After First Power-On

As V_{EN} is pulled down to below 0.3V by external resistor or switch, the controller stops switching after 300ns delay and keeps all PWM output in tri-state. At the moment, the PGOOD signal is also pulled down by internal open-drain switch. In order to prevent short through from high-side MOSFET to low-side MOSFET, the PWM outputs a short low pulse before entering tri-state when PGOOD goes low. As a result, an internal switch will be turned on

to discharge the output capacitors through the route from VSEN trace to GND. The discharge impedance is around 70Ω. Besides, for the application of SPS mode, the REFOUT is also discharged by an internal resistor when EN goes low. The power-off sequence of RT8848C by EN is shown in Figure 9.

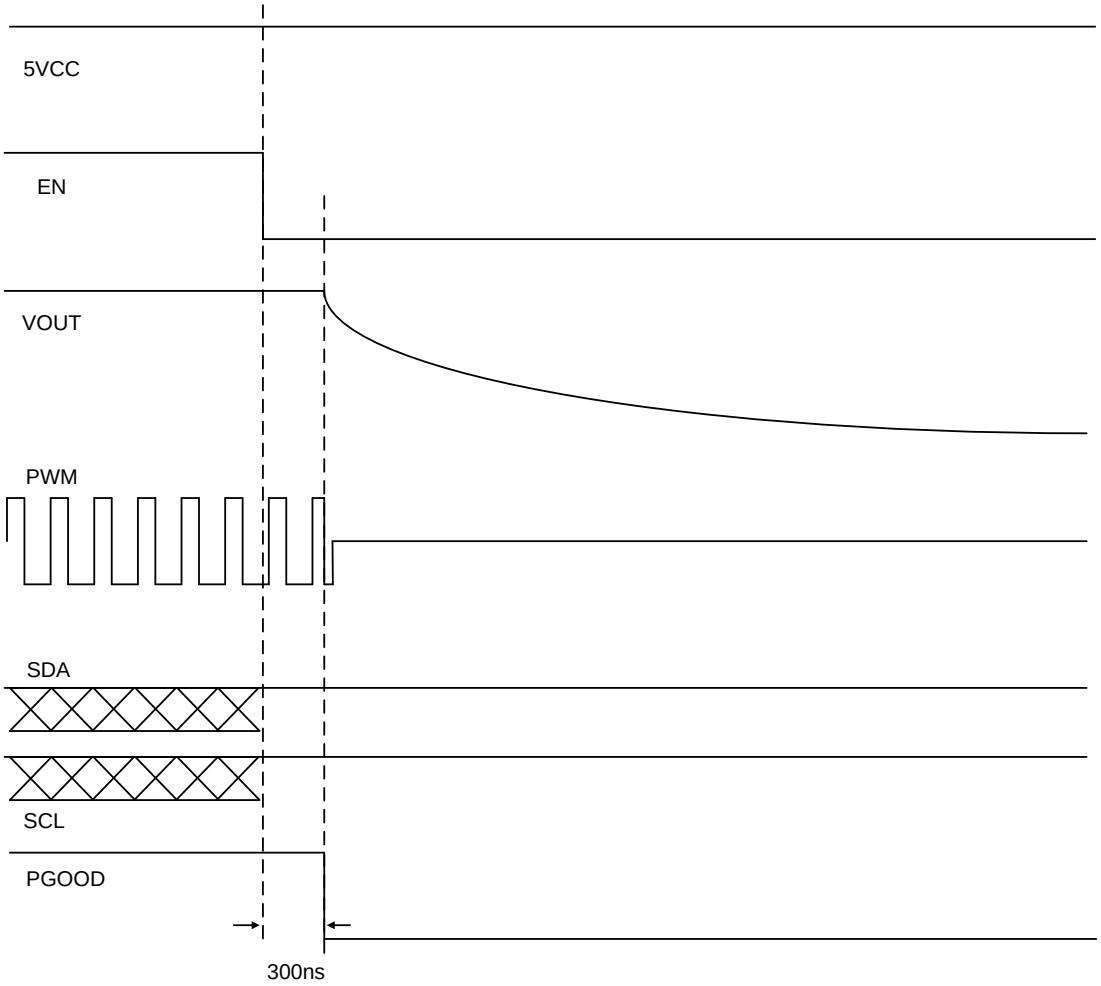


Figure 9. Power-Off Sequence of RT8848C by EN

15.4 PWMVID Function

The RT8848C supports PWMVID function to dynamically adjust the REFIN voltage for different GPU operating conditions. As shown in Figure 10, a PWMVID circuit consists of a PWM buffer, a bias V_{REF} voltage and a RC filter. An external PWM signal is applied to VID pin, which controls the PWM buffer output's high/low status. The output of buffer(REFADJ) is integrated by the external RC filter, and divided by a resister network to achieve reference voltage(REFIN). The voltage of REFIN can be calculated as:

$$V_{REFIN} = V_{REF} \times D \times \frac{R_{2\_VID} // \left(R_{3\_VID} + R_{4\_VID} + R_{5\_VID}\right)}{R_{1\_VID} + R_{2\_VID} // \left(R_{3\_VID} + R_{4\_VID} + R_{5\_VID}\right)} \times \frac{R_{4\_VID} + R_{5\_VID}}{R_{3\_VID} + R_{4\_VID} + R_{5\_VID}} +$$

$$V_{REF} \times \frac{R_{1\_VID} // \left(R_{3\_VID} + R_{4\_VID} + R_{5\_VID}\right)}{R_{2\_VID} + R_{1\_VID} // \left(R_{3\_VID} + R_{4\_VID} + R_{5\_VID}\right)} \times \frac{R_{4\_VID} + R_{5\_VID}}{R_{3\_VID} + R_{4\_VID} + R5\_VID}$$

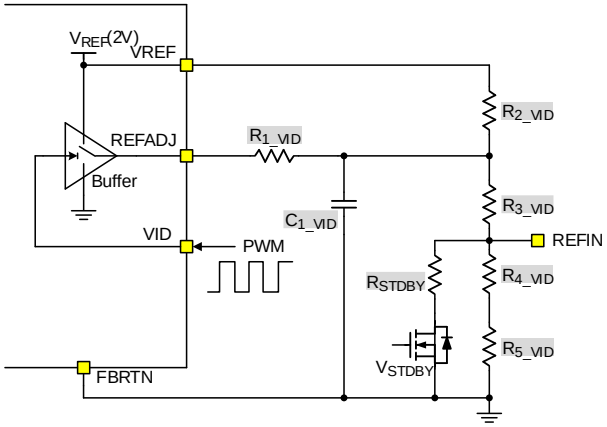


Figure 10. PWMVID Circuit

where V_{REF} is the bias reference voltage (typically 2V), and D is the duty cycle of PWM input signal. For internal LDO compensation, a decoupling capacitor of 0.1μF/0603 between VREF pin and local GND is necessary.

For PWMVID dynamic output voltage transition, the settling time that the output voltage transits from the old voltage to a new voltage depends on the time constant of PWMVID circuit, which can be calculated as:

$\tau = R_{1\_VID} // R_{2\_VID} // (R_{3\_VID} + R_{4\_VID} + R_{5\_VID}) \times C_{1\_VID}$ The settling time T_{SET_VID} of REFIN transition is around 5 times of τ which is independent of the voltage step size and PWM frequency.

$$T_{SET\_VID} = 5 \times \tau$$

Moreover, it should be noticed that the PWMVID function is only active after PGOOD goes high. Before activating PWMVID function, the REFADJ pin keeps at high impedance status.

15.5 BOOT Mode and Standby Mode

There are two operation modes included in PWMVID structure: boot mode and standby mode. In boot mode, the operation of output voltage ramps up in a power-on sequence. During boot mode, the controller ignores the PWMVID signal, and REFADJ enters high-impedance status before PGOOD goes high. The operating phase number in boot mode can be set via PINSET3 or I^2C register 0x45[3:1].

During standby mode, GPU stops the PWMVID transaction and sends a standby control signal to enter standby mode. An additional switch in parallel with original PWMVID resistors will be switched on to reduce the REFIN voltage. When V_{REFIN} is lower than 0.15V, the controller enters standby mode and all PWM outputs enter tri-state. On the other hand, the controller exits standby mode once V_{REFIN} is higher than 0.2V as standby control signal is released. The controller follows I^2C register 0x45[3:1] setting to decide the phase number during VOUT reboot. Besides, the PGOOD signal keeps high in standby mode. The V_{REFIN} in standby mode can be calculated as the following equation shows:

$$V_{REFIN} = V_{REF} \times \frac{R_{STDBY} // (R_{4\_VID} + R_{5\_VID})}{R_{2\_VID} + R_{3\_VID} + R_{STDBY} // (R_{4\_VID} + R_{5\_VID})}$$

15.6 Current Balance

The RT8848C senses each phase current through ISENx pin for current balance. The sensed current ICBx is mirrored to the current balance circuit, comparing with the average current, and adjusting each phase PWM width to optimize current and thermal balance. The current balance circuit increases the duty cycle of the phase which has smaller phase current as compared to other rails and decreases the duty cycle of the phase which has larger phase current. In addition, there are some registers for improving the current balance performance when the default setting cannot achieve good current balance result. The current balance gain and current balance offset

can be adjusted through I^{2}C register 0x11~0x20. The settings for each register are summarized at the section of register tables below. It increases current balance gain of the phase which has larger current than other rails or reduces current balance gain of the phase which has smaller current than other rails. If current balance cannot be improved by adjusting current balance gain, add an offset on the phase which has larger phase current than other rails. Moreover, the RT8848C also provides total current balance gain settings (0x55[4:3], 0x5F[1:0]) to add more flexibility on improving the current balance result with different board layout conditions.

15.7 Power State Input

The RT8848C supports automatic phase shedding and adjustable high/low phase count according to PSI input voltage. There are three operation modes: High Phase Count (HPC) mode, Auto Phase Shedding (APS) mode and Low Phase Count (LPC) mode.

Table 1 shows recommended PSI setting voltage threshold of the three operation modes. In LPC mode, the operation phase number is determined by PINSET2 or I^{2}C register 0x4F[6:4]. The operation phase number with respect to register settings are listed in Table 2. In APS mode, the operation phase number dynamically increases or decreases depending on output load current. In HPC mode, the controller operates in maximum phase number, which is determined by detecting the status of ISENx pins during PWM pin setting process at first power-on.

Table 1. Operation Mode and PSI Voltage Setting

Operation Mode	PSI Voltage Setting
High Phase Count Mode	1.6V to 5.5V
Auto Phase Shedding Mode	0.8V to 1.2V
Low Phase Count Mode	0V to 0.4V

Table 2. Operation Phase Number Setting in LPC Mode

Low Phase Count	Register 0x4F[6:4]
1Phase	000
2Phase	001
3Phase	010
4Phase	011
5Phase	100
6Phase	101
7Phase	110
8Phase	111

15.8 Auto Phase Shedding

The RT8848C provides Auto Phase Shedding (APS) function to dynamically change operating phase number depending on different output currents. The switching loss and conduction loss can be reduced in light load by reducing the phase number to improve light load efficiency. Moreover, the system efficiency can be optimized through changing phase number according to output load. The APS function is active when the following conditions are satisfied:

1. PSI pin voltage is within 0.8V to 1.2V.
2. APS function works as PGOOD goes high after power-on sequence

During the PWM pin setting process at first power-on, the APS current thresholds (APL1/APL2/APL3/APL4) are determined by PINSET3. After power-on, the APS current thresholds (APL1~APL4) can be modified by I^{2}C

registers (0x01~0x04) respectively. The hysteresis of APL1/APL2/APL3/APL4 and operating phase number at each stage are also programmable through I^2C registers (0x05~0x08, 0x09~0x0D) as shown in Table 3 and

Table 4. The APL1~APL4 thresholds can be calculated as:

V_{APL1} = DEC(0x01[7:0]) x 12.5mV

V_{APL2} = DEC(0x02[7:0]) x 12.5mV

V_{APL3} = DEC(0x03[7:0]) x 12.5mV

V_{APL4} = DEC(0x04[7:0]) x 12.5mV

The V_{IMON} reporting value is applied to compare with each APL threshold to change the phase number with regard to register setting. There are five current zones summarized as below:

If $V_{IMON} < V_{APL1}$, the controller operates in phase number PH_LCS0 as addressed in register 0x0D.

If $V_{APL1} < V_{IMON} < V_{APL2}$, the controller operates in phase number PH_LCS1 as addressed in register 0x0C.

If $V_{APL2} < V_{IMON} < V_{APL3}$, the controller operates in phase number PH_LCS2 as addressed in register 0x0B.

If $V_{APL3} < V_{IMON} < V_{APL4}$, the controller operates in phase number PH_LCS3 as addressed in register 0x0A.

If $V_{IMON} > V_{APL4}$, the controller operates in phase number PH_LCS4 as addressed in register 0x09.

When setting the operating phase number of each current zone, always keep the following rules:

Rule1: PH_LCS0 ≤ PH_LCS1 ≤ PH_LCS2 ≤ PH_LCS3 ≤ PH_LCS4

Rule2: $V_{APL1} \le V_{APL2} \le V_{APL3} \le V_{APL4}$

If violating either rule1 or rule2, the controller is forced into full phase operation mode. It requires to reboot VCC to unlock the APS logic latch in full phase mode.

The RT8848C also supports Soft Phase Shedding Down that there is a delay time (default = 80μs) within each phase zone transition to prevent output undershoot or overshoot from PSI switching during down phase shedding. The delay time is configurable through I^2C register 0x5D[2:0].

Table 3. APL Hysteresis Register Setting

	I^2C Register			
APL_HYS	APL_HYS1 0x05[2:0]	APL_HYS2 0x06[2:0]	APL_HYS3 0x07[2:0]	APL_HYS4 0x08[2:0]
0mV	000	000	000	000
12.5mV	001	001	001	001
25mV	010	010	010	010
37.5mV	011	011	011	011
50mV	100	100	100	100
62.5mV	101	101	101	101
75mV	110	110	110	110
87.5mV	111	111	111	111

Table 4. Operating Phase Number in Each Current Zone

	I²C Register				
Phase Number	PH_LCS0 0x0D[2:0]	PH_LCS1 0x0C[2:0]	PH_LCS2 0x0B[2:0]	PH_LCS3 0x0A[2:0]	PH_LCS4 0x09[2:0]
1Phase	000	000	000	000	000
2Phase	001	001	001	001	001
3Phase	010	010	010	010	010
4Phase	011	011	011	011	011
5Phase	100	100	100	100	100
6Phase	101	101	101	101	101
7Phase	110	110	110	110	110
8Phase	111	111	111	111	111

15.9 AC Droop

The RT8848C adopts an outstanding feature, i.e. AC-droop, to effectively suppress load transient ring back and to control overshoot well for zero loadline application. Figure 11 shows the condition without AC-droop control. The output voltage without AC-droop control has extra ring back ΔV2 due to C area charge.

Figure 12 shows the condition with AC-droop control. While loading occurs, the controller temporarily changes VID target to short-term voltage target. Short-term voltage target is related to transient loading current ΔI_{CC} and can be represented as the following:

Short_Term_Voltage_Target

DCR type

$$AC\_DROOP = V_{CS\_SUM} \times \frac{AI\_SET}{AV} = \frac{I_{OUT\_SUM} \times DCR}{N} \times \frac{AI\_SET}{AV}$$

N = phase number, AV = EA gain = R1_comp/R2_comp

AI_SET = 48/24/12/6

SPS type

$$AC\_DROOP = \frac{V_{CS\_SUM}}{8} \times \frac{AI\_SET}{AV} = \frac{I_{OUT\_SUM} \times DCR}{8} \times \frac{AI\_SET}{AV}$$

AI_SET = 12/6/3/2

AV = EA_GAIN = R_{1_comp}/R_{2_comp}

where the V_{CS_SUM} is the sum of current sensing signal from DCR sensing or SPS current sensing. For DCR sensing, the $V_{CS\_SUM} = V_{CSPSUM} - V_{CSNSUM} = I_{OUT\_SUM}$ x DCR/N. The current gain (AI) can be set by Pin Setting of AI Gain. Users can adjust AI gain by I²C register 0x41[3:2] to set desired short-term voltage target. The short-term voltage target reverts to VID target slowly after approximately 100μs. The short-term voltage target can help inductor current not to exceed loading current too much and then the ring back can be suppressed. Referring to Figure 12, the overshoot amplitude is reduced to only ΔV3.

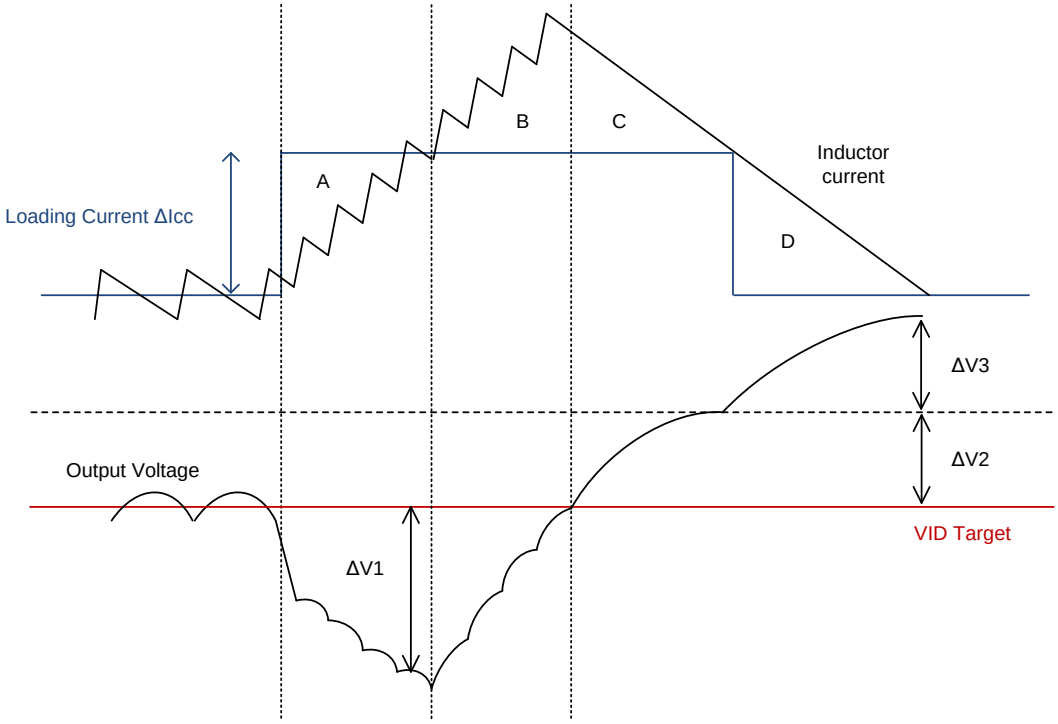


Figure 11. Zero Loadline without AC-droop Control

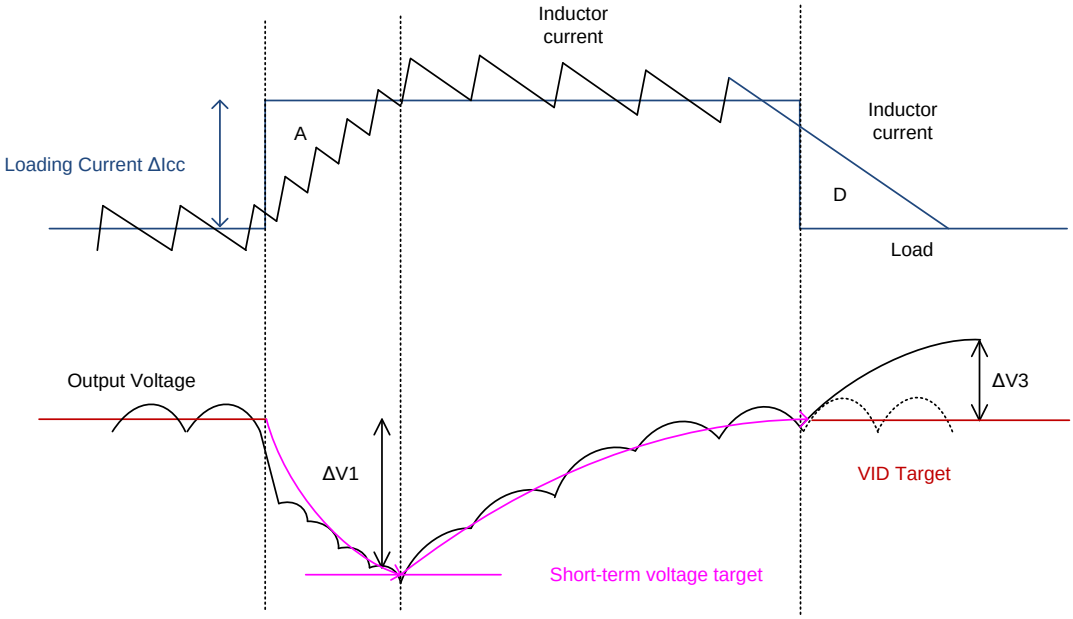


Figure 12. Zero Loadline with AC-droop Control

15.10 Power Good

The PGOOD pin is an open-drain output, and requires a pull-up resistor (10kΩ/0603). During soft-start time period, the PGOOD remains low. When the output voltage reaches to REFIN voltage, PGOOD is pulled high and latched. If one of the protections (OVP/UVP/SOC/TSEN/OTP) is triggered or EN goes low during operation, the PGOOD will be pulled low immediately.

15.11 Output Overvoltage Protection (OVP)

In order to prevent abnormal output high voltage which may induce catastrophic damage on chip or power devices, the RT8848C features an output OVP mechanism. According to different V_{REFIN} voltage setup, the OVP threshold has two methods to define. First, if V_{REFIN} is lower than 1.33V, the OVP threshold is fixed at absolute OVP protection threshold (typically 2V, programmable by I^2C register 0x25[1:0]). Second, if V_{REFIN} is higher than 1.33V, the OVP threshold is a relative OVP protection threshold, which equals to 1.5 times V_{REFIN} (the weighting factor is programmable by I^2C register 0x26[1:0]). A typical OVP protection mechanism is shown in Figure 13. When V_{SEN} is larger than OVP threshold for longer than 1µs deglitch time, the OVP protection is triggered. In the moment, the PGOOD is pulled down and NVP function is enabled. The OVP status is also recorded in I^2C register 0x2A[0]. After NVP function is enabled, the controller holds PWM at low status to discharge output capacitors until reaching VID reference. Besides, in order to prevent over large negative inductor current that may damage MOSFETs or driver, the controller switches PWM in tri-state or low pulse to regulate the output voltage at VID reference within 45µs before VID down. After 45µs delay time from the beginning of OVP triggering point, the controller starts to discharge the output voltage with a slow ramping down slew rate (1.5mV/µs). Within the soft-stop process, the controller holds PWM in tri-state as V_{SEN} is higher than VID reference and holds PWM in low status as V_{SEN} is larger than VID reference. Once OVP is triggered, the controller needs to re-toggle EN or re-cycle VCC to release from latched mode and clear I^2C flag 0x2A[0].

Moreover, the OVP function can be enabled or disabled through I^2C register 0x29[0]. It should be noticed that only analog OVP protection function can be disabled, the digital indicator of OVP (0x2A[0]) will be asserted if OVP is detected.

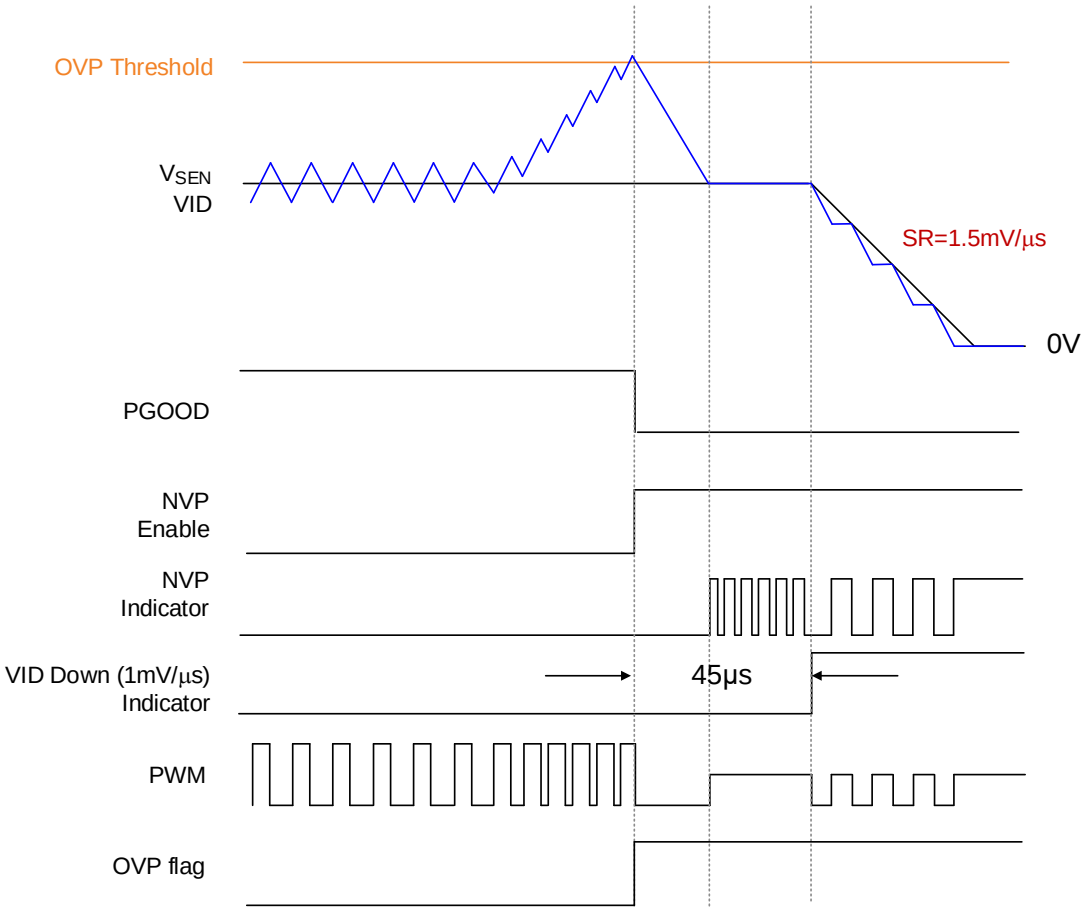


Figure 13. Output Overvoltage Protection Mechanism

15.12 Output Undervoltage Protection (UVP)

In order to prevent power stages from over-heating because of output voltage clamped by OCP, the RT8848C features an output UVP mechanism. A typical UVP protection mechanism is shown in Figure 14. If the output voltage drops below UVP trip threshold for longer than 3μs (typical), the UVP is triggered, and the controller forces all PWM outputs to tri-state, and an internal switch will be turned on to discharge the output capacitors through the route from VSEN trace to GND. The discharge impedance is around 70Ω. At the same time, the PGOOD is pulled down, and the UVP status is recorded in I^2C register 0x2A[1]. Besides, the UVP threshold is programmable through I^2C register 0x27[1:0]. The default threshold is 0.4 times VREFIN. Once UVP is triggered, the controller needs to re-toggle EN or re-cycle VCC to release from latched mode and clear I^2C flag 0x2A[1].

Moreover, the UVP function can be enabled or disabled through I^2C register 0x29[1]. It should be noticed that only analog UVP protection function can be disabled, and the digital indicator of UVP (0x2A[1]) will be asserted if UVP is detected. The UVP protection is masked during power-on sequence before PGOOD goes high.

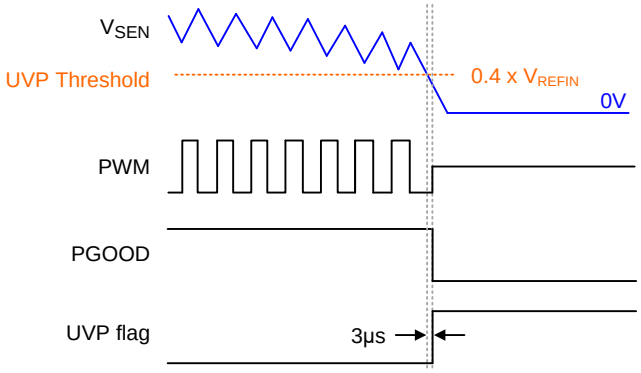


Figure 14. Typical UVP Protection Mechanism

15.13 Over-Temperature Protection (OTP)

The RT8848C features an OTP circuitry to prevent die overheating due to excessive power dissipation. A typical OTP protection mechanism is shown in Figure 15. When die temperature exceeds 150°C (programmable through I^2C register 0x28[1:0]) for longer than 45μs deglitch time, the controller forces all PWM outputs to tri-state. At the moment, the PGOOD is pulled down and the OTP status is recorded in I^2C register 0x2A[3]. For continuous operation, provide adequate cooling so that the junction temperature does not exceed OTP threshold. Once OTP is triggered, the controller needs to re-toggle EN or re-cycle VCC to release from latched mode and clear I^2C flag 0x2A[3].

Moreover, the OTP function can be enabled or disabled through I^2C register 0x29[3]. It should be noticed that only analog OTP protection function can be disabled, and the digital indicator of OTP (0x2A[3]) will be asserted if OTP is detected.

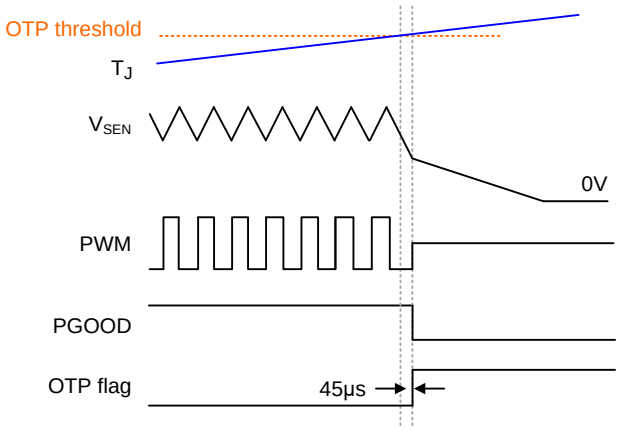


Figure 15. Typical OTP Protection Mechanism

15.14 TSEN Over-Temperature Protection (TSEN OTP)

The RT8848C features TSEN protection function which monitors the local temperature of power stages (MOSFETs or power inductors) during heavy load operation to prevent devices from overheating and catastrophic damage. According to operation modes of the controller, the TSEN protection can be categorized as DCR mode application and SPS mode application. As shown in Figure 16, the V_{TSEN} voltage is generated by a voltage divider. For different thermistor selection, the temperature can be monitored by a NTC or a PTC. For NTC case, a NTC thermistor is suggested to be placed near the hottest point of the power stage and in parallel with R_P, generally close to the power inductor and low-side MOSFET at phase 1. Besides, for PTC case, a PTC thermistor should be placed in parallel with R_S and near the hottest point of the power stage. For both cases, as temperature rises, the V_{TSEN} increases. The V_{TSEN} voltage is then converted to 8-bit digital data by internal ADC converter. The ADC result is compared with V_{TSEN} shutdown threshold, V_{TSEN_SD}, to trigger the protection mechanism. If V_{TSEN} is higher than V_{TSEN_SD} (V_{TSEN_SD} = 0.8V) for longer than deglitch time, which is programmable through I^2C register 0x33[1:0], the controller forces all PWM outputs to tri-state. At the moment, the PGOOD is pulled down and the TSEN OTP status is recorded in I^2C register 0x2A[4]. The protection mechanism is shown in Figure 18.

For PTCthermistor case, $V_{TSEN} = \frac{(R_S // R_{PTC})}{R_P + (R_S // R_{PTC})} \times V_{CC}$ For NTCthermistor case, $V_{TSEN} = \frac{R_S}{R_S + (R_P // R_{NTC})} \times V_{CC}$

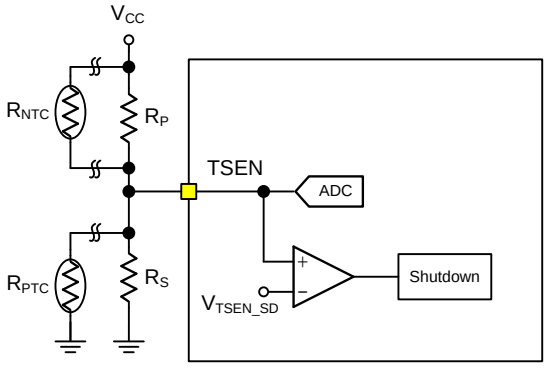


Figure 16. TSEN Pin Application Circuit in DCR Mode

On the other hand, Figure 17 shows a SPS mode application. The TSEN pin is connected to the TMON pin of SPS IC with a decoupling capacitor (C_F = 1nF/0603/6.3V) placed at local side of the controller to reduce noise coupling through layout trace. Generally, the temperature characteristic of SPS's TMON reporting is positive temperature coefficient. Therefore, as temperature rises, the V_{TSEN} increases. The V_{TSEN} voltage is then converted to 8-bit digital data by internal ADC converter. The ADC result is compared with V_{TSEN} shutdown threshold, V_{TSEN_SD}, to trigger the protection mechanism. If V_{TSEN} is larger than V_{TSEN_SD} (V_{TSEN_SD} = 0.8V) for longer than deglitch time, which is programmable through I^2C register 0x33[1:0], the controller forces all PWM outputs to tri-state. At the moment, the PGOOD is pulled down, and the TSEN OTP status is recorded in I^2C register 0x2A[4]. Besides, the design of R_{TS1} and R_{TS2} are based on the transfer function of T_J and V_{TMON} from SPS's datasheet. The protection mechanism is shown in Figure 18.

$$V_{TSEN} = \frac{R_{TS2}}{R_{TS1} + R_{TS2}} \times V_{TMON}$$

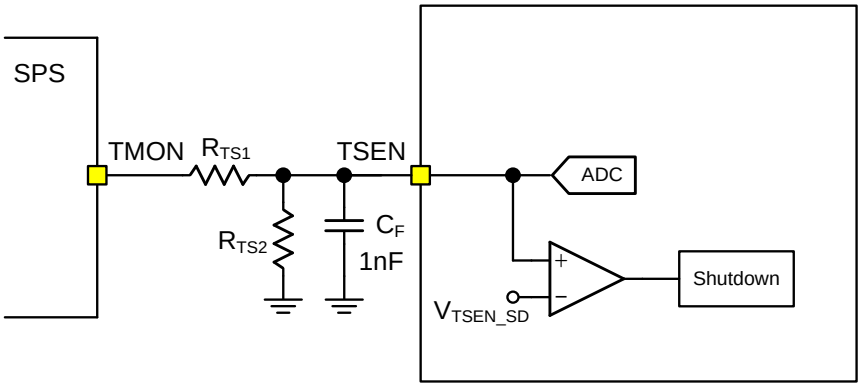


Figure 17. TSEN Pin Application Circuit in SPS Mode

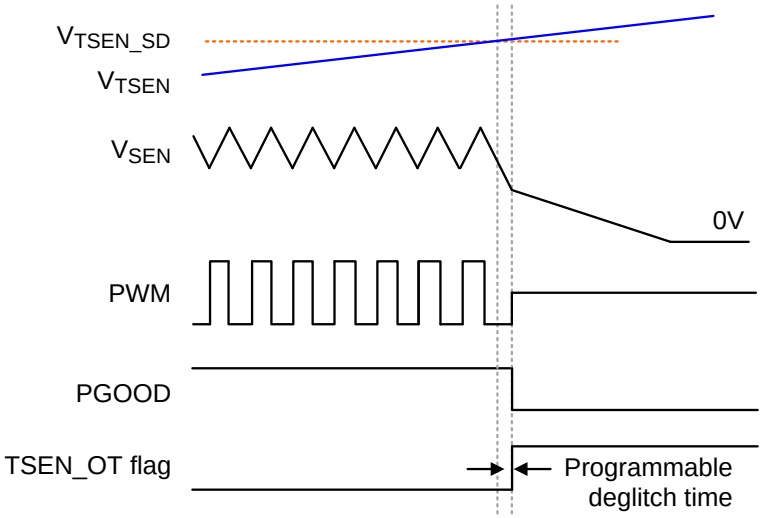


Figure 18. TSEN OTP Protection Mechanism with NTC or PTC

For both SPS mode and DCR mode, the controller needs to re-toggle EN or re-cycle VCC to release from latched mode and clear I^{2}C flag 0x2A[4] after TSEN OTP is triggered. Moreover, the TSEN OTP function can be enabled or disabled through I^{2}C register 0x29[4]. It should be noticed that only analog TSEN OTP protection function can be disabled, the digital indicator of TSEN OTP (0x2A[4]) will be asserted if TSEN OTP is detected.

15.15 Sum Overcurrent Protection (SOCP)

The RT8848C provides Sum Overcurrent Protection (SOCP) to prevent power system from overcurrent operation. The SOCP protection circuit is shown in Figure 19. First, the per-phase inductor currents are added together to generate a mirrored current I_{SUM}. The I_{SUM} is in parallel with a I_{BIAS}, which provides a fixed 0.6V offset on V_{IMON}, and flowing out from IMON pin to an external resistor, R_{IMON}. The voltage across R_{IMON} is then converted to 8-bit digital data by internal ADC converter. The ADC result is compared with SOCP threshold, $V_{IMON\_OC\_TH}$ (programmable through I^{2}C register 0x24[5:0]), to trigger the protection mechanism. According to the application type (SPS type or DCR type), the V_{IMON} has different calculation formulas. The formulas are demonstrated as below:

For SPS type, V_{IMON} (V) = V_{CS_SUM} (V)/8 x 1.5 x R_{IMON} (kΩ) + 0.6V

For DCR type, V_{IMON} (V) = V_{CS_SUM} (V) x 1.5 x R_{IMON} (kΩ) + 0.6V

, where V_{CS_SUM} is the current sensing voltage from DCR sum current sensing network or SPS's IMON feedback

signal. It should be noticed that SPS's V_{CS_SUM} current is the sum of current signal inputs from ISEN1 to ISEN8. Therefore, the selection of R_{IMON} for a specified total load current protection can be derived as below:

For SPS type, R_{IMON} (kΩ) = [$V_{IMON\_OC\_TH}$ (V) – 0.6V]/$V_{CS\_SUM,max}$ (V)/1.5 x 8

For DCR type, R_{IMON} (kΩ) = [$V_{IMON\_OC\_TH}$ (V) – 0.6V]/$V_{CS\_SUM,max}$ (V)/1.5

, where $V_{CS\_SUM,max}$ is the current sensing voltage at the specified limitation of total load current.

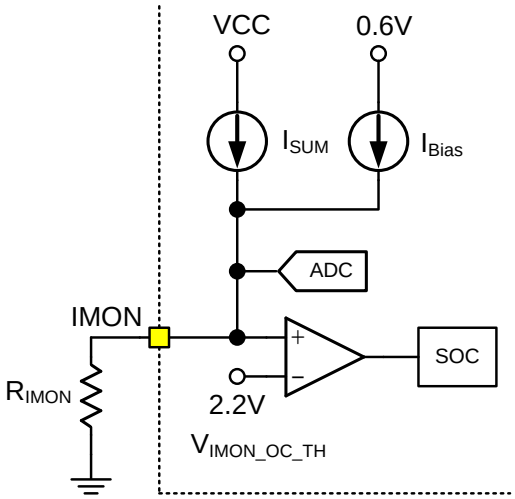


Figure 19. Sum OCP Protection Circuit

The protection mechanism of SOCP is shown in Figure 20. As the total load current increases, the voltage of V_{IMON} increases proportionally. If V_{IMON} is larger than $V_{IMON\_OC\_TH}$ for longer than deglitch time, which is programmable through I^2C register 0x23[1:0], the controller forces all PWM outputs to tri-state. At the moment, the PGOOD is pulled down and the SOCP status is recorded in I^2C register 0x2A[2]. Once SOCP is triggered, the controller needs to re-toggle EN or re-cycle VCC to release from latched mode and clear I^2C flag 0x2A[2].

Moreover, the SOCP function can be enabled or disabled through I^2C register 0x29[2]. It should be noticed that only analog SOCP protection function can be disabled; the digital indicator of SOCP (0x2A[2]) will be asserted if SOCP is detected. DO NOT put any decoupling capacitor near IMON pin since it affects the accuracy of IMON reporting.

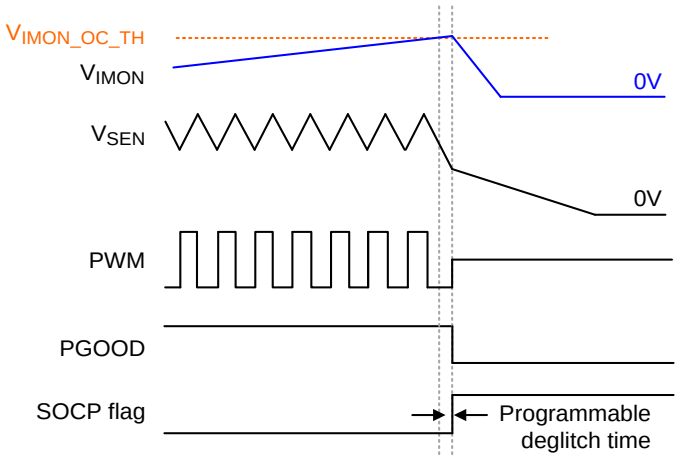


Figure 20. Sum OCP Protection Mechanism

15.16 Per-Phase Overcurrent Protection (Per-Phase OCP)

The RT8848C features per-phase current limit mechanism to prevent overcurrent event. The per-phase current

limit circuit employs a unique “valley” current sensing algorithm. If the magnitude of the current sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The per-phase OCP protection circuit is shown in Figure 21. The per-phase current-limit threshold is decided by the differential voltage across R_{CH_OC}, V_{CH_OC}, which is generated by an internal current source (programmable through I^2C register 0x21[7:0], 0x22[7:0]). When DCR sensing circuit is adopted, in order to ensure the accuracy of current signal over a wide range of temperatures, it is recommended to use a PTC thermistor in parallel with R_{CH_OC}. The PTC thermistor should be placed near power inductor at phase 1. Then, the current-limit threshold can be calculated by the following equation:

$$V_{CH\_OC}(V) = 20\mu \times R_{CH\_OC}(\Omega)$$

$$I_{OC\_PH\_Valley}(A) = \frac{V_{CH\_OC}(V) - 0.6}{16 \times DCR(\Omega)}$$

Where the $I_{OC\_PH\_Valley}$ is the per-phase inductor valley current-limit threshold and DCR is the inductor’s DCR resistor. For SPS type application, the DCR represents the current reporting gain of SPS chip. Moreover, it should be noticed that the per-phase OCP limits the inductor valley current instead of average current. When average output current is larger than ($I_{OC\_PH\_Valley}$ + $\Delta I_L/2$), the output voltage will start to ramp down because inductor valley current is limited by OCP threshold. The output capacitor is discharged by the current deviation between inductor current and output load. Besides, the OCP indicator is detected dynamically according to the comparator output of per-phase OCP protection circuit. The protection mechanism of per-phase OCP is shown in Figure 22. The per-phase OCP flag (recorded in I^2C register 0x2B[7:0]) is asserted as inductor sensing current, I_{MON_PH}, is larger than I_{OC_PH}. On the other hand, if inductor sensing current is lower than I_{OC_PH}, the OCP flag is de-asserted. There is around 100ns comparator delay time in per-phase OCP protection circuit. Also, the PGOOD remains at high status during OCP process.

In addition, for multi-phase application with common-N DCR current sensing circuit, the PCB impedance from inductor output point to VOUT remoting point (GPU side) induces a DC offset on current feedback signal as shown in Figure 36 in Application Information section.

$$V_{CSi} = \frac{\left(1 + \frac{sL}{DCR}\right)}{(1 + sC_XR_X)} \times DCR \times I_{Li} + \frac{I_{Li} \times R_{pcbi} - \frac{1}{N} \times \sum_{i=1}^{N} I_{Li} \times R_{pcbi}}{(1 + sC_XR_X)}$$ The OCP design threshold should be adjusted according to Rpcb values. There are OCP gains which are programmable through I^2C registers (0x21[7:0], 0x22[7:0]) to adjust OCP threshold for each phase based on V_{CH_OC}, which is decided by R_{CH_OC}. The OCP threshold with OCP gain factor for each phase can be represented as below:

$$I_{OC\_PH\_Valley}(A) = \frac{V_{CH\_OC}(V) \times OCP\_gain - 0.6}{16 \times DCR(\Omega)}$$

When considering the Rpcb term in current sensing feedback signal, the OCP should follow below methods to design. The OCP gain is applied to compensate the Rpcb term offset on DCR term (real current signal). The design target is to make each phase’s real OCP threshold equal. Therefore, the one with Rpcb_min should be programmed with minimum OCP gain (ex. 0.7x). And the equation can be simplified as below:

$$I_{OC} \times \left(DCR + R_{pcb\_min} - R_{pcb\_avg}\right) \times 16 + 0.6V = V_{CH\_OC} \times 0.7$$

The other phases should follow the Rpcb deviation value to choose the suitable OCP gain.

$$OCP\_gain = \frac{I_{OC} \times \left(DCR + R_{pcb\_n} - R_{pcb\_avg}\right) \times 16 + 0.6}{V_{CH\_OC}}$$, where Rpcb_n is the Rpcb trace value of phase N.

For different types of application, if per-phase OCP is not necessary, users can disable the per-phase OCP function by I^2C register 0x4D[1:0].

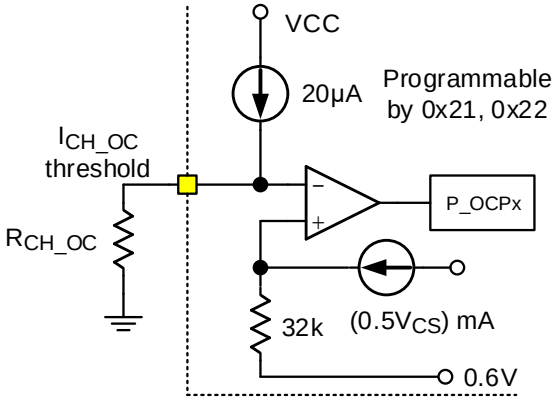


Figure 21. Per-Phase OCP Protection Circuit

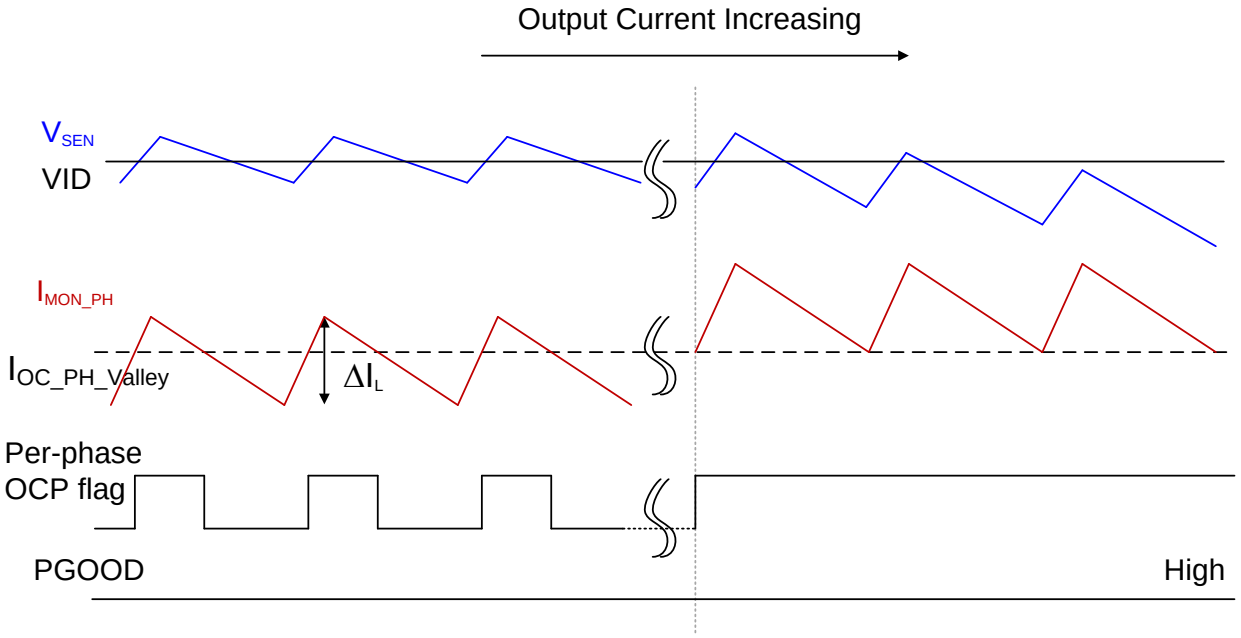


Figure 22. Per-Phase OCP Protection Mechanism

ADC Function

The RT8848C supports analog to digital converter (ADC) to monitor VSEN, VIMON and VTSEN voltages. The ADC function is initialized and starts to work after PGOOD signal has been pulled high. The ADC circuits for VSEN and TSEN operates periodically with time space of 40.5μs and the ADC circuit for VIMON operates periodically with time space of 13.5μs. Users can access the ADC results from I^2C registers 0x2E[7:0], 0x2F[7:0] and 0x30[7:0] for voltage of VIMON, VSEN and VTSEN respectively. The voltage measurement reported in these registers are an average measurement over time period defined in I^2C register 0x31[1:0], 0x32[1:0] and 0x33[1:0] respectively. Besides, the ADC circuit for VIMON conversion will shorten the operation time space to 6.75μs when SOCP is triggered to prevent power stage from overcurrent operation. The SOCP delay time can be programmed by I^2C register 0x23[1:0]. The definition of registers are summarized in the section of register tables below.

16 Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

16.1 PINSET Pin Setting

The RT8848C features PINSET pin setting function for multi-functional programming. There are total three PINSET groups provided by RT8848C to support different application configurations. The PINSET functions are defined with related I^{2}C registers, and the function assignments are summarized in Table 5.

Table 5. PINSET Function Assignments

	Bit 3	Bit 2	Bit 1	Bit 0
PINSET1_V: 0x40	Ramp Amplitude		Soft-start Slew Rate	PWM Tri-state Voltage Level
PINSET1_I: 0x41	AI Gain		SPS/DCR Mode Selection	
PINSET2_V: 0x42	Per-phase Switching Frequency		Address Code for Slave Device	
PINSET2_I: 0x43	Middle Drive Enable/Disable	Operating Phase Number in PSI = L		
PINSET3_V: 0x44	APL Thresholds			
PINSET3_I: 0x45	Operating Phase Number during Cold/Warm Boot			

For PINSET1 pin setting circuit as shown in Figure 23, a pair of voltage dividers is used to set up the internal ramp amplitude, soft-start slew rate, PWM tri-state voltage level, AI gain and SPS/DCR mode selection. There is an internal current source (80μA) flowing out from PINSET1 pin to external resistor. The voltage across $R_{2\_PINSET1}$ is then sensed by internal sensor and decoded to decide the PINSET1 configuration. Besides, the ramp amplitude can also be set via I^{2}C register 0x4F[3:0]. The soft-start slew rate can be set via I^{2}C register 0x40[1]. The PWM tri-state voltage level cab be set via I^{2}C register 0x40[0]. The AI gain can be set via I^{2}C register 0x41[3:2]. The SPS/DCR mode selection can be set via I^{2}C register 0x41[1].

For PINSET2 pin setting circuit as shown in Figure 24, a pair of voltage dividers is used to set up the per-phase switching frequency, address code for slave device, middle drive function and operating phase number in PSI = L. There is an internal current source (80μA) flowing out from PINSET2 pin to external resistor. The voltage across $R_{2\_PINSET2}$ is then sensed by internal sensor and decoded to decide the PINSET2 configuration. Besides, the per-phase switching frequency can also be set via I^{2}C register 0x0F[4:0]. The address code for slave device can be set via I^{2}C register 0x42[1:0]. The middle drive function can be set via I^{2}C register 0x43[3]. The operating phase number in PSI=L can be set via I^{2}C register 0x4F[6:4].

For PINSET3 pin setting circuit as shown in Figure 25, a pair of voltage dividers is used to set up the APL thresholds and operating phase number during cold/warm boot. There is an internal current source (80μA) flowing out from PINSET3 pin to external resistor. The voltage across $R_{2\_PINSET3}$ is then sensed by internal sensor and decoded to decide the PINSET3 configuration. Besides, the APL thresholds can also be set via I^{2}C register 0x01[7:0] to 0x04[7:0] respectively. The operating phase number during cold/warm boot can be set via I^{2}C register 0x45[3:1]. If PINSET3 is not necessary, users can leave this pin floating and the default setting for RT8848C is shown in Table 6. It should be noticed that APS function is disabled by 0x2D[0]=1 and PSI logic is also locked at high logic,

which makes RT8848C operate in full phase condition. If users want to enable APS and PSI function after power-on, the APS function can be turned on by register 0x2D[0]=0 and PSI function can be activated by register 0x2D[2]=0.

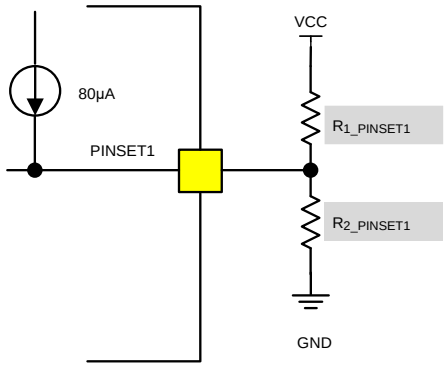


Figure 23. PINSET1 Pin Setting Circuit

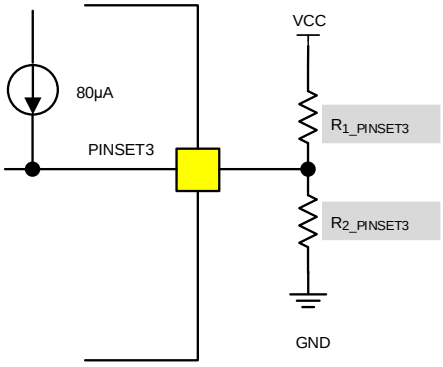


Figure 25. PINSET3 Pin Setting Circuit

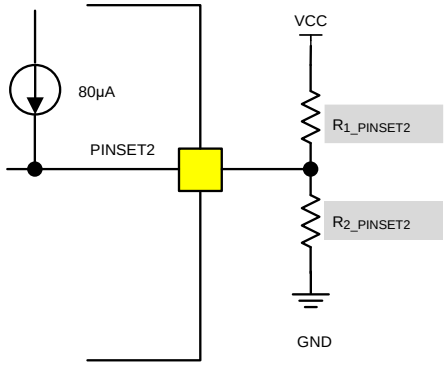


Figure 24. PINSET2 Pin Setting Circuit

Table 6. Register Setting Configuration as PINSET3 is Floating

Register	Default Code	Function Setting
0x44[3:0]	1000	APL1 = 0.2V APL2 = 0.4V APL3 = 0.8V APL4 = 1.2V
0x45[3:1]	111	Operation phase number during soft-start = 8Phase
0x2D[2]	1	Internal PSI logic locks at high logic no matter external PSI pin configuration
0x2D[0]	1	Disable APS mode and operating in full phase mode

For different PINSET1/PINSET2/PINSET3 configurations, the recommended resistor values are summarized in Table 7. In order to reduce the complexity of design, a useful design tool and GUI are well prepared for the development of GPU power with RT8848C.

Table 7. PINSET1/PINSET2/PINSET3 Register Table

PINSET1/PINSET2/PINSET3 Register Table					
CODEV 0x40[3:0] 0x42[3:0] 0x44[3:0]	CODEI 0x41[3:1] 0x43[3:1] 0x45[3:1]	SETV (mV)	SETI (mV)	R1(kΩ)	R2(kΩ)
0000	000	50	100	open	1.25
0000	001	50	300	open	3.75
0000	010	50	500	open	6.25
0000	011	50	700	open	8.75
0000	100	50	900	open	11.25
0000	101	50	1100	open	13.75
0000	110	50	1300	open	16.25
0000	111	50	1500	open	18.75
0001	000	150	100	41.67	1.29
0001	001	150	300	125.00	3.87
0001	010	150	500	208.33	6.44
0001	011	150	700	291.67	9.02
0001	100	150	900	375.00	11.60
0001	101	150	1100	458.33	14.18
0001	110	150	1300	541.67	16.75
0001	111	150	1500	625.00	19.33
0010	000	250	100	25.00	1.32
0010	001	250	300	75.00	3.95
0010	010	250	500	125.00	6.58
0010	011	250	700	175.00	9.21
0010	100	250	900	225.00	11.84
0010	101	250	1100	275.00	14.47
0010	110	250	1300	325.00	17.11
0010	111	250	1500	375.00	19.74
0011	000	350	100	17.86	1.34
0011	001	350	300	53.57	4.03
0011	010	350	500	89.29	6.72
0011	011	350	700	125.00	9.41
0011	100	350	900	160.71	12.10
0011	101	350	1100	196.43	14.78
0011	110	350	1300	232.14	17.47
0011	111	350	1500	267.86	20.16
0100	000	450	100	13.89	1.37
0100	001	450	300	41.67	4.12

PINSET1/PINSET2/PINSET3 Register Table					
CODEV 0x40[3:0] 0x42[3:0] 0x44[3:0]	CODEI 0x41[3:1] 0x43[3:1] 0x45[3:1]	SETV (mV)	SETI (mV)	R1(kΩ)	R2(kΩ)
0100	010	450	500	69.44	6.87
0100	011	450	700	97.22	9.62
0100	100	450	900	125.00	12.36
0100	101	450	1100	152.78	15.11
0100	110	450	1300	180.56	17.86
0100	111	450	1500	208.33	20.60
0101	000	550	100	11.36	1.40
0101	001	550	300	34.09	4.21
0101	010	550	500	56.82	7.02
0101	011	550	700	79.55	9.83
0101	100	550	900	102.27	12.64
0101	101	550	1100	125.00	15.45
0101	110	550	1300	147.73	18.26
0101	111	550	1500	170.45	21.07
0110	000	650	100	9.62	1.44
0110	001	650	300	28.85	4.31
0110	010	650	500	48.08	7.18
0110	011	650	700	67.31	10.06
0110	100	650	900	86.54	12.93
0110	101	650	1100	105.77	15.80
0110	110	650	1300	125.00	18.68
0110	111	650	1500	144.23	21.55
0111	000	750	100	8.33	1.47
0111	001	750	300	25.00	4.41
0111	010	750	500	41.67	7.35
0111	011	750	700	58.33	10.29
0111	100	750	900	75.00	13.24
0111	101	750	1100	91.67	16.18
0111	110	750	1300	108.33	19.12
0111	111	750	1500	125.00	22.06
1000	000	850	100	7.35	1.51
1000	001	850	300	22.06	4.52
1000	010	850	500	36.76	7.53
1000	011	850	700	51.47	10.54
1000	100	850	900	66.18	13.55

PINSET1/PINSET2/PINSET3 Register Table					
CODEV 0x40[3:0] 0x42[3:0] 0x44[3:0]	CODEI 0x41[3:1] 0x43[3:1] 0x45[3:1]	SETV (mV)	SETI (mV)	R1(kΩ)	R2(kΩ)
1000	101	850	1100	80.88	16.57
1000	110	850	1300	95.59	19.58
1000	111	850	1500	110.29	22.59
1001	000	950	100	6.58	1.54
1001	001	950	300	19.74	4.63
1001	010	950	500	32.89	7.72
1001	011	950	700	46.05	10.80
1001	100	950	900	59.21	13.89
1001	101	950	1100	72.37	16.98
1001	110	950	1300	85.53	20.06
1001	111	950	1500	98.68	23.15
1010	000	1050	100	5.95	1.58
1010	001	1050	300	17.86	4.75
1010	010	1050	500	29.76	7.91
1010	011	1050	700	41.67	11.08
1010	100	1050	900	53.57	14.24
1010	101	1050	1100	65.48	17.41
1010	110	1050	1300	77.38	20.57
1010	111	1050	1500	89.29	23.73
1011	000	1150	100	5.43	1.62
1011	001	1150	300	16.30	4.87
1011	010	1150	500	27.17	8.12
1011	011	1150	700	38.04	11.36
1011	100	1150	900	48.91	14.61
1011	101	1150	1100	59.78	17.86
1011	110	1150	1300	70.65	21.10
1011	111	1150	1500	81.52	24.35
1100	000	1250	100	5.00	1.67
1100	001	1250	300	15.00	5.00
1100	010	1250	500	25.00	8.33
1100	011	1250	700	35.00	11.67
1100	100	1250	900	45.00	15.00
1100	101	1250	1100	55.00	18.33
1100	110	1250	1300	65.00	21.67
1100	111	1250	1500	75.00	25.00

PINSET1/PINSET2/PINSET3 Register Table					
CODEV 0x40[3:0] 0x42[3:0] 0x44[3:0]	CODEI 0x41[3:1] 0x43[3:1] 0x45[3:1]	SETV (mV)	SETI (mV)	R1(kΩ)	R2(kΩ)
1101	000	1350	100	4.63	1.71
1101	001	1350	300	13.89	5.14
1101	010	1350	500	23.15	8.56
1101	011	1350	700	32.41	11.99
1101	100	1350	900	41.67	15.41
1101	101	1350	1100	50.93	18.84
1101	110	1350	1300	60.19	22.26
1101	111	1350	1500	69.44	25.68
1110	000	1450	100	4.31	1.76
1110	001	1450	300	12.93	5.28
1110	010	1450	500	21.55	8.80
1110	011	1450	700	30.17	12.32
1110	100	1450	900	38.79	15.85
1110	101	1450	1100	47.41	19.37
1110	110	1450	1300	56.03	22.89
1110	111	1450	1500	64.66	26.41
1111	000	1550	100	4.03	1.81
1111	001	1550	300	12.10	5.43
1111	010	1550	500	20.16	9.06
1111	011	1550	700	28.23	12.68
1111	100	1550	900	36.29	16.30
1111	101	1550	1100	44.35	19.93
1111	110	1550	1300	52.42	23.55
1111	111	1550	1500	60.48	27.17

[Note] Users should strictly follow the table for PINSET1/PINSET2/PINSET3 pin setting. The resistor value variation should be within ± 1% of the recommended value. Richtek has developed a useful design tool to support PINSET resistors selection.

16.2 Switching Frequency

The switching frequency of RT8848C is programmable by two methods. One is by PINSET2 pin setting with external resistors. The pin setting for switching frequency is detected at first power-on and can be changed by I^2C command later. The other method is by changing I^2C register 0x0F[4:0] after first power-on. The register will keep the written data unless VCC power is recycled.

The RT8848C supports diode emulation mode (DEM) to improve the efficiency at light load. It should be noticed that DEM can only be activated as the controller operates in single phase and PSI=L or PSI=M. The DEM function is adjustable by I^2C register 0x2D[1]. When 0x2D[1]=0, the DEM function is enabled. In DEM, the controller automatically reduces switching frequency at light load conditions to maintain high efficiency. The reduction of frequency is achieved smoothly. As the output current decreases from heavy load conditions, the inductor current is also reduced, and eventually comes to the point that its current valley touches zero, which is the boundary between continuous conduction and discontinuous conduction modes. To emulate the behavior of diodes, the controller changes the PWM output from low-state to tri-state when the inductor sensing current is lower than zero-current detection (ZCD) threshold (typically 0A). The ZCD threshold can be adjusted by enabling ZCD offset function through I^2C register 0x34[5:0]. As the load current is further decreased, it takes longer time to discharge the output capacitor to the level that requires the next “ON” cycle. Contrarily, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction. The transition load point between DEM and CCM operation is shown in Figure 26 and can be calculated as follows:

$$I_{LOAD\_BCM} = \frac{V_{IN} - V_{OUT}}{2L} \times t_{ON}$$

,where t_{ON} is the on-time of high-side MOSFET.

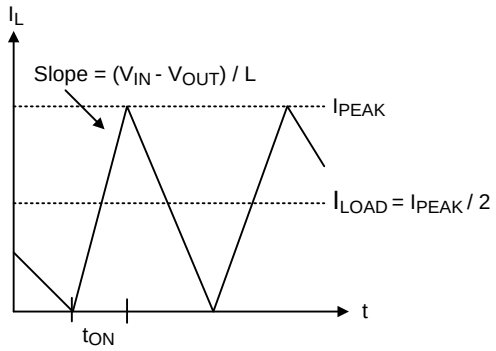


Figure 26. Boundary Condition of DEM/CCM

The switching frequency in DEM can be calculated as follows:

$$f_{SW}(I_{LOAD}) = \frac{2LI_{LOAD}}{V_{IN}t_{ON}^2\left(\frac{V_{IN}}{V_{OUT}} - 1\right)}$$

,where I_{LOAD} is smaller than I_{LOAD_BCM}.

As shown in the equation, switching frequency is a function of output load current, I_{LOAD}, and it is proportional to I_{LOAD}, which means it becomes higher at heavy load and reduces to almost zero at a very light load. Besides, inductor selection can also change the switching frequency in DEM. Choosing large inductance makes more switching loss as compared to small inductance. However, the core loss of inductor increases with larger inductor

current ripple for a given inductor. That is, proper selection of inductor based on efficiency target is important.

On the other hand, as 0x2D[1]=1, the DEM function is disabled. The controller always operates in continuous conduction mode (CCM), unlike DEM that enables zero current detection to reject negative inductor current when low-side MOSFET turns on. The inductor current can be negative until next on-time is generated in CCM. The switching frequency is approximately unchanged from no load to full load. Therefore, benefits like better transient response from light load to heavy load and smaller EMI/EMC come along with CCM. Nevertheless, poor efficiency in light load is a tradeoff.

There is a limitation to the controller's output PWM frequency. Since the minimum PWM pulse width is around 50ns (typical), the switching frequency starts to decrease as the conversion ratio of VOUT to VIN is too small, which makes equivalent on time pulse smaller than minimum PWM pulse width. Besides, when VID is set below 0.6V, the switching frequency follows the equation below to change.

$$f_{sw} = \frac{VID}{0.6} \times f_{sw\_set}$$

, where the f_{SW_set} is the desired frequency set by PINSET2 or I^2C register 0x0F[4:0]. The relation of f_{SW} and VID setting is shown in Figure 27.

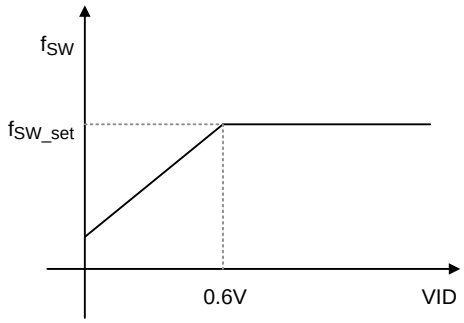


Figure 27. Frequency Setting vs. VID

16.3 Remote Sense Setting

In order to allow the load voltage to be accurately detected to avoid the voltage drop from output to load, the RT8848C uses a high-accuracy differential amplifier to directly detect the voltage at the end of GPU through the VSEN and FBRTN pins. The VOUT sensing network from the controller to the output load needs to be specially designed according to different load conditions. The output voltage detection circuit has two loops, the remote sense path (from the controller to the load end of GPU) and the local sense path (from the controller to the output capacitor) as shown in

Figure 28. When the load is GPU, in order to make the GPU voltage consistent with REFIN, the R_{Remote} must be set to 0Ω. At this time, the purpose of local sense path is to avoid the output overvoltage caused by the GPU disconnection. Therefore, the R_{Local} must be placed a 10Ω to 100Ω resistor. If the GPU is not used, the R_{Local} must be set to 0Ω to avoid PWM jitter caused by delayed output voltage signal. Considering the components placement, it is recommended to place all the detecting resistors on the controller side. This setting can minimize the path of local sense, and make the system debug easier as any noise coupling occurs on the sensing path.

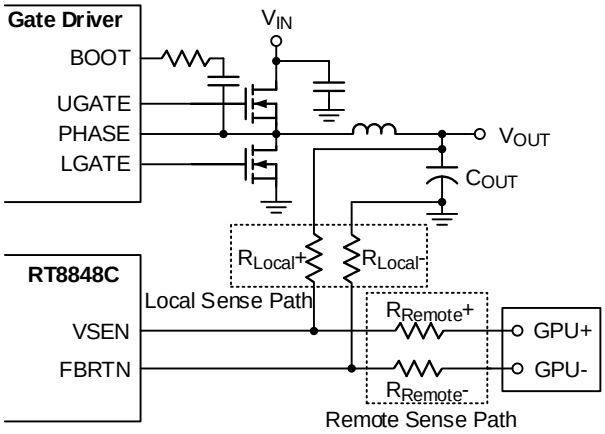


Figure 28. Output Voltage Sensing

16.4 Current Sensing

The RT8848C provides per-phase current sensing amplifier for different current sensing topology, including DCR current sensing and SPS current sensing. This current signal is used for loop control, zero current detection, current balance and per-phase current limit.

16.5 DCR Current Sensing

The RT8848C can support inductor DCR current sensing to get each phase current signal, as illustrated in Figure 29. An external low-pass filter, R_{X1} and C_X, reconstructs the current signal. The low-pass filter time constant R_{X1} x C_X should match time constant L/DCR of Inductance and DCR. The R_{X1} and C_X can be fine-tuned for transient performance. If RC network time constant is smaller than inductor time constant L/DCR, V_{CS} current signal leads the inductor current signal, and early triggers per-phase current limit during load transient. If RC network time constant is larger than inductor time constant L/DCR, V_{CS} current signal has a sluggish rise and delays triggering per-phase current limit during load transient. If RC network time constant matches inductor time constant L/DCR, the trigger level of per-phase current limit will meet the desired value. R_{X1} is highly recommended to be two 0603 size resistors in series to enhance the current signal accuracy. X7R type capacitor is suggested for C_X in the application. R_{X2} is optional for preventing V_{CS} from exceeding current sense amplifier input range (–10mV~90mV). Generally, the time constant of (R_{X1} // R_{X2}) x C_X should match L/DCR. However, due to PDN mismatch effect in common-N network, the Rx value should be properly designed according to PDN values. The detailed discussion is shown in Design Considerations section for Common N Current Sensing Circuit. The current sense lines must be routed as differential pair from the inductor to the controller on the same layer. The recommended layout is shown in Figure 30. The selection of SPS/DCR mode can be configured by PINSET1 setting.

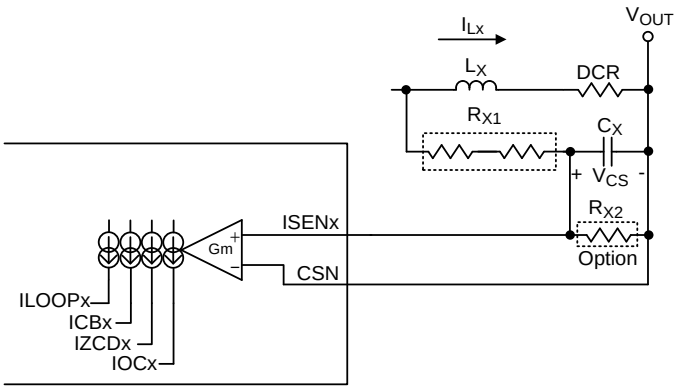


Figure 29. Inductor DCR Current Sensing Method

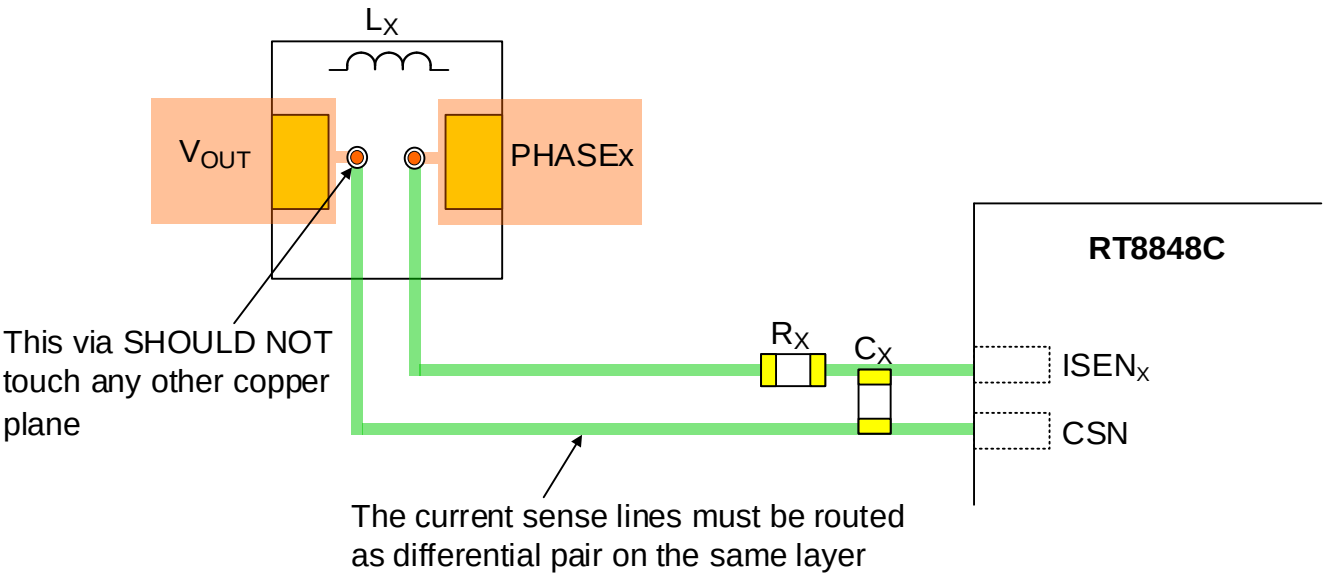


Figure 30. PCB Layout of DCR Current Sensing

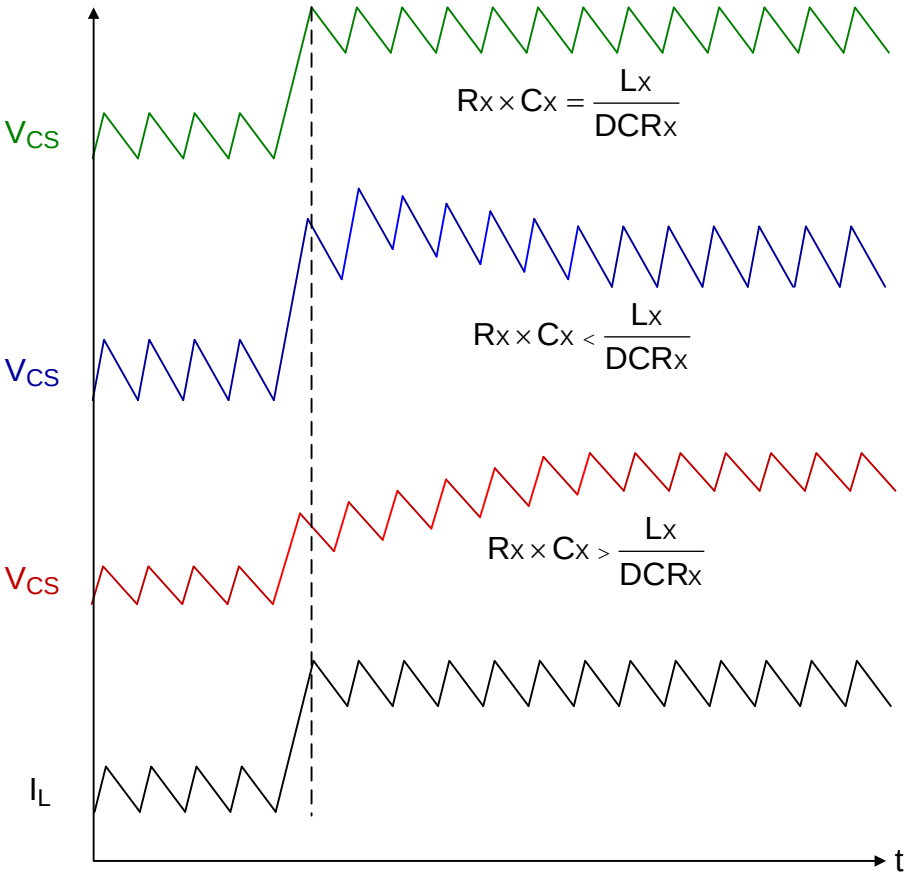


Figure 31. All Kinds of RC Network Time Constant

16.6 SPS Current Sensing

The RT8848C current sensing circuit can also support SPS current sensing. SPS (Smart Power Stage) can accurately detect the internal MOSFET current for a reference of PWM controller, SPS current sensing circuit simplifies the quantity of components on the external circuit and provides a more accurate current signal unlike DCR detection circuit. SPS has two kinds of current signal, current output and voltage output. Figure 32 shows the current reporting circuit of different current signals respectively. When the SPS current sensing is used, the PINSET1 should be configured to SPS mode. The inverting input of the current-sense amplifier generates a 1.36V reference voltage for SPS current sensing circuit. The current is reported to the controller as a differential voltage between the ISENx and REFOUT pins with a conversion gain to represent the inductor current I_L, as shown in the equations below.

Current Type Signal:

$$V_{ISENx-REFOUT} = gain(A/A) \times I_L \times R_{IMON}$$

Voltage Type Signal:

$$V_{ISENx-REFOUT} = gain(V/A) \times I_L \times \frac{R_{IMON2}}{R_{IMON1} + R_{IMON2}}$$

For larger current sense gain as voltage type, it is recommended to place a voltage divider resistor between IOUT and REFIN pins to avoid the controller's current amplifier input voltage range exceeding −10mV~90mV.

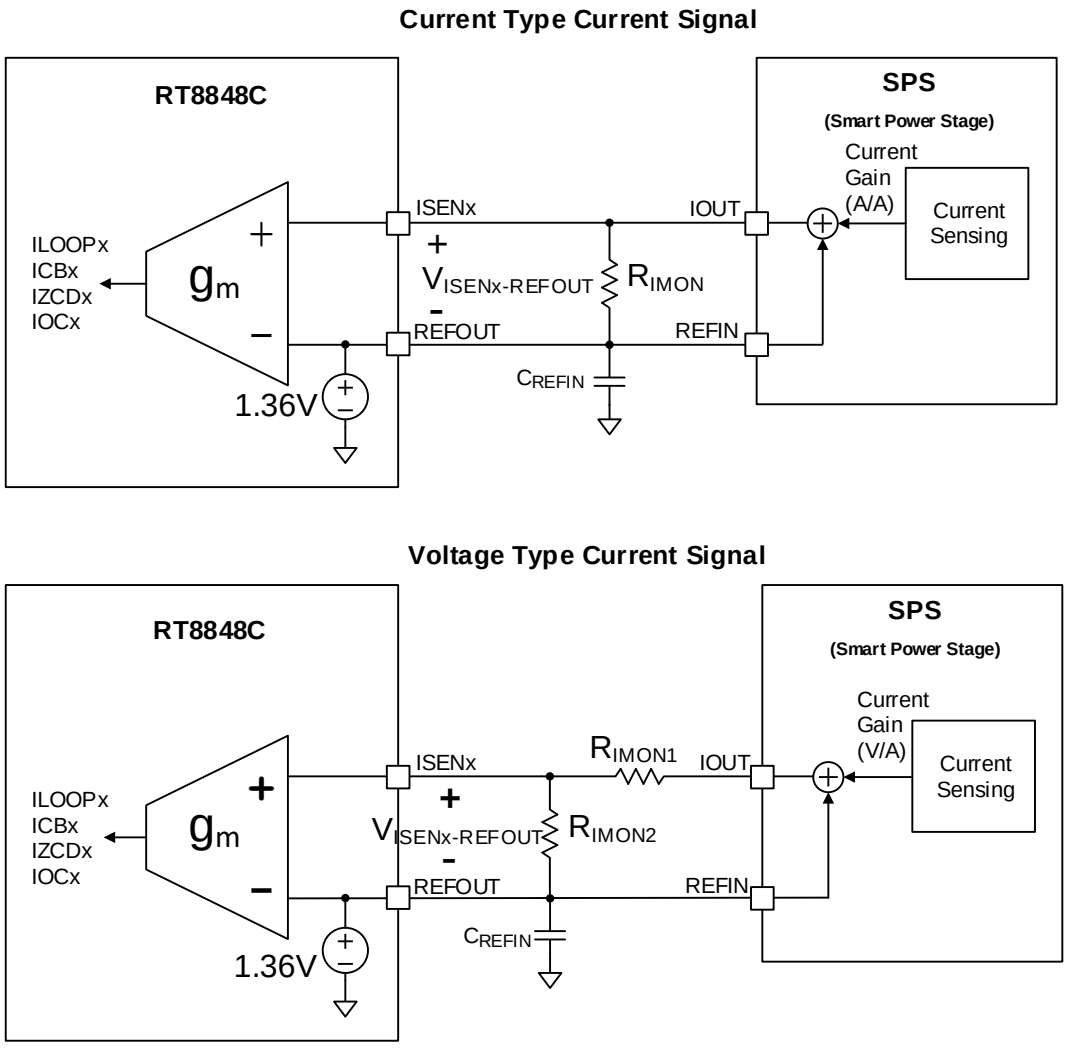


Figure 32. SPS Current Sensing

16.7 Total Load Current Sense

The RT8848C can support both conventional DCR network sense from inductor and a smart power stage (SPS) which can directly provide a current monitor signal (IMON). For SPS application, the sum current can be achieved by adding the IMON signal on ISENx pin from each SPS. For DCR application, the RT8848C applies a low input offset current sense amplifier to sense the total load current flowing through inductors for droop function and IMON sum current signal as shown in Figure 33. The voltage across C_{SUM} is proportional to the total load current, and the output current of current amplifier (I_{SUM}) is also proportional to the load current of the voltage regulator. The sensed current I_{SUM} represents the total output current of the regulator, and it is directly used for droop function, total output overcurrent protection and auto-phase shedding function. The I_{SUM} can be calculated by the following equation:

$$I_{SUM} = I_{OUT} \times \frac{R_{DC}}{N}$$

, where R_{DC} is the DCR of output inductor L, N is the operation phase number.

Moreover, in order to get the in-phase inductor current, the R_{PH1-8} and C_{SUM} should follow the equation below.

$$\frac{L}{R_{DC}} = \frac{R_{PH} \times C_{SUM}}{N}$$

, where the R_{PH} is equal to R_{PH1-8}. Generally, for the C_{SUM}, it is suggested to place a 100nF/0603 capacitor. Besides, connect a resistor (Rn) between each phase's output feedback node to prevent large current if there is some voltage drop generated. The recommended Rn design value is detailed in following section: Design Considerations for Common N Current Sensing Circuit.

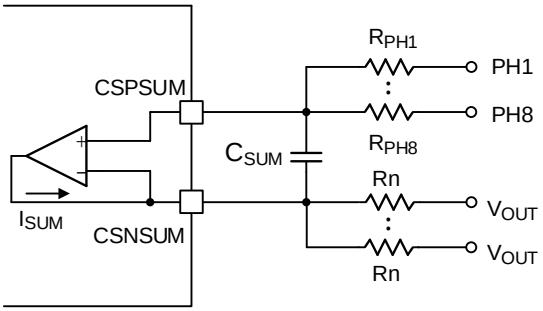


Figure 33. Total Load Current Sense Circuit

16.8 Compensator Design

The RT8848C does not need a complex type II or type III compensator to optimize control loop performance. It can adopt a simple type I compensator (one pole, one zero) in the G-NAVP^{TM} topology to fine tune ACLL performance. The one pole and one zero compensator is shown in

Figure 34. For OVR4i+ specification, it is recommended to adjust compensator according to load transient ring back level. Default compensator values are referred to the design tool. The location of pole and zero can be calculated by the following equation:

$$\text{Pole position : } \frac{1}{2\pi R_{1\_comp} \times C_{1\_comp}}$$

$$\text{Zero position : } \frac{1}{2\pi R_{2\_comp} \times C_{2\_comp}}$$

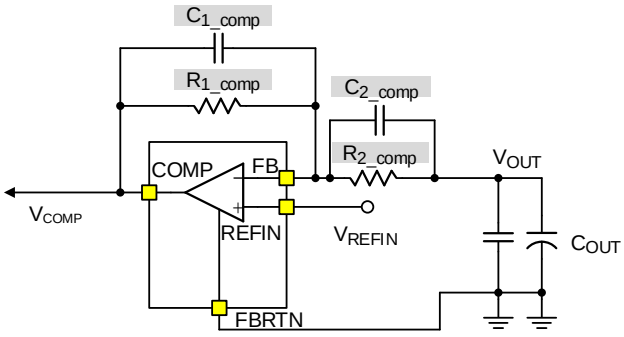


Figure 34. Type I Compensator

16.9 Output Voltage DC Offset

The RT8848C implements an output voltage offset function to adjust output DC voltage with a positive or negative offset. This function can be enabled by I^2C register 0x0E[5]=1 and disabled as 0x0E[5]=0. When voltage offset function is activated, a source current flows out of FB pin to V_{OUT} for generating a negative dc offset on V_{OUT}; contrarily, a sink current flows into FB pin from V_{OUT} for generating a positive dc offset on V_{OUT}. The equivalent

circuit is shown in Figure 35. The magnitude of source and sink current can be adjusted by I²C register 0x0E[4:0]. The setting of register 0x0E[5:0] is summarized in the section of register tables below. As result, the output voltage can be calculated by the following equation as output voltage offset function is enabled.

$$V_{OUT} = V_{REFIN} + I_{offset} \times R_{2\_comp}$$

, where the Ioffset is offset current set by register 0x0E[3:0].

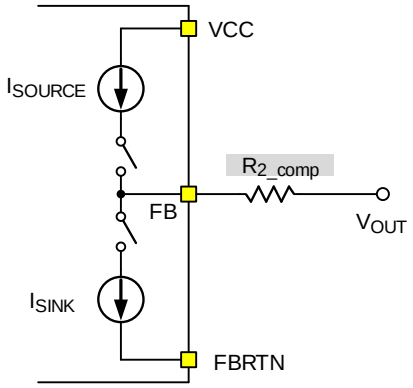


Figure 35. V_{OUT} DC Offset Circuit

16.10 Phase Number of Operation

The RT8848C supports 8/7/6/5/4/3/2/1 phase operation. During PWM pin setting process in first power-on sequence, the detection of hardware setting for maximum operating phase number is executed. The ISENx pins are detected and phase is disabled if voltage is higher than VCC−0.5V. Therefore, the phase can be disabled by connecting the ISENx pin to VCC = 5V with a pull high resistor (100kΩ). The maximum phase number of operation is determined and latched at each PWM pin setting detection. The configurations for 8/7/6/5/4/3/2/1 phase operation are summarized in Table 8. It should be noticed that ISEN1 cannot be connected to VCC since at least 1-phase operation is necessary. Please strictly follow Table 8 for phase disable. Incorrect pin pull up/down connection may cause catastrophic fault during power-on. When the ISENX pin is pulled high by 5VCC, the DCR or SPS current sensing circuit of that phase should be disconnected. Moreover, the phase number of operation by hardware setting has the highest priority to decide the maximum allowable phase number in actual operation. Other methods such as pin setting or I²C registers will be limited by hardware setting.

Table 8. Operation Phase Number Hardware Settings

Configuration	Pin Configuration, Pull High to Target							
	ISEN8	ISEN7	ISEN6	ISEN5	ISEN4	ISEN3	ISEN2	ISEN1
8-phase	--	--	--	--	--	--	--	--
7-phase	VCC	--	--	--	--	--	--	--
6-phase	X	VCC	--	--	--	--	--	--
5-phase	X	X	VCC	--	--	--	--	--
4-phase	X	X	X	VCC	--	--	--	--
3-phase	X	X	X	X	VCC	--	--	--
2-phase	X	X	X	X	X	VCC	--	--
1-phase	X	X	X	X	X	X	VCC	--

Note:

1. “--” denotes normal connection.

2. “X” denotes floating
3. Use 100kΩ pull up resistor for connection with VCC = 5V

16.11 Design Considerations for Common N Current Sensing Circuit

The RT8848C adopts common N current sensing structure for saving the pin numbers of IC package. For DCR type application, the DCR current sensing RC circuit (Rx, Cx) is in parallel with power inductor of each phase. As shown in Figure 36, the negative sides of Cx are connected together and routed to CSNSUM pin of the IC. In order to prevent large leakage current induced by differential voltage between each phases’ output nodes, it is necessary to place a small resistor (Rn) in series to minimize the leakage current on common N circuit loop. However, the differential voltage from each phase’s output node to common N point still affects the current feedback signal, and the feedback current signal can be derived as below.

$$V_{CSi} = \frac{\left(1 + \frac{sL}{DCR}\right)}{(1 + sC_XR_X)} \times DCR \times I_{Li} + \frac{I_{Li} \times R_{pcbi} - \frac{1}{N} \times \sum_{i=1}^{N} I_{Li} \times R_{pcbi}}{(1 + sC_XR_X)}$$ It can be observed that the differential voltage comes from the difference of Rpcb layout impedance. Therefore, for minimizing the effect of Rpcb impedance on current feedback signal, the PCB layout of each phase from inductor output to loading point (GPU) should be as symmetric as possible.

However, it is hard to layout the Rpcb perfectly match each other, and with different DCR selection, the Rpcb variation has different tolerance. Since the current balance gain for Phase1~Phase8 can be programmed separately via I^2C command, the Rpcb design criterion can be derived according to these parameters as below.

$$\frac{V_{CS\_max}}{V_{CS\_min}} = \frac{DCR + R_{pcb\_max} - R_{pcb\_avg}}{DCR + R_{pcb\_min} - R_{pcb\_avg}} < 32$$

, where the 32 is calculated by dividing CBGain_max(2) with CBGain_min(1/16).

On the other hand, for SPS type application, the current feedback signal is generated by SPS’s IMON signal and stands on a REFOUT reference voltage. Since REFOUT reference voltage is provided by the controller and connected to CSNSUM pin with a short wire, there is no leakage route as DCR type application. The asymmetric problem of Rpcb impedance is solved.

For the selection of Rn the RC time delay on common-N voltage (V_{CSNSUM}) should be considered, since the RC time constant of (Rn, Cn) affects the response time of current feedback signal. If RC time constant is larger than switching period($1/f_{SW}$), where f_{SW} is switching frequency of PWM, the current feedback signal will be delayed and the loop response becomes slower. Therefore, the RC time constant should be smaller than switching period to guarantee the transient performance. Generally, the minimum value of Cn is suggested to be larger than 10nF/0603/6.3V for noise filtering on local CSNSUM pin. Then, the selection guide of Rn follows the criterion below:

$$2\pi R_nC_n < \frac{1}{f_{SW}}$$

For example, if Cn is designed with 10nF and f_{SW} = 300kHz, the Rn is recommended to be 50Ω.

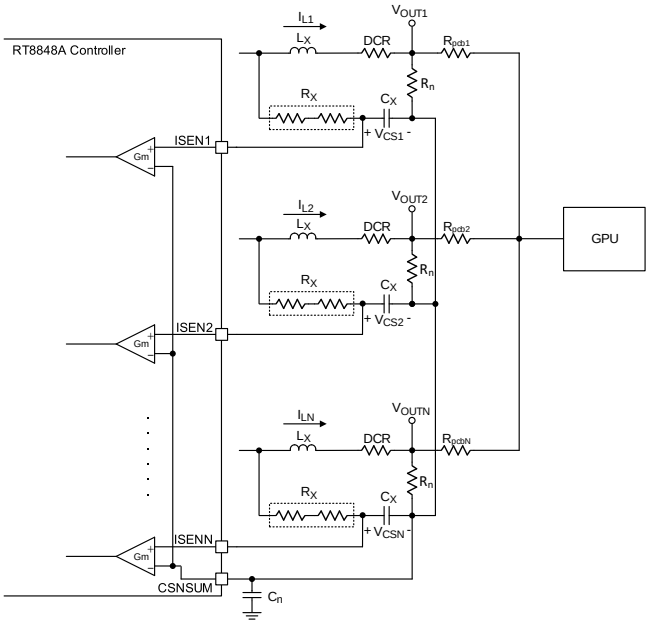


Figure 36. DCR Current Sensing with Common N Structure

The selection of Rx also affects the zero current detection threshold due to PDN (power delivery network) DC offset as shown in above V_{CSi} equation. The PDN DC offset generates a DC offset on each phase's V_{ISEN} signal and make the controller unable to detect correct current signal. As shown in Figure 37, the V_{ISEN} signal (green waveform), which applying Rx*Cx = L/DCR, has slow falling slew rate and induces a very large negative inductor current on low-side power MOSFET. This phenomenon may worsen the phase shedding performance since the controller spends more time to turn off the shedding phases. In order to improve the accuracy of zero current detection, the Rx*Cx time constant should be reduced to compensate the DC offset. As shown in Figure 37, the V_{ISEN} (red waveform) signal, which applies Rx*Cx = L/DCR/k, has larger AC current ripple than the green waveform. The AC current ripple of the red waveform is 1/k times of AC current ripple of the green waveform. Moreover, the falling slew rate of the red waveform is also faster than that of the green waveform. Therefore, the negative inductor current can be reduced because V_{ISEN} can reach the ZCD threshold with faster slew rate. The design value of k factor is calculated by the following equation:

$$k_j = \frac{DCR}{DCR + R_{PCBj} - \frac{1}{N} \times \sum_{i=1}^{j} \left(R_{PCBi}\right)}$$

Where N is the maximum operating phase number, and j is the operating phase number before phase shedding, DCR is the DCR value of inductor and R_{PCBi} is the PDN value of each phase. It should be noticed that the k factors are different when operating with different phase number. In order to optimize the performance of APS transition, the smallest k factor (k>0 and k<1) is selected and applied to design the Rx resistor value. According to the calculated k factor value, the respective low-side MOSFET switched off moment are summarized as below.

a. For k = 1, low-side MOSFET switched off at inductor current = 0A.

b. For k>0 and k<1, low-side MOSFET switched off at inductor current < 0A.

c. For k<0 or k>1, low-side MOSFET switched off at inductor current > 0A.

d. $k \neq 0$.

Finally, the value of Rx is designed with following equation:

$$R_x = \frac{L}{DCR} \times \frac{1}{C_x} \times k$$

Where k>0 and k<1.

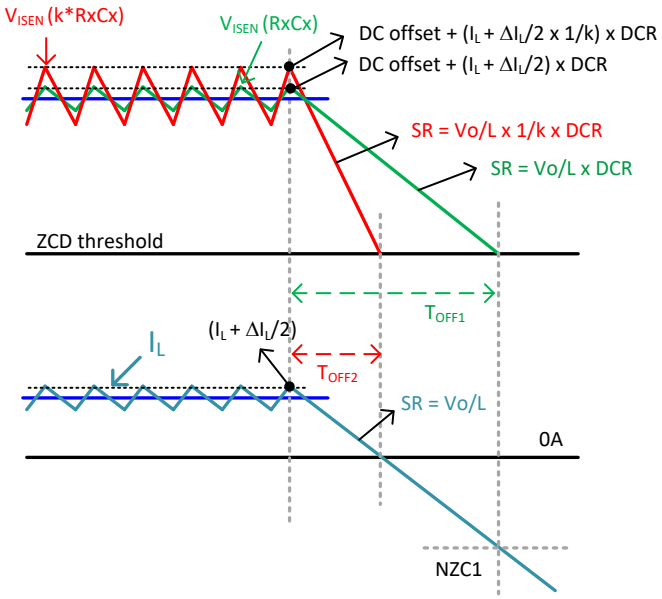


Figure 37. PDN Compensation Method

16.12 Inductor Selection Guide

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response, but they increase the inductor ripple current and output voltage ripple and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required and transient response will be slower since more time is required to change current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current (ΔI_L) about 20-50% of the desired full output load current. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency (f_{SW}), the maximum output current ($I_{OUT(MAX)}$) and estimating a ΔI_L as certain percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \text{ and } I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$ To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are minimum requirements. To maintain control of inductor current in overload and short-circuit conditions, some applications may desire current ratings up to the current limit value. However, the IC's output undervoltage shutdown feature makes this unnecessary for most applications.

For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements. For

low inductor core losses, some types of shielded ferrite core is usually the best; although they may be larger or more expensive, they may probably have fewer EMI and other noise problems.

16.13 Output Cap Selection Guide

The Buck output regulator of RT8848C is optimized for ceramic output capacitors, and the best performance will be obtained by using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR and ESL and stored charge. These three ripple components are called ESR ripple, ESL ripple and capacitive ripple. Since ceramic capacitors have extremely low ESR, ESL and relatively little capacitance, all these components should be considered if ripple is critical. The decomposition of output ripple is shown in Figure 38. The formulas to describe each component are listed below.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(ESL)} = \frac{d}{dt} I_L \times ESL$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

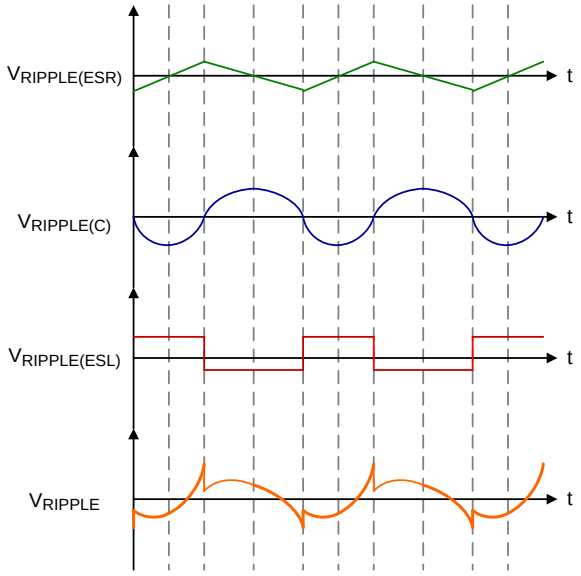


Figure 38. Output Ripple Decomposition

It should be noticed that the output voltage ripple reduces as operating phase number increases. For multi-phase operation, the frequency of output inductor sum current increases to N times (N is the operating phase number) of single-phase current, and the output voltage ripple is also reduced to 1/N as compared to single-phase condition. In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The G-NAVP™ transient response is very quick and output transients are usually small. However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur

slowly with respect to the IC's switching frequency. But some modern digital loads can exhibit nearly instantaneous load changes and the following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the G-NAVP™ control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. The behavior diagram of output voltage drop is depicted in Figure 39. Calculate the approximate on-time (ignore the parasitic) and maximum duty cycle for a given input and output voltage as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}, \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but both of these can be ignored since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as:

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

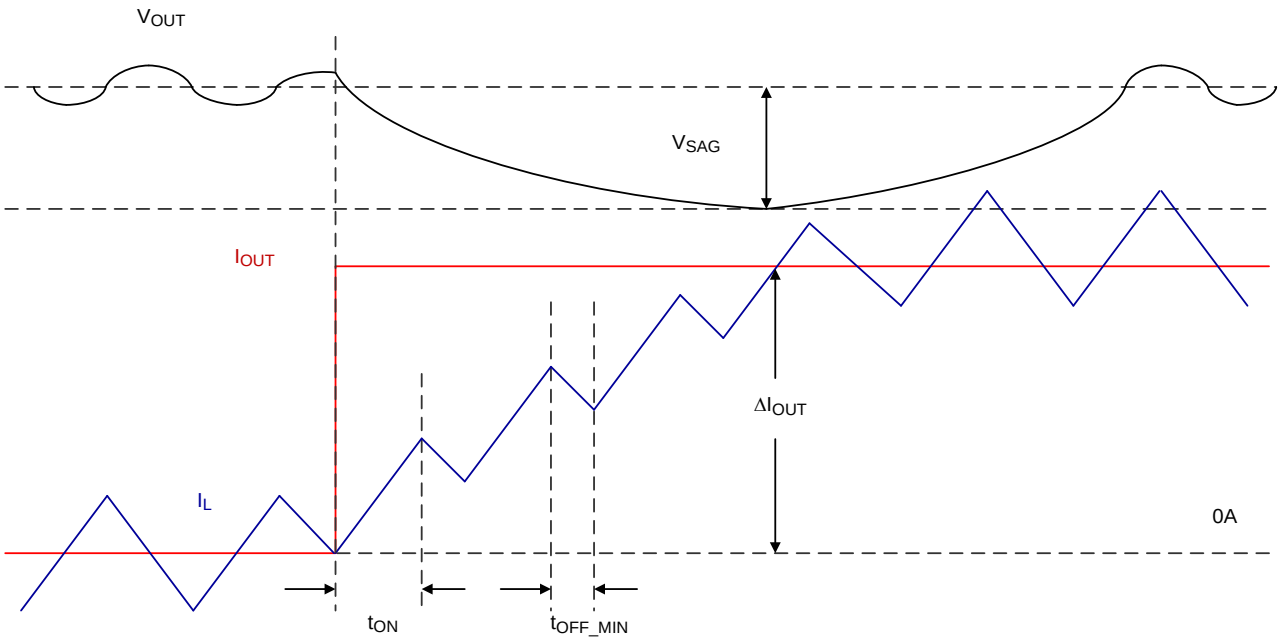


Figure 39. Output Voltage Drop (V_{SAG}) Estimation as Output Load Current Step Up

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage:

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

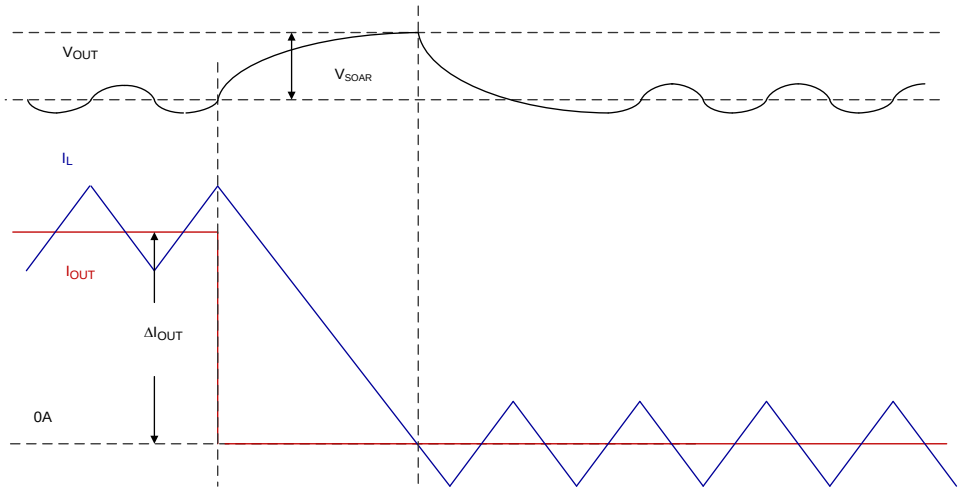


Figure 40. Output Voltage Soar (V_{SOAR}) Estimation as Output Load Current Step Down

Most applications never experience instantaneous full load steps, and the RT8848C's high switching frequency and fast transient response can easily control voltage regulation at all times. Therefore, sag and soar are seldom an issue except in very low-voltage CPU core or DDR memory supply applications, particularly for devices with high clock frequencies and quick changes into and out of sleep modes. In such applications, simply increasing the amount of ceramic output capacitor (sag and soar are directly proportional to capacitance) or adding extra bulk capacitance can easily eliminate any excessive voltage transients.

In any application with large quick transients, soar and sag should be calculated to make sure that overvoltage protection and undervoltage protection will not be triggered.

In addition, the recommended dielectric type of the capacitor is X7R, which has the best performance among temperature and DC and AC bias voltage variations. The variation of the capacitance value with temperature, DC bias voltage and switching frequency needs to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

16.14 Input Cap Selection Guide

A buck converter generates a pulsating ripple current with high di/dt at the input. Without input capacitors, ripple current is supplied by the upper power source. Printed circuit board (PCB) resistance and inductance causes high-voltage ripple that disrupts electronic devices. The circulating ripple current results in increased conducted and radiated EMI. Input capacitors provide a short bypass path for ripple current and stabilize bus voltage during a transient event.

The capacitor voltage rating should meet reliability and safety requirements. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design. Among the different types of capacitors, the multilayer ceramic capacitor (MLCC) is particularly good regarding allowable ripple current due to low ESR and ESL. The following equation is used to estimate the required effective capacitance that will meet the ripple requirement.

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1-D)}{\Delta V_{IN\_PP} \times f_{SW}}$$

where D is calculated as below:

$$D = \frac{V_O}{V_{IN} \times \eta}$$

Besides the ripple-voltage requirement, the ceramic capacitors should meet the thermal stress requirement as well. The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation:

$$I_{RMS} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left[(1 - \frac{V_{OUT}}{V_{IN}}) \times I_{OUT}^2 + \frac{\Delta I_L^2}{12} \right]}$$

Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Besides, since the ESL of ceramic capacitors plays a significant role on voltage spike at input and phase node, it is desirable to add a small capacitor with low ESL near VIN pin.

While the MLCC is excellent regarding allowable ripple current, it is well-known the regarding effective capacitance, it is necessary to meet transient response requirements. There can be two VIN spikes during the transient: the first spike is related to the ESR; and the second spike is caused by the difference between the buck converter input current (i_{IN_B}) and the VIN bus converter output current (i_{PS}) as depicted in Figure 41. Both spikes should be lower than the VIN undershoot or overshoot requirement (VIN_tran). First, since the MLCCs have very small ESR, the component of ESR drop can almost be ignored. The second spike is related to the response of the VIN bus converter. The rising time of the converter output current during a transient event, T_{R_PS}, can be approximated by the following equation:

$$T_{R\_PS} \cong \frac{0.35}{f_{BW\_PS}}$$

, where f_{BW_PS} is the control loop bandwidth of buck converter.

The equivalent capacitance of the input capacitors should be greater than that calculated with following equation:

$$C_{IN} \geq \frac{\frac{1}{2} \times I_{Step} \times D_{max} \times T_{R\_PS}}{V_{IN\_Tran}}$$

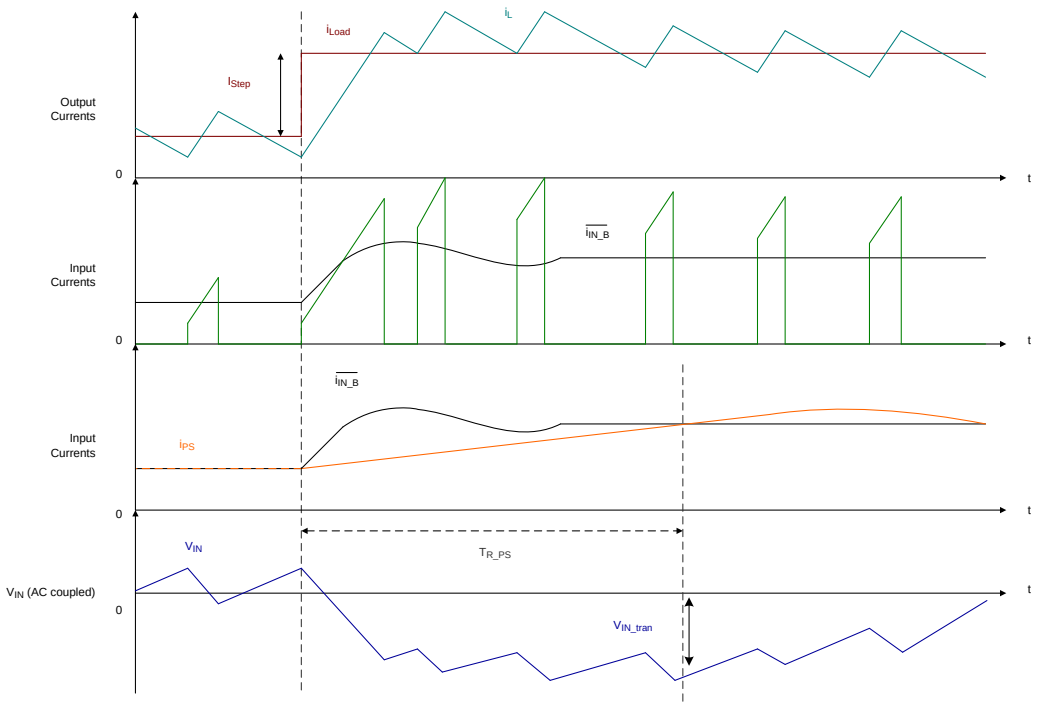


Figure 41. VIN Transient Current Diagram

Either Vin ripple (ΔV_{IN_PP}) or Vin transient ripple (V_{IN_Tran}) should meet the design requirements. Moreover, it should be noticed that many de-rating factors, including Vbias dc voltage, ac voltage and operating temperature, make equivalent capacitance be smaller than the capacitance without bias.

16.15 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-40L 5x5 package, the thermal resistance, θ_{JA}, is 27.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)} = (125°C - 25°C)/(27.5°C/W) = 3.63W$ for WQFN-40L 5x5 package

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 42 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

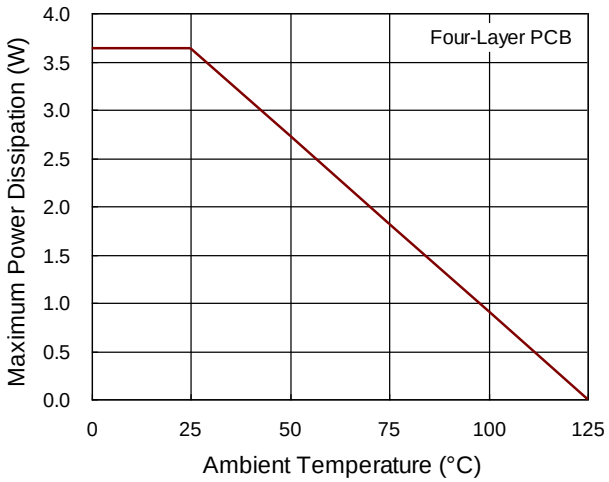


Figure 42. Derating Curve of Maximum Power Dissipation

16.16 Layout Considerations

Layout is very important in high-frequency switching converter design. If designed improperly, the PCB can radiate excessive noise and contribute to the loop instability. There are some layout rules to followed when using the RT8848C as controller.

- When using the RT8848C with DCR current sensing type application, the current sense lines MUST be routed as differential pair on the same layer. Noise couple should be away from these traces. The RC components of DCR current sensing network should be placed at the controller side.
- When using the RT8848C with DCR current sensing type application, the PCB impedance from inductor output to GPU load should be symmetric to other phases in multi-phase application. Symmetrically layout can improve current balance performance. Bad layouts which are not symmetric will induce worse current balance.
- When using the RT8848C with DCR current sensing type application, the vias at inductor side SHOULD NOT touch any other copper plane to prevent additional voltage drop on DCR circuit loop.
- When using the RT8848C with DCR current sensing type application, RESERVE a resistor (Rn) in series with DCR current sensing RC circuit to prevent large leakage current in multi-phase application. DO NOT place this resistor between inductor output node and CSNSUM pin as shown in Figure 44. This connection will make RT8848C false trigger current protection.
- The GPU local voltage should be monitored with kelvin-sensing circuit and the differential pair should be routed parallel on the same layer. Keep these traces away from the high switching signal and coupling noise.
- The RGND of PWMVID circuit should be connected to FBRTN pin as reference. PWMVID circuit includes VREF, REFIN, REFADJ and PWMVID. Connect the components with RGND as reference ground to these pins. The VREF decoupling capacitor should be placed near VREF pin.
- A RC filter (R=2.2Ω/0603 and C = 1μF/0603) from bias voltage to VCC pin is necessary; it should be placed as close physically possible to VCC pin. There is around 50mA sink current during POR duration, the maximum resistance of RC filter should be smaller than 2.2Ω.
- A decoupling capacitor (10nF/0603) from CSNSUM to GND should be placed as close to CSNSUM pin as possible.

- For the connection of REFOUT pin. As for SPS application (by setting the PINSET1 to SPS mode), REFOUT outputs 1.38V (typ.) to the REFIN pin of SPS. Connect a 0.47μF/0603 decoupling capacitor near this pin, and the equivalent capacitance on this pin should be smaller than 1.6μF. Besides, as for DCR current sensing application (by setting the PINSET1 to DCR mode), REFOUT is regarded as an input pin and it should be connected to the positive terminal of output capacitor.
- DO NOT put any decoupling capacitor near IMON pin since it affects the accuracy of IMON reporting. Place a resistor from IMON pin to GND as close as possible. For NTC compensation, users can place a NTC resistor at power inductor side (phase 1) and in parallel with IMON resistor at the controller side.
- Place a RC filter before VIN pin for stable operation. The filter capacitor should be placed as close to VIN pin as possible.
- The exposed pad is the ground of logic control circuits. For better power dissipation, it should be soldered to a large ground plane with enough thermal vias.

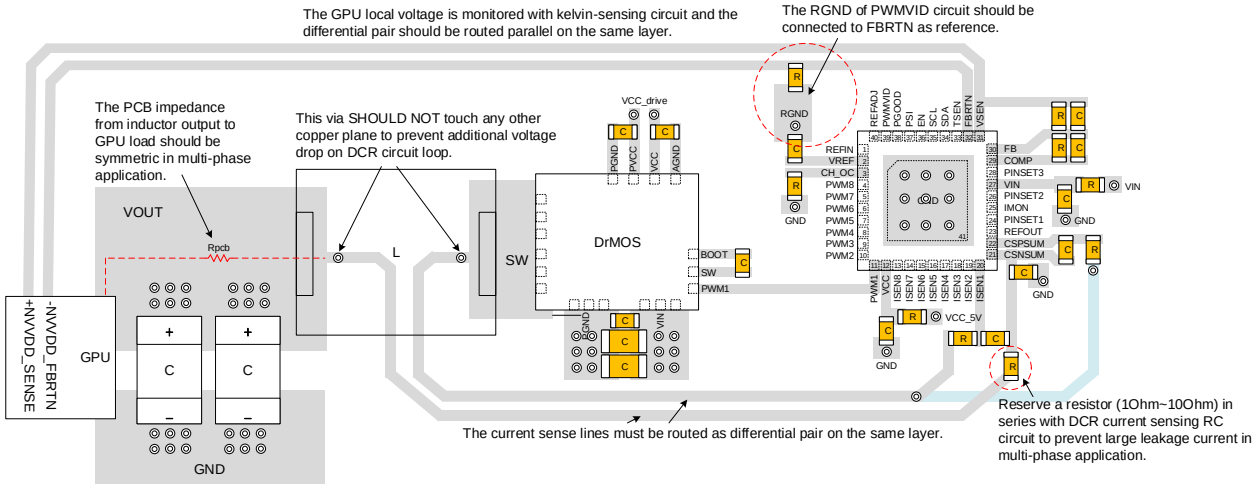


Figure 43. Layout Suggestion for RT8848C with DCR Type Application

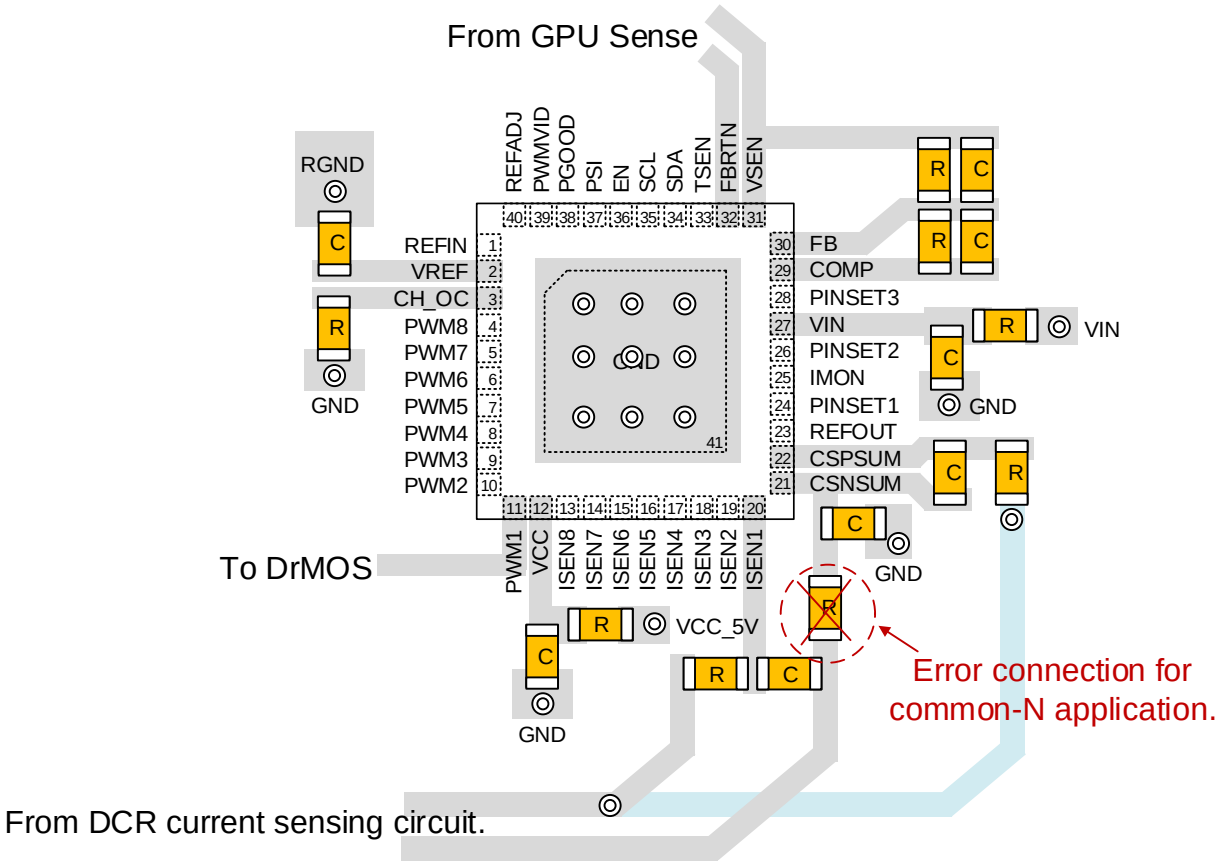


Figure 44. Error Connection for DCR Common-N Application

16.17 I²C Interface (SDA & SCL)

The RT8848C features an I²C interface to allow users to adjust various operating parameters. The supported operating parameters that can be adjusted through I²C communication are summarized in the register tables below. The data transfers follow the format shown in Figure 45. After the START condition (S), a slave address is sent. A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still tries to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such a transfer.

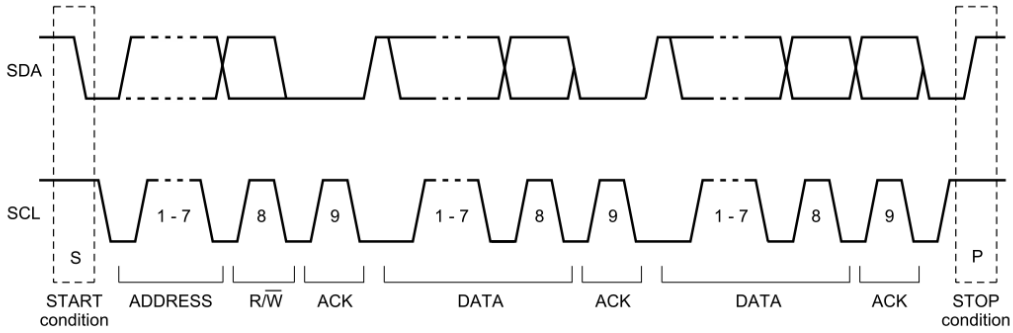


Figure 45. An Example of I²C Data Transfer

17 Functional Register Description

Table 9. Register Map Breakdown

Region	Register Range	Restriction
Host User	0x0D~0x45, 0x49, 0x4B~0x50, 0x55, 0x5F	1. Restricted access for Write if 0x00 = 0xA6 2. Read/Write accessible if 0x00 ≠ 0xA6
	0x01~0x0C, 0x46~0x48, 0x4A, 0x5D	1. Restricted access for Write if 0x00 = 0xA6 or PSI ≠ High 2. Read/Write accessible if 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1)
IC Vendor	0x35, 0x51~0x5C, 0x5E, 0x8B~0x8F	Restricted access for Write if 0x00 = 0xA6
	0x60~0x8A, 0x90~0xFF	Restricted access for Write

Register Tables

0x00[7:0] for Updating Register 0x01 to 0x0F			
Bits	**Attribute**	**Default**	**Description**
7:0	RW	0	0x00[7:0]: Receive I2C data after PGOOD = H, otherwise, NAK when PGOOD = L 10100110 = Lock 0x01~0x5F registers Others = Unlock 0x01~0x5F registers, according to Table 9 for register restriction.

[1] The data of 0x01 to 0x5F can be updated when 0x00 is not programmed as 0xA6. In order to prevent overwriting during normal operation, users can write 0x00 = 0xA6 to lock the register data from 0x01 to 0x5F.

0x01[7:0] APL1 Threshold in Auto-phase Shedding Mode			
Bits	**Attribute**	**Default**	**Description**
7:0	RW	00010000	0x01[7:0]: APL1 threshold Default data is detected from PINSET PWM2 if PWM pin setting function is enabled. APL1 = DEC(0x01[7:0]) x 12.5mV

[1] The register value of 0x01[7:0] can only be programmed when 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1).

0x02[7:0] APL2 Threshold in Auto-phase Shedding Mode			
Bits	Attribute	Default	Description
7:0	RW	00100000	0x02[7:0]: APL2 threshold Default data is detected from PINSET PWM3 if PWM pin setting function is enabled. APL2 = DEC(0x02[7:0]) x 12.5mV

[1] The register value of 0x02[7:0] can only be programmed when 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1).

0x03[7:0] APL3 Threshold in Auto-phase Shedding Mode			
Bits	**Attribute**	**Default**	**Description**
7:0	RW	01000000	0x03[7:0]: APL3 threshold Default data is detected from PINSET PWM5 if PWM pin setting function is enabled. APL3 = DEC(0x03[7:0]) x 12.5mV

[1] The register value of 0x03[7:0] can only be programmed when 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1).

0x04[7:0] APL4 Threshold in Auto-phase Shedding Mode			
Bits	**Attribute**	**Default**	**Description**
7:0	RW	01100000	0x04[7:0]: APL4 threshold Default data is detected from PINSET PWM7 if PWM pin setting function is enabled. APL4 = DEC(0x04[7:0]) x 12.5mV

[1] The register value of 0x04[7:0] can only be programmed when 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1).

0x05[2:0] APL1 Hysteresis Margin in Auto-phase Shedding Mode			
Bits	**Attribute**	**Default**	**Description**
2:0	RW	100	0x05[2:0]: APL1 hysteresis margin The APL1 high threshold = APL1 + APL1_Hys The ALP1 low threshold = APL1 – APL1_Hys APL1_Hys = DEC(0x05[2:0]) x 12.5mV

[1] The register value of 0x05[2:0] can only be programmed when 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1).

0x06[2:0] APL2 Hysteresis Margin in Auto-phase Shedding Mode			
Bits	**Attribute**	**Default**	**Description**
2:0	RW	100	0x06[2:0]: APL2 hysteresis margin The APL2 high threshold = APL2 + APL2_Hys The ALP2 low threshold = APL2 – APL2_Hys APL2_Hys = DEC(0x06[2:0]) x 12.5mV

[1] The register value of 0x06[2:0] can only be programmed when 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1).

0x07[2:0] APL3 Hysteresis Margin in Auto-phase Shedding Mode			
Bits	**Attribute**	**Default**	**Description**
2:0	RW	100	0x07[2:0]: APL3 hysteresis margin The APL3 high threshold = APL3 + APL3_Hys The ALP3 low threshold = APL3 – APL3_Hys APL3_Hys = DEC(0x07[2:0]) x 12.5mV

[1] The register value of 0x07[2:0] can only be programmed when 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1).

0x08[2:0] APL4 Hysteresis Margin in Auto-phase Shedding Mode			
Bits	**Attribute**	**Default**	**Description**
2:0	RW	100	0x08[2:0]: APL4 hysteresis margin The APL4 high threshold = APL4 + APL4_Hys The ALP4 low threshold = APL4 – APL4_Hys APL4_Hys = DEC(0x08[2:0]) x 12.5mV

[1] The register value of 0x08[2:0] can only be programmed when 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1).

0x09[2:0] LCS4 Operating Phase Number in Auto-phase Shedding Mode			
Bits	**Attribute**	**Default**	**Description**
2:0	RW	111	0x09[2:0]: LCS4 operating phase number 000: 1Phase 001: 2Phase 010: 3Phase 011: 4Phase 100: 5Phase 101: 6Phase 110: 7Phase 111: 8Phase

[1] The register value of 0x09[2:0] can only be programmed when 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1).

0x0A[2:0] LCS3 Operating Phase Number in Auto-phase Shedding Mode			
Bits	**Attribute**	**Default**	**Description**
2:0	RW	101	0x0A[2:0]: LCS3 operating phase number 000: 1Phase 001: 2Phase 010: 3Phase 011: 4Phase 100: 5Phase 101: 6Phase 110: 7Phase 111: 8Phase

[1] The register value of 0x0A[2:0] can only be programmed when 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1).

0x0B[2:0] LCS2 Operating Phase Number in Auto-phase Shedding Mode			
Bits	**Attribute**	**Default**	**Description**
2:0	RW	011	0x0B[2:0]: LCS2 operating phase number 000: 1Phase 001: 2Phase 010: 3Phase 011: 4Phase 100: 5Phase 101: 6Phase 110: 7Phase 111: 8Phase

[1] The register value of 0x0B[2:0] can only be programmed when 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1).

0x0C[2:0] LCS1 Operating Phase Number in Auto-phase Shedding Mode			
Bits	**Attribute**	**Default**	**Description**
2:0	RW	001	0x0C[2:0]: LCS1 operating phase number 000: 1Phase 001: 2Phase 010: 3Phase 011: 4Phase 100: 5Phase 101: 6Phase 110: 7Phase 111: 8Phase

[1] The register value of 0x0C[2:0] can only be programmed when 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1).

0x0D[2:0] LCS0 Operating Phase Number in Auto-phase Shedding Mode			
Bits	**Attribute**	**Default**	**Description**
2:0	RW	000	0x0D[2:0]: LCS0 operating phase number 000: 1Phase 001: 2Phase 010: 3Phase 011: 4Phase 100: 5Phase 101: 6Phase 110: 7Phase 111: 8Phase

[1] The register value of 0x0D[2:0] can only be programmed when 0x00 ≠ 0xA6.

0x0E[5:0] for Output Voltage DC Offset			
Bits	**Attribute**	**Default**	**Description**
5	RW	0	0x0E[5]: Enable or Disable 0 = Disable 1 = Enable
4	RW	0	0x0E[4]: Positive or Negative 0 = Negative (sink current) 1 = Positive (source current)
3:0	RW	0000	0x0E[3:0]: Offset Current, I_{offset} 0000 = 0μA 0001 = 1μA 0010 = 2μA 0011 = 3μA 0100 = 4μA 0101 = 5μA 0110 = 6μA 0111 = 7μA 1000 = 8μA 1001 = 9μA 1010 = 10μA 1011 = 11μA 1100 = 12μA 1101 = 13μA 1110 = 14μA 1111 = 15μA

[1] The register value of 0x0E[5:0] can only be programmed when 0x00 ≠ 0xA6.

0x0F[4:0] Frequency Setup			
Bits	**Attribute**	**Default**	**Description**
4:0	RW	00000	0x0F[4:0]: Frequency Setup 00000: 250kHz 00001: 300kHz 00010: 350kHz 00011: 400kHz 00100: 450kHz 00101: 500kHz 00111: 600kHz 01001: 700kHz 01011: 800kHz 01101: 900kHz 01111: 1000kHz 10001: 1100kHz 10011: 1200kHz 10101: 1300kHz 10111: 1400kHz 11011: 1600kHz

[1] The register value of 0x0F[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x11[4:0] Current Balance Gain for Phase1			
Bits	**Attribute**	**Default**	**Description**
4:0	RW	10000	0x11[4:0]: Current Balance Gain for Phase1 00000 = 1/16 00001 = 2/16 … 01111 = 16/16 10000 = 17/16 (default) 10001 = 18/16 … 11110 = 31/16 11111 = 32/16

[1] The register value of 0x11[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x12[4:0] Current Balance Offset for Phase1			
Bits	**Attribute**	**Default**	**Description**
4	RW	0	0x12[4]: Current Balance Offset Direction for Phase1 0 = Positive 1 = Negative
3:0	RW	0000	0x12[3:0]: Current Balance Offset for Phase1 0000 = 15mV/V_{REFIN} (default) 0001 = 30mV/ V_{REFIN} … 1110 = 225mV/ V_{REFIN} 1111 = 240mV/ V_{REFIN}

[1] The register value of 0x12[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x13[4:0] Current Balance Gain for Phase2			
Bits	**Attribute**	**Default**	**Description**
4:0	RW	10000	0x13[4:0]: Current Balance Gain for Phase2 00000 = 1/16 00001 = 2/16 … 01111 = 16/16 10000 = 17/16 (default) 10001 = 18/16 … 11110 = 31/16 11111 = 32/16

[1] The register value of 0x13[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x14[4:0] Current Balance Offset for Phase2			
Bits	**Attribute**	**Default**	**Description**
4	RW	0	0x14[4]: Current Balance Offset Direction for Phase2 0 = Positive 1 = Negative
3:0	RW	0000	0x14[3:0]: Current Balance Offset for Phase2 0000 = 15mV/V_{REFIN} (default) 0001 = 30mV/ V_{REFIN} … 1110 = 225mV/ V_{REFIN} 1111 = 240mV/ V_{REFIN}

[1] The register value of 0x14[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x15[4:0] Current Balance Gain for Phase3			
Bits	**Attribute**	**Default**	**Description**
4:0	RW	10000	0x15[4:0]: Current Balance Gain for Phase3 00000 = 1/16 00001 = 2/16 … 01111 = 16/16 10000 = 17/16 (default) 10001 = 18/16 … 11110 = 31/16 11111 = 32/16

[1] The register value of 0x15[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x16[4:0] Current Balance Offset for Phase3			
Bits	**Attribute**	**Default**	**Description**
4	RW	0	0x16[4]: Current Balance Offset Direction for Phase3 0 = Positive 1 = Negative
3:0	RW	0000	0x16[3:0]: Current Balance Offset for Phase3 0000 = 15mV/V_{REFIN} (default) 0001 = 30mV/ V_{REFIN} … 1110 = 225mV/ V_{REFIN} 1111 = 240mV/ V_{REFIN}

[1] The register value of 0x16[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x17[4:0] Current Balance Gain for Phase4			
Bits	**Attribute**	**Default**	**Description**
4:0	RW	10000	0x17[4:0]: Current Balance Gain for Phase4 00000 = 1/16 00001 = 2/16 … 01111 = 16/16 10000 = 17/16 (default) 10001 = 18/16 … 11110 = 31/16 11111 = 32/16

[1] The register value of 0x17[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x18[4:0] Current Balance Offset for Phase4			
Bits	**Attribute**	**Default**	**Description**
4	RW	0	0x18[4]: Current Balance Offset Direction for Phase4 0 = Positive 1 = Negative
3:0	RW	0000	0x18[3:0]: Current Balance Offset for Phase4 0000 = 15mV/V_{REFIN} (default) 0001 = 30mV/ V_{REFIN} … 1110 = 225mV/ V_{REFIN} 1111 = 240mV/ V_{REFIN}

[1] The register value of 0x18[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x19[4:0] Current Balance Gain for Phase5			
Bits	**Attribute**	**Default**	**Description**
4:0	RW	10000	0x19[4:0]: Current Balance Gain for Phase5 00000 = 1/16 00001 = 2/16 … 01111 = 16/16 10000 = 17/16 (default) 10001 = 18/16 … 11110 = 31/16 11111 = 32/16

[1] The register value of 0x19[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x1A[4:0] Current Balance Offset for Phase5			
Bits	**Attribute**	**Default**	**Description**
4	RW	0	0x1A[4]: Current Balance Offset Direction for Phase5 0 = Positive 1 = Negative
3:0	RW	0000	0x1A[3:0]: Current Balance Offset for Phase5 0000 = 15mV/V_{REFIN} (default) 0001 = 30mV/ V_{REFIN} … 1110 = 225mV/ V_{REFIN} 1111 = 240mV/ V_{REFIN}

[1] The register value of 0x1A[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x1B[4:0] Current Balance Gain for Phase6			
Bits	**Attribute**	**Default**	**Description**
4:0	RW	10000	0x1B[4:0]: Current Balance Gain for Phase6 00000 = 1/16 00001 = 2/16 … 01111 = 16/16 10000 = 17/16 (default) 10001 = 18/16 … 11110 = 31/16 11111 = 32/16

[1] The register value of 0x1B[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x1C[4:0] Current Balance Offset for Phase6			
Bits	**Attribute**	**Default**	**Description**
4	RW	0	0x1C[4]: Current Balance Offset Direction for Phase6 0 = Positive 1 = Negative
3:0	RW	0000	0x1C[3:0]: Current Balance Offset for Phase6 0000 = 15mV/V_{REFIN} (default) 0001 = 30mV/ V_{REFIN} … 1110 = 225mV/ V_{REFIN} 1111 = 240mV/ V_{REFIN}

[1] The register value of 0x1C[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x1D[4:0] Current Balance Gain for Phase7			
Bits	**Attribute**	**Default**	**Description**
4:0	RW	10000	0x1D[4:0]: Current Balance Gain for Phase7 00000 = 1/16 00001 = 2/16 … 01111 = 16/16 10000 = 17/16 (default) 10001 = 18/16 … 11110 = 31/16 11111 = 32/16

[1] The register value of 0x1D[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x1E[4:0] Current Balance Offset for Phase7			
Bits	**Attribute**	**Default**	**Description**
4	RW	0	0x1E[4]: Current Balance Offset Direction for Phase7 0 = Positive 1 = Negative
3:0	RW	0000	0x1E[3:0]: Current Balance Offset for Phase7 0000 = 15mV/V_{REFIN} (default) 0001 = 30mV/ V_{REFIN} … 1110 = 225mV/ V_{REFIN} 1111 = 240mV/ V_{REFIN}

[1] The register value of 0x1E[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x1F[4:0] Current Balance Gain for Phase8			
Bits	**Attribute**	**Default**	**Description**
4:0	RW	10000	0x1F[4:0]: Current Balance Gain for Phase8 00000 = 1/16 00001 = 2/16 … 01111 = 16/16 10000 = 17/16 (default) 10001 = 18/16 … 11110 = 31/16 11111 = 32/16

[1] The register value of 0x1F[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x20[4:0] Current Balance Offset for Phase8			
Bits	**Attribute**	**Default**	**Description**
4	RW	0	0x20[4]: Current Balance Offset Direction for Phase8 0 = Positive 1 = Negative
3:0	RW	0000	0x20[3:0]: Current Balance Offset for Phase8 0000 = 15mV/V_{REFIN} (default) 0001 = 30mV/ V_{REFIN} … 1110 = 225mV/ V_{REFIN} 1111 = 240mV/ V_{REFIN}

[1] The register value of 0x20[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x21[7:0] Per-phase OCP Threshold Gain Setting (Phase1 to Phase4)			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	00	0x21[7:6]: Phase 4 OCP threshold gain 00 = 1x 01 = 0.9x 10 = 0.8x 11 = 0.7x
5:4	RW	00	0x21[5:4]: Phase 3 OCP threshold gain 00 = 1x 01 = 0.9x 10 = 0.8x 11 = 0.7x
3:2	RW	00	0x21[3:2]: Phase 2 OCP threshold gain 00 = 1x 01 = 0.9x 10 = 0.8x 11 = 0.7x
1:0	RW	00	0x21[1:0]: Phase 1 OCP threshold gain 00 = 1x 01 = 0.9x 10 = 0.8x 11 = 0.7x

[1] The register value of 0x21[7:0] can only be programmed when 0x00 ≠ 0xA6.

0x22[7:0] Per-phase OCP Threshold Gain Setting (Phase5 to Phase8)			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	00	0x22[7:6]: Phase 8 OCP threshold gain 00 = 1x 01 = 0.9x 10 = 0.8x 11 = 0.7x
5:4	RW	00	0x22[5:4]: Phase 7 OCP threshold gain 00 = 1x 01 = 0.9x 10 = 0.8x 11 = 0.7x
3:2	RW	00	0x22[3:2]: Phase 6 OCP threshold gain 00 = 1x 01 = 0.9x 10 = 0.8x 11 = 0.7x
1:0	RW	00	0x22[1:0]: Phase 5 OCP threshold gain 00 = 1x 01 = 0.9x 10 = 0.8x 11 = 0.7x

[1] The register value of 0x22[7:0] can only be programmed when 0x00 ≠ 0xA6.

0x23[1:0] Sum OCP Delay Time			
Bits	**Attribute**	**Default**	**Description**
1:0	RW	01	0x23[1:0]: Sum OCP delay time 00 = 112μs 01 = 56μs (default) 10 = 28μs 11 = 14μs

[Note] The register value of 0x23[1:0] can only be programmed when 0x00 ≠ 0xA6.

0x24[5:0] Sum OCP Threshold Adjustment			
Bits	**Attribute**	**Default**	**Description**
5	RW	0	0x24[5]: Sum OCP threshold increase or decrease 0 = Positive (increase) 1 = Negative (decrease)
4:0	RW	00000	0x24[4:0]: Sum OCP Threshold Offset If 0x24[5] = 0, SOCP_th = 2.2V + DEC(0x24[4:0])*50mV If 0x24[5] = 1, SOCP_th = 2.2V - DEC(0x24[4:0])*50mV

[1] The default SOCP threshold is 2.2V; users can adjust SOCP threshold via adjusting this bit for design requirement.

[2] The register value of 0x24[5:0] can only be programmed when 0x00 ≠ 0xA6.

0x25[1:0] Absolute OVP Threshold Setting			
Bits	**Attribute**	**Default**	**Description**
1:0	RW	00	0x25[1:0]: Absolute OVP threshold setting 00 = 2V 01 = 1.8V 10 = 2.2V 11 = 2.4V

[1] The register value of 0x25[1:0] can only be programmed when 0x00 ≠ 0xA6.

0x26[1:0] Relative OVP Threshold Setting			
Bits	**Attribute**	**Default**	**Description**
1:0	RW	00	0x26[1:0]: Relative OVP threshold setting 00 = 150% of V_{REF} 01 = 140% of V_{REF} 10 = 130% of V_{REF} 11 = 120% of V_{REF}

[1] The register value of 0x26[1:0] can only be programmed when 0x00 ≠ 0xA6.

0x27[1:0] UVP Threshold Setting			
Bits	**Attribute**	**Default**	**Description**
1:0	RW	00	0x27[1:0]: UVP threshold setting 00 = 40% of V_{REF} 01 = 30% of V_{REF} 10 = 50% of V_{REF} 11 = 60% of V_{REF}

[1] The register value of 0x27[1:0] can only be programmed when 0x00 ≠ 0xA6.

0x28[1:0] OTP Threshold Setting			
Bits	**Attribute**	**Default**	**Description**
1:0	RW	00	0x28[1:0]: OTP threshold setting 00 = 150°C 01 = 160°C 10 = 170°C 11 = 140°C

[1] The register value of 0x28[1:0] can only be programmed when 0x00 ≠ 0xA6.

0x29[4:0] Protection Disable Setting			
Bits	**Attribute**	**Default**	**Description**
4	RW	0	0x29[4]: TMON_OTP function 0 = Enable 1 = Disable
3	RW	0	0x29[3]: OTP function 0 = Enable 1 = Disable
2	RW	0	0x29[2]: Sum OCP function 0 = Enable 1 = Disable
1	RW	0	0x29[1]: UVP function 0 = Enable 1 = Disable
0	RW	0	0x29[0]: OVP function 0 = Enable 1 = Disable

[1] The register value of 0x29[4:0] can only be programmed when 0x00 ≠ 0xA6.

0x2A[4:0] Protection Indication Bits for TMON_OTP, OTP, SOCP, UVP and OVP			
Bits	**Attribute**	**Default**	**Description**
4	RO	0	0x2A[4]: TMON_OTP indication 0 = No TMON_OTP 1 = TMON_OTP is triggered
3	RO	0	0x2A[3]: OTP indication 0 = No OTP 1 = OTP is triggered
2	RO	0	0x2A[2]: Sum OCP indication 0 = No Sum OCP 1 = Sum OCP is triggered
1	RO	0	0x2A[1]: UVP indication 0 = No UVP 1 = UVP is triggered
0	RO	0	0x2A[0]: OVP indication 0 = No OVP 1 = OVP is triggered

0x2B[7:0] Protection Indication Bit for Per-phase OCP			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	0x2B[7]: Phase8 OCP indication 0 = No per-phase OCP 1 = Per-phase OCP is triggered
6	RO	0	0x2B[6]: Phase7 OCP indication 0 = No per-phase OCP 1 = Per-phase OCP is triggered
5	RO	0	0x2B[5]: Phase6 OCP indication 0 = No per-phase OCP 1 = Per-phase OCP is triggered
4	RO	0	0x2B[4]: Phase5 OCP indication 0 = No per-phase OCP 1 = Per-phase OCP is triggered
3	RO	0	0x2B[3]: Phase4 OCP indication 0 = No per-phase OCP 1 = Per-phase OCP is triggered
2	RO	0	0x2B[2]: Phase3 OCP indication 0 = No per-phase OCP 1 = Per-phase OCP is triggered
1	RO	0	0x2B[1]: Phase2 OCP indication 0 = No per-phase OCP 1 = Per-phase OCP is triggered
0	RO	0	0x2B[0]: Phase1 OCP indication 0 = No per-phase OCP 1 = Per-phase OCP is triggered

[1] The register of 0x2B is only effective if 0x4D[0]=1; otherwise, 0x2B register remains at 0.

0x2C[1:0] AEAGM Gain Setting			
Bits	**Attribute**	**Default**	**Description**
1:0	RW	10	0x2C[1:0]: AEAGM gain 00 = 4 01 = 6 10 = 8 (default) 11 = 10

[1] The register value of 0x2C[1:0] can only be programmed when 0x00 ≠ 0xA6.

0x2D[2:0] APS Mode Configuration and Pulse Skipping Mode Configuration			
Bits	**Attribute**	**Default**	**Description**
2	RW	0	0x2D[2]: Internal PSI logic as PINSET3 pin is floating 0 = Internal PSI logic follows external PSI pin configuration 1 = Internal PSI logic locks at high logic regardless of external PSI pin configuration
1	RW	1	0x2D[1]: PSK mode configuration as PSI = L 0 = Enable PSK mode 1 = Disable PSK mode
0	RW	0	0x2D[0]: APS mode configuration as PSI = M 0 = Enable APS mode 1 = Disable APS mode and operate in full-phase mode

[1] The register value of 0x2D[2:0] can only be programmed when 0x00 ≠ 0xA6.

0x2E[7:0] ADC Results for V_{IMON}			
Bits	**Attribute**	**Default**	**Description**
7:0	RO	00000000	0x2E[7:0]: ADC Results for V_{IMON} , 1LSB = 6.25mV 00000000 = 0mV 00000001 = 6.25mV …. 11111110 = 1587.5mV 11111111 = 1593.75mV

0x2F[7:0] ADC Results for V_{SEN}			
Bits	**Attribute**	**Default**	**Description**
7:0	RO	00000000	0x2E[7:0]: ADC Results for V_{SEN} , 1LSB = 6.25mV 00000000 = 0mV 00000001 = 6.25mV …. 11111110 = 1587.5mV 11111111 = 1593.75mV

0x30[7:0] ADC Results for V_{TSEN}			
Bits	**Attribute**	**Default**	**Description**
7:0	RO	00000000	0x2E[7:0]: ADC Results for V_{SEN} , 1LSB = 12.5mV 00000000 = 0mV 00000001 = 12.5mV …. 11111110 = 3175mV 11111111 = 3187.5mV

0x31[1:0] ADC Average Times for V_{IMON}			
Bits	**Attribute**	**Default**	**Description**
1:0	RW	00	0x31[1:0]: ADC Average Times for V_{IMON} 00 = average 8 times (112μs) (default) 01 = average 4 times (56μs) 10 = average 2 times (28μs) 11 = average 16 times (224μs)

[1] The register value of 0x31[1:0] can only be programmed when 0x00 ≠ 0xA6.

0x32[1:0] ADC Average Times for V_{SEN}			
Bits	**Attribute**	**Default**	**Description**
1:0	RW	00	0x32[1:0]: ADC Average Times for V_{SEN} 00 = average 8 times (336μs) (default) 01 = average 4 times (168μs) 10 = average 2 times (84μs) 11 = average 16 times (672μs)

[1] The register value of 0x32[1:0] can only be programmed when 0x00 ≠ 0xA6.

0x33[1:0] ADC Average Times for V_{TSEN}			
Bits	**Attribute**	**Default**	**Description**
1:0	RW	00	0x33[1:0]: ADC Average Times for V_{TSEN} 00 = average 8 times (336μs) (default) 01 = average 4 times (168μs) 10 = average 2 times (84μs) 11 = average 16 times (672μs)

[1] The register value of 0x33[1:0] can only be programmed when 0x00 ≠ 0xA6.

0x34[5:0] ZCD Threshold Offset Setting			
Bits	**Attribute**	**Default**	**Description**
5	RW	1	0x34[5]: ZCD offset function enable/disable 0 = disable ZCD offset 1 = enable ZCD offset
4	RW	1	0x34[4]: ZCD offset increase or decrease 0 = increase 1 = decrease
3:0	RW	0010	0x34[3:0]: ZCD threshold If 0x34[4] = 0, ZCD threshold = + DEC(0x34[3:0]) x 0.31mV If 0x34[4] = 1, ZCD threshold = - DEC(0x34[3:0]) x 0.31mV

[1] The register value of 0x34[5:0] can only be programmed when 0x00 ≠ 0xA6.

0x36[2:0] Operating Phase Number Indicator			
Bits	**Attribute**	**Default**	**Description**
2:0	RO	000	0x36[2:0]: operating phase number indicator 000 = 1Phase 001 = 2Phase 010 = 3Phase 011 = 4Phase 100 = 5Phase 101 = 6Phase 110 = 7Phase 111 = 8Phase

0x37[7:0] Vendor ID			
Bits	**Attribute**	**Default**	**Description**
7:0	RO	1E	0x37[7:0]: vendor ID

0x38[7:0] Device ID			
Bits	**Attribute**	**Default**	**Description**
7:0	RO	48	0x38[7:0]: device ID

0x40[3:0] PINSET_V1			
Bits	**Attribute**	**Default**	**Description**
3:2	RW	--	0x40[3:2]: Internal Ramp Magnitude 00 = 200mV 01 = 300mV 10 = 500mV 11 = 800mV
1	RW	--	0x40[1]: Soft-start V_{OUT} Ramping Up Slew Rate 0 = 1.5mV/μs 1 = 3mV/μs
0	RW	--	0x40[0]: Tri-state Voltage Level 0 = 1.9V 1 = 1.65V

[1] The value of 0x40[3:2] is set by PINSET1 setting at first power-on, and it is decoded to 0x4F[3:0] for internal ramp magnitude setting. Users can adjust internal ramp magnitude through modifying 0x4F[3:0] after power-on sequence.

[2] The register value of 0x40[3:0] can only be programmed when 0x00 ≠ 0xA6.

[3] The default value of 0x40[3:0] is decided by PINSET1 setting at first power-on.

0x41[3:0] PINSET_I1			
Bits	**Attribute**	**Default**	**Description**
3:2	RW	--	0x41[3:2]: AI Gain For DCR Type Application (0x41[1]=0) 00 = 6 01 = 12 10 = 24 11 = 48 For SPS Type Application (0x41[1]=1) 00 = 2 01 = 3 10 = 6 11 = 12
1	RW	--	0x41[1]: SPS/DCR Selection Type 0 = DCR Mode 1 = SPS Mode
0	Reserved	0	Reserved

[1] The register value of 0x41[3:0] can only be programmed when 0x00 ≠ 0xA6.

[2] The default value of 0x41[3:0] is decided by PINSET1 setting at first power-on.

[3] It should be noticed that register 0x41[1] cannot be changed after the controller is power-on.

0x42[3:0] PINSET_V2			
Bits	**Attribute**	**Default**	**Description**
3:2	RW	--	0x42[3:2]: Switching Frequency 00 = 250 kHz 01 = 400 kHz 10 = 550 kHz 11 = 700 kHz
1:0	RW	--	0x42[1:0]: Slave Device Address Code 00 = 0x48(7-bit slave address), 0x90 (8-bit Write), 0x91 (8-bit Read) 01 = 0x4A(7-bit slave address), 0x94 (8-bit Write), 0x95 (8-bit Read) 10 = 0x4C(7-bit slave address), 0x98 (8-bit Write), 0x99 (8-bit Read) 11 = 0x4E(7-bit slave address), 0x9C (8-bit Write), 0x9D (8-bit Read)

[1] The value of 0x42[3:2] is set by PINSET2 setting at first power-on, and it is decoded to 0x0F[4:0] for switching frequency setting. Users can adjust switching frequency through modifying 0x0F[4:0] after power-on sequence.

[2] The register value of 0x42[3:0] can only be programmed when 0x00 ≠ 0xA6.

[3] The default value of 0x42[3:0] is decided by PINSET2 setting at first power-on.

0x43[3:0] PINSET_I2			
Bits	**Attribute**	**Default**	**Description**
3	RW	--	0x43[3]: Middle Drive with Internal OP Circuit When the controller operates in DEM mode and inductor current reaches zero current or lower, the controller will drive the PWM output at tri-state level with internal OP circuit. 0 = Disable 1 = Enable
2:1	RW	--	0x43[2:1]: Operating Phase Number as PSI = Low 00 = 1Phase 01 = 2Phase 10 = 3Phase 11 = 4Phase
0	Reserved	0	Reserved

[1] The value of 0x43[2:1] is set by PINSET2 setting at first power-on, and it is decoded to 0x4F[6:4] for operating phase number setting at PSI=Low. Users can adjust switching frequency through modifying 0x4F[6:4] after power-on sequence.

[2] The register value of 0x43[3:0] can only be programmed when 0x00 ≠ 0xA6.

[3] The default value of 0x43[3:0] is decided by PINSET2 setting at first power-on.

0x44[3:0] PINSET_V3			
Bits	**Attribute**	**Default**	**Description**
3:0	RW	--	0x44[3:0]: APL Threshold APL1 = DEC(0x44[3:0]) x 2 x 12.5mV APL2 = DEC(0x44[3:0]) x 4 x 12.5mV APL3 = DEC(0x44[3:0]) x 8 x 12.5mV APL4 = DEC(0x44[3:0]) x 12 x 12.5mV

[1] The value of 0x44[3:0] is set by PINSET3 setting at first power-on, and it is decoded to 0x01[7:0] to 0x04[7:0] for APLx threshold settings. Users can adjust APLx threshold through modifying 0x01[7:0] to 0x04[7:0] after power-on sequence.

[2] The register value of 0x44[3:0] can only be programmed when 0x00 ≠ 0xA6.

[3] The default value of 0x44[3:0] is decided by PINSET3 setting at first power-on.

0x45[3:0] PINSET_I3			
Bits	**Attribute**	**Default**	**Description**
3:1	RW	--	0x45[3:1]: Operating Phase Number During Soft-start 000 = 1Phase 001 = 2Phase 010 = 3Phase 011 = 4Phase 100 = 5Phase 101 = 6Phase 110 = 7Phase 111 = 8Phase
0	Reserved	0	Reserved

[1] The register value of 0x45[3:1] can only be programmed when 0x00 ≠ 0xA6.

[2] The default value of 0x45[3:0] is decided by PINSET3 setting at first power-on.

0x46[5:0] APS Transition Delay Time			
Bits	**Attribute**	**Default**	**Description**
5:3	RW	001	0x46[5:3]: APS Phase Up Delay Time When V_{IMON} increases and is higher than phase up threshold, the controller increases operating phase number after “APS phase up delay time”. 000 = 0μs 001 = 1μs (default) 010 = 2μs 011 = 4μs 100 = 8μs 101 = 16μs 110 = 32μs 111 = 64μs
2:0	RW	001	0x46[2:0]: APS Phase Up Hold Time After the controller increases operating phase number, there is a “phase up hold time” to prevent the controller from adding phase again during “phase up hold time”. The next phase up transition can only be executed after the “phase up hold time” plus “APS phase up delay time” if V_{IMON} is higher than next phase up threshold. 000 = 0μs 001 = 5μs (default) 010 = 10μs 011 = 15μs 100 = 20μs 101 = 25μs 110 = 30μs 111 = 35μs

[1] The register value of 0x46[5:0] can only be programmed when 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1).

0x47[2:0] APS Phase Up to Full Phase Mask Time			
Bits	**Attribute**	**Default**	**Description**
2:0	RW	010	0x47[2:0]: APS Phase Up to Full Phase Mask Time After the controller increases operating phase number, the controller masks any triggering sources (QR or Anti-overshoot) that may induce controller phase up to full phase directly. The mask time is designed to prevent the controller from entering full phase operation triggered by QR or Anti-overshoot. 000 = 0μs 001 = 5μs 010 = 10μs (default) 011 = 15μs 100 = 20μs 101 = 25μs 110 = 30μs 111 = 35μs

[1] The register value of 0x47[2:0] can only be programmed when 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1).

0x48[3:0] Current Balance Disable Time During Phase Up and Down			
Bits	**Attribute**	**Default**	**Description**
3:0	RW	1011	0x48[3:0]: Current Balance Disable Time After the controller increases or decreases operating phase number, the controller disables current balance function for a “current balance disable time” period. 0000 = 0μs 0001 = 20μs 0010 = 40μs 0011 = 60μs 0100 = 80μs 0101 = 100μs 0110 = 120μs 0111 = 140μs 1000 = 160μs 1001 = 180μs 1010 = 200μs 1011 = 220μs (default) 1100 = 240μs 1101 = 260μs 1110 = 280μs 1111 = 300μs

[1] The register value of 0x48[3:0] can only be programmed when 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1).

0x49[7:0] QR Pulse Width and QR Threshold Setting, Anti-overshoot Threshold Setting			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	0x49[7:6]: QR Pulse Width When V_{SEN} drops down below (V_{REFIN} – QR threshold), the controller will forcibly turn on every phases' high-side MOSFET for a QR pulse width time. 00 = 0.5 x T_{ON} 01 = 0.7 x T_{ON} (default) 10 = 1.0 x T_{ON} 11 = 2.0 x T_{ON} Where T_{ON} is decided by V_{IN}, V_{OUT} and F_{SW}
5:3	RW	011	0x49[5:3]: QR Threshold 000 = V_{REFIN} - 20mV 001 = V_{REFIN} - 30mV 010 = V_{REFIN} - 40mV 011 = V_{REFIN} - 50mV (default) 100 = V_{REFIN} - 60mV 101 = V_{REFIN} - 70mV 110 = V_{REFIN} - 80mV 111 = V_{REFIN} - 90mV
2:0	RW	011	0x49[2:0]: Anti-overshoot Threshold 000 = V_{REFIN} + 20mV 001 = V_{REFIN} + 30mV 010 = V_{REFIN} + 40mV 011 = V_{REFIN} + 50mV (default) 100 = V_{REFIN} + 60mV 101 = V_{REFIN} + 70mV 110 = V_{REFIN} + 80mV 111 = V_{REFIN} + 90mV

[1] The register value of 0x49[7:0] can only be programmed when 0x00 ≠ 0xA6.

0x4A[5:0] APS Deglitch Time and PWM Low Pulse Time			
Bits	**Attribute**	**Default**	**Description**
5:3	RW	010	0x4A[5:3]: APS Deglitch Time When PSI status transits either from high or low to middle state (APS mode), the controller will enter APS mode if PSI keeps at middle state level for longer than “APS deglitch time”. 000 = 0μs 001 = 0.1μs 010 = 0.2μs (default) 011 = 0.4μs 100 = 0.8μs 101 = 1.6μs 110 = 3.2μs 111 = 6.4μs
2:0	RW	011	0x4A[2:0]: PWM Low Pulse Time During operating phase up in APS mode, the incremental phases will first generate a PWM low pulse to charge the bootstrap capacitor on DRMOS side before entering normal operation. 000 = 0μs 001 = 0.1μs 010 = 0.2μs 011 = 0.3μs (default) 100 = 0.4μs 101 = 0.5μs 110 = 0.6μs 111 = 0.7μs

[1] The register value of 0x4A[5:0] can only be programmed when 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1).

0x4B[7:0] Reserved Register for Customer Usage			
Bits	**Attribute**	**Default**	**Description**
7:0	RW	00000000	0x4B[7:0]: Reserved Register for Customer Usage No effect to IC functionality.

[1] The register value of 0x4B[7:0] can only be programmed when 0x00 ≠ 0xA6.

0x4C[6:0] Low Pass Filter for V_{REFIN} and Pull Down Current in CCM/DEM			
Bits	**Attribute**	**Default**	**Description**
6:5	RW	01	0x4C[6:5]: Low Pass Filter for V_{REFIN} Signal Internal low pass filter to filter out the external V_{REFIN} signal. Low pass delay time = 5 X τ (time constant of internal R, C) 00 = 37.5μs 01 = 25μs (default) 10 = 12.5μs 11 = 0μs
4:2	RW	010	0x4C[4:2]: V_{SEN} Pull Down Current in CCM 000 = 0mA 001 = 0.1mA 010 = 0.2mA (default) 011 = 0.3mA 100 = 0.4mA 101 = 0.5mA 110 = 0.6mA 111 = 0.7mA
1:0	RW	10	0x4C[1:0]: V_{SEN} Pull Down Current in DEM A pull down current is generated on V_{SEN} pin when PWM enters tri-state level for longer than 40μs. 00 = 0mA 01 = 1.5mA 10 = 3mA (default) 11 = 5mA

[1] The register value of 0x4C[6:0] can only be programmed when 0x00 ≠ 0xA6.

0x4D[1:0] Per-phase OCP Enable/Disable			
Bits	**Attribute**	**Default**	**Description**
1	RW	0	0x4D[1]: Per-phase OCP Analog Functionality 0 = Disable 1 = Enable
0	RW	0	0x4D[0]: Per-phase OCP Digital Flag Detection 0 = Disable 1 = Enable

[1] The register value of 0x4D[1:0] can only be programmed when 0x00 ≠ 0xA6.

0x4E[2:0] Middle Drive Function for Tri-state Control			
Bits	**Attribute**	**Default**	**Description**
2	RW	1	0x4E[2]: Internal setting
1	RW	0	0x4E[1]: Middle Drive with OP2K Circuit The controller keeps driving the PWM output at tri-state level with internal 2kΩ resistor. (There is additional power consumption of 1mA/phase on VCC in CCM condition.) 0 = Disable 1 = Enable
0	RW	1	0x4E[0]: Middle Drive with HIZR Circuit When controller operates in DEM mode and inductor current reaches zero current or lower, the controller drives the PWM output at tri-state level for 200ns and leaves floating after that. 0 = Disable 1 = Enable

[1] The register value of 0x4E[2:0] can only be programmed when 0x00 ≠ 0xA6.

0x4F[6:0] Operating Phase Number as PSI = Low and Internal Ramp Magnitude			
Bits	**Attribute**	**Default**	**Description**
6:4	RW	000	0x4F[6:4]: Operating Phase Number as PSI = Low 000 = 1Phase (default) 001 = 2Phase 010 = 3Phase 011 = 4Phase 100 = 5Phase 101 = 6Phase 110 = 7Phase 111 = 8Phase
3:0	RW	0011	0x4F[3:0]: Internal Ramp Magnitude 0000 = 150mV 0001 = 200mV 0010 = 250mV 0011 = 300mV (default) 0100 = 350mV 0101 = 400mV 0110 = 450mV 0111 = 500mV 1000 = 600mV 1001 = 700mV 1010 = 800mV 1011 = 900mV 1100 = 1000mV 1101 = 1100mV 1110 = 1200mV 1111 = 1300mV

[1] The register value of 0x4F[6:0] can only be programmed when 0x00 ≠ 0xA6.

0x50[7:0] QR Pulse Function Enable			
Bits	**Attribute**	**Default**	**Description**
7:0	RW	10001111	0x50[7:0]: QR Pulse Function Enable 0x80 = Disable QR pulse 0x8F = Enable QR pulse (default)

[1] The register value of 0x50[7:0] can only be programmed when 0x00 ≠ 0xA6.

0x54[3:0] CCM Ramp Hold Voltage			
Bits	**Attribute**	**Default**	**Description**
3:0	RW	0111	0x54[3:0]: CCM Ramp Hold Voltage Height setting

[1] The register value of 0x54[3:0] can only be programmed when 0x00 ≠ 0xA6.

0x55[4:0] Current Balance Functional Settings/Anti-overshoot Setting			
Bits	**Attribute**	**Default**	**Description**
4:3	RW	00	0x55[4:3]: Total Current Balance Gain Set1 The total current balance gain is decided by multiplying 0x55[4:3] and 0x5F[1:0] to achieve a final total current balance gain value. 00 = 1 01 = 3/4 10 = 2/4 11 = 1/4
2	RW	0	0x55[2]: Current Balance Functionality 0 = Enable current balance 1 = Disable current balance
1	RW	0	0x55[1]: Current Balance Low Pass Filter Internal RC filter time constant is around 6μs. 0 = 1 x RC 1 = 0.5 x RC
0	RW	1	0x55[0]: Anti-overshoot Functionality 0 = Disable anti-overshoot 1 = Enable anti-overshoot

[1] The register value of 0x55[4:0] can only be programmed when 0x00 ≠ 0xA6.

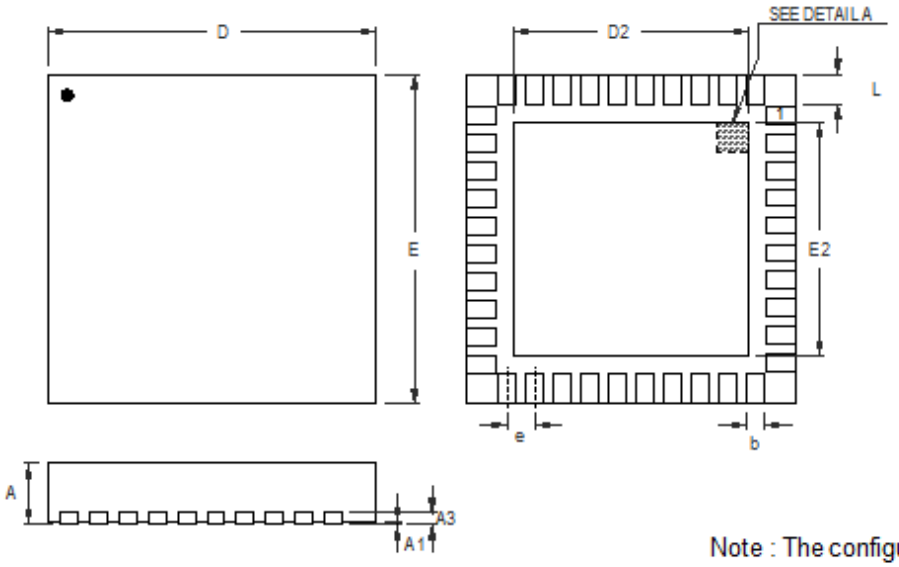
0x5D[2:0] APS Phase Shedding Delay Time			
Bits	**Attribute**	**Default**	**Description**
2:0	RW	000	0x5D[2:0]: APS Phase Shedding Delay Time 000 = 80μs (default) 001 = 160μs 010 = 320μs 011 = 640μs 100 = 5μs 101 = 10μs 110 = 20μs 111 = 40μs

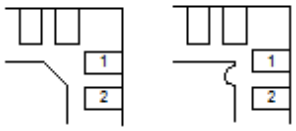
[1] The register value of 0x5D[2:0] can only be programmed when 0x00 ≠ 0xA6 and (PSI = High or 0x2D[2] = 1).

0x5F[1:0] Current Balance Functional Settings2			
Bits	**Attribute**	**Default**	**Description**
1:0	RW	00	0x5F[1:0]: Total Current Balance Gain Set2 00 = 1 (default) 01 = 2 10 = 1/2 11 = 1

[1] The register value of 0x5F[1:0] can only be programmed when 0x00 ≠ 0xA6.

18 Outline Dimension





DETAIL A

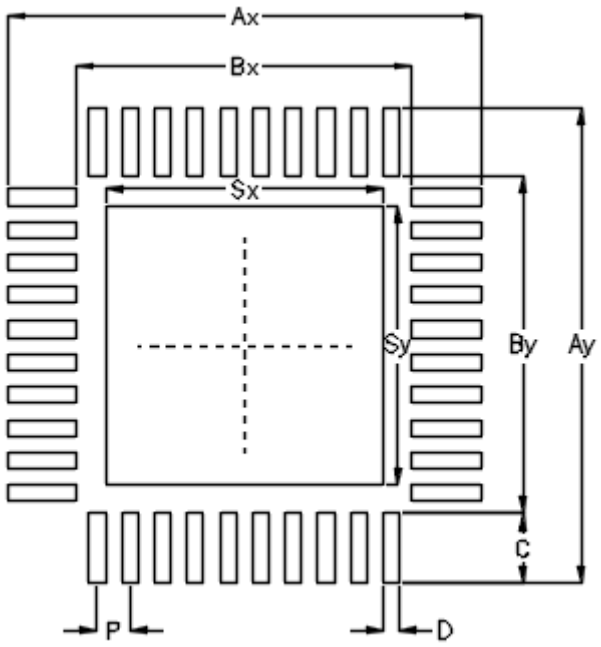
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

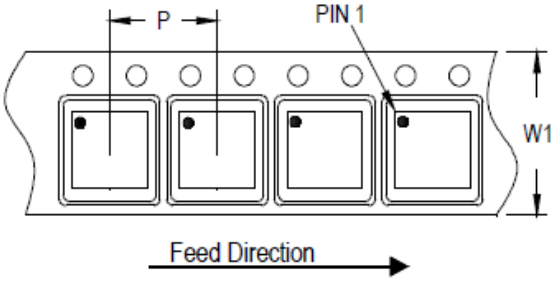
19 Footprint Information

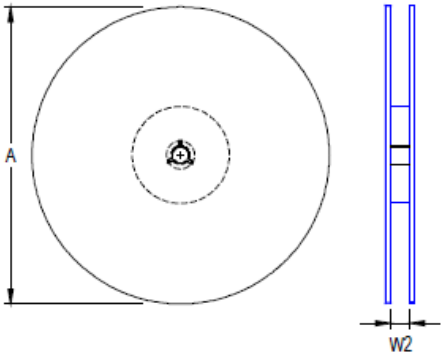


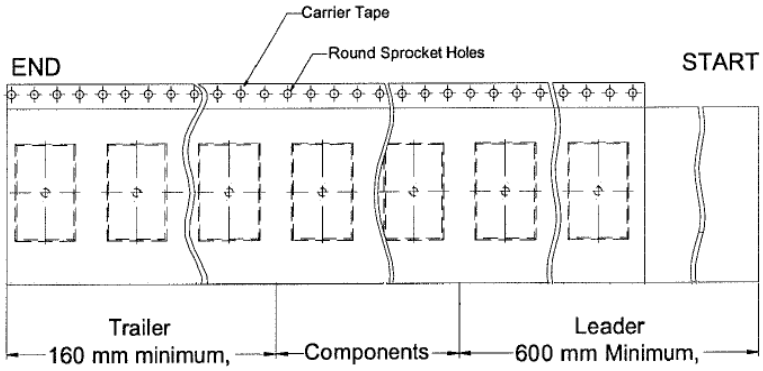
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN5*5-40	40	0.40	5.80	5.80	4.10	4.10	0.85	0.20	3.40	3.40	±0.05

20 Packing Information

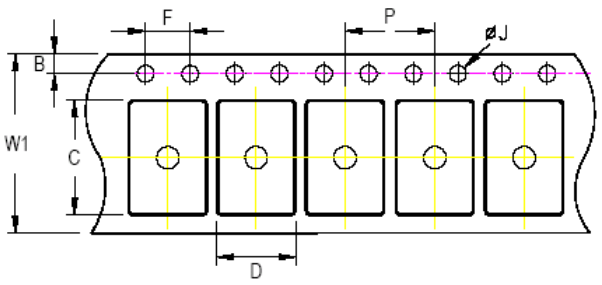
20.1 Tape and Reel Data

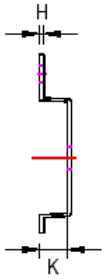






Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 5x5	12	8	180	7	1,500	160	600	12.4/14.4





C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton		
	Size	Units	Item	Weight(Kg)	Reels	Units	Item	Boxes	Unit
QFN/DFN 5x5	7”	1,500	Box A	0.1	3	4,500	Carton A	12	54,000
			Box E	0.03	1	1,500	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description	Item
02	2024/7/6	Modify	Ordering Information on P2 Electrical Characteristics on P4 Operations on P11, P12 Recommended Operating Conditions on P24 Application Information on P34, P45
03	2024/12/21	Modify	General Description on P1 Functional Register Description on P81
04	2024/4/22	Modify	Operations on P22