Multi-Phase PWM Controller for CPU Core Power Supply

General Description

The RT8856 is a single/dual phase PWM controller with two integrated MOSFET drivers. Moreover, it is compliant with Intel IMVP6.5 Voltage Regulator Specification to fulfill its mobile CPU Vcore power supply requirements. The RT8856 adopts NAVP™ (Native AVP) which is Richtek's proprietary topology derived from finite DC gain compensator peak current mode, making it an easy setting PWM controller that meets all Intel AVP (Active Voltage Positioning) mobile CPU requirements.

The output voltage of the RT8856 is set by 7-bit VID code. The built-in high accuracy DAC converts the VID code ranging from 0V to 1.5V with 12.5mV per step. The system accuracy of the controller can reach 1.5%. The part supports VID on-the-fly and mode change on-the-fly functions that are fully compliant with IMVP6.5 specification. It operates in single phase, dual phase and RFM. It can reach up to 90% efficiency in different modes according to different loading conditions. The droop load line can be easily programmed by setting the DC gain of the error amplifier. With proper compensation, the load transient can achieve optimized AVP performance. This chip controls soft-start and output transition slew rate via a capacitor. It supports both DCR and sense resistor current sensing. The current mode NAVP™ topology with high accuracy current sensing amplifier well balances the RT8856's channel currents.

The RT8856 provides power good, clock enabling and thermal throttling output signals for IMVP6.5 specification. It also features complete fault protection functions including over voltage, under voltage, negative voltage, over current, thermal shutdown, and under voltage lockout.

The RT8856 is available in a WQFN-40L 6x6 small foot print package.

Applications

- IMVP6.5 Core Supply
- Multi-phase CPU Core Supply
- AVP Step-Down Converter
- Notebook/ Desktop Computer/ Servers

Features

- **1/2 Phase PWM Controller with 2 Integrated MOSFET Drivers**
- **IMVP6.5 Compatible Power Management States (DPSRLVR, $\overline{\text{PSI}}$, Extended Deeper Sleep Mode)**
- **NAVP (Native AVP) Topology**
- **7-bit DAC**
- **0.8% DAC Accuracy**
- **Fixed V_{BOOT} (1.1V)**
- **Differential Remote Voltage Sensing**
- **Programmable Output Transition Slew Rate Control**
- **Accurate Current and Thermal Balance**
- **System Thermal Compensation AVP**
- **Ringing Free Mode at Light Load Conditions**
- **Fast Transient Response**
- **Power Good**
- **Clock Enable Output**
- **Thermal Throttling**
- **Current Monitor Output**
- **Switching Frequency up to 1MHz Per Phase**
- **OVP, UVP, NVP, OCP, OTP, UVLO**
- **40-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Ordering Information

RT8856□□

- Package Type
  QW : WQFN-40L 6X6 (W-Type)
  (Exposed Pad-Option 1)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

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Marking Information

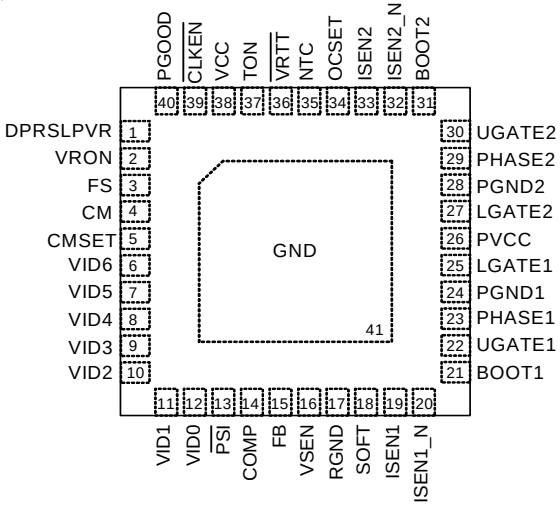
RT8856
GQW
YMDNN
●

RT8856GQW : Product Number

YMDNN : Date Code

Pin Configurations

(TOP VIEW)



WQFN-40L 6x6

Typical Application Circuit

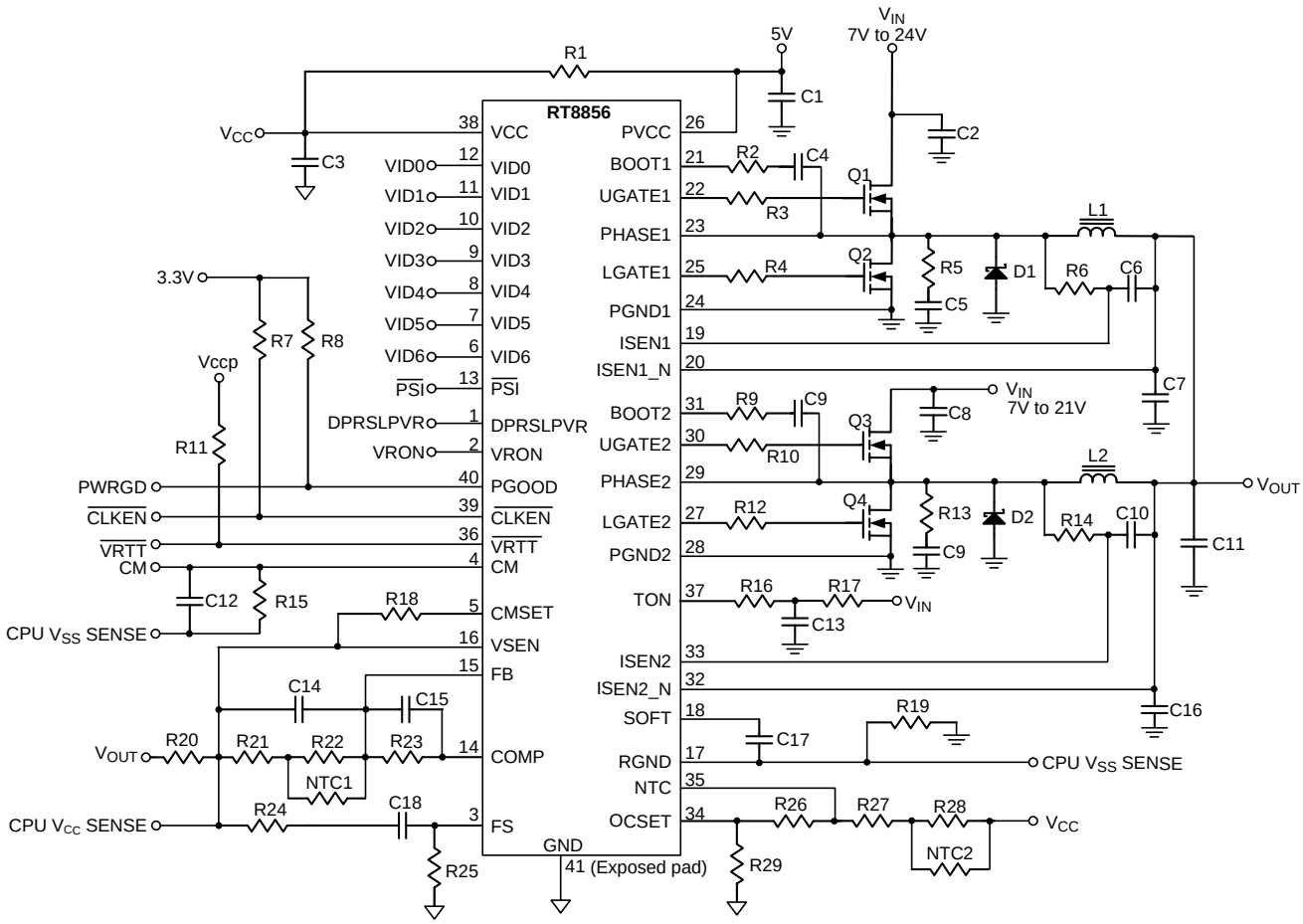


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Table 1. IMVP6.5 VID code table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output
0	0	0	0	0	0	0	1.5000V
0	0	0	0	0	0	1	1.4875V
0	0	0	0	0	1	0	1.4750V
0	0	0	0	0	1	1	1.4625V
0	0	0	0	1	0	0	1.4500V
0	0	0	0	1	0	1	1.4375V
0	0	0	0	1	1	0	1.4250V
0	0	0	0	1	1	1	1.4125V
0	0	0	1	0	0	0	1.4000V
0	0	0	1	0	0	1	1.3875V
0	0	0	1	0	1	0	1.3750V
0	0	0	1	0	1	1	1.3625V
0	0	0	1	1	0	0	1.3500V
0	0	0	1	1	0	1	1.3375V
0	0	0	1	1	1	0	1.3250V
0	0	0	1	1	1	1	1.3125V
0	0	1	0	0	0	0	1.3000V
0	0	1	0	0	0	1	1.2875V
0	0	1	0	0	1	0	1.2750V
0	0	1	0	0	1	1	1.2625V
0	0	1	0	1	0	0	1.2500V
0	0	1	0	1	0	1	1.2375V
0	0	1	0	1	1	0	1.2250V
0	0	1	0	1	1	1	1.2125V
0	0	1	1	0	0	0	1.2000V
0	0	1	1	0	0	1	1.1875V
0	0	1	1	0	1	0	1.1750V
0	0	1	1	0	1	1	1.1625V
0	0	1	1	1	0	0	1.1500V
0	0	1	1	1	0	1	1.1375V
0	0	1	1	1	1	0	1.1250V
0	0	1	1	1	1	1	1.1125V
0	1	0	0	0	0	0	1.1000V

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output
0	1	0	0	0	0	1	1.0875V
0	1	0	0	0	1	0	1.0750V
0	1	0	0	0	1	1	1.0625V
0	1	0	0	1	0	0	1.0500V
0	1	0	0	1	0	1	1.0375V
0	1	0	0	1	1	0	1.0250V
0	1	0	0	1	1	1	1.0125V
0	1	0	1	0	0	0	1.0000V
0	1	0	1	0	0	1	0.9875V
0	1	0	1	0	1	0	0.9750V
0	1	0	1	0	1	1	0.9625V
0	1	0	1	1	0	0	0.9500V
0	1	0	1	1	0	1	0.9375V
0	1	0	1	1	1	0	0.9250V
0	1	0	1	1	1	1	0.9125V
0	1	1	0	0	0	0	0.9000V
0	1	1	0	0	0	1	0.8875V
0	1	1	0	0	1	0	0.8750V
0	1	1	0	0	1	1	0.8625V
0	1	1	0	1	0	0	0.8500V
0	1	1	0	1	0	1	0.8375V
0	1	1	0	1	1	0	0.8250V
0	1	1	0	1	1	1	0.8125V
0	1	1	1	0	0	0	0.8000V
0	1	1	1	0	0	1	0.7875V
0	1	1	1	0	1	0	0.7750V
0	1	1	1	0	1	1	0.7625V
0	1	1	1	1	0	0	0.7500V
0	1	1	1	1	0	1	0.7375V
0	1	1	1	1	1	0	0.7250V
0	1	1	1	1	1	1	0.7125V
1	0	0	0	0	0	0	0.7000V
1	0	0	0	0	0	1	0.6875V

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VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output
1	0	0	0	0	1	0	0.6750V
1	0	0	0	0	1	1	0.6625V
1	0	0	0	1	0	0	0.6500V
1	0	0	0	1	0	1	0.6375V
1	0	0	0	1	1	0	0.6250V
1	0	0	0	1	1	1	0.6125V
1	0	0	1	0	0	0	0.6000V
1	0	0	1	0	0	1	0.5875V
1	0	0	1	0	1	0	0.5750V
1	0	0	1	0	1	1	0.5625V
1	0	0	1	1	0	0	0.5500V
1	0	0	1	1	0	1	0.5375V
1	0	0	1	1	1	0	0.5250V
1	0	0	1	1	1	1	0.5125V
1	0	1	0	0	0	0	0.5000V
1	0	1	0	0	0	1	0.4875V
1	0	1	0	0	1	0	0.4750V
1	0	1	0	0	1	1	0.4625V
1	0	1	0	1	0	0	0.4500V
1	0	1	0	1	0	1	0.4375V
1	0	1	0	1	1	0	0.4250V
1	0	1	0	1	1	1	0.4125V
1	0	1	1	0	0	0	0.4000V
1	0	1	1	0	0	1	0.3875V
1	0	1	1	0	1	0	0.3750V
1	0	1	1	0	1	1	0.3625V
1	0	1	1	1	0	0	0.3500V
1	0	1	1	1	0	1	0.3375V
1	0	1	1	1	1	0	0.3250V
1	0	1	1	1	1	1	0.3125V
1	1	0	0	0	0	0	0.3000V

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output
1	1	0	0	0	0	1	0.2875V
1	1	0	0	0	1	0	0.2750V
1	1	0	0	0	1	1	0.2625V
1	1	0	0	1	0	0	0.2500V
1	1	0	0	1	0	1	0.2375V
1	1	0	0	1	1	0	0.2250V
1	1	0	0	1	1	1	0.2125V
1	1	0	1	0	0	0	0.2000V
1	1	0	1	0	0	1	0.1875V
1	1	0	1	0	1	0	0.1750V
1	1	0	1	0	1	1	0.1625V
1	1	0	1	1	0	0	0.1500V
1	1	0	1	1	0	1	0.1375V
1	1	0	1	1	1	0	0.1250V
1	1	0	1	1	1	1	0.1125V
1	1	1	0	0	0	0	0.1000V
1	1	1	0	0	0	1	0.0875V
1	1	1	0	0	1	0	0.0750V
1	1	1	0	0	1	1	0.0625V
1	1	1	0	1	0	0	0.0500V
1	1	1	0	1	0	1	0.0375V
1	1	1	0	1	1	0	0.0250V
1	1	1	0	1	1	1	0.0125V
1	1	1	1	0	0	0	0.0000V
1	1	1	1	0	0	1	0.0000V
1	1	1	1	0	1	0	0.0000V
1	1	1	1	0	1	1	0.0000V
1	1	1	1	1	0	0	0.0000V
1	1	1	1	1	0	1	0.0000V
1	1	1	1	1	1	0	0.0000V
1	1	1	1	1	1	1	0.0000V

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Functional Pin Description

Pin No.	Pin Name	Pin Function
1	DPRSLPVR	Deeper Sleep Mode Signal. Together with $\overline{PSI}$, the combination of these two pins indicates the power management states.
2	VRON	Voltage Regulator Enabler.
3	FS	Frequency Setting. Connect this pin with a resistor to ground to set the operating frequency.
4	CM	Current Monitor Output. This pin outputs a voltage proportional to the output current.
5	CMSET	Current Monitor Output Gain Externally Setting. Connect this pin with one resistor to VSEN while CM pin is connected to ground with another resistor. The current monitor output gain can be set by the ratio of these two resistors.
6 to 12	VID[6:0]	Voltage ID. DAC voltage identification inputs for IMVP6.5. The logic threshold is 30% of VCCP as the maximum value for low state and 70% of VCCP as the minimum value for the high state. VCCP is 1.05V.
13	$\overline{PSI}$	Power Status Indicator II. Together with DPRSLPVR, the combination of these two pins indicates the power management states.
14	COMP	Compensation. This pin is the output node of the error amplifier.
15	FB	Feedback. This is the negative input node of the error amplifier.
16	VSEN	Positive Voltage Sensing Pin. This pin is the positive node of the differential voltage sensing.
17	RGND	Return Ground. This pin is the negative node of the differential remote voltage sensing.
18	SOFT	Soft-Start. This pin provides soft-start function and slew rate control. The capacitance of the slew rate control capacitor is restricted to be larger than 10nF. The feedback voltage of the converter follows the ramping voltage on the SOFT pin during soft-start and other voltage transitions according to different modes of operation and VID change.
19	ISEN1	Positive Input of Phase1 Current Sense.
20	ISEN1_N	Negative Input of Phase1 Current Sense.
21	BOOT1	Bootstrap Power Pin of Phase1. This pin powers the high side MOSFET drivers. Connect this pin to the junction of the bootstrap capacitor with the cathode of the bootstrap diode. Connect the anode of the bootstrap diode to the PVCC pin.
22	UGATE1	Upper Gate Drive of Phase1. This pin drives the gate of the high side MOSFETs.
23	PHASE1	Return Node of Phase1 High Side Driver. Connect this pin to high side MOSFET sources together with the low side MOSFET drains and the inductor.
24	PGND1	Driver Ground of Phase1.
25	LGATE1	Lower Gate Drive of Phase1. This pin drives the gate of the low side MOSFETs.
26	PVCC	Driver Power.
27	LGATE2	Lower Gate Drive of Phase2. This pin drives the gate of the low side MOSFETs.
28	PGND2	Driver Ground of Phase2.
29	PHASE2	Return Node of Phase2 High Side Driver. Connect this pin to high side MOSFET sources together with the low side MOSFET drains and the inductor.

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Pin No.	Pin Name	Pin Function
30	UGATE2	Upper Gate Drive of Phase2. This pin drives the gate of the high side MOSFETs.
31	BOOT2	Bootstrap Power Pin of Phase2. This pin powers the high side MOSFET drivers. Connect this pin to the junction of the bootstrap capacitor with the cathode of the bootstrap diode. Connect the anode of the bootstrap diode to the PVCC pin.
32	ISEN2_N	Negative Input of Phase2 Current Sense.
33	ISEN2	Positive input of Phase2 Current Sense.
34	OCSET	Over Current Protection Setting. Connect a resistive voltage divider from VCC to ground and connect the joint of the voltage divider to the OCSET pin. The voltage, V_{OCSET}, determines the over current threshold, I_{LIM}.
35	NTC	Thermal Detection Input for $\overline{VRTT}$ Circuit. Connect this pin with a resistive voltage divider from VCC using NTC on the top to set the thermal management threshold level.
36	$\overline{VRTT}$	Voltage Regulator Thermal Throttling. This open-drain output pin indicates the temperature exceeding the preset level when it is pulled low.
37	TON	Connect this pin to VIN with one resistor. This resistor value sets the ripple size in ringing free mode.
38	VCC	Chip Power.
39	$\overline{CLKEN}$	Inverted Clock Enable. This open-drain pin is an output indicating the start of the PLL locking of the clock chip.
40	PGOOD	Power Good Indicator.
41 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

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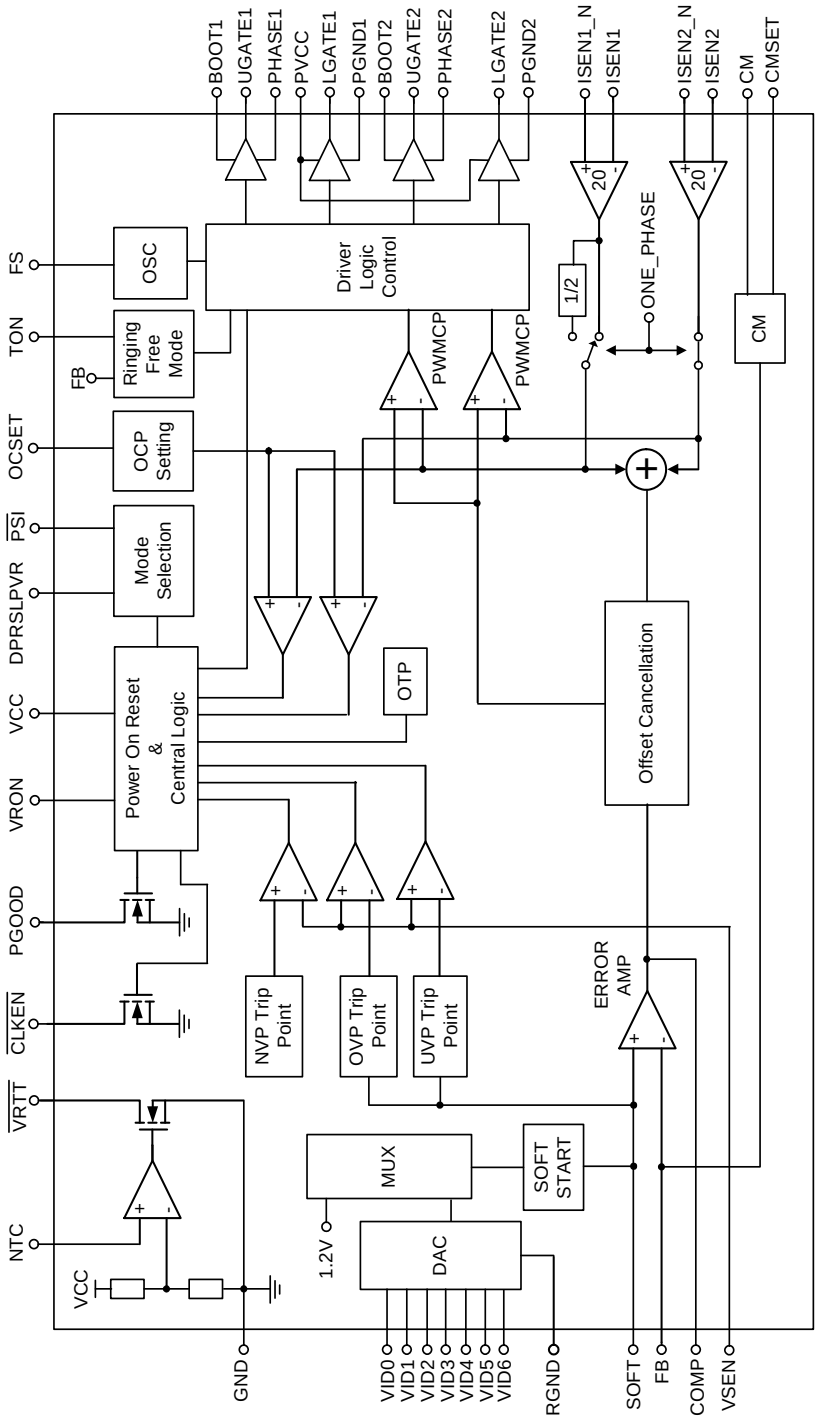
Function Block Diagram



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Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 6.5V
- RGND, PGNDx to GND ---------- –0.3V to 0.3V
- VIDx to GND ---------- –0.3V to (V_{CC} + 0.3V)
- $\overline{PSI}$, VRON to GND ---------- –0.3V to (V_{CC} + 0.3V)
- PGOOD, $\overline{CLKEN}$, $\overline{VRTT}$ to GND ---------- –0.3V to (V_{CC} + 0.3V)
- VSEN, FB, COMP, SOFT, FS, OCSET, CM, CMSET, NTC to GND ---------- –0.3V to (V_{CC} + 0.3V)
- ISENx, ISEN1_N, ISEN2_N to GND ---------- –0.3V to (V_{CC} + 0.3V)
- PVCC to PGNDx ---------- –0.3V to 6.5V
- LGATEx to PGNDx ---------- –0.3V to (PVCC + 0.3V)
- PHASEx to PGNDx ---------- –0.3V to 28V
- BOOTx to PHASEx ---------- –0.3V to 6.5V
  < 5ns ---------- –8V to 36V
- UGATEx to PHASEx ---------- –0.3V to (BOOTx – PHASEx)
- PGOOD ---------- –0.3V to (V_{CC} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  WQFN–40L 6x6 ---------- 2.941W
- Package Thermal Resistance (Note 2)
  WQFN-40L 6x6, θ_{JA} ---------- 34°C/W
  WQFN-40L 6x6, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{CC} ---------- 4.5V to 5.5V
- Battery Voltage, V_{IN} ---------- 7V to 24V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Current	I_{VCC} + I_{PVCC}	R_{FS} = 33kΩ, V_{VRON} = 3.3V, Not Switching	--	--	10	mA
Shutdown Current	I_{CC} + I_{PVCC}	V_{VRON} = 0V	--	--	5	μA
Soft-Start/Slew Rate Control (based on 10nF C_{SS})						
Soft-Start / Soft-Shutdown	I_{SS1}	V_{SOFT} = 1.5V	16	20	24	μA
Deeper Sleep Exit/VID Change Slew Current	I_{SS2}	V_{SOFT} = 1.5V	80	100	120	μA

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator							
Frequency	Frequency	f_{OSC}	R_{FS} = 33kΩ, V_{DAC} > 1.05	270	300	330	kHz
	Variation		R_{FS} = 5kΩ to 50kΩ	–20	--	20	%
Frequency Range			Per phase	200	--	1000	kHz
Maximum Duty Cycle			Per phase	--	50	--	%
FS pin Output Voltage		V_{FS}	R_{FS} = 33kΩ, V_{DAC} > 1.05	1	1.05	1.1	V
Reference and DAC							
DC Accuracy		V_{FB}	V_{DAC} = 0.7500 – 1.5000 (No Load, Active Mode)	–0.8	0	0.8	%VID
			V_{DAC} = 0.5000 – 0.7500	–7.5	0	7.5	mV
Boot Voltage		V_{BOOT}		1.089	1.1	1.111	V
Error Amplifier							
DC Gain			R_L = 47kΩ	70	80	--	dB
Gain-Bandwidth Product		GBW	C_{LOAD} = 5pF	--	10	--	MHz
Slew Rate		SR	C_{LOAD} = 10pF (Gain = –4, R_F = 47kΩ, V_{OUT} = 0.5V – 3V)	--	5	--	V/μs
Output Voltage Range		V_{COMP}	R_L = 47kΩ	0.5	--	3.6	V
MAX Source/Sink Current		I_{OUTEA}	V_{COMP} = 2V	--	250	--	μA
Current Sense Amplifier							
Input Offset Voltage		V_{OSCS}		–1	--	1	mV
Impedance at Neg. Input		R_{ISENx_N}		1	--	--	MΩ
Impedance at Pos. Input		R_{ISENx}		1	--	--	MΩ
DC Gain		A_I		--	10	--	V/V
Input Range		V_{ISENx_IN}		–50	--	100	mV
RFM TON Setting							
TON Pin Output Voltage		V_{TON}	R_{TON} = 80kΩ, V_{TON} = V_{DAC} = 0.75V	–5	0	5	%
DEM ON-Time Setting		t_{ON}	I_{RTON} = 80μA	--	350	--	ns
R_{TON} Current Range		I_{RTON}		25	--	280	μA
Protection							
Under Voltage Lockout Threshold		V_{UVLO}	Falling edge	4.1	4.3	4.5	V
Under Voltage Lockout Threshold Hysteresis		ΔV_{UVLO}		--	200	--	mV
Absolute Over Voltage Protection Threshold		V_{OVABS}	(With respect to 1.5V, ±50mV)	1.45	1.5	1.55	V
Relative Over Voltage Protection Threshold		V_{OV}	(With respect to V_{VID}, ±50mV)	150	200	250	mV
Under Voltage Protection Threshold		V_{UV}	Measured at VSEN with respect to unloaded output voltage (UOV) (for 0.8 < UOV < 1.5)	–350	–300	–250	mV
Negative Voltage Protection Threshold		V_{NV}	Measured at VSEN with respect to GND	–100	--	--	mV

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit Threshold Voltage (Average)		V_{ILIM}	Σ ($V_{ISENx} - V_{ISENx\_N}$) / N, V_{OCSET} = 0.625V, $V_{ILIMT(nom)}$ = 25mV	23	25	27	mV
Current Limit Threshold Voltage (per phase)		V_{ILIM_PH}	$V_{ILIMITPH}$ / V_{ILIMIT}	--	150	--	%
Thermal Shutdown Threshold		T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	10	--	°C
Logic Inputs							
VRON Input Threshold Voltage	Logic-High	V_{IH}	With respect to 3.3V, 70%	2.31	--	--	V
	Logic-Low	V_{IL}	With respect to 3.3V, 30%	--	--	0.99	
Leakage Current of VRON				–1	--	1	µA
DAC (VID0 – VID6), $\overline{PSI}$ and DPRSLPVR Input Threshold Voltage	Logic-High	V_{IH}	With respect to 1.1V, 70%	0.77	--	--	V
	Logic-Low	V_{IL}	With respect to 1.1V, 30%	--	--	0.33	
Leakage Current of DAC (VID0 – VID6), $\overline{PSI}$ and DPRSLPVR				–1	--	1	µA
Power Good							
PGOOD Threshold		V_{TH_PGOOD}		--	1	--	V
PGOOD Low Voltage		V_{PGOOD}	I_{PGOOD} = 4mA	--	--	0.4	V
PGOOD Delay		t_{PGOOD}	$\overline{CLKEN}$ Low to PGOOD High	3	--	20	ms
Clock Enable							
$\overline{CLKEN}$ Low Voltage		$V_{\overline{CLKEN}}$	$I_{\overline{CLKEN}}$ = 4mA	--	--	0.4	V
Thermal Throttling							
Thermal Throttling Threshold		V_{OT}	Measure at NTC with respect to V_{CC}	--	80	--	$\%V_{DD}$
Thermal Throttling Threshold Hysteresis		V_{OT_HY}	At V_{CC} = 5V	--	100	--	mV
$\overline{VRTT}$ Output Voltage		$V_{\overline{VRTT}}$	$I_{\overline{VRTT}}$ = 40mA	--	--	0.4	V
Current Monitor							
Current Monitor Maximum Output Voltage in Operating Range			V_{DAC} = 1V, V_{RCMSET} = 90mV, R_{CM} = 50kΩ, R_{CMSET} = 10kΩ	0.855	0.9	0.945	V
Current Monitor Maximum Output Voltage				--	--	1.15	V
Gate Driver							
UGATE Driver Source		$R_{UGATEsr}$	$V_{BOOTx} - V_{PHASEx}$ = 5V $V_{BOOTx} - V_{UGATEx}$ = 1V	--	0.7	--	Ω
UGATE Driver Sink		$R_{UGATEsk}$	V_{UGATE} = 1V	--	0.6	--	Ω
LGATE Driver Source		$R_{LGATEsr}$	V_{PVCC} = 5V, $V_{PVCC} - V_{LGATE}$ = 1V	--	0.7	--	Ω
LGATE Driver Sink		$R_{LGATEsk}$	V_{LGATE} = 1V	--	0.3	--	Ω
UGATE Driver Source/Sink Current		I_{UGATE}	$V_{BOOT} - V_{PHASE}$ = 5V V_{UGATE} = 2.5V	--	3	--	A
LGATE Driver Source Current		$I_{LGATEsr}$	V_{LGATE} = 2.5V	--	3	--	A

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LGATE Driver Sink Current	$I_{LGATEsk}$	V_{LGATE} = 2.5V	--	5	--	A
Internal Boost Charging Switch On-Resistance	R_{BOOT}	PVCC to BOOTx	--	30	--	Ω

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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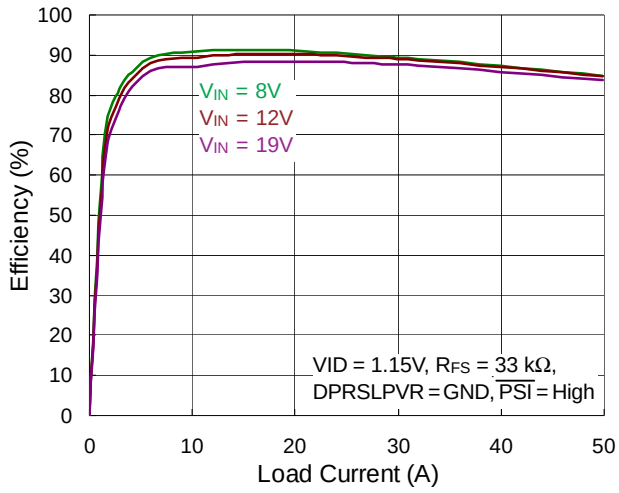
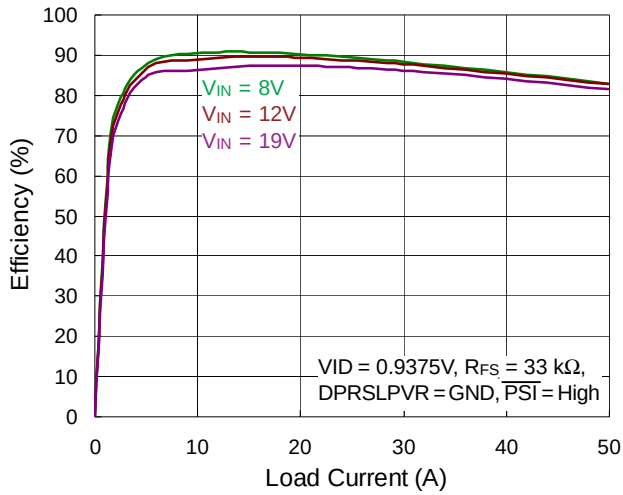
Typical Operating Characteristics

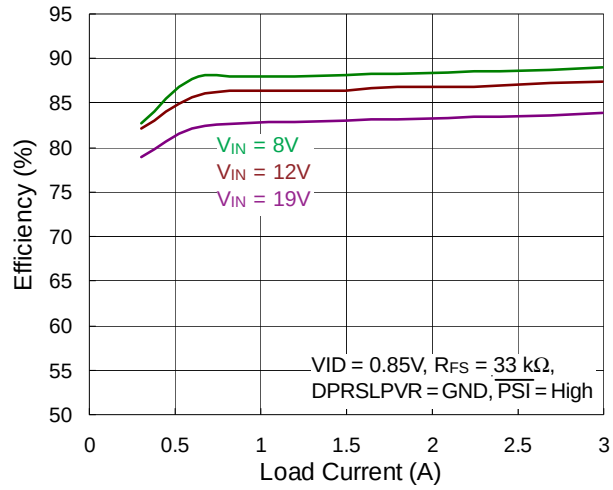
CCM Efficiency vs. Load Current



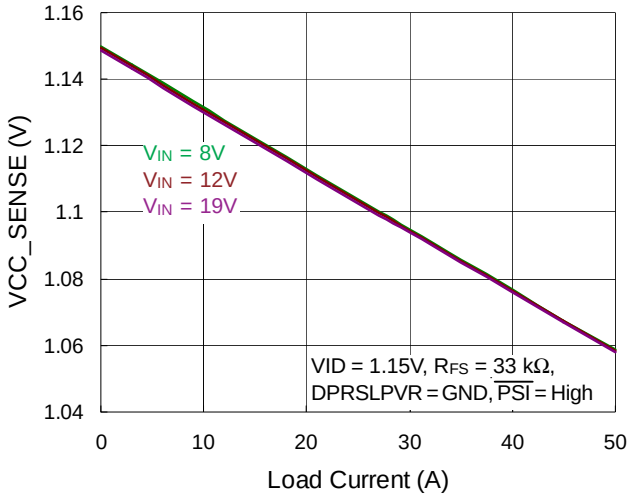
CCM Efficiency vs. Load Current



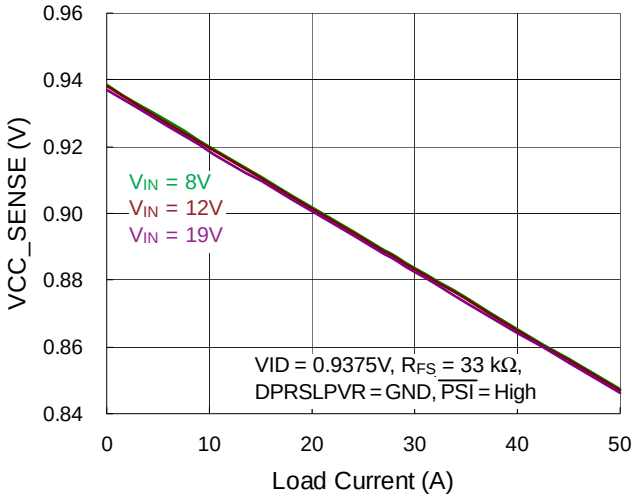
DEM Efficiency vs. Load Current



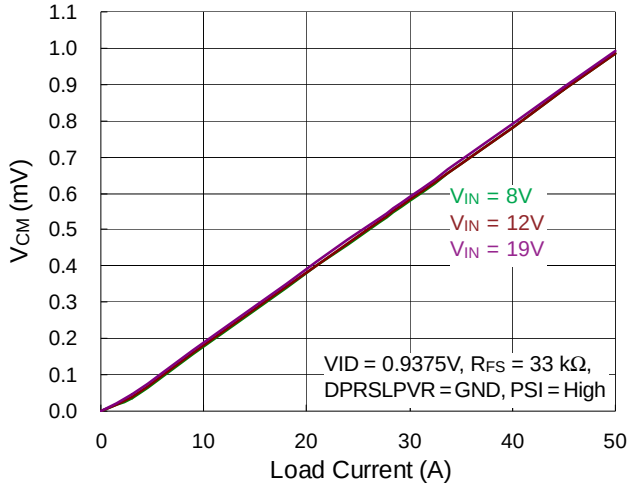
CCM VCC_SENSE vs. Load Current



CCM VCC_SENSE vs. Load Current



V_{CM} vs. Load Current



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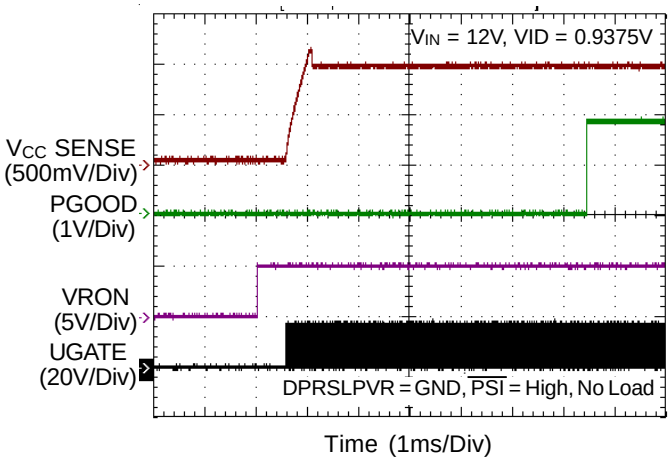
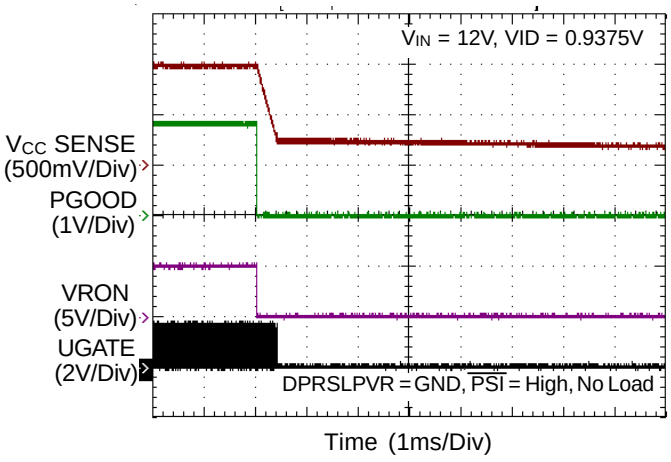
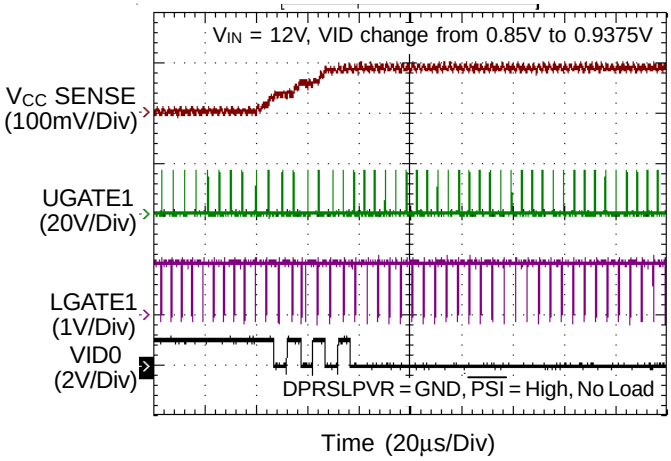
Power On from VRON



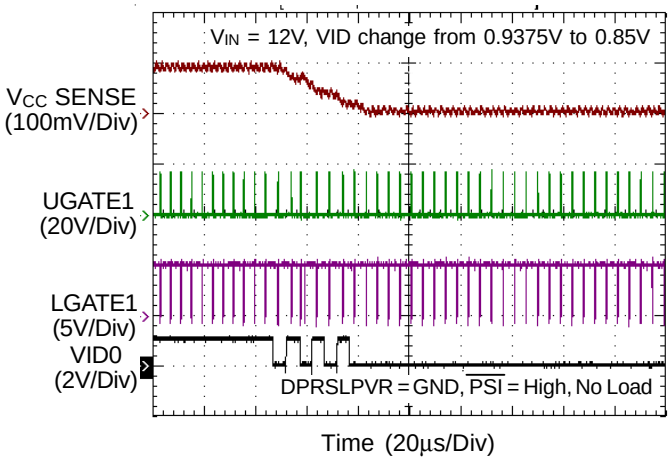
Power Off from VRON



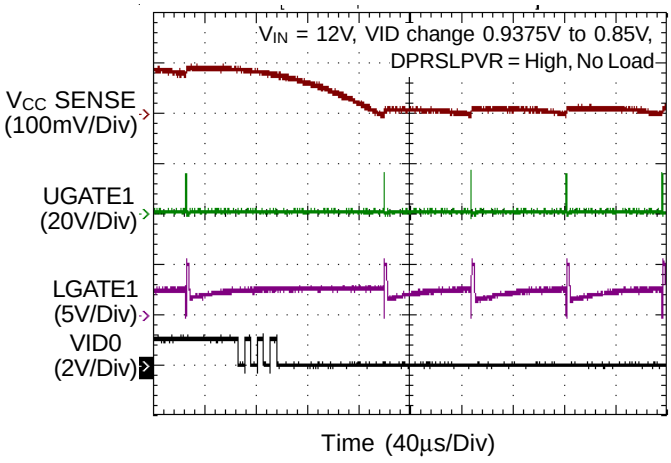
CCM VID Change Up



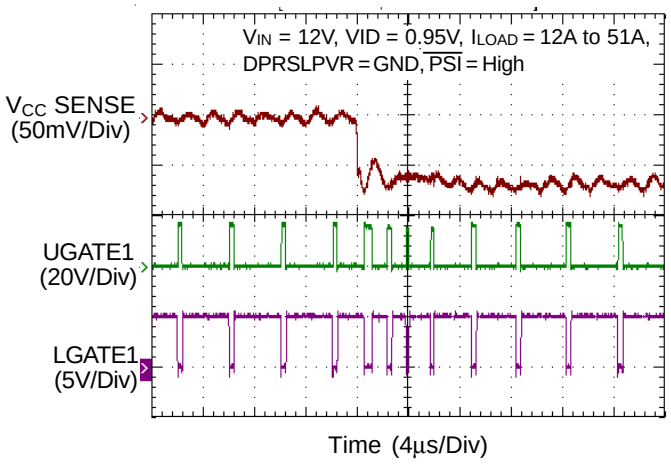
CCM VID Change Down



RFM VID Change Down



CCM Load Transient Response



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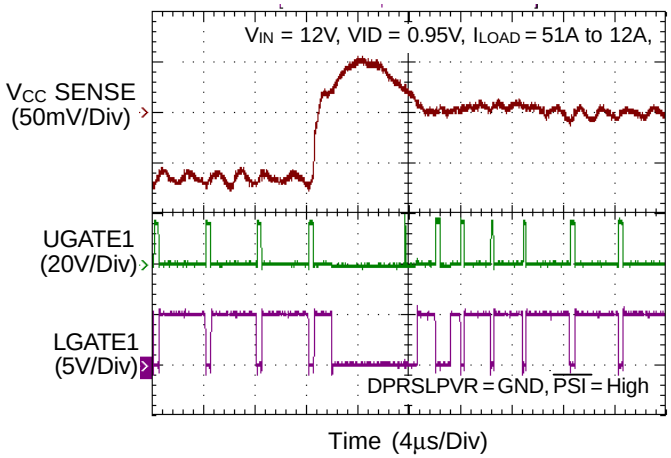
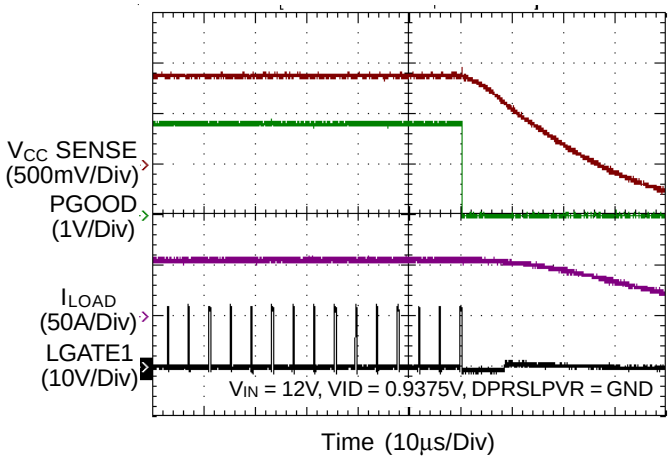
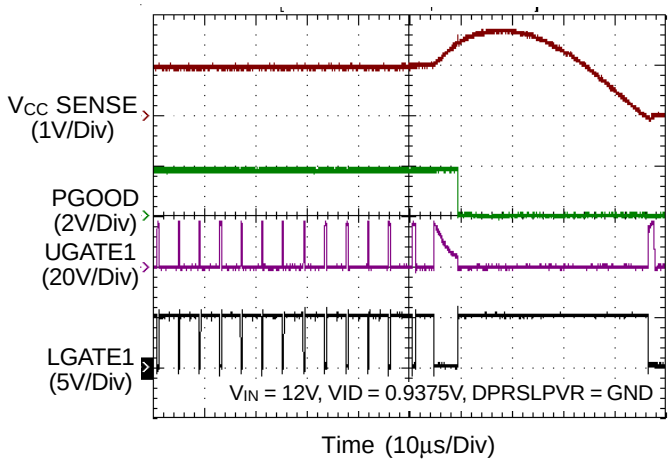
CCM Load Transient Response



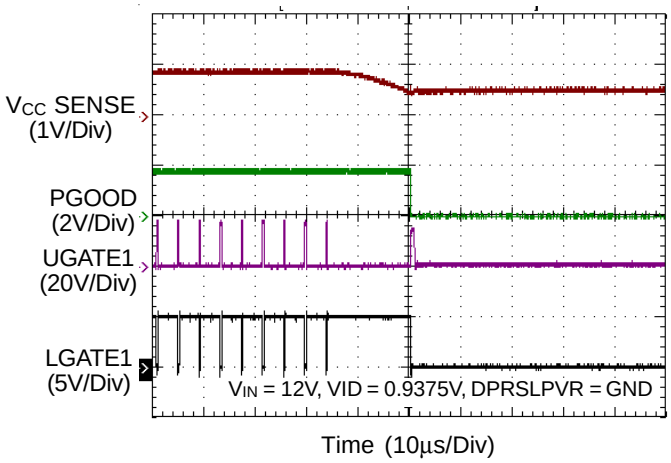
Over Current Protection



Over Voltage Protection



Under Voltage Protection



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Application Information

The RT8856 is a 1/2-phase DC/DC controller and includes embedded gate drivers for reduced system cost and board area. The number of phases is not only user selectable, but also dynamically changeable based on Intel's IMVP6.5 control signals to optimize efficiency. Phase currents are continuously sensed for loop control, droop tuning, and over current protection. The internal 7-bit VID DAC and a low offset differential amplifier allow the controller to maintain high voltage regulating accuracy to meet Intel's IMVP6.5 specification.

Design Tool

To reduce the efforts and errors caused by manual calculations, a user friendly design tool is now available on request.

This design tool calculates all necessary design parameters by entering user's requirements. Please contact Richtek's representatives for details.

Phase Selection and Operation Modes

The maximum number of operating phase is programmable by setting ISEN2_N. After the initial turn-on of the RT8856, an internal comparator checks the voltage at the ISEN2_N pin. To set the RT8856 as a pure single phase PWM controller, connect ISEN2_N to a voltage higher than (V_{CC} - 1V) at power on. The controller will then disable phase 2 (hold UGATE2 and LGATE2 low) and operate as a single phase PWM controller.

The RT8856 also works in conjunction with Intel's IIMVP6.5 control signals, such as ~~PSI~~ and DPRSLPVR. Table 2 shows the control signal truth table for operation modes of the RT8856.

For high current demand, the controller will operate with both phases active. These two phase gate signals are interleaved. This achieves minimal output voltage ripple and best transient performance.

For reduced current demand, only one phase is active. For 1-phase operation, the power stage can minimize switching losses and maintain transient response capability.

At lowest current levels, the controller enters single phase Ringing-Free Mode (RFM) to achieve highest efficiency.

Table 2. Control signal truth table for operation modes

DPRSLPVR	$\overline{PSI}$	Operation mode
0	1	Multi-phase CCM
0	0	Single-phase CCM
1	1	S Single-phase RFM, slow C4E
1	0	Single-phase RFM, slow C4E

Differential Remote Sense Setting

The RT8856 includes differential, remote sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pin voltages, V_{CC_SENSE} and V_{SS_SENSE}. V_{SS_SENSE} is connected to RGND pin. The V_{CC_SENSE} is connected to FB pin with a resistor to build the negative input path of the error amplifier. Connect VSEN to V_{CC_SENSE} for $\overline{CLKEN}$, PGOOD, OVP, and UVP sense. The 7-bit VID DAC and the precision voltage reference are referred to RGND for accurate remote sensing.

Current Sense Setting

The RT8856 continuously sense the output current of each phase. Therefore, the controller can be less noise sensitive and get more accurate current sharing between phases. Low offset amplifiers are used for loop control and current limit. The internal current sense amplifier gain (A_I) is fixed to be 10. The ISENx and ISENx_N denote the positive and negative input of the current sense amplifier of each phase, respectively. Users can either use a current-sense resistor or the inductor's DCR for current sensing.

Using inductor's DCR allows higher efficiency as shown in Figure 1. If

$$\frac{L}{DCR} = R_X \times C_X \quad (1)$$

then the current sense performance will be optimum. For example, choosing L = 0.36μH with 1mΩ DCR and C_X = 100nF, yields R_X :

$$R_X = \frac{0.36\mu H}{1.0m\Omega \times 100nF} = 3.6k\Omega \quad (2)$$

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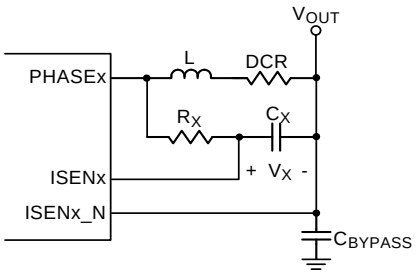

Figure 1. Lossless Inductor Sensing

Since the inductance tolerances are normally observed to be 20%, the resistor, R_X, has to be tuned on board by examining the transient voltage. If the output voltage transient has an initial dip below the minimum load line requirement with a slow recovery, R_X is chosen too small. Vice versa, with a resistance too large, the output voltage transient has only a small initial dip and the recovery is too fast, thus causing a ring-back.

Using current sense resistor in series with the inductor can have better accuracy, but the efficiency is a trade-off. Considering the equivalent inductance (L_{ESL}) of the current sense resistor, an RC filter is recommended. The RC filter calculation method is similar to the above-mentioned inductor DCR sensing method .

Loop Control

The RT8856 adopts Richtek's proprietary NAVP™ topology. NAVP™ is based on the finite-gain peak current mode PWM topology. The output voltage, V_{OUT}, will decrease with increasing output load current. The control loop consists of PWM modulator with power stage, current sense amplifier and error amplifier as shown in Figure 2.

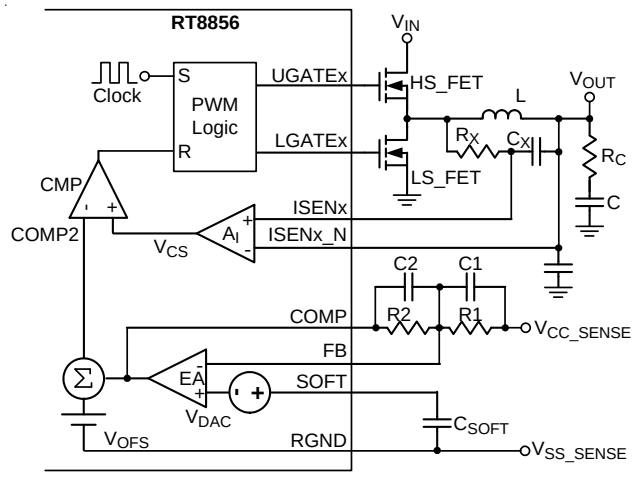

Figure 2. Simplified Schematic for Droop and Remote Sense in CCM

Similar to the peak current mode control with finite compensator gain, the HS_FET on-time is determined by both the internal clock and the PWM comparator which compares the EA output with the output of current sense amplifier. When load current increases, V_{CS} increases, the steady state COMP voltage also increases and makes the V_{OUT} decrease, hence achieving AVP. A near-DC offset (V_{OFS}) is added to the output EA to cancel the inherent output offset of finite-gain peak current mode controller.

In RFM, HS_FET is turned on with constant TON when V_{CS} is lower than V_{COMP2}. Once the HS_FET is turned off, LS_FET is turned on automatically. By Ringing-Free Technique, the LS_FET allows only partial of negative current when the inductor free-wheeling current reaches negative. The switching frequency will be proportionately reduced, thus the conduction and switching losses will be greatly reduced.

Droop Setting (with Temperature Compensation)

It's very easy to achieve Active Voltage Positioning (AVP) by properly setting the error amplifier gain with respect to the native droop characteristics. The target is to have Equation (3)

$$V_{OUT} = V_{SOFT} - I_{LOAD} \times R_{DROOP} \quad (3)$$

then solving the switching condition $V_{COMP2} = V_{CS}$ in Figure 2 yields the desired error amplifier gain as

$$A_V = \frac{R2}{R1} = \frac{A_I \times R_{SENSE}}{R_{DROOP}} \quad (4)$$

where A_I is the internal current sense amplifier gain. R_{SENSE} is the current sense resistor. If there is no external sense resistor, it is the DCR of the inductor. R_{DROOP} is the resistive slope value of the converter output and is the desired static output impedance, e.g. –1.9mΩ or –3mΩ for IMVP6.5 specification. Increasing A_V can make load line more shallow as shown in Figure 3.

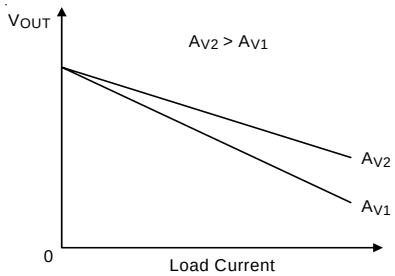

Figure 3. Error Amplifier Gain (A_V) Influence on V_{OUT} Accuracy

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Since the DCR of inductor is highly temperature dependent, it affects the output accuracy at hot conditions. Temperature compensation is recommended for the lossless inductor DCR current sense method. Figure 4 shows a simple but effective way of compensating the temperature variations of the sense resistor using an NTC thermistor placed in the feedback path.

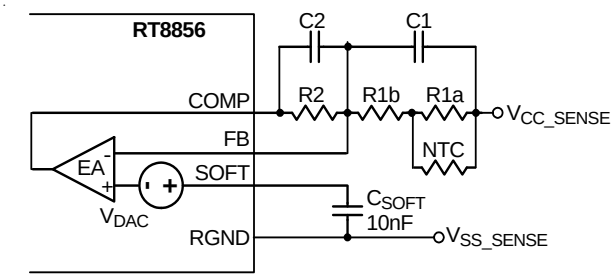

Figure 4. Loop Setting with Temperature Compensation

Usually, R1a is set to equal R_{NTC} (25°C). R1b is selected to linearize the NTC's temperature characteristic. For a given NTC, design is to get R1b and R2 and then C1 and C2. According to Equation (4), to compensate the temperature variations of the sense resistor, the error amplifier gain (A_V) should have the same temperature coefficient with R_{SENSE}. Hence,

$$\frac{A_{V,\,HOT}}{A_{V,\,COLD}} = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} \quad (5)$$

From Equation (4), Av can be obtained at any temperature (T) as shown below :

$$A_{V,\,T} = \frac{R2}{R1a\,//\,R_{NTC,\,T} + R1b} \quad (6)$$

The standard formula for the resistance of NTC thermistor as a function of temperature compensation is given by :

$$R_{NTC,\,T} = R_{25}\; e^{\left\{\beta\left[\left(\frac{1}{T+273}\right)-\left(\frac{1}{298}\right)\right]\right\}} \quad (7)$$

where R_{25} is the thermistor's nominal resistance at room temperature, β (beta) is the thermistor's material constant in Kelvins, and T is the thermistor's actual temperature in Celsius.

To calculate DCR value at different temperature, use the equation below :

$$DCR_T = DCR_{25} \text{ x } [1 + 0.00393 \text{ x } (T - 25)] \quad (8)$$

where the 0.00393 is the temperature coefficient of the copper. For a given NTC thermistor, solving Equation (6) at room temperature (25°C) yields

$$R2 = A_{V,\,25} \text{ x } (R1b + R1a\,//\,R_{NTC,\,25}) \quad (9)$$

where $A_{V,\,25}$ is the error amplifier gain at room temperature and can be obtained from Equation (4). R1b can be obtained by substituting Equation (9) to (5),

$$R1b = \frac{\frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} \times (R1a\,//\,R_{NTC,\,HOT}) - (R1a\,//\,R_{NTC,\,HOT})}{\left(1 - \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}}\right)} \quad (10)$$

Loop Compensation

Optimized compensation of the RT8856 allows for best possible load step response of the regulator's output. A type-II compensator with one pole and one zero is adequate for a proper compensation. Figure 4 shows the compensation circuit. Prior design procedure shows how to select the resistive feedback components for the error amplifier gain. Next, the C1 and C2 must be calculated for the compensation. The target is to achieve constant resistive output impedance over the widest possible frequency range.

The pole frequency of the compensator must be set to compensate the output capacitor ESR zero :

$$f_P = \frac{1}{2 \times \pi \times C \times R_C} \quad (11)$$

where C is the capacitance of output capacitor, and R_C is the ESR of output capacitor. C2 can be calculated as follows :

$$C2 = \frac{C \times R_C}{R2} \quad (12)$$

The zero of compensator has to be placed at half of the switching frequency to filter the switching related noise. such that,

$$C1 = \frac{1}{(R1b + R1a\,//\,R_{NTC,\,25}) \times \pi \times f_{SW}} \quad (13)$$

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Frequency Setting

High frequency operation optimizes the application for smaller component size, but trads off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low frequency operation offers the best overall efficiency at the expense of component size and board space.

Connect a resistor (R_{FS}) between FS and ground to set the switching frequency (f_{SW}) per phase :

$$R_{FS}(k\Omega) = \frac{300(kHz) \times 33(k\Omega)}{f_{SW}(kHz)} \quad (14)$$

A resistor of 5kΩ to 50kΩ corresponds to switching frequency of 1MHz to 200kHz, respectively.

Soft-Start and Mode Change Slew Rates

The RT8856 uses 2 slew rates for various modes of operation. These two slew rates are internally determined by commanding one of two bi-directional current sources on to the SOFT pin (I_{SS}). The 7-bit VID DAC and the precision voltage reference are referred to RGND for accurate remote sensing. Hence, connect a capacitor (C_{SOFT}) from SOFT pin to RGND for controlling the slew rate as shown in Figure 4. The capacitance of capacitor is restricted to be larger than 10nF. The voltage on SOFT pin (V_{SOFT}) is higher than the reference voltage of the error amplifier at about 0.9V.

The first current of typically 20μA is used to charge or discharge the C_{SOFT} during soft-start, soft-shutdown. The second current of typically 100μA is used during other voltage transitions, including VID change and transitions between operation modes.

The IMVP6.5 specification specifies the critical timing associated with regulating the output voltage. The symbol, SLEWRATE, as given in the IMVP6.5 specification will determine the choice of the SOFT capacitor, $C_{SOFT,}$ by the following equation :

$$C_{SOFT}(nF) = \frac{I_{SS}(\mu A)}{SLEWRATE(mV/\mu s)} \quad (15)$$

Power Up Sequence

With the controller's VCC voltage above the POR threshold (typ. 4.3V), the power-up sequence begins when VRON exceeds the 3.3V logic high threshold. Approximately 20μs later, SOFT and V_{CORE} starts ramping up to boot voltage (1.1V) with maximum phases. The slew rate during power-up is 20μA/C_{SOFT}. The RT8856 pulls $\overline{CLKEN}$ low after V_{VSEN} rises above 1V for 73μs. Right after $\overline{CLKEN}$ goes low, SOFT and V_{CORE} starts ramping to first DAC value. After $\overline{CLKEN}$ goes low for approximate 4.7ms, PGOOD is asserted HIGH. DPRSLPVR and $\overline{PSI}$ are valid right after PGOOD is asserted. UVP is masked as long as V_{SOFT} is less than 1V.

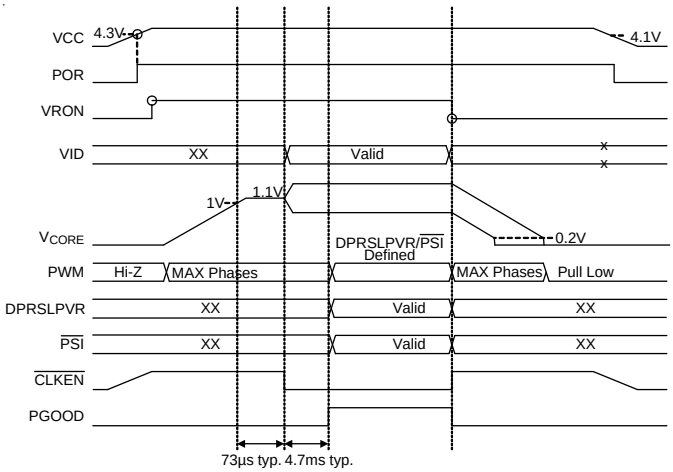

Figure 5. Timing Diagram for Power-Up and Power-Down

Power Down

When VRON goes low, the RT8856 enters low-power shutdown mode. PGOOD is pulled low immediately and V_{SOFT} ramps down with slew rate of 20μA/C_{SOFT}. V_{VSEN} also ramps down following V_{SOFT} with maximum phases. After V_{VSEN} falls below 200mV, the RT8856 turns off both high side and low side MOSFETs. A discharging resistor at VSEN will be enabled and the analog part will be turned off.

Deeper Sleep Mode Transitions

After DPRSLPVR goes high, the RT8856 immediately disables phase 2 (UGATE2 and LGATE2 forced low) and enters 1-phase deeper sleep mode operation. If the VIDs are set to a lower voltage setting, the output drops at a rate determined by the load and the output capacitance. The internal target V_{SOFT} still ramps as before, and UVP, OCP and OVP are masked for 73μs.

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The RT8856 provides 2 slew rates for deeper sleep mode entry/ exit. For standard deeper sleep exit, the RT8856 immediately activates all enabled phases and ramps the output voltage to the DAC code provided by the processor at the slew rate of 100μA/C_{SOFT}. The RT8856 remains in 1-phase ringing free mode and ramps the output voltage to the DAC code provided by the processor at the slew rate of 20μA/C_{SOFT}.

Current Limit Setting

The RT8856 compares a programmable current limit set point to the voltage from the current sense amplifier output for Over Current Protection (OCP). The voltage applied to OCSET pin defines the desired current limit threshold, I_{LIM} :

$$V_{OCSET} = 25 \times I_{LIM} \times R_{SENSE} \quad (16)$$

Connect a resistive voltage divider from VCC to GND, with the joint of the voltage divider connected to OCSET pin as shown in Figure 6. For a given R_{OC2},

$$R_{OC1} = R_{OC2} \times \left(\frac{V_{CC}}{V_{OCSET}} - 1 \right) \quad (17)$$

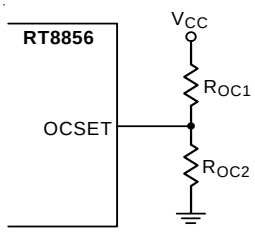

Figure 6. OCP Setting Without Temperature Compensation

The OCP works in two stages :

- Stage 1 : Average inductor current exceeds the current limit threshold, I_{LIM}, defined by V_{OCSET}, but remains smaller than 150% of I_{LIM} If the over current condition remains valid for 16 cycles, the OCP latches and the system shuts down.
- Stage 2 : Any inductor current exceeds 150% of I_{LIM} then OCP latches instantaneously.

Latched OCP forces driver high impedance with UGATEx = 0 and LGATEx = 0. After latched OCP happens, V_{VSEN} will be monitored. When V_{VSEN} falls below 200mV, a discharging resistor at VSEN will be enabled.

If inductor DCR is used as current sense component, then temperature compensation is recommended to protect under all conditions. Figure 7 shows a typical OCP setting with temperature compensation.

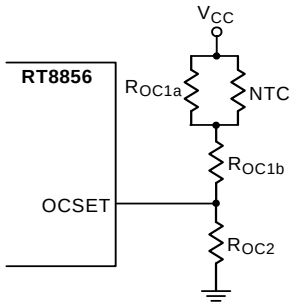

Figure 7. OCP Setting with Temperature Compensation

Usually, select R_{OC1a} equal to thermistor's nominal resistance at room temperature. Ideally, V_{OCSET} should have same temperature coefficient as R_{SENSE} (Inductor DCR) :

$$\frac{V_{OCSET,\,HOT}}{V_{OCSET,\,COLD}} = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} \quad (18)$$

According to the basic circuit calculation, V_{OCSET} can be obtained at any temperature :

$$V_{OCSET,\,T} = \frac{R_{OC2}}{R_{OC1a} // R_{NTC,\,T} + R_{OC1b} + R_{OC2}} \quad (19)$$

Re-write Equation (18) from (19), and get V_{OCSET} at room temperature

$$\frac{R_{OC1a} // R_{NTC,\,COLD} + R_{OC1b} + R_{OC2}}{R_{OC1a} // R_{NTC,\,HOT} + R_{OC1b} + R_{OC2}} = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} \quad (20)$$

$$V_{OCSET,\,25} = \frac{R_{OC2}}{R_{OC1a} // R_{NTC,\,25} + R_{OC1b} + R_{OC2}} \quad (21)$$

Solving Equation (20) and (21) yields R_{OC1b} and R_{OC2}

$$R_{OC2} = \frac{\alpha \times R_{EQU,\,HOT} - R_{EQU,\,COLD} + (1-\alpha) \times R_{EQU,\,25}}{\frac{V_{CC}}{V_{OCSET,\,25}} \times (1-\alpha)} \quad (22)$$

$$R_{OC1b} = \frac{(\alpha - 1) \times ROC2 + \alpha \times R_{EQU,\,HOT} - R_{EQU,\,COLD}}{(1-\alpha)} \quad (23)$$

where

$$\alpha = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} = \frac{DCR_{25} \times [1 + 0.00393 \times (T_{HOT} - 25)]}{DCR_{25} \times [1 + 0.00393 \times (T_{COLD} - 25)]} \quad (24)$$

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$R_{EQU, T} = R1a // R_{NTC, T}$ (25)

For example, the following design parameters are given :

DCR =1mΩ, V_{CC} = 5V, $I_{L, Ripple}$ = 5A

$R_{OC1a} = R_{NTC, 25}$ = 10kΩ, β_{NTC} = 2400

For –20°C to 100°C operation range, to set OCP trip current I_{TRIP} = 57A when operating with maximum phases :

$$I_{LIM} = \frac{57A}{2} + 5A = 33.5A$$

$$V_{OCSET, 25} = 25 \times 33.5A \times 1m\Omega = 0.8375V$$

$R_{NTC, -20}$ =41.89kΩ, $R_{NTC, 100}$ = 1.98kΩ

$R_{SENSE, -20}$ =0.82 mΩ, $R_{SENSE, 100}$ =1.29mΩ

$\Rightarrow R_{OC2}$ = 2.437kΩ, R_{OC1b} = 7.113kΩ

Over Voltage Protection (OVP)

The OVP circuit is triggered under two conditions :

- Condition 1 : When V_{VSEN} exceeds 1.55V.
- Condition 2 : When V_{VSEN} exceeds V_{DAC} by 200mV.

If either condition is valid, the RT8856 latches the LGATEx =1 and UGATEx = 0 as crowbar to the output voltage of VR. Turning on all LS_FETs can lead to very large reverse inductor current and potentially result in negative output voltage of VR. To prevent damage of the CPU by negative voltage, the RT8856 turns off all LS_FETs when V_{VSEN} has fallen below –100mV.

Under Voltage Protection (UVP)

If V_{VSEN} is less than V_{DAC} by 300mV or more, a UVP fault is latched and the RT8856 turns off both upper side and lower side MOSFETs. V_{VSEN} is monitored after UVP is valid. When V_{VSEN} falls below 200mV, a discharging resistor at VSEN will be enabled.

Negative Voltage Protection (NVP)

During shutdown or protection state, when V_{VSEN} is lower than –100mV, the controller will force LGATEx = 0 and UGATEx = 0 for preventing negative voltage. Once V_{VSEN} recovers to be more than 0mV, NVP will be suspended and LGATEx = 1 will be enabled again.

Over Temperature Protection (OTP)

Over Temperature Protection prevents the VR from damage. OTP is considered to be the final protection stage against overheating of the VR. The thermal throttling VRTT should be set to assert prior to OTP to manage the VR power. When this measure is insufficient to keep the die temperature of the controller below the OTP threshold, OTP will be asserted and latched. The die temperature of the controller is monitored internally by a temperature sensor. As a result of OTP triggering, a soft shutdown will be launched and V_{VSEN} will be monitored. When V_{VSEN} is less than 200mV, the driver remains in high impedance state and the discharging resistor at VSEN pin will be enabled. A reset can be executed by cycling VCC or VRON.

Thermal Throttling Control

Intel IMVP6.5 technology supports thermal throttling of the processor to prevent catastrophic thermal damage. The RT8856 includes a thermal monitoring circuit to detect an exceeded user defined temperature on a VR point. The thermal monitoring circuit senses the voltage change across the NTC pin. Figure 8 shows the principle of setting the temperature threshold. Connect an external resistive voltage divider between Vcc and GND. This divider uses a Negative Temperature Coefficient (NTC) thermistor and a resistor. The joint of the voltage divider is connected to the NTC pin in order to generate a voltage that is proportional to the temperature. The RT8856 pulls VRTT low if the voltage on the NTC pin is greater than 0.8 x V_{CC}. The internal VRTT comparator has a hysteresis of 100mV to prevent high frequency VRTT oscillation when the temperature is near the setting point. The minimum assertion/de-assertion time for VRTT toggling is 1.5ms.

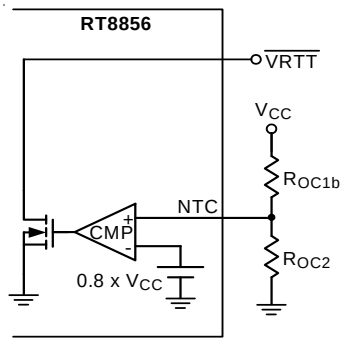

Figure 8. Thermal Throttling Setting Principle

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Users can use the same NTC thermistor for both thermal throttling and current limit setting as shown in Figure 9. Just divide the R_{OC1b} into R_{TTa} and R_{TTb}, and write the V_{NTC} equation at thermal throttling temperature TT°C :

$$R_{TTa} + R_{TTb} = R_{OC1b} \quad (26)$$

$$\frac{R_{OC2} + R_{TTb}}{R_{OC2} + R_{OC1b} + R_{OC1a} // R_{NTC,\ TT°C}} \times V_{CC} = 0.8 \times V_{CC} \quad (27)$$

Solving (26) and (27) for R_{TTa} and R_{TTb} as :

$$R_{TTb} = 4 \text{ x } (R_{OC1a} // R_{NTC,\ TT°C}) - R_{OC2} \quad (28)$$

$$R_{TTa} = R_{OC1b} - R_{TTb} \quad (29)$$

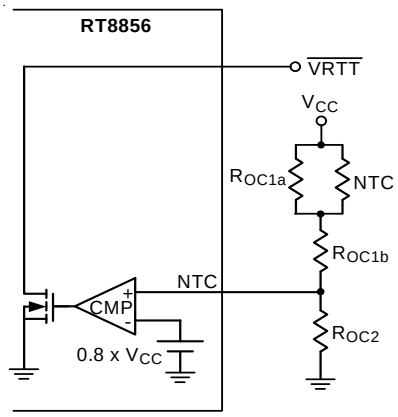

Figure 9. Using single NTC Thermistor for Thermal Throttling and Current Limit Setting

Current Monitor

The current monitor allows the system to accurately monitor the CPU's current dissipation and quickly predict whether the system is about to overheat before the significantly slower temperature sensor signals an over temperature alert. The voltage output of CM pin is proportional to the output current. This pin is connected to ground with one resistor while CMSET pin is connected to V_{VSEN} with another resistor. By choosing the appropriate ratio of these two resistors, current monitor gain can be set and V_{CM} will be 1V with maximum output current. Maximum value of V_{CM} is clamped at 1.15V.

$$V_{CM} = I_{LOAD} \times R_{DROOP} \times 2 \times \frac{R_{CM}}{R_{CMSET}} \quad (30)$$

Inductor Selection

The switching frequency and ripple current determine the inductor value as follows :

$$L_{MIN} = N \times \frac{V_{OUT(MIN)} \times (1 - D_{MIN})}{f_{SW} \times I_{Ripple}} \quad (31)$$

where N is the total number of phases. D_{MIN} is the minimum duty at highest input voltage V_{IN}.

Higher inductance yields in less ripple current and hence in higher efficiency. The flaw is the slower transient response of the power stage to load transients. This might increase the need for more output capacitors driving the cost up. Find a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The core must be large enough not to saturate at the peak inductor current.

Output Capacitor Selection

Output capacitors are used to obtain high bandwidth for the output voltage beyond the bandwidth of the converter itself. Usually, the CPU manufacturer recommends a capacitor configuration. Two different kinds of output capacitors can be found, bulk capacitors closely located to the inductors and ceramic output capacitors in close proximity to the load. The latter ones are for mid frequency decoupling with especially small ESR and ESL values while the bulk capacitors have to provide enough stored energy to overcome the low frequency bandwidth gap between the regulator and the CPU.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

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For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-40L 6x6 packages, the thermal resistance, θ_{JA}, is 34°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (34°C/W) = 2.941W for WQFN-40L 6x6 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 10 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

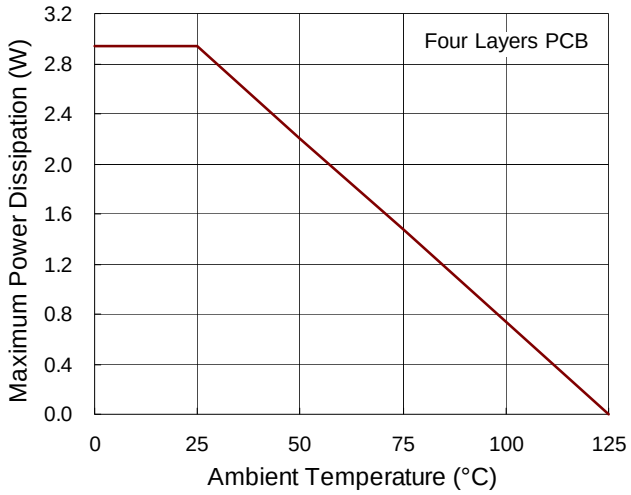

Figure 10. Derating Curve of Maximum Power Dissipation

Layout Considerations

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all of the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for optimum PC board layout :

- Keep the high current paths short, especially at the ground terminals.
- Keep the power traces and load connections short. This is essential for high efficiency.
- Connect slew rate control capacitor at SOFT pin to RGND.
- When trade offs in trace lengths must be made, it's preferable to allow the inductor charging path to be made longer than the discharging path.
- Place the current sense component close to the controller. ISENx and ISENx_N connections for current limit and voltage positioning must be made using Kelvin sense connections to guarantee the current sense accuracy. PCB trace from the sense nodes should be paralleled back to controller.
- Route high speed switching nodes away from sensitive analog areas (SOFT, COMP, FB, VSEN, ISENx, ISENx_N, CM, CMSET, etc...)

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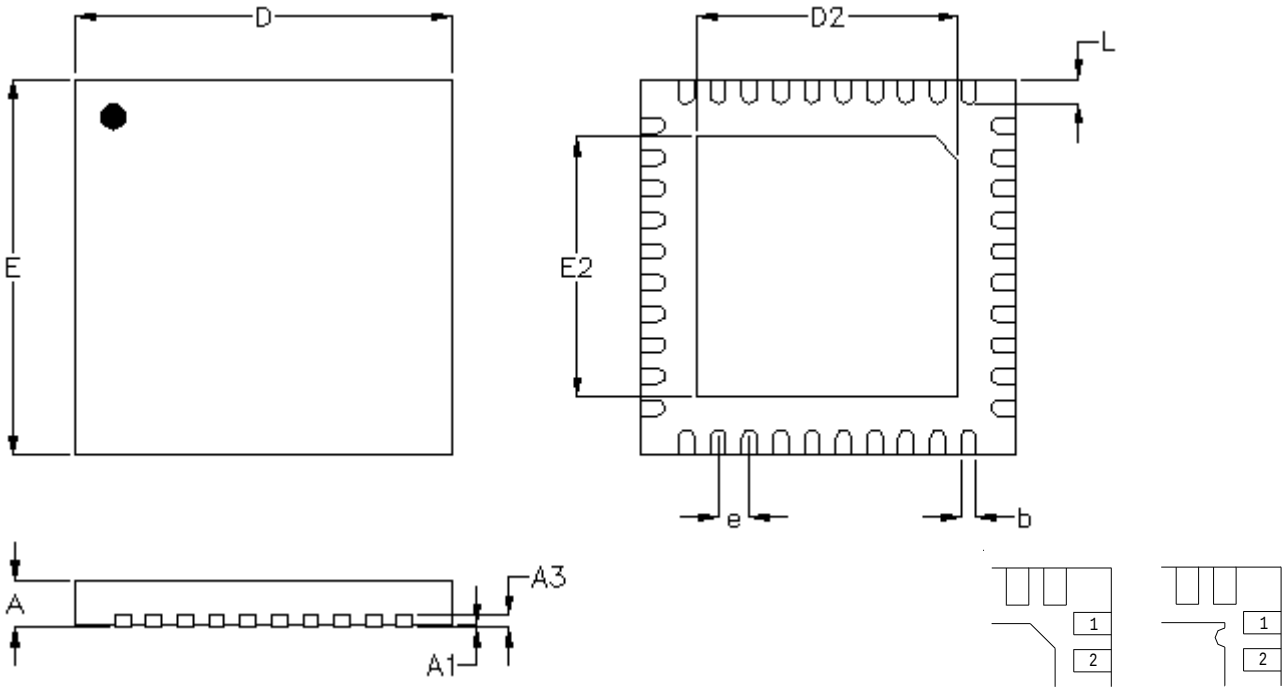
Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min.	Max.	Min.	Max.
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.180	0.300	0.007	0.012
D		5.950	6.050	0.234	0.238
D2	Option1	4.000	4.750	0.157	0.187
	Option2	3.470	3.570	0.137	0.141
E		5.950	6.050	0.234	0.238
E2	Option1	4.000	4.750	0.157	0.187
	Option2	2.570	2.670	0.101	0.105
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

W-Type 40L QFN 6x6 Package

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