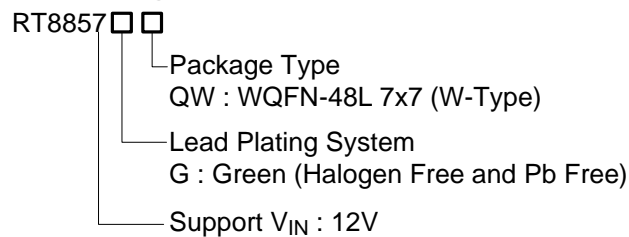


4/3/2/1-Phase PWM Controller with Embedded Drivers for CPU Core Power Supply

General Description

The RT8857 is a 4/3/2/1-phase synchronous buck controller with 2 integrated MOSFET drivers for Intel VR11.1/VR10.x and AMD K8/K8_M2 CPUs power application. The RT8857 uses differential inductor DCR current sense to achieve phase current balance and active voltage positioning. Other features include adjustable operating frequency, adjustable soft start, power good indication, external error-amp compensation, over voltage protection, over current protection, VRHOT sensing and IMON for various applications. The RT8857 comes to a small footprint with WQFN-48L 7x7 package.

Ordering Information



Note :

- V_{IN} is the input voltage of MOSFET power stage.
- Richtek products are :
 - ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
 - ▶ Suitable for use in SnPb or Pb-free soldering processes.

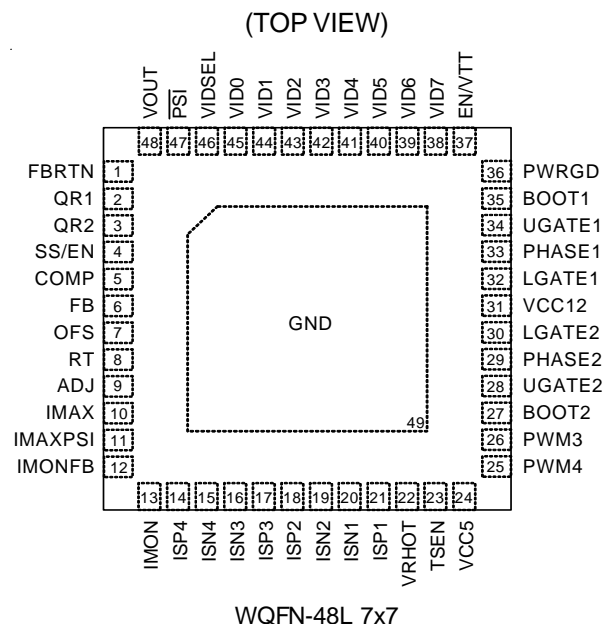
Applications

- Desktop CPU Core Power
- Low Voltage, High Current DC/DC Converter

Features

- 12V Power Supply Voltage
- 4/3/2/1-Phase Power Conversion
- 2 Embedded MOSFET Drivers
- Internal Regulated 5V Output
- VID table for INTEL VR11.1/VR10.x and AMD K8/K8_M2 CPUs
- Continuous Differential Inductor DCR Current Sense
- Adjustable Soft Start
- Adjustable Frequency
- Power Good Indication
- Adjustable Over Current Protection
- Over Voltage Protection
- VRHOT Sensing with External Thermistor
- IMON Output Current Indication
- Power State Indicator (\overline{PSI})
- Small 48-Lead WQFN Package
- RoHS Compliant and Halogen Free

Pin Configuration



Typical Application Circuit

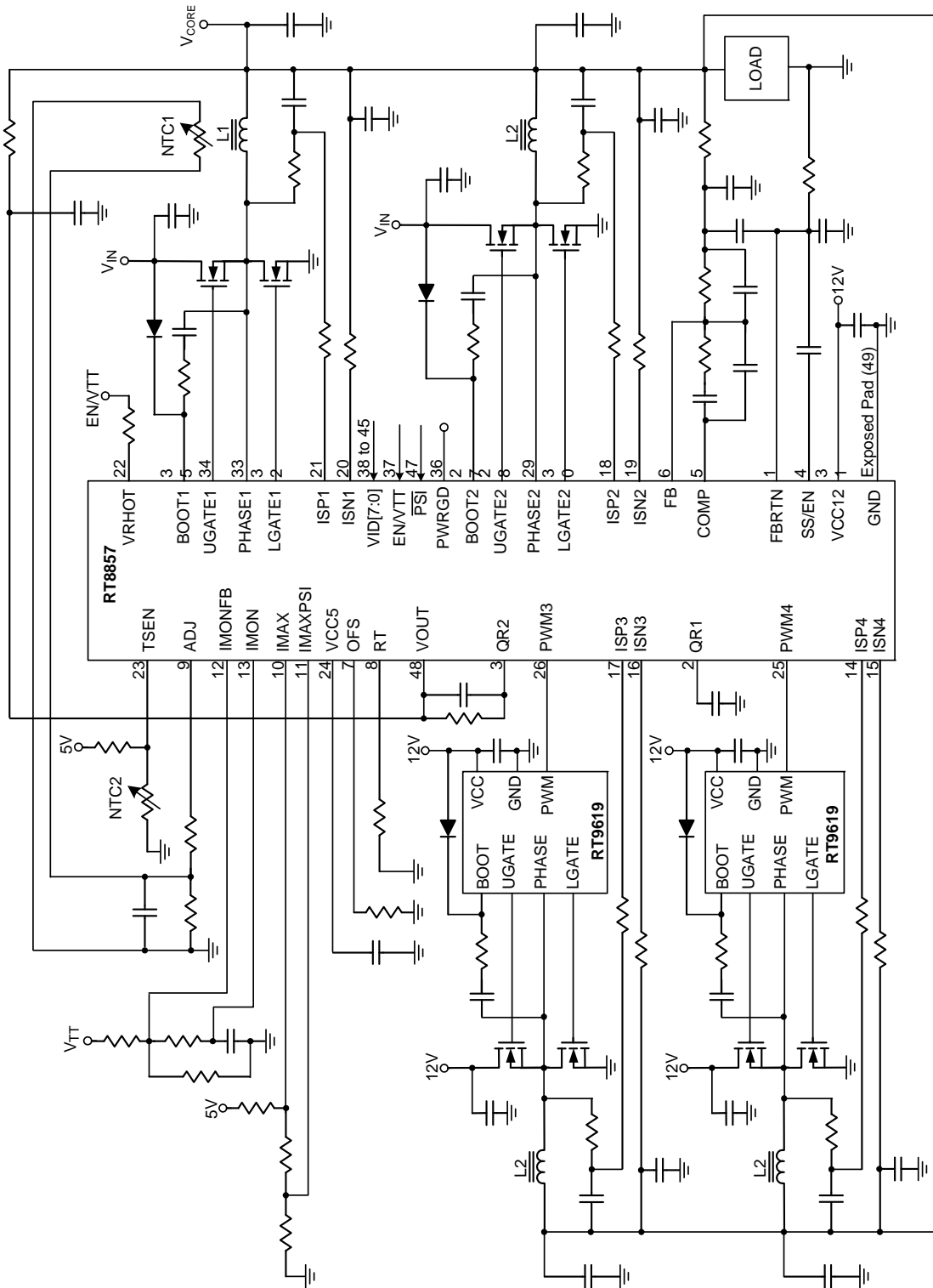


Table 1. VR11.1 VID CodeTable

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Voltage |
|------|------|------|------|------|------|------|------|---------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OFF |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | OFF |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1.60000 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1.59375 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1.58750 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1.58125 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1.57500 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1.56875 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1.56250 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1.55625 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1.55000 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1.54375 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1.53750 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1.53125 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1.52500 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1.51875 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1.51250 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1.50625 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1.50000 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1.49375 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1.48750 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1.48125 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1.47500 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1.46875 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1.46250 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1.45625 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1.45000 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1.44375 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1.43750 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1.43125 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1.42500 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1.41875 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1.41250 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1.40625 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1.40000 |

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Voltage |
|------|------|------|------|------|------|------|------|---------|
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1.39375 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1.38750 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1.38125 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1.37500 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1.36875 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1.36250 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1.35625 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1.35000 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1.34375 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1.33750 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1.33125 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1.32500 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1.31875 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1.31250 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1.30625 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1.30000 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1.29375 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1.28750 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1.28125 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1.27500 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1.26875 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1.26250 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1.25625 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1.25000 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1.24375 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1.23750 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1.23125 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1.22500 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1.21875 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1.21250 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1.20625 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1.20000 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1.19375 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1.18750 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1.18125 |

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Voltage |
|------|------|------|------|------|------|------|------|---------|
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1.17500 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1.16875 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1.16250 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1.15625 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1.15000 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1.14375 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1.13750 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1.13125 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1.12500 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1.11875 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1.11250 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1.10625 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1.10000 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1.09375 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1.08750 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1.08125 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1.07500 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1.06875 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1.06250 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1.05625 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1.05000 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1.04375 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1.03750 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1.03125 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1.02500 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1.01875 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1.01250 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1.00625 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1.00000 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0.99375 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0.98750 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0.98125 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0.97500 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0.96875 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0.96250 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0.95625 |

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Voltage |
|------|------|------|------|------|------|------|------|---------|
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0.95000 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0.94375 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0.93750 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0.93125 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0.92500 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0.91875 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0.91250 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0.90625 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0.90000 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0.89375 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0.88750 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0.88125 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0.87500 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0.86875 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0.86250 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0.85625 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0.85000 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0.84375 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0.83750 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0.83125 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0.82500 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.81875 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.81250 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.80625 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0.80000 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0.79375 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0.78750 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0.78125 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0.77500 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0.76875 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0.76250 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0.75625 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0.75000 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0.74375 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0.73750 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0.73125 |

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Voltage |
|------|------|------|------|------|------|------|------|---------|
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0.72500 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0.71875 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0.71250 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0.70625 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0.70000 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0.69375 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0.68750 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0.68125 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0.67500 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0.66875 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0.66250 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0.65625 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0.65000 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0.64375 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0.63750 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0.63125 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0.62500 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0.61875 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0.61250 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0.60625 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0.60000 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0.59375 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0.58750 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0.58125 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0.57500 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0.56875 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0.56250 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0.55625 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0.55000 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0.54375 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0.53750 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0.53125 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0.52500 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0.51875 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0.51250 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0.50625 |

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Voltage |
|------|------|------|------|------|------|------|------|---------|
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0.50000 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | OFF |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | OFF |

Table 2. Output Voltage Program (VRD10.x + VID6)

| Pin Name | | | | | | | Nominal Output Voltage DACOUT |
|----------|------|------|------|------|------|------|-------------------------------|
| VID4 | VID3 | VID2 | VID1 | VID0 | VID5 | VID6 | |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1.60000V |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1.59375V |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1.58750V |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1.58125V |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1.57500V |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1.56875V |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1.56250V |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1.55625V |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1.55000V |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1.54375V |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1.53750V |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1.53125V |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1.52500V |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1.51875V |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1.51250V |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1.50625V |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1.50000V |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1.49375V |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1.48750V |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1.48125V |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1.47500V |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1.46875V |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1.46250V |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1.45625V |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1.45000V |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1.44375V |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1.43750V |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1.43125V |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1.42500V |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1.41875V |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1.41250V |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1.40625V |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1.40000V |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1.39375V |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1.38750V |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1.38125V |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1.37500V |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1.36875V |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1.36250V |

| Pin Name | | | | | | | Nominal Output Voltage DACOUT |
|----------|------|------|------|------|------|------|-------------------------------|
| VID4 | VID3 | VID2 | VID1 | VID0 | VID5 | VID6 | |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1.35625V |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1.35000V |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1.34375V |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1.33750V |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1.33125V |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1.32500V |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1.31875V |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1.31250V |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1.30625V |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1.30000V |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1.29375V |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1.28750V |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1.28125V |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1.27500V |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1.26875V |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1.26250V |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1.25625V |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1.25000V |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1.24375V |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1.23750V |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1.23125V |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1.22500V |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1.21875V |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1.21250V |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1.20625V |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1.20000V |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1.19375V |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1.18750V |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1.18125V |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1.17500V |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1.16875V |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1.16250V |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1.15625V |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1.15000V |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1.14375V |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1.13750V |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1.13125V |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1.12500V |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1.11875V |

| Pin Name | | | | | | | Nominal Output Voltage DACOUT |
|----------|------|------|------|------|------|------|-------------------------------|
| VID4 | VID3 | VID2 | VID1 | VID0 | VID5 | VID6 | |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1.11250V |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1.10625V |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1.10000V |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1.09375V |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | OFF |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | OFF |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | OFF |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | OFF |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1.08750V |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1.08125V |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1.07500V |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1.06875V |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1.06250V |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1.05625V |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1.05000V |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1.04375V |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1.03750V |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1.03125V |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1.02500V |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1.01875V |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1.01250V |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1.00625V |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1.00000V |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0.99375V |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0.98750V |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0.98125V |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0.97500V |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0.96875V |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0.96250V |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0.95625V |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0.95000V |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0.94375V |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0.93750V |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0.93125V |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0.92500V |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0.91875V |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0.91250V |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0.90625V |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0.90000V |

| Pin Name | | | | | | | Nominal Output Voltage DACOUT |
|----------|------|------|------|------|------|------|-------------------------------|
| VID4 | VID3 | VID2 | VID1 | VID0 | VID5 | VID6 | |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0.89375V |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0.88750V |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0.88125V |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0.87500V |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0.86875V |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0.86250V |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0.85625V |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0.85000V |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0.84375V |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0.83750V |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0.83125V |

Table 3. Output Voltage Program (K8)

| VID4 | VID3 | VID2 | VID1 | VID0 | Nominal Output Voltage DACOUT |
|------|------|------|------|------|-------------------------------|
| 0 | 0 | 0 | 0 | 0 | 1.550 |
| 0 | 0 | 0 | 0 | 1 | 1.525 |
| 0 | 0 | 0 | 1 | 0 | 1.500 |
| 0 | 0 | 0 | 1 | 1 | 1.475 |
| 0 | 0 | 1 | 0 | 0 | 1.450 |
| 0 | 0 | 1 | 0 | 1 | 1.425 |
| 0 | 0 | 1 | 1 | 0 | 1.400 |
| 0 | 0 | 1 | 1 | 1 | 1.375 |
| 0 | 1 | 0 | 0 | 0 | 1.350 |
| 0 | 1 | 0 | 0 | 1 | 1.325 |
| 0 | 1 | 0 | 1 | 0 | 1.200 |
| 0 | 1 | 0 | 1 | 1 | 1.275 |
| 0 | 1 | 1 | 0 | 0 | 1.250 |
| 0 | 1 | 1 | 0 | 1 | 1.225 |
| 0 | 1 | 1 | 1 | 0 | 1.200 |
| 0 | 1 | 1 | 1 | 1 | 1.175 |
| 1 | 0 | 0 | 0 | 0 | 1.150 |
| 1 | 0 | 0 | 0 | 1 | 1.125 |
| 1 | 0 | 0 | 1 | 0 | 1.100 |
| 1 | 0 | 0 | 1 | 1 | 1.075 |
| 1 | 0 | 1 | 0 | 0 | 1.050 |
| 1 | 0 | 1 | 0 | 1 | 1.025 |
| 1 | 0 | 1 | 1 | 0 | 1.000 |
| 1 | 0 | 1 | 1 | 1 | 0.975 |
| 1 | 1 | 0 | 0 | 0 | 0.950 |
| 1 | 1 | 0 | 0 | 1 | 0.925 |
| 1 | 1 | 0 | 1 | 0 | 0.900 |
| 1 | 1 | 0 | 1 | 1 | 0.875 |
| 1 | 1 | 1 | 0 | 0 | 0.850 |
| 1 | 1 | 1 | 0 | 1 | 0.825 |
| 1 | 1 | 1 | 1 | 0 | 0.800 |
| 1 | 1 | 1 | 1 | 1 | Shutdown |

Note: (1) 0 : Connected to GND

(2) 1 : Open

Table 4. Output Voltage Program (K8_M2)

| Pin Name | | | | | | Nominal Output Voltage DACOUT |
|----------|------|------|------|------|------|-------------------------------|
| VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1.5500 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1.5250 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1.5000 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1.4750 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1.4500 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1.4250 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1.4000 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1.3750 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1.3500 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1.3250 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1.3000 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1.2750 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1.2500 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1.2250 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1.2000 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1.1750 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1.1500 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1.1250 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1.1000 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1.0750 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1.0500 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1.0250 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1.0000 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0.9750 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0.9500 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0.9250 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0.9000 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0.8750 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0.8500 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0.8250 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0.8000 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0.7750 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0.7625 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0.7500 |

| Pin Name | | | | | | Nominal Output Voltage DACOUT |
|----------|------|------|------|------|------|-------------------------------|
| VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | |
| 1 | 0 | 0 | 0 | 1 | 0 | 0.7375 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0.7250 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0.7125 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0.7000 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0.6875 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0.6750 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0.6625 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0.6500 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0.6375 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0.6250 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0.6125 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0.6000 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0.5875 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0.5750 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0.5625 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0.5500 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0.5375 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0.5250 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0.5125 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0.5000 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0.4875 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0.4750 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0.4625 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0.4500 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0.4375 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0.4250 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0.4125 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0.4000 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0.3875 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0.3750 |

Note: (1) 0 : Connected to GND

(2) 1 : Open

(3) The voltage above are load independent for desktop and server platforms. For mobile platforms the voltage above correspond to zero load current.

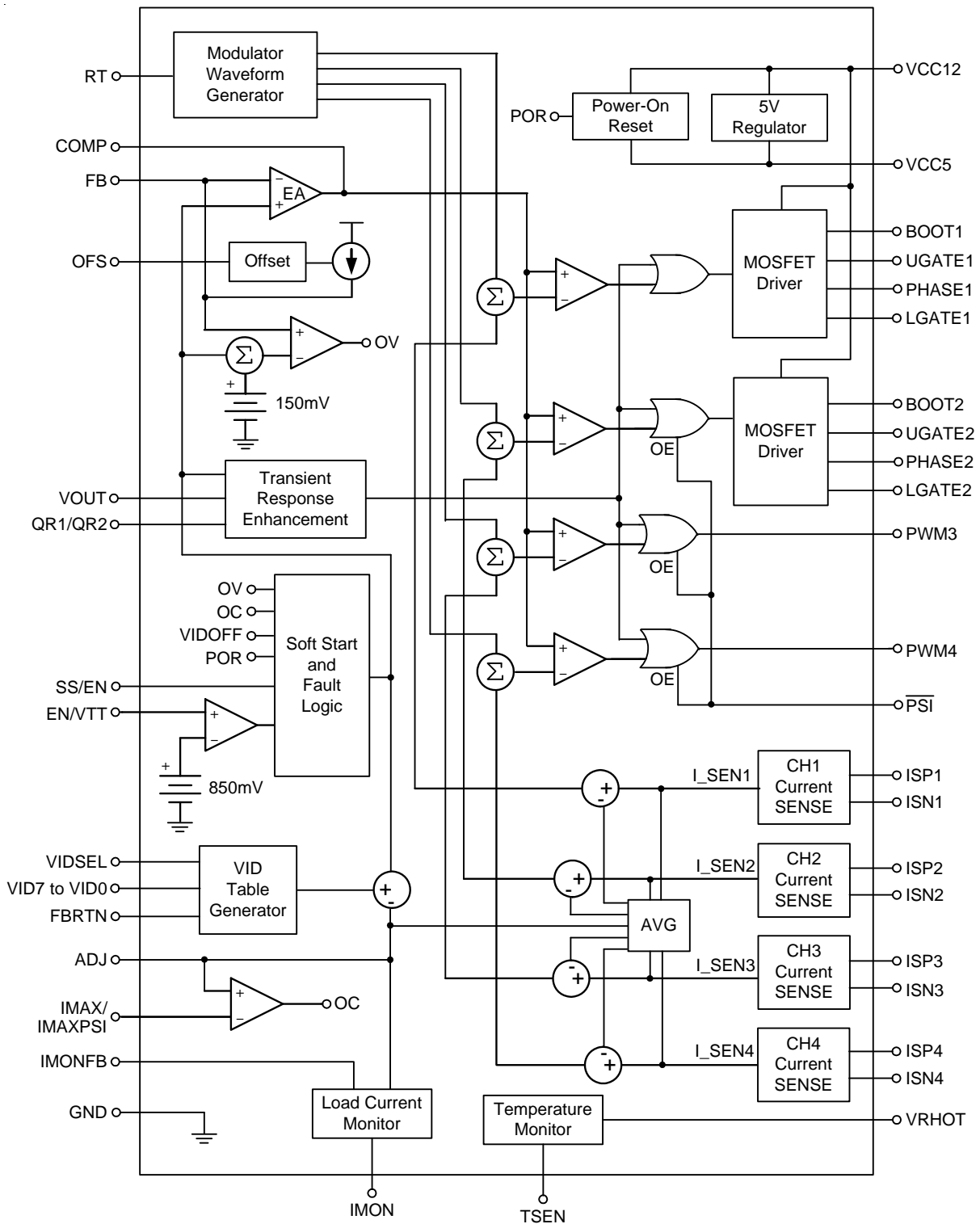
Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---------------------|-------------------------|---|
| 1 | FBRTN | Negative Remote Sense Pin of Output Voltage. |
| 2 | QR1 | Quick Response Setting Pins for Load Transition. |
| 3 | QR2 | Quick Response Setting Pins for Load Transition. |
| 4 | SS/EN | Connect this pin to GND by a capacitor to adjust soft start time. Pull this pin to GND to disable controller. |
| 5 | COMP | Output of error-amp and input of PWM comparator. |
| 6 | FB | Inverting input of error-amp. |
| 7 | OFS | Connect this pin to GND or 5V by a resistor to set no-load offset voltage. |
| 8 | RT | Connect this pin to GND by a resistor to adjust frequency. |
| 9 | ADJ | Connect this pin to GND by a resistor to set load line. |
| 10 | IMAX | Negative input of OCP comparator. (Positive input of OCP comparator is ADJ). |
| 11 | IMAXPSI | OCP Setting in Power Saving Mode. |
| 12 | IMONFB | Current Monitor Gain/Offset Adjustment. |
| 13 | IMON | Current Monitor Output. |
| 14, 17, 18, 21 | ISP4, ISP3, ISP2, ISP1 | Positive current sense pin of channel 1, 2, 3 and 4. |
| 15, 16, 19, 20 | ISN4, ISN3, ISN2, ISN1 | Negative current sense pin of channel 1, 2, 3 and 4. |
| 22 | VRHOT | Temperature Monitor Output. |
| 23 | TSEN | Temperature Sense Input. |
| 24 | VCC5 | 5V LDO Output for System Power Supply. |
| 25, 26 | PWM4, PWM3 | PWM Output for Channel 4 and Channel 3. |
| 27, 35 | BOOT2, BOOT1 | Bootstrap Supply for Channel 2 and Channel 1. |
| 28, 34 | UGATE2, UGATE1 | Upper Gate Driver for Channel 2 and Channel 1. |
| 29, 33 | PHASE2, PHASE1 | Switching Node of Channel 2 and Channel 1. |
| 30, 32 | LGATE2, LGATE1 | Lower Gate Driver for Channel 2 and Channel 1. |
| 31 | VCC12 | IC Power Supply. Connect to 12V. |
| 36 | PWRGD | Power Good Indicator. |
| 37 | EN/VTT | VTT Voltage Detector Input. |
| 38 to 45 | VID7 to VID0 | Voltage Identification Input for DAC. |
| 47 | $\overline{\text{PSI}}$ | Power Status Indicator II. |
| 48 | VOUT | Feedback of Regulated Output. |
| 46 | VIDSEL | VID DAC Selection Pin. |
| 49 (Exposed pad) | GND | The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. |

VID Table Selection

| VIDSEL | VID [7] | Table |
|--------|---------|--------|
| VTT | X | VR11 |
| GND | X | VR10.x |
| VCC5 | VTT | K8 |
| VCC5 | GND | K8_M2 |

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ----- -0.3V to 15V
- BOOTx to PHASEx ----- -0.3V to 15V
- BOOTx to GND
 - DC ----- -0.3V to 30V
 - < 200ns ----- -0.3V to 42V
- PHASEx to GND
 - DC ----- -2V to 15V
 - < 200ns ----- -5V to 30V
- Input/Output Voltage ----- -0.3V to (VCC5 + 0.3)V
- Power Dissipation, P_D @ T_A = 25°C
 - WQFN-48L 7x7 ----- 3.226W
- Package Thermal Resistance (Note 2)
 - WQFN-48L 7x7, θ_{JA} ----- 31°C/W
- Junction Temperature ----- 150°C
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- ESD Susceptibility (Note 3)
 - HBM (Human Body Mode) ----- 2kV
 - MM (Machine Mode) ----- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, VCC12 ----- 12V ± 10%
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- 0°C to 70°C

Electrical Characteristics

(VCC12 = 12V, V_{GND} = 0V, T_A = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|-----------------------------|----------------------|-----------------------------------|------|----------------------------|------|------|
| VCC12 Supply Input | | | | | | |
| VCC12 Supply Voltage | VCC12 | | 10.8 | 12 | 13.2 | V |
| VCC12 Supply Current | I _{CC} | | -- | 6 | -- | mA |
| VCC5 Power | | | | | | |
| VCC5 Supply Voltage | VCC5 | I _{LOAD} = 10mA (Note 5) | 4.75 | 5.0 | 5.25 | V |
| VCC5 Output Sourcing | I _{VCC5} | | 10 | -- | -- | mA |
| Power-On Reset | | | | | | |
| VCC12 Rising Threshold | V _{VCC12TH} | VCC12 rising | 9.2 | 9.6 | 10.0 | V |
| VCC12 Hysteresis | V _{VCC12HY} | VCC12 falling | -- | 0.9 | -- | V |
| Load Current Monitor | | | | | | |
| IMON Maximum Output Voltage | | | -- | V _T (Note 6) | -- | V |
| EN/VTT | | | | | | |
| EN/VTT Rising Threshold | V _{ENVTT} | EN/VTT rising | 0.80 | 0.85 | 0.90 | V |
| Enable Hysteresis | V _{ENVTTHY} | EN/VTT falling | -- | 100 | -- | mV |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|-----------------------------------|----------------------|---|------|-----|------|------|
| Reference Voltage accuracy | | | | | | |
| DAC Accuracy | | 1V to 1.6V | -0.5 | -- | +0.5 | % |
| | | 0.8V to 1V | -5 | -- | +5 | mV |
| | | 0.5V to 0.8V | -8 | -- | +8 | mV |
| Error Amplifier | | | | | | |
| DC Gain | ADC | No load | -- | 80 | -- | dB |
| Gain-Bandwidth | GBW | C _{LOAD} = 10pF | -- | 10 | -- | MHz |
| Slew Rate | SR | C _{LOAD} = 10pF | 10 | -- | -- | V/us |
| Output voltage range | V _{COMP} | | 0.5 | | 3.6 | V |
| Max Current | IEA_SLEW | Slew | 300 | -- | -- | uA |
| Power Sequence | | | | | | |
| PWRGD Low Voltage | V _{PGOOD} | I _{PWRGD} = 4mA | -- | -- | 0.4 | V |
| Soft-Start Delay | T _{D1} | | -- | 2 | -- | ms |
| V _{BOOT} Duration | T _{D3} | | -- | 0.8 | -- | ms |
| PWRGD Delay | T _{D5} | Measured the time form V _{BOOT} change to PWRGD = 1 | -- | 1.6 | -- | ms |
| Current Sense Amplifier | | | | | | |
| Max Current | I _{GMMAX} | V _{CSP} = 1.3V Sink current from CSN | 100 | -- | -- | uA |
| Input Offset Voltage | V _{OCS} | | -2 | 0 | +2 | mV |
| Running Frequency | f _{OSC} | R _{RT} = 40kΩ | 270 | 300 | 330 | kHz |
| RT Pin Voltage | V _{RT} | R _{RT} = 40kΩ | 0.76 | 0.8 | 0.84 | V |
| Ramp Slope | V _{RAMP} | R _{RT} = 40kΩ | -- | 22 | -- | %/V |
| Soft Start | | | | | | |
| Soft Start Current | I _{SS1} | Slew | 12 | 16 | 20 | uA |
| VID Change Current | I _{SS2} | Slew | 120 | 160 | 200 | uA |
| Gate Driver | | | | | | |
| UGATE Drive Source | R _{UGATEsr} | BOOT – PHASE = 8V 250mA source current | -- | 1 | -- | Ω |
| UGATE Drive Sink | R _{UGATEsk} | BOOT – PHASE = 8V 250mA sink current | -- | 1 | -- | Ω |
| LGATE Drive Source | R _{LGATEsr} | V _{LGATE} = 8V | -- | 1 | -- | Ω |
| LGATE Drive Sink | R _{LGATEsk} | 250mA sink current | -- | 0.8 | -- | Ω |
| Protection | | | | | | |
| Over-Voltage Threshold | V _{OVP} | Sweep FB Voltage, V _{FB} – V _{EAP} | 125 | 150 | 175 | mV |
| Over-Current Threshold | V _{OCP} | Sweep I _{MAX} Voltage, V _{I_{MAX}} – V _{ADJ} | -10 | 0 | +10 | mV |
| Dynamic Characteristic | | | | | | |
| UGATE Rise Time | t _{rUGATE} | C _{iss} = 3000p | -- | 15 | -- | ns |
| UGATE Fall Time | t _{fUGATE} | | -- | 10 | -- | ns |
| LGATE Rise Time | t _{rLGATE} | | -- | 15 | -- | ns |
| LGATE Fall Time | t _{fLGATE} | | -- | 10 | -- | ns |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|--|-------------------|------------------------------------|-----|-----------------------------|-----|------|
| Input Threshold | | | | | | |
| VID7 to VID0, VIDSEL Rising Threshold | VID7 to 0, VIDSEL | VID7 to VID0 rising, VIDSEL rising | -- | 1/2V _{TT} + 12.5mV | -- | V |
| VID7 to VID0 Hysteresis | VID7 to 0_Hy | VID7 to VID0 falling | -- | 25 | -- | mV |
| $\overline{\text{PSI}}$ Rising Threshold | V _{PSI} | $\overline{\text{PSI}}$ rising | -- | 1/2V _{TT} + 12.5mV | -- | V |

Note 1. Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a effective single layer thermal conductivity test board of JEDEC thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Test condition : The RT8857 normal operating, an extra static DC current load 10mA applying at VCC5 pin.

Note 6. The maximum output voltage of power monitor will be restricted by EN/VTT pin input voltage.

Application Information

The RT8857 is a 4/3/2/1-phase synchronous buck DC/DC converter with 2 embedded MOSFET drivers. The internal VID DAC is designed to interface with the Intel VR11.x/10.x and AMD K8/K8_M2 compatible CPUs.

Power Ready Detection

During start-up, the RT8857 will detect VCC12, VCC5 and VTT. When VCC12 > 9.6V, VCC5 > 4.6V and VTT > 0.85V, POR will go high. POR (Power On Reset) is the internal signal to indicate all powers are ready to let the RT8857 and the companioned MOSFET drivers work properly. When POR = L, the RT8857 will try to turn off both high side and low side MOSFETs.

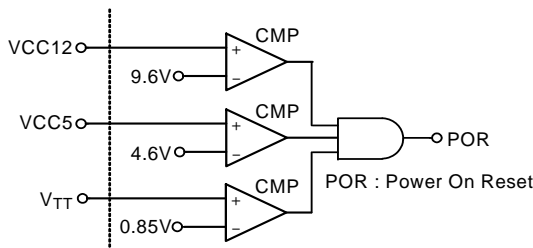


Figure 1. Circuit for Power Ready Detection

Phase Detection

The number of operational phases is determined by the internal circuitry that monitors the ISNn voltages during start up. Normally, the RT8857 operates as a 4-phase PWM controller. Pull ISN4 and ISP4 to VCC5 programs 3-phase operation, pull ISN3 and ISP3 to VCC5 programs 2-phase operation, and pull ISN2 and ISP2 to VCC5 programs 1-phase operation. The RT8857 detects the voltage of ISN4, ISN3 and ISN2 at POR rising edge. At the rising edge, the RT8857 detects whether the voltage of ISN4, ISN3 and ISN2 are higher than “VCC5 – 1V” respectively to decide how many phases should be active. Phase detection is only active during start up. When POR = H, the number of operational phases is determined and latched. The unused PWM pins can be connected to 5V or GND or left floating.

Phase Switching Frequency

The phase switching frequency of the RT8857 is set by an external resistor connected from the RT pin to GND. The frequency follows the graph in Figure 2.

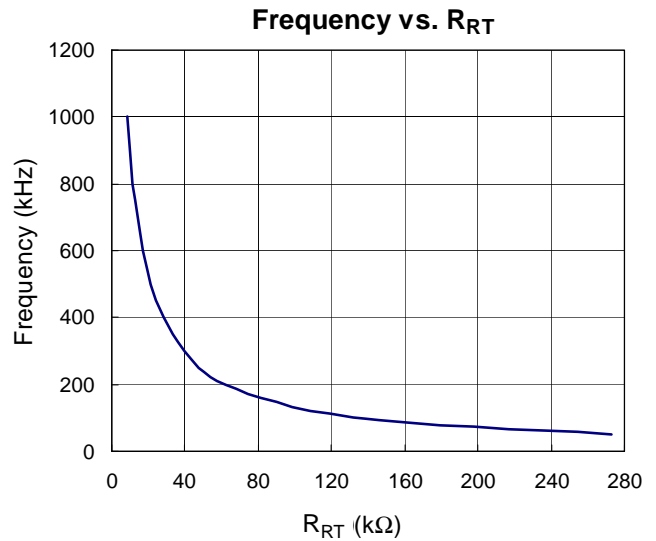


Figure 2. R_{RT} vs Phase Switching Frequency

Soft Start

Output current of OPSS (I_{SS}) is limited and variant

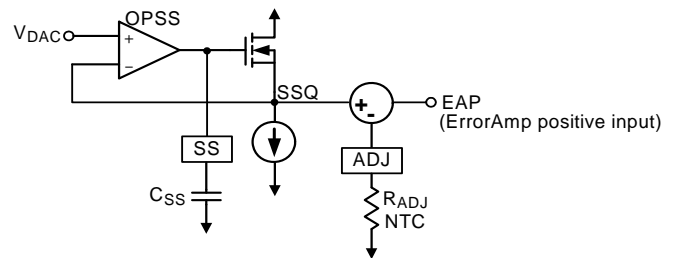


Figure 4. Circuit for Soft Start and Dynamic VID

The V_{OUT} start-up time is set by a capacitor from the SS pin to GND. In power_on_reset state (POR = L), the SS pin is held at GND. After power_on_reset stae (POR = H) and an extra delay 1600us, V_{SS} and V_{SSQ} begin to rise till V_{SSQ} = V_{BOOT}. When V_{SSQ} = V_{BOOT}, the RT8857 stays in this state for 800us waiting for valid VID code sent by CPU. After receiving valid VID code, V_{OUT} continues ramping up or down to the voltage specified by VID code. Before PWRGD = H, output current of OPSS (I_{SS}) is limited to 80uA (I_{SS1}). When PWRGD = H, I_{SS} is limited to 80uA (I_{SS2}). The soft start waveform is shown in Figure 5.

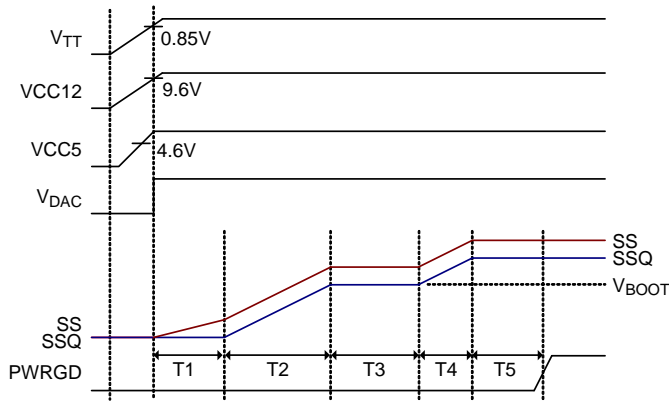


Figure 5. Soft Start Waveforms

V_{OUT} will trace V_{EAP} which is equal to " $V_{SSQ} - V_{ADJ}$ ". V_{ADJ} is a small voltage signal which is proportional to I_{OUT} . This voltage is used to generate loadline and will be described later. T1 is the delay time from power_on_reset state to the beginning of V_{OUT} rising.

$$T1 = 1600\mu s + 0.6V \times C_{SS} / I_{SS1} \quad (1)$$

T2 is the soft start time from $V_{OUT} = 0$ to $V_{OUT} = V_{BOOT}$.

$$T2 = V_{BOOT} \times C_{SS} / I_{SS1} \quad (2)$$

T3 is the dwelling time for $V_{OUT} = V_{BOOT}$. T3 = 800us.

T4 is the soft start time from $V_{OUT} = V_{BOOT}$ to $V_{OUT} = V_{DAC}$.

$$T4 \sim |V_{DAC} - V_{BOOT}| \times C_{SS} / I_{SS1} \quad (3)$$

T5 is the power good delay time, T5 \sim 1600us.

Dynamic VID

The RT8857 can accept VID input changing while the controller is running. This allows the output voltage (V_{OUT}) to change while the DC/DC converter is running and supplying current to the load. This is commonly referred to as VID on-the-fly (OTF). A VID OTF can occur under either light or heavy load conditions. The CPU changes the VID inputs in multiple steps from the start code to the finish code. This change can be positive or negative. Theoretically, V_{OUT} should follow V_{DAC} which is a staircase waveform. In the RT8857, as mentioned in soft start session, V_{DAC} slew rate is limited by I_{SS2}/C_{SS} when $PWRGD = H$. This slew rate limiter works as a low pass filter of V_{DAC} and makes the bandwidth of V_{DAC} waveform finite. By smoothing V_{DAC} staircase waveform, V_{OUT} will no longer overshoot or undershoot. On the other hand, C_{SS} will increase the settling time of V_{OUT} during VID OTF. In most cases, 1nF to 30nF ceramic capacitor is suitable

Output Voltage Differential Sensing

The RT8857 uses differential sensing by a high gain low offset ErrorAmp. The CPU voltage is sensed between the FB and FBRTN pins. A resistor (R_{FB}) connects FB pin and the positive remote sense pin of the CPU (V_{CCP}). FBRTN pin connects to the negative remote sense pin of CPU (V_{CCN}) directly. The ErrorAmp compares $EAP (= V_{DAC} - V_{ADJ})$ with the V_{FB} to regulate the output voltage.

No-Load Offset

In Figure 6, I_{OFSN} or I_{OFSP} are used to generate no-load offset. Either I_{OFSN} or I_{OFSP} is active during normal operation. It should be noted that users can only enable one polarity of no-load offset. Do not connect OFS pin to GND and to V_{CC5} at the same time. Connect a resistor from OFS pin to GND to activate I_{OFSN} . I_{OFSN} flows through R_{ADJ} from ADJ pin to GND. In this case, negative no-load offset voltage (V_{OFSN}) is generated.

$$V_{OFSN} = I_{OFSN} \times R_{ADJ} = 0.8 \times R_{ADJ} / R_{OFS} \quad (4)$$

Connect a resistor from OFS pin to V_{CC5} to activate I_{OFSP} . I_{OFSP} flows through R_{FB} from the V_{CCP} to FB pin. In this case, positive no-load offset voltage (V_{OFSP}) is generated.

When positive no-load offset is selected, the RT8857 will generate another internal 8uA current source to eliminate dead zone problem of droop function. This 8uA current will be injected into ADJ resistors, producing a small initial negative no-load offset. Therefore, when OFS pin is connected to V_{CC5} through a resistor, the positive no-load offset can be calculated as :

$$\begin{aligned} V_{OFSP} &= I_{OFSP} \times R_{FB} - 8\mu A \times R_{ADJ} \\ &= 6.4 \times \frac{R_{FB}}{R_{OFS}} - 8\mu A \times R_{ADJ} \end{aligned} \quad (5)$$

The RT8857 provides wide range no-load positive offset for over-clocking applications. The I_{OFSP} capability can supply from 30uA to 640uA, which means in Equation (5), R_{OFS} can range from 240kΩ to 10kΩ. Other resistances of R_{OFS} exceeding this range can also provide no-load positive offset but cannot be guaranteed by Equation (5).

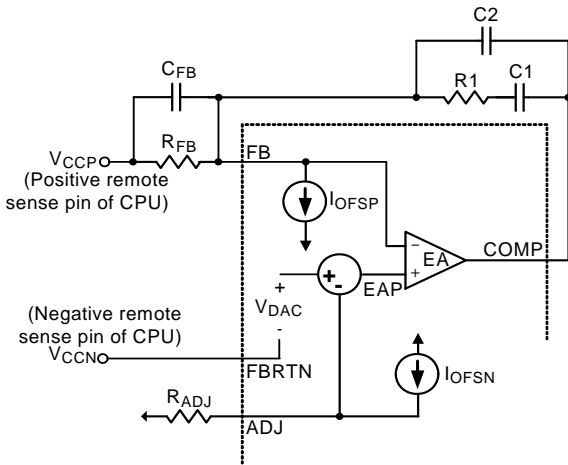


Figure 6. Circuit for V_{OUT} Differential Sensing and No Load Offset

Load Transient Quick Response

The RT8857 utilizes a new quick response feature to supply heavy load current demand during instantaneous load application transient. The RT8857 detects load transient and reacts via V_{OUT} pin. When V_{OUT} drops during load application transient, the quick response comparator will send asserted signals to turn on high side MOSFETs and turn off low side MOSFETs. The LA1 signal, which is a weaker quick response signal, will turn on only arbitrary two channels', high side MOSFETs while turning off low side MOSFETs also. The LA2 signal, which is a stronger quick response signal, will turn on all channel's high side MOSFETs while turning off low side MOSFETs also. Therefore, the influence of total quick response function of the RT8857 is adjustable, and the magnitude of quick response is flexible via fine-tuning the resistors connected to pin QR1 and QR2.

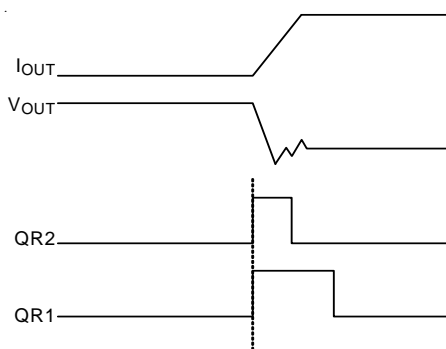


Figure 7

Output Current Sensing

The RT8857 provides low input offset current-sense amplifier (CSA) to monitor the output current of every channel. Output current of CSA (I_{X[n]}) is used for channel current balance and active voltage position. In this inductor current sensing topology, R_S and C_S must be set according to the equation below :

$$L/DCR = R_S \times C_S \tag{6}$$

Then the output current of CSA will follow the equation below :

$$I_X = [I_L \times DCR - V_{OFS-CSA} + 235n \times (R_{CSP} - R_{CSN})] / R_{CSN} \tag{7}$$

235nA is typical value of CSA input offset current. V_{OFS-CSA} is the input offset voltage of CSA. V_{OFS-CSA} of the RT8857 is smaller than +/- 1mV. Usually, "V_{OFS-CSA} + 235n x (R_{CSP} - R_{CSN})" is negligible except at very light load and the equation can be simplified as the equation below :

$$I_X = I_L \times DCR / R_{CSN} \tag{8}$$

Loadline

Output current of CSA is summed and averaged in RT8857. Then 0.5Σ(I_{X[n]}) is sent to ADJ pin. Because ΣI_{X[n]} is a PTC (Positive Temperature Coefficient) current, an NTC (Negative Temperature Coefficient) resistor is needed to connect ADJ pin to GND. If the NTC resistor is properly selected to compensate the temperature coefficient of I_{X[n]}, the voltage on ADJ pin will be proportional to I_{OUT} without temperature effect. In the RT8857, the positive input of ErrorAmp is "V_{DAC} - V_{ADJ}". V_{OUT} will follow "V_{DAC} - V_{ADJ}", too. Thus, the output voltage decreasing linearly with I_{OUT} is obtained. The loadline is defined as

$$LL(\text{loadline}) = \Delta V_{OUT} / \Delta I_{OUT} = \Delta V_{ADJ} / \Delta I_{OUT} = 0.5 \times DCR \times R_{ADJ} / R_{CSN} \tag{9}$$

Briefly, the resistance of R_{ADJ} sets the resistance of loadline. The temperature coefficient of R_{ADJ} compensates the temperature effect of loadline.

Current Balance

In Figure 8, $I_{X[n]}$ is the current signal which is proportional to current flowing through channel n. In Figure 9, the current error signals $I_{ERRn} (= I_{X[n]} - \text{AVG}(I_{X[n]}))$ are used to raise or lower the internal sawtooth waveforms (RAMP[1] to RAMP[n]) which are compared with ErrorAmp output (COMP) to generate PWM signal. The raised sawtooth waveform will decrease the PWM duty of the corresponding channel while the lowered will increase. Eventually, current flowing through each channel will be balanced.

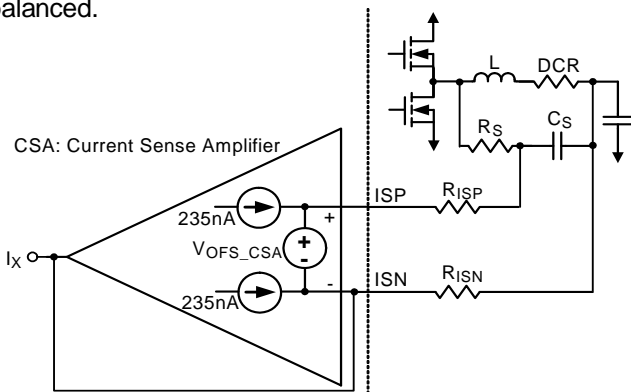


Figure 8. Circuit for Channel Current Sensing

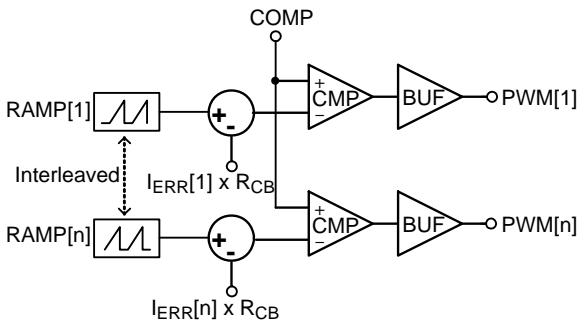


Figure 9. Circuit for Channel Current Balance

Channel Current Adjust

If channel current is not balanced due to asymmetric PCB layout of power stage, external resistors can be adjusted to correct current imbalance. Figure 10 shows two types of current imbalance, constant ratio type and constant difference type.

If the initial current distribution is constant ratio type, according to Equation (8), reduce $R_{CSN}[1]$ can reduce $I_L[1]$ and improve current balance. If the initial current distribution is constant difference type, according to Equation (7), increase $R_{CSP}[1]$ can reduce $I_L[1]$ and improve current balance.

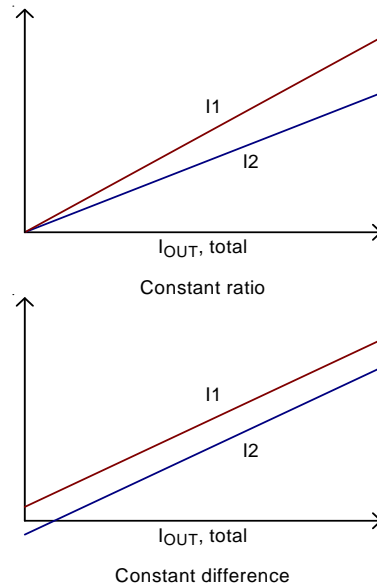


Figure 10. Channel Current vs. Total Current

Over Current Protection (OCP)

The RT8857 provides single phase OCP and multi-phase OCP according to the operation condition. In Figure 11, single phase OCP (IMAXPSI) and multi-phase OCP (IMAX) thresholds can be set by external resistors :

$$V_{IMAX} = V_{CC5} \times \frac{R2 + R3}{R1 + R2 + R3} \tag{10}$$

$$V_{IMAXPSI} = V_{CC5} \times \frac{R3}{R1 + R2 + R3} \tag{11}$$

Once V_{ADJ} is larger than the negative input of CP comparator, OCP will be triggered and latched, and the RT8857 will turn off both high side and low side MOSFETs of all channels. A 20us delay after OCP detection is used to prevent false trigger.

Over Voltage Protection (OVP)

The over voltage protection monitors the output voltage via the FB pin. Once V_{FB} exceeds " $V_{EAP} + 150mV$ ", OVP is triggered and latched. The RT8857 will try to turn on low side MOSFET and turn off high side MOSFET to protect CPU. A 20us delay is used in OVP detection circuit to prevent false trigger.

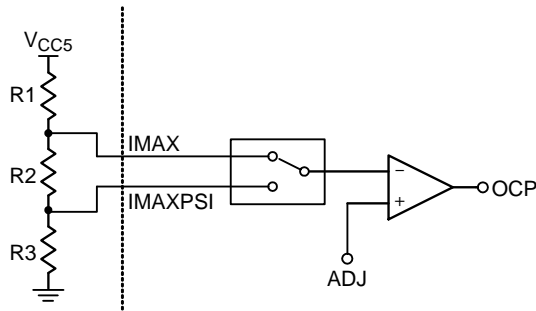


Figure 11. Over Current Protection

Output Current Monitoring (IMON)

The RT8857 senses load current and output a voltage signal to indicated the instantaneous load current status. Since the sensed total current is injected into the resistors connected to ADJ pin, ADJ voltage than is used for IMON function as shown in Figure 12. Through the resistor network R1, R2 and R3, IMON voltage will be proportional to ADJ pin voltage according to the Equation :

$$V_{IMON} = \frac{R3}{R1 // R2 // R3} \times V_{ADJ} - \frac{R3}{R1} \times V_{TT} \quad (12)$$

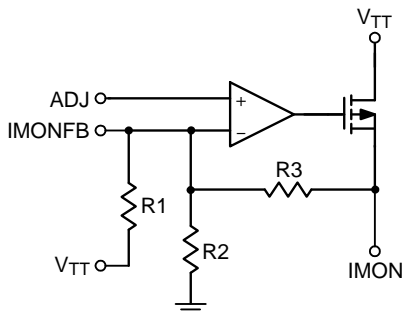


Figure 12. Output Current Monitoring

Thermal Monitoring (VRHOT)

The RT8857 provides thermal monitoring function via sensing TSEN pin voltage. Through the voltage divider R1 and R_{NTC}, the voltage of TSEN is typically set to be higher than 0.33 x V_{CC5} when ambient temperature is lower than VRHOT assertion target. When ambient temperature rises, TSEN voltage will fall, and VRHOT signal will be set to high if TSEN voltage drops below 0.28 x V_{CC5}. Accordingly, VRHOT will be reset to low once TSEN voltage rises above 0.33 x V_{CC5}. Correctly choose the resistance of R1 and R_{NTC} can assert and de-assert VRHOT accurately at target ambient temperature.

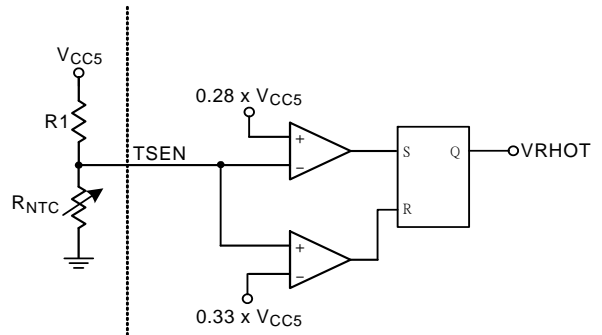


Figure 13. Thermal Monitoring

Power State Indicator (\overline{PSI})

The RT8857 supports PSI# function for VR11.1 CPUs and platform users. The RT8857 will monitor PSI pin input voltage to change the operating state. When PSI is high (higher than 1/2 V_{TT} + 12.5mV), the RT8857 operates as a full-channel interleaving PWM controller and all channels are active. When input voltage is low (lower than V_{TT} + 12.5mV), the RT8857 will change to single phase operation mode and only channel 1 is active. Since channel 2 includes embedded driver, the RT8857 will automatically disable channel 2 by forcing UGATE2 and LGATE2 into high impedance state when input voltage is low. The RT8857 will also disable channel 3 and channel 4 by sending continuous tri-state signals (~2.5V) from PWM3 and PWM4 to external drivers when input voltage is low. Therefore, 2 external drivers which support tri-state shutdown should be used if \overline{PSI} function is considered, and the RT9619 is recommended to be the external drivers for VR11.1 compatibility.

During \overline{PSI} asserted period, e.g., input voltage is low, if the RT8857 receives dynamic VID change command, the RT8857 will enter interleaving mode operation and all channels will be activated. \overline{PSI} command will be ignored during dynamic VID operation, and \overline{PSI} will be blanked for about 100us after dynamic VID change is completed.

Loop Compensation

The RT8857 is a synchronous Buck converter with two control loops : voltage loop and current balance loop. Since the function of the current balance loop is to maintain the current balance between each active channel, its influence to converter stability will be negligible compared with the voltage feedback loop. Therefore, to compensate the

voltage loop will be the main task to maintain converter stability.

The converter duty-to-output transfer function G_d is :

$$G_d = \frac{V_{OUT}}{D} \frac{1}{1 + \frac{S}{R\sqrt{\frac{L}{C}}} + \frac{S^2}{\left(\frac{1}{\sqrt{LC}}\right)^2}} \quad (13)$$

and the modulator gain of the converter is :

$$F_m = \frac{1}{V_P} \quad (14)$$

Where V_{OUT} is the output voltage of the converter, R is the loading resistance, L and C are the output inductance and capacitance, and V_P is the peak-to-peak voltage of ramp applied at modulator input. The overall loop gain after compensation can be described as :

$$\text{Loop Gain} = T = G_d \times F_m \times A \quad (15)$$

Where A denotes as compensation gain. To compensate a typical voltage mode buck converter, there are two ordinary compensation schemes, well known as type-II compensator and type-III compensator. The choice of using type-II or type-III compensator will be up to platform designers, and the main concern will be the position of the capacitor ESR zero and mid-frequency to high-frequency gain boost. Typically, the ESR zero of output capacitor will tend to stabilize the effect of output LC double poles, hence the position of the output capacitor ESR zero in frequency domain may influence the design of voltage loop compensation. If $F_{Z_{ESR}}$ is $< 1/2F_{CO}$ where F_{CO} denotes cross-over frequency, type-II compensation will be sufficient for voltage stability. If $F_{Z_{ESR}}$ is $> 1/2F_{CO}$ (or higher gain and phase margin is required at mid-frequency to high-frequency), then type-III compensation may be a better solution for voltage loop compensation.

A typical type-II compensation network is shown in Figure 14.

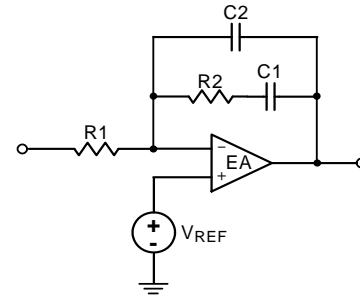


Figure 14. Type-II Compensation

$R1$ can be determined independently from DC considerations. Normally choose $R1$ that the current passing by will be around 1mA. Therefore,

$$R1 = \frac{V_{REF}}{1\text{mA}} \quad (16)$$

Then determine $R2$ by the boosted gain of loop gain at crossover :

$$R2 = R1 \times \frac{V_P}{V_{IN(MAX)}} \times \left(\frac{F_{Z_{ESR}}}{F_{LC}} \right)^2 \times \frac{F_{CO}}{F_{Z_{ESR}}} \quad (17)$$

Where $V_{IN(MAX)}$ is the max input voltage of power stage, V_P is the peak-to-peak voltage of ramp applied at modulator input, $F_{Z_{ESR}}$ is the frequency of output capacitor ESR zero, and F_{LC} is the frequency of output LC :

$$F_{Z_{ESR}} = \frac{1}{2\pi \times R_{ESR} \times C} \quad (18)$$

$$F_{LC} = \frac{1}{2\pi \times \sqrt{LC}} \quad (19)$$

After determining the phase margin at crossover frequency, the position of zero and pole produced by type-II compensation network, F_Z and F_P , can then be determined. The bode plot of type-II compensation is shown in Figure15, where

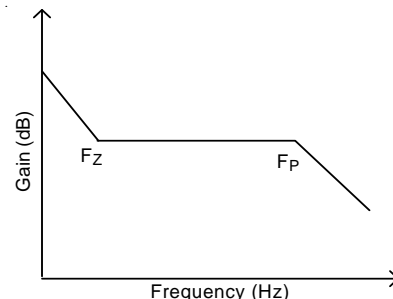


Figure 15. Bode Plot of Type-II Compensation

$$F_Z = \frac{1}{2\pi \times R2 \times C1} \tag{20}$$

$$F_P = \frac{1}{2\pi \times R2 \times (C1 \parallel C2)} \tag{21}$$

F_Z can be determined by the following Equation :

$$\tan^{-1}\left(\frac{F_{CO}}{F_Z}\right) - \tan^{-1}\left(\frac{F_Z}{F_{CO}}\right) \geq 90^\circ + P.M. - \tan^{-1}\left(\frac{F_{CO}}{F_{ZERO, ESR}}\right) \tag{22}$$

By properly choosing F_Z to fit equation (22), C₁ can then be determined by :

$$C1 = \frac{1}{2\pi \times R2 \times F_Z} \tag{23}$$

and C₂ can be determined by :

$$C2 = \frac{1}{2\pi \times R2 \times \left(\frac{F_{CO}^2}{F_Z} - \frac{1}{C1}\right)} \tag{24}$$

A typical type-III compensation contains two zeros and two poles where the extra one zero and one pole compared with type-II compensation are added for stabilizing the system when ESR zero is relatively far from LC double poles in frequency domain. Figure16. and Figure.17 shows the typical circuit and bode plot of the type-III compensation.

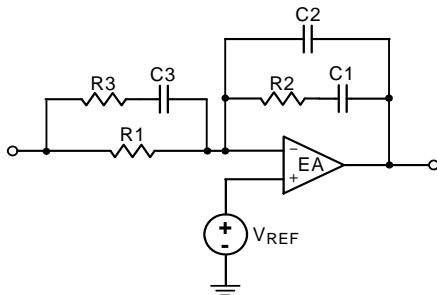


Figure 16. Type-III Compensation

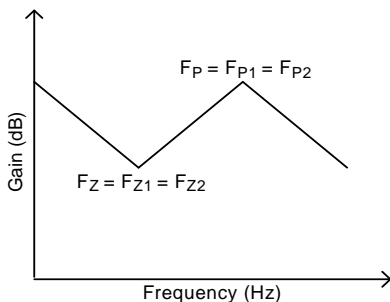


Figure 17. Bode Plot of the Type-III Compensation

After determining desired phase margin, according to the following Equation :

$$\tan^{-1}\left(\frac{F_{CO}}{F_Z}\right) - \tan^{-1}\left(\frac{F_Z}{F_{CO}}\right) \geq \frac{P.M.}{2} + 45^\circ \tag{25}$$

and

$$F_P = \frac{F_{CO}^2}{F_Z} \tag{26}$$

F_Z and F_P can be determined by choosing proper F_{CO} to F_Z ratio to meet Equation (25). Again, R₁ can be determined by the Equation (16).

R₂ can be determined by the following Equation :

$$R2 = R1 \times \frac{V_P}{V_{IN(MAX)}} \times \left(\frac{F_{CO}}{F_{LC}}\right)^2 \times \frac{F_Z}{F_{CO}} \tag{27}$$

Other component values of the Type-III compensation can then be calculated as :

$$C1 = \frac{1}{2\pi \times R2 \times F_Z} \tag{28}$$

$$C2 = \frac{1}{2\pi \times R2 \times F_P - \frac{1}{C1}} \tag{29}$$

$$C3 = \frac{1}{2\pi \times R1 \times F_Z} \tag{30}$$

$$R3 = \frac{1}{2\pi \times C3 \times F_P} \tag{31}$$

Layout Considerations

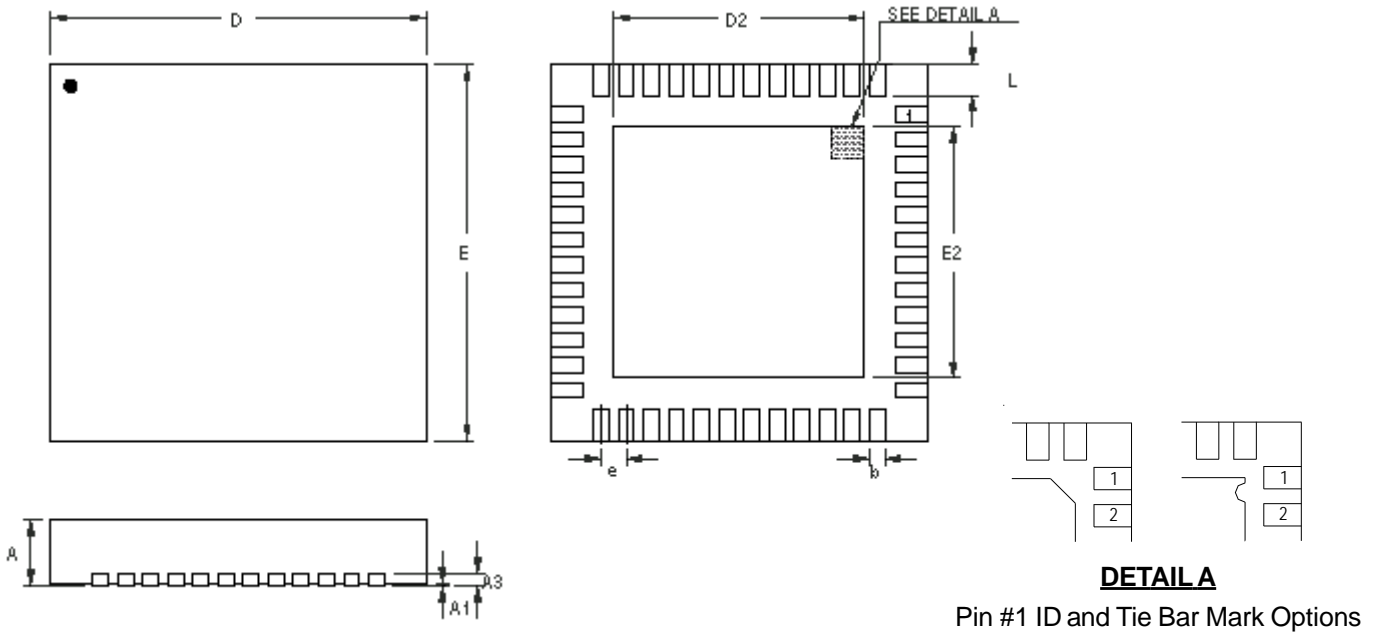
For best performance of the RT8857, the following guidelines must be strictly followed :

- ▶ Input bulk capacitors and MLCCS have to be put near high side MOSFETs. The connection plane of input capacitors and high side MOSFETs then can be kept as square as possible.
- ▶ The shape of phase planes (the connection plane between high side MOSFETs, low side MOSFETs and output inductors) have to be as square as possible. Long traces, thin bars or separated islands must be avoided in phase planes.
- ▶ Keep snubber circuits or damping elements near its objects. Phase RC snubbers have to be close to low side MOSFETs, UGATE damping resistors have to be close to high side MOSFETs, and boot to phase damping resistors have to be close to high side MOSFETs and phase planes. Also keep the traces of these snubbers circuits as short as possible.

- ▶ The area of V_{IN} plane (power stage 12V V_{IN}) and V_{OUT} plane (output bulk capacitors and inductors connection plane) have to be as wide as possible. Long traces or thin bars must be avoided in these planes. The plane trace width must be wide enough to carry large input/output current (40mil/A).
- ▶ The following traces have to be wide and short : UGATE, LGATE, BOOT, PHASE, and VCC12. Make sure the width of these traces are wide enough to carry large driving current(at least 40mil).
- ▶ The voltage feedback loop contains two traces, VCC and VSS, which are Kelvin sensed from CPU socket or output capacitors. These two traces are suggested above 10mil width and put away from high (di/dt) switching elements such as high side MOSFETs, low side MOSFETs, phase plane etc. The circuit elements of voltage feedback loop, such as feedback loop short resistors and voltage loop compensation RCs, have to be kept near the RT8857 and also away from switching elements.
- ▶ The current sense mechanism of the RT8857 is fully differential Kelvin sense. Therefore, the current sense loops of the RT8857 contain two traces : the positive traces(ISP1 to ISP4) come from the positive node of output inductors(the node connecting phase plane) and the negative traces (ISN1 to ISN4) come from the negative node of output inductors(the node connecting output plane).

DO NOT connect the current sense traces from phase plane or output plane. Only connect these traces from both sides of output inductors can achieve the goal of precise Kelvin sense. The current sense feedback loops have to be routed away from switching elements, and the current sense RC elements have to be put near their respective ISN or ISP pins of the RT8857 and also away from noise switching elements. At least 10 mil width is suggested for current sense feedback loops.

Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.200 | 0.300 | 0.008 | 0.012 |
| D | 6.950 | 7.050 | 0.274 | 0.278 |
| D2 | 5.050 | 5.250 | 0.199 | 0.207 |
| E | 6.950 | 7.050 | 0.274 | 0.278 |
| E2 | 5.050 | 5.250 | 0.199 | 0.207 |
| e | 0.500 | | 0.020 | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |

W-Type 48L QFN 7x7 Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City
 Hsinchu, Taiwan, R.O.C.
 Tel: (8863)5526789

Richtek products are sold by description only. Customers should obtain the latest relevant information and data sheets before placing orders and should verify that such information is current and complete. Richtek cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Richtek product. Information furnished by Richtek is believed to be accurate and reliable. However, no responsibility is assumed by Richtek or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Richtek or its subsidiaries.