500mA, Low Dropout, Low Noise Ultra-Fast Without Bypass Capacitor CMOS LDO Regulator

General Description

The RT9013C is a high-performance, 500mA LDO regulator, offering extremely high PSRR and ultra-low dropout. Ideal for portable RF and wireless applications with demanding performance and space requirements.

The RT9013C quiescent current as low as 25μA, further prolonging the battery life. The RT9013C also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices.

The RT9013C consumes typical 0.7μA in shutdown mode and has fast turn-on time less than 40μs. The other features include ultra-low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. Available in WDFN-6L 2x2 package.

Ordering Information

RT9013C-□□□

- Package Type
  QW : WDFN-6L 2x2 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- Fixed Output Voltage
  33 : 3.3V

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

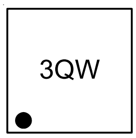
Features

- **Wide Operating Voltage Ranges : 2.2V to 5.5V**
- **Low Dropout : 250mV at 500mA**
- **Ultra-Low-Noise for RF Application**
- **Ultra-Fast Response in Line/Load Transient**
- **Current Limiting Protection**
- **Thermal Shutdown Protection**
- **High Power Supply Rejection Ratio**
- **Output Only 1μF Capacitor Required for Stability**
- **TTL-Logic-Controlled Shutdown Input**

Applications

- CDMA/GSM Cellular Handsets
- Portable Information Appliances
- Laptop, Palmtops, Notebook Computers
- Hand-Held Instruments
- Mini PCI & PCI-Express Cards
- PCMCIA & New Cards

Marking Information

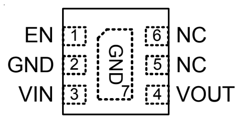


3Q : Product Code

W : Date Code

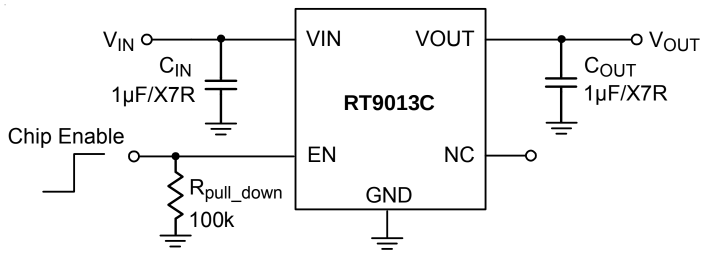
Pin Configurations

(TOP VIEW)



WDFN-6L 2x2

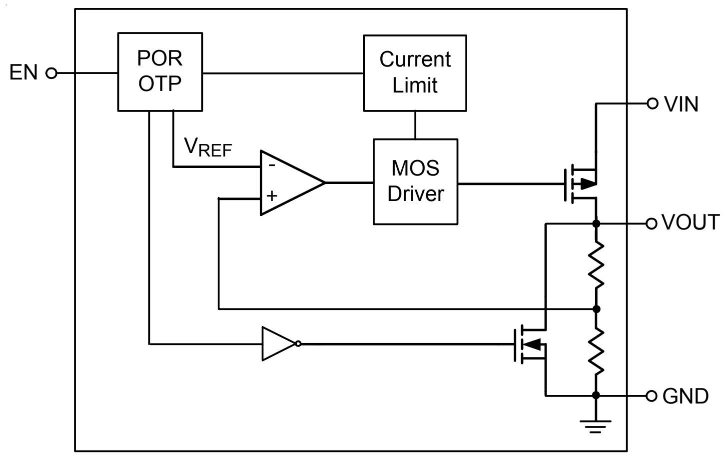
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Enable Input Logic, Active High. When the EN goes to a logic low, the device will be shutdown mode.
2, 7 (Exposed Pad)	GND	Common Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
3	VIN	Supply Input.
4	VOUT	Regulator Output.
5, 6	NC	No Internal Connection.

Function Block Diagram



Operation

Basic Operation

The RT9013C is a low quiescent current linear regulator designed especially for low external components system. The input range is from 2.2V to 5.5V

Output transistor

The RT9013C builds in a P-MOSFET output transistor which provides a low switch-on resistance for low dropout voltage applications.

Error Amplifier

The Error Amplifier compares the internal reference voltage with the output feedback voltage from the internal divider, and controls the Gate voltage of P-MOSFET to support good line regulation and load regulation at output voltage.

Enable

The RT9013C delivers the output power whenit is set to enable state. When it works in disable state, there is no output power and the operation quiescent current is almost zero.

Current Limit Protection

The RT9013C provides current limit function to prevent the device from damages during over-load or shorted circuit condition. This current is detected by an internal sensing transistor.

Over Temperature Protection

The over temperature protection function will turn off the P-MOSFET when the junction temperature exceeds 160°C (typ.), V_{IN} > 2.2V and the output current exceed 50mA. Once the junction temperature cools down by approximately 30°C, the regulator will automatically resume operation.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- 6V
- EN Input Voltage ---------- 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-6L 2x2 ---------- 0.606W
- Package Thermal Resistance (Note 2)
  WDFN-6L 2x2, θ_{JA} ---------- 165°C/W
  WDFN-6L 2x2, θ_{JC} ---------- 20°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.2V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = V_{OUT} + 0.5V, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 1μF (Ceramic, X7R), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.2	--	5.5	V
Output Noise Voltage	V_{ON}	V_{OUT} = 1.5V, C_{OUT} = 1μF, I_{OUT} = 0mA	--	30	--	μV_{RMS}
Output Voltage Accuracy (Fixed Output Voltage)	ΔV_{OUT}	I_{OUT} = 10mA	–2	0	+2	%
Quiescent Current (Note 5)	I_Q	V_{EN} = 5V, I_{OUT} = 0mA	--	25	50	μA
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	0.7	1.5	μA
Current Limit	I_{LIM}	R_{LOAD} = 0Ω, 2.2V ≤ V_{IN} < 2.6V	0.4	0.5	0.85	A
		R_{LOAD} = 0Ω, 2.7V ≤ V_{IN} ≤ 5.5V	0.5	0.6	0.85	A
Dropout Voltage (Note 6)	V_{DROP}	I_{OUT} = 400mA, 2.2V ≤ V_{IN} < 2.7V	--	160	320	mV
		I_{OUT} = 500mA, 2.7V ≤ V_{IN} ≤ 5.5V	--	250	400	
Load Regulation (Note 7) (Fixed Output Voltage)	ΔV_{LOAD}	1mA < I_{OUT} < 400mA 2.2V ≤ V_{IN} < 2.7V	--	--	0.6	%
		1mA < I_{OUT} < 500mA 2.7V ≤ V_{IN} ≤ 5.5V	--	--	1	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
EN Threshold Voltage	Logic-Low	V_{IL}		0	--	0.6	V
	Logic-High	V_{IH}		1.2	--	5.5	
Enable Pin Current		I_{EN}		--	0.1	1	μA
Power Supply Rejection Rate		PSRR	I_{OUT} = 100mA, f = 10kHz	--	–50	--	dB
Line Regulation		ΔV_{LINE}	V_{IN} = (V_{OUT}+0.5) to 5.5V, I_{OUT} = 1mA	--	0.01	0.2	%/V
Thermal Shutdown Temperature		T_{SD}		--	170	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	30	--	

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a low effective thermal conductivity single-layer test board per JEDEC 51-3. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Quiescent, or ground current, is the difference between input and output currents. It is defined by $I_Q = I_{IN} - I_{OUT}$ under no load condition (I_{OUT} = 0mA). The total current drawn from the supply is the sum of the load current plus the ground pin current.

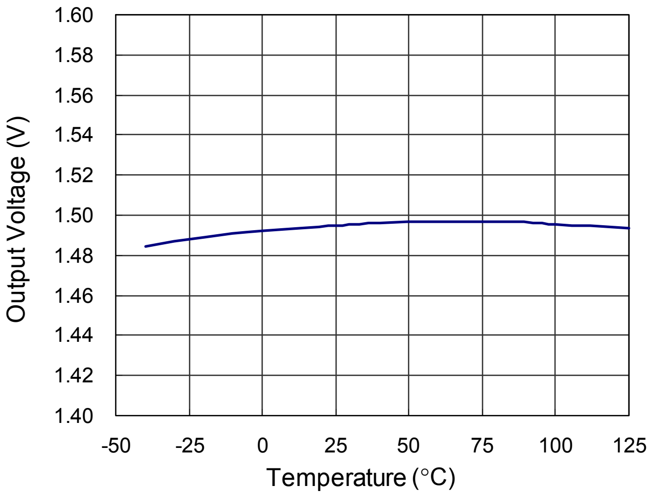
Note 6. The dropout voltage is defined as V_{IN} -V_{OUT}, which is measured when V_{OUT} is $V_{OUT(NORMAL)}$ - 100mV.

Note 7. Regulation is measured at constant junction temperature by using a 2ms current pulse. Devices are tested for load regulation in the load range from 10mA to 500mA.

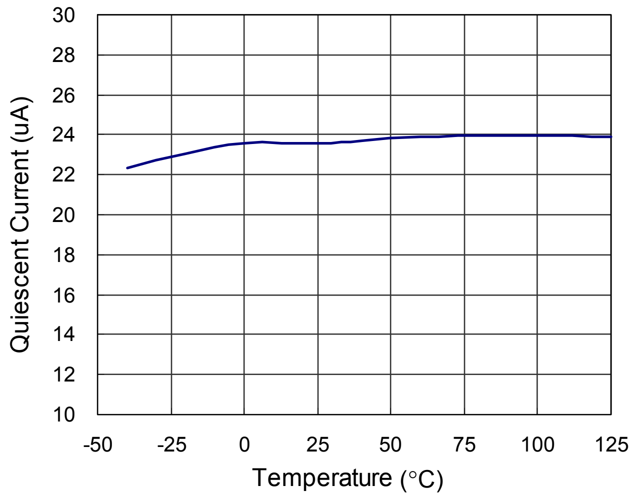
Typical Operating Characteristics

(C_{IN} = C_{OUT} = 1µ/X7R, unless otherwise specified)

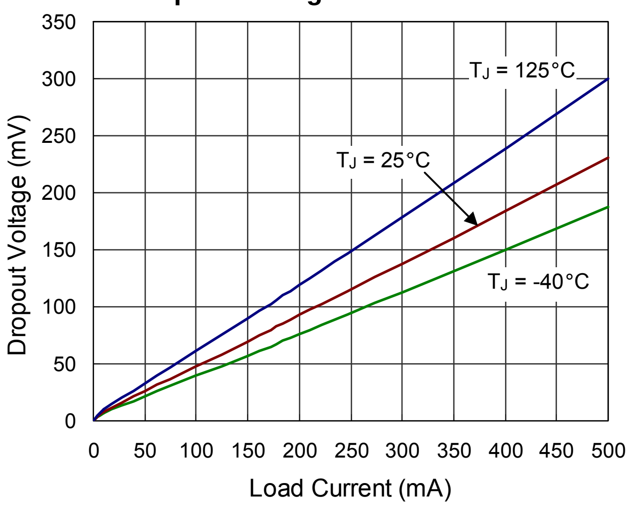
Output Voltage vs. Temperature



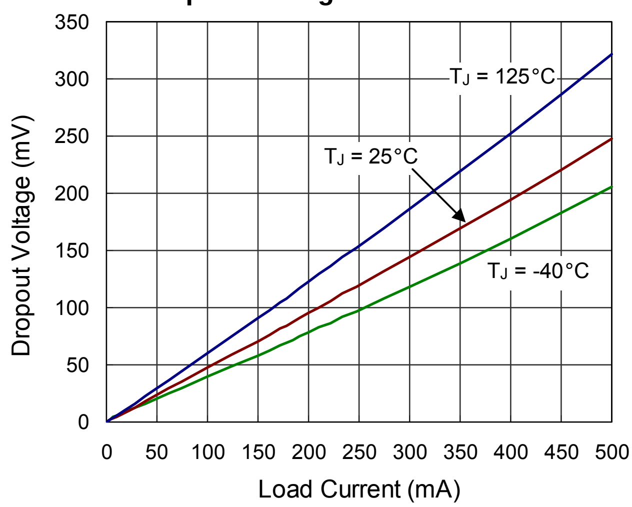
Quiescent Current vs. Temperature



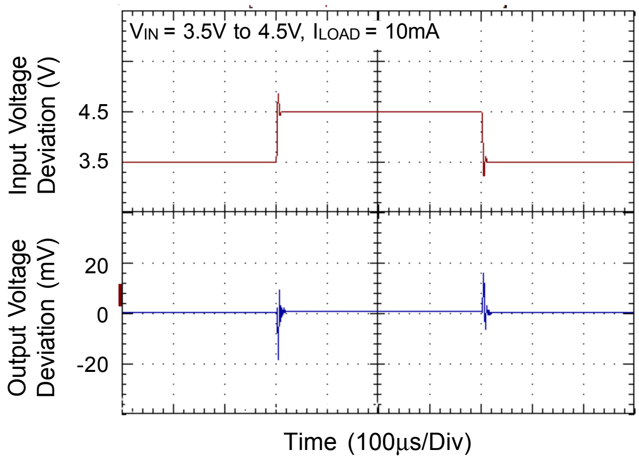
Dropout Voltage vs. Load Current



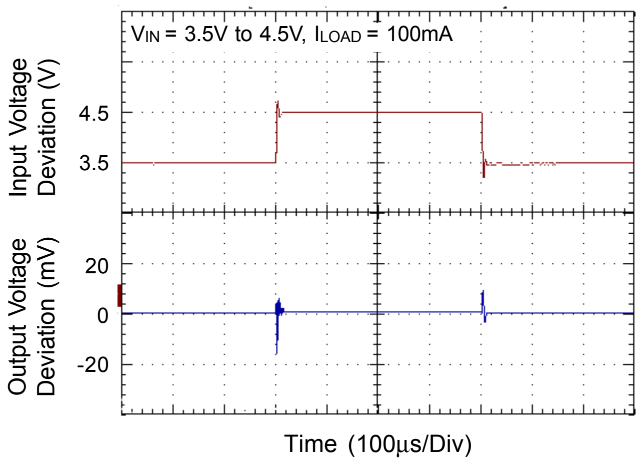
Dropout Voltage vs. Load Current



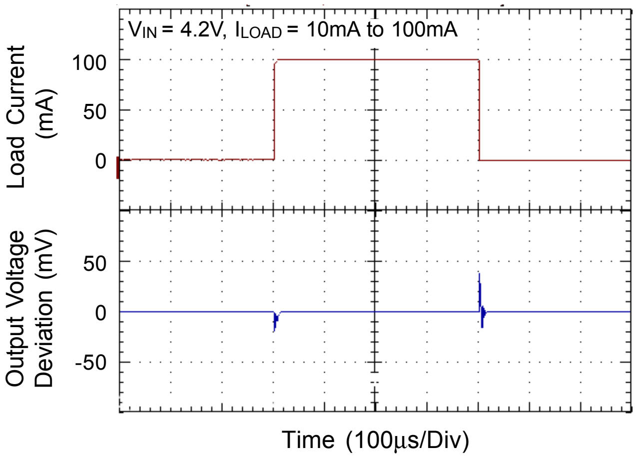
Line Transient Response



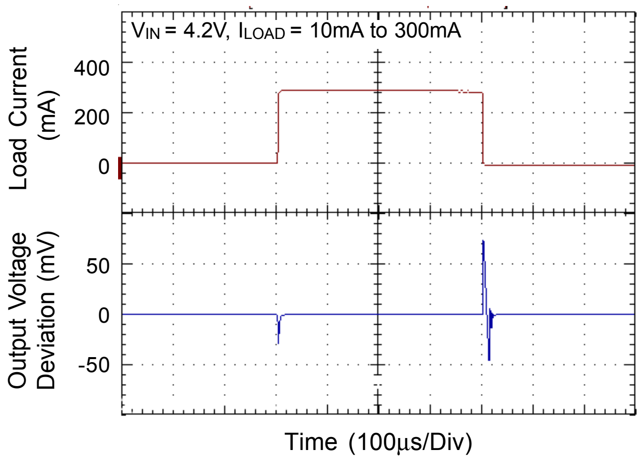
Line Transient Response



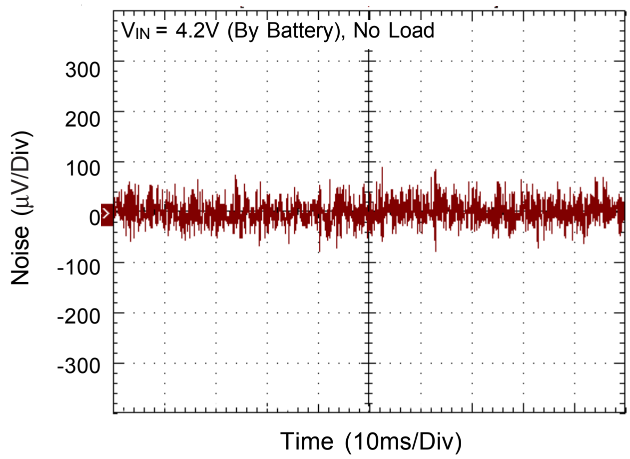
Load Transient Response



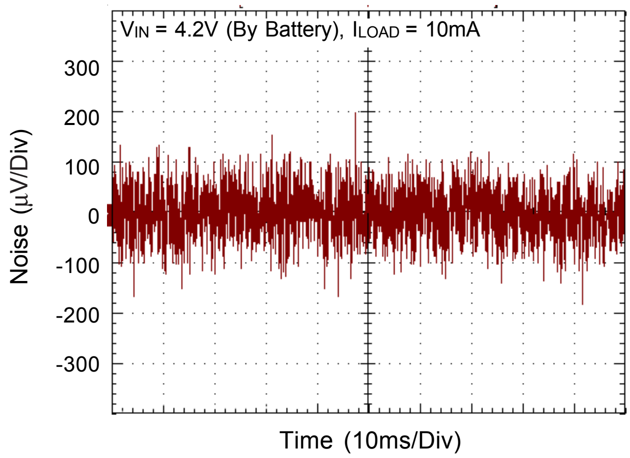
Load Transient Response



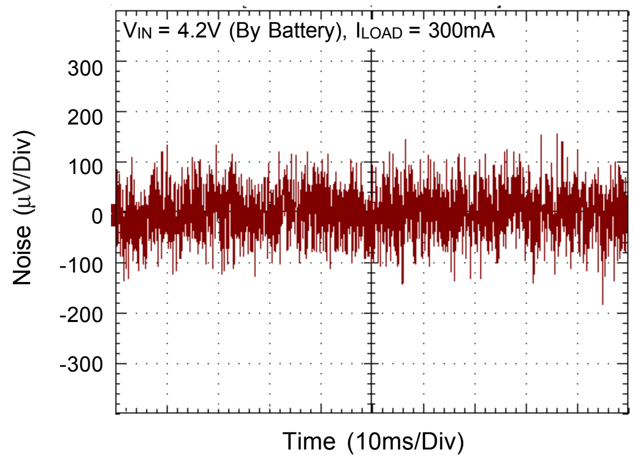
Noise



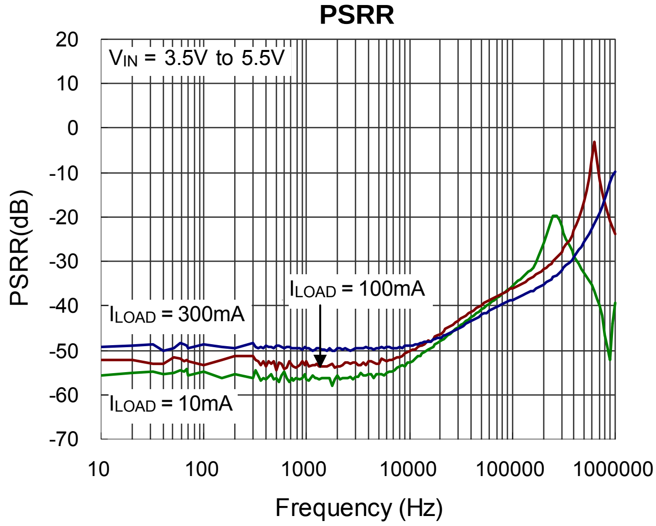
Noise



Noise



PSRR



Applications Information

Like any low-dropout regulator, the external capacitors used with the RT9013C must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 1μF/X7R on the RT9013C input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The RT9013C is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 5mΩ on the RT9013C output ensures stability. The RT9013C still works well with output capacitor of other types due to the wide stable ESR range. Figure 1. shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the RT9013C and returned to a clean analog ground.

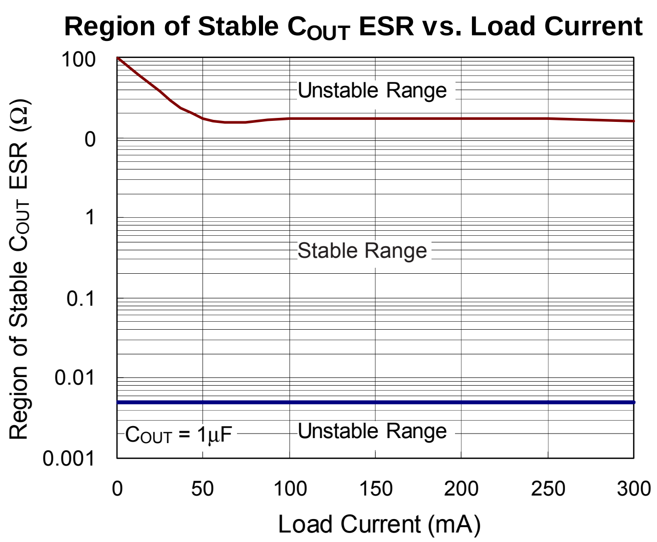


Figure 1

Enable

The RT9013C goes into sleep mode when the EN pin is in a logic low condition. During this condition, the RT9013C has an EN pin to turn on or turn off regulator, When the EN pin is logic hight, the regulator will be turned on. The supply current to 0.7μA typical. The EN pin may be directly tied to V_{IN} to keep the part on. The Enable input is CMOS logic and cannot be left floating.

PSRR

The power supply rejection ratio (PSRR) is defined as the gain from the input to output divided by the gain from the supply to the output. The PSRR is found to be

$$\text{PSRR} = 20 \times \log\left(\frac{\Delta\text{Gain Error}}{\Delta\text{Supply}}\right)$$

Note that when heavy load measuring, Δsupply will cause Δtemperature. And Δtemperature will cause Δoutput voltage. So the heavy load PSRR measuring is include temperature effect.

Current limit

The RT9013C contains an independent current limiter, which monitors and controls the pass transistor's gate voltage, limiting the output current to 0.6A (typ.). The output can be shorted to ground indefinitely without damaging the part.

Thermal Considerations

Thermal protection limits power dissipation in RT9013C. When the operation junction temperature exceeds 170°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turn on again after the junction temperature cools by 30°C.

For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-6L 2x2 package, the thermal resistance, θ_{JA}, is 165°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (165°C/W) = 0.606W for WDFN-6L 2x2 packages

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

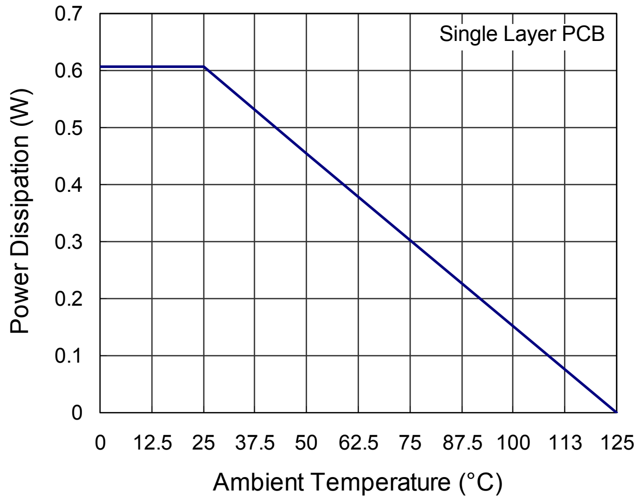
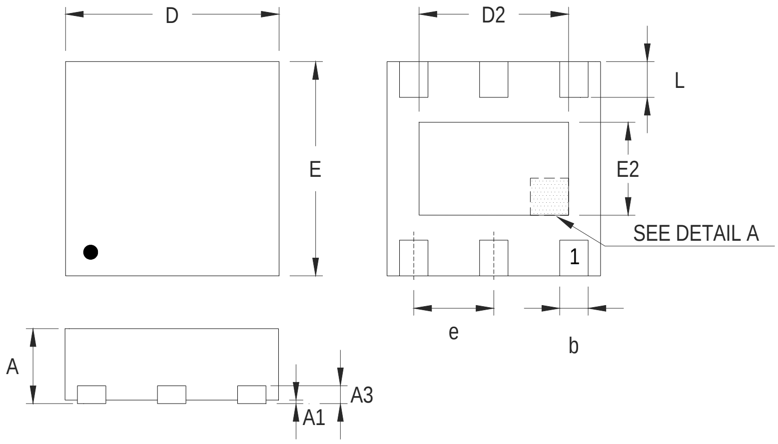
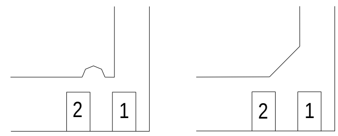


Figure 2. Derating Curve of Maximum Power Dissipation

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.350	0.008	0.014
D	1.950	2.050	0.077	0.081
D2	1.000	1.450	0.039	0.057
E	1.950	2.050	0.077	0.081
E2	0.500	0.850	0.020	0.033
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

W-Type 6L DFN 2x2 Package

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