

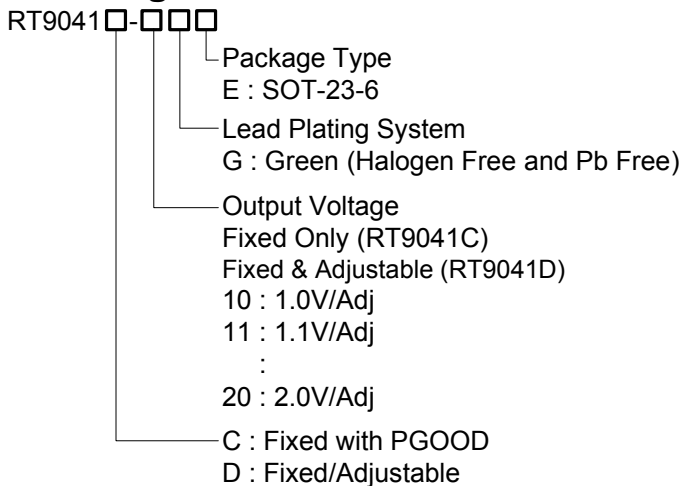
500mA, Low Voltage, LDO Regulator with External Bias Supply

General Description

The RT9041C/D are low-voltage, low-dropout linear regulators with an external bias supply input. The bias supply drives the gate of the internal N-MOSFET, making these devices ideal for applications that require low voltage outputs from low voltage inputs. The RT9041C/D provide fixed voltages from 1V to 2V with 0.1V increment. Additionally, RT9041D is capable of using external resistors to provide adjustable output voltages. The RT9041C/D include current limit and thermal shutdown features that protect the regulator in the event of a fault condition.

The RT9041C/D is available in a SOT-23-6 package.

Ordering Information



Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Features

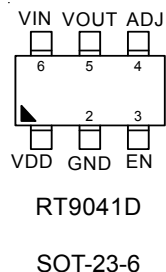
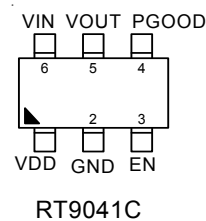
- $\pm 1\%$ Output Voltage Accuracy
- No Minimum Load Current Required
- 1V to 5.5V Input Supply Voltage
- 3V to 5.5V Input Bias Supply Voltage
- PGOOD Open-Drain Output (RT9041C)
- Support both Fixed/Adjustable Mode (RT9041D)
- Low Supply Current
- 5 μ A (max) Shutdown Supply Current
- RoHS Compliant and Halogen Free

Applications

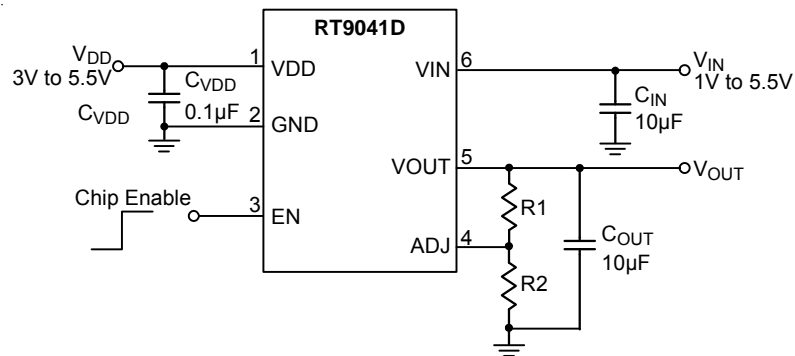
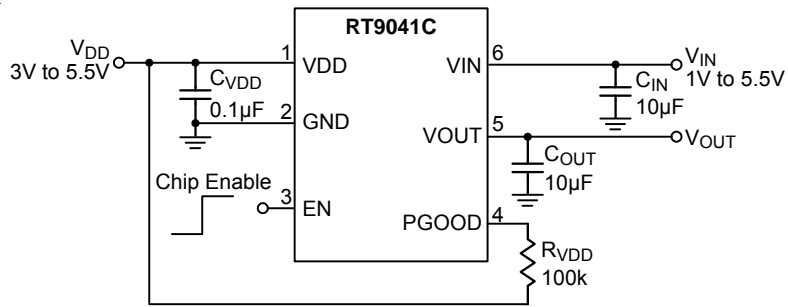
- Notebook Computers
- VID Power Supplies
- PDAs
- Cell Phones
- Low-Dropout Regulators with External Bias Supply

Pin Configurations

(TOP VIEW)



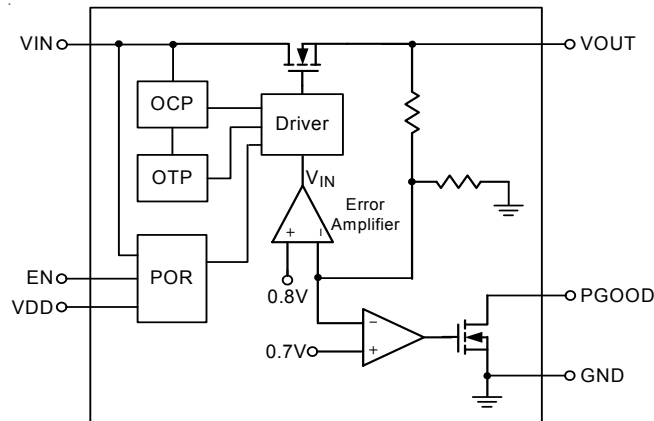
Typical Application Circuit



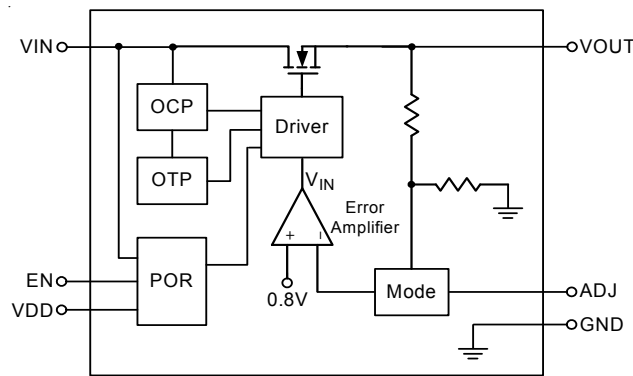
Function Pin Description

Pin No.		Pin Name	Pin Function
RT9041C	RT9041D		
1	1	VDD	Supply Voltage of Control Circuitry.
6	6	VIN	Supply Input Voltage.
5	5	VOUT	Output Voltage.
3	3	EN	Chip Enable (Active High).
2	2	GND	Ground.
4	--	PGOOD	Power Good Open Drain Output.
--	4	ADJ	Output Voltage Adjust Pin. Set the output voltage by the internal feedback resistors when ADJ is grounded. If external feedback resistors is used, $V_{OUT} = V_{REF} \times (R1 + R2)/R2$.

Function Block Diagram



RT9041C



RT9041D

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ----- 6V
- Control Voltage, V_{DD} ----- 6V
- Other Input/Output Pins ----- 6V
- Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$
 SOT-23-6 ----- 0.4W
- Package Thermal Resistance (Note 2)
 SOT-23-6, θ_{JA} ----- 250°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
 HBM (Human Body Model) ----- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN} ----- 1V to 5.5V
- Control Voltage, V_{DD} ----- 3V to 5.5V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

Electrical Characteristics

($V_{IN} = 1.8\text{V}$, $I_{LOAD} = 1\text{mA}$, $C_{OUT} = 10\mu\text{F}$, $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input						
Output Voltage Range (for RT9041C only)	V_{OUT}		1	--	2	V
Output Voltage Range (for RT9041D only)	V_{OUT}		0.8	--	2.5	V
Bias Input Under Voltage Lockout			--	2.7	--	V
V_{IN} Shutdown Current	I_{SHDN}	$1\text{V} < V_{IN} < 5.5\text{V}$, $V_{IN} = V_{OUT} + 0.6\text{V}$	--	1	5	μA
Quiescent Current	I_Q	$3\text{V} < V_{DD} < 5.5\text{V}$	--	160	250	μA
V_{DD} Shutdown Current	I_{SHDN}	$3\text{V} < V_{DD} < 5.5\text{V}$	--	1	5	μA
Regulator Characteristics						
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN}$	$I_{OUT} = 10\text{mA}$, $1.5\text{V} < V_{IN} < 5.5\text{V}$, $V_{IN} = V_{OUT} + 0.6\text{V}$	-0.1	--	0.1	%/V
Load Regulation	$\Delta V_{OUT} / \Delta I_{IN}$	$V_{IN} = V_{OUT} + 0.6\text{V}$, $I_{OUT} = 1\text{mA}$ to 500mA	--	0.2	1	%
Output Voltage Accuracy (RT9041C)	ΔV_{OUT}	$V_{IN} = V_{OUT} + 0.6\text{V}$, $I_{OUT} = 10\text{mA}$	-1	--	1	%
Output Voltage Accuracy (RT9041D)	ΔV_{OUT}	$V_{IN} = V_{OUT} + 0.6\text{V}$, $I_{OUT} = 10\text{mA}$, Short ADJ to GND	-1	--	1	%
Reference Voltage (RT9041D)		$I_{OUT} = 10\text{mA}$	0.792	0.8	0.808	V
Dropout Voltage	V_{DROP}	$I_{LOAD} = 300\text{mA}$, $V_{DD} - V_{OUT} \geq 2.1\text{V}$	--	200	300	mV
		$I_{LOAD} = 500\text{mA}$, $V_{DD} - V_{OUT} \geq 2.1\text{V}$	--	300	500	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit	I _{LIM}	R _{LOAD} = 0	550	700	1400	mA
Thermal-Shutdown Temp	T _{SD}	3V < V _{BIAS} < 5.5V	--	160	--	°C
Thermal-Shutdown Hysteresis	ΔT _{SD}		--	20	--	°C
ADJ						
ADJ Pin Threshold (RT9041D)			--	0.2	--	V
PGOOD Comparator						
Comparator Threshold		% of regulated output voltage	--	88	--	%
Comparator Hysteresis	V _{HYST}	(Note 5)	--	10	--	mV
Logic and I/O						
EN Input Voltage	Logic-High	V _{IH}	1.6	--	--	V
	Logic-Low	V _{IL}	--	--	0.8	
EN Current	I _{EN}	V _{EN} = 5V	--	12	--	μA
PGOOD Output Low Voltage (RT9041C)		PGOOD sinking 1mA	--	--	0.1	V
PGOOD Output High Leakage Current (RT9041C)		0 < V _{PGOOD} < V _{IN}	-1	--	1	μA
Dynamics						
PGOOD Propagation Delay (RT9041C)	t _{PGOOD}	Rising edge within 5% of regulation level	1	--	5	ms

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

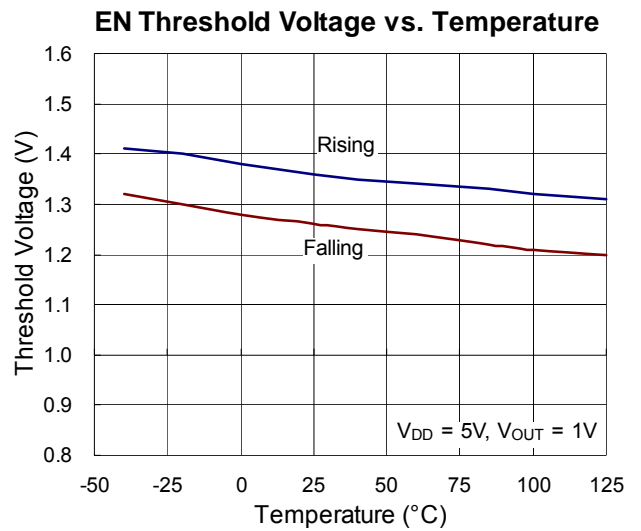
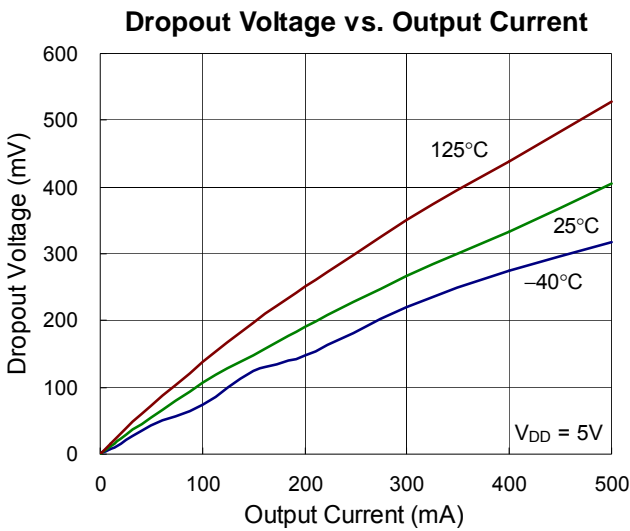
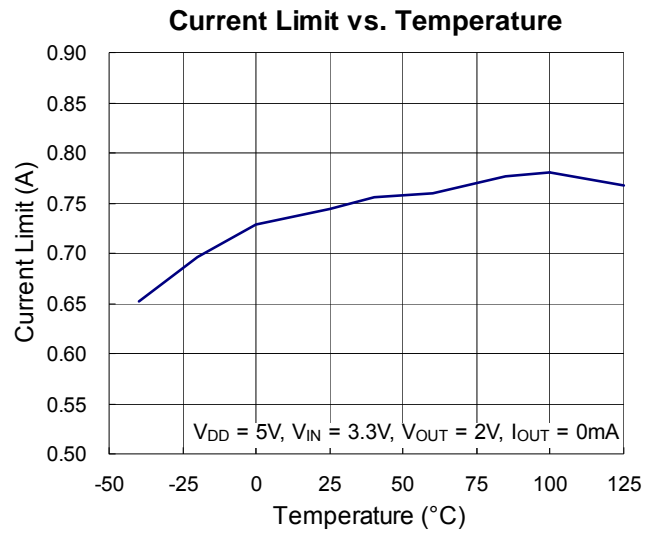
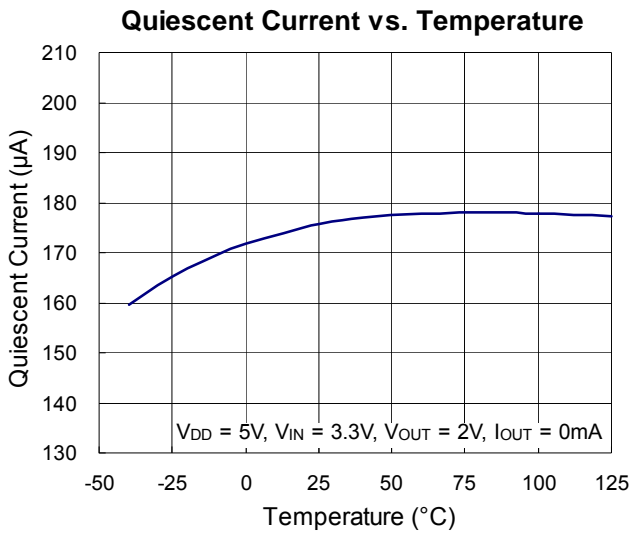
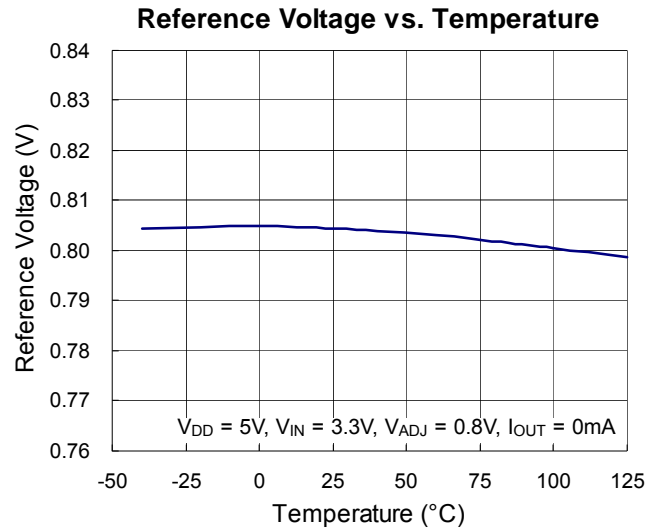
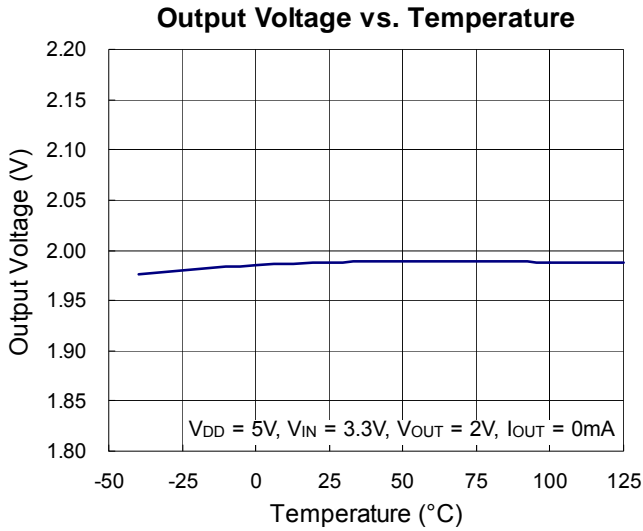
Note 2. θ_{JA} is measured at T_A = 25°C on a low effective thermal conductivity single-layer test board per JEDEC 51-3

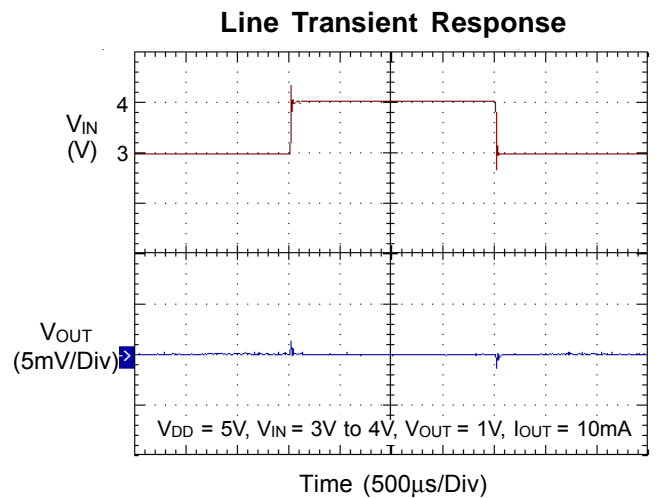
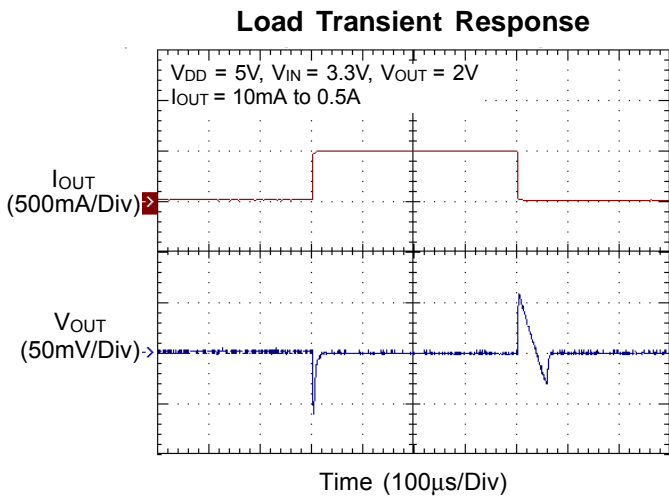
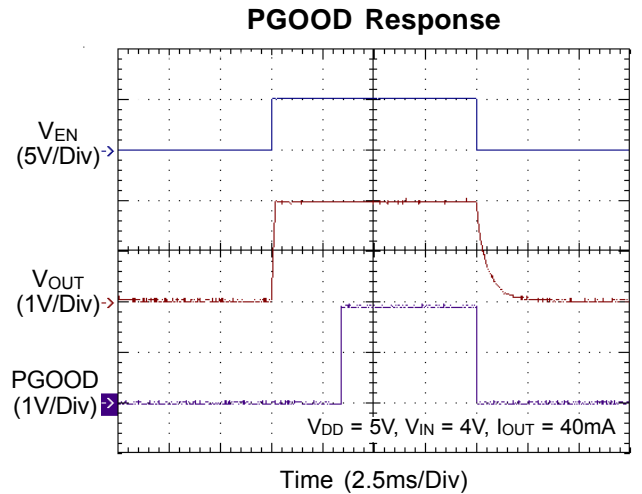
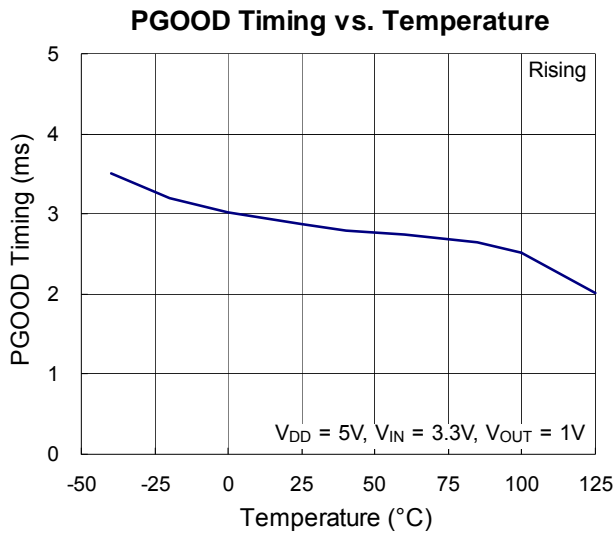
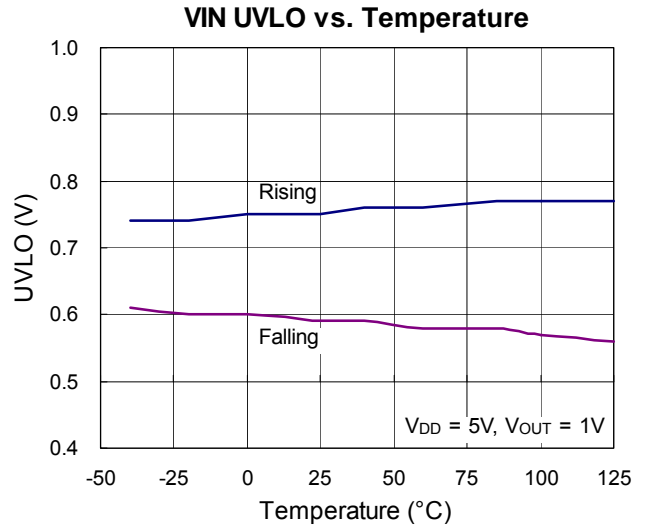
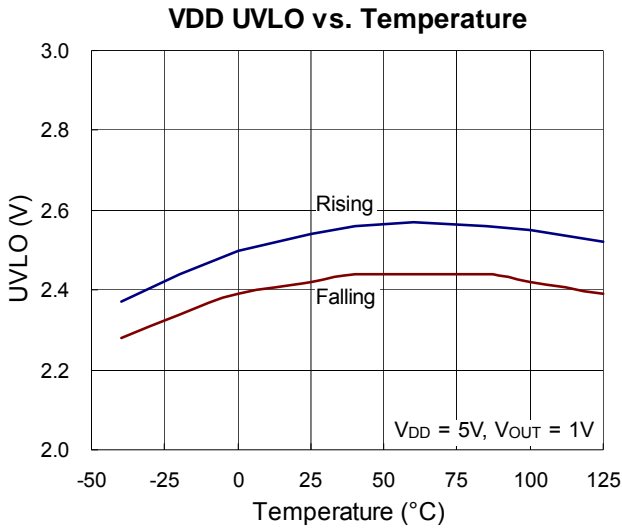
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

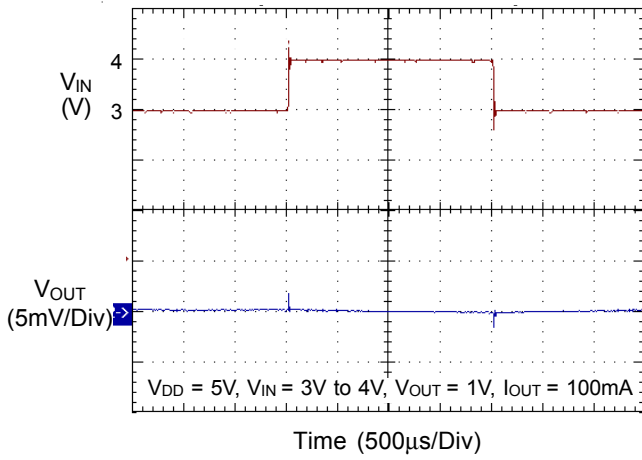
Note 5. Guaranteed by design.

Typical Operating Characteristics

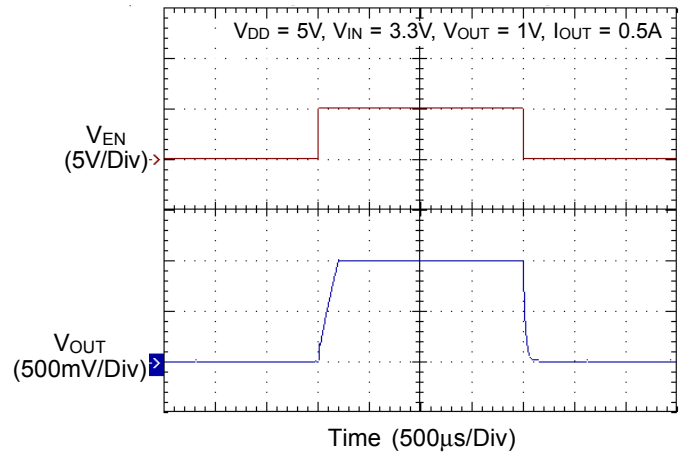




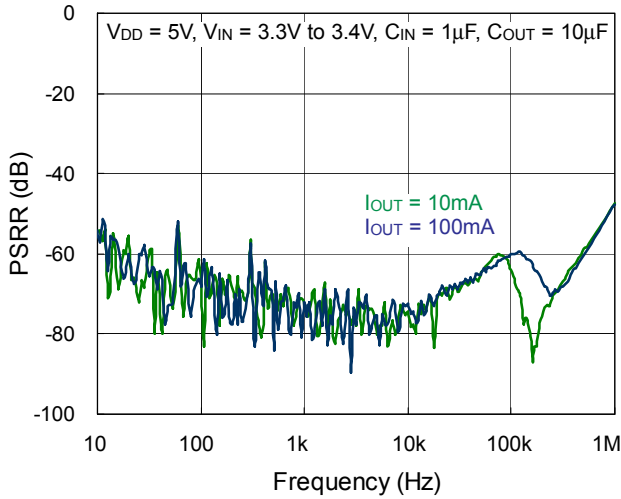
Line Transient Response



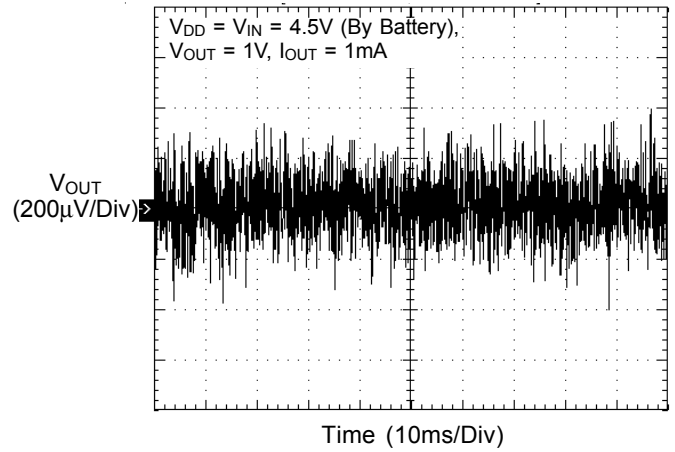
EN Response



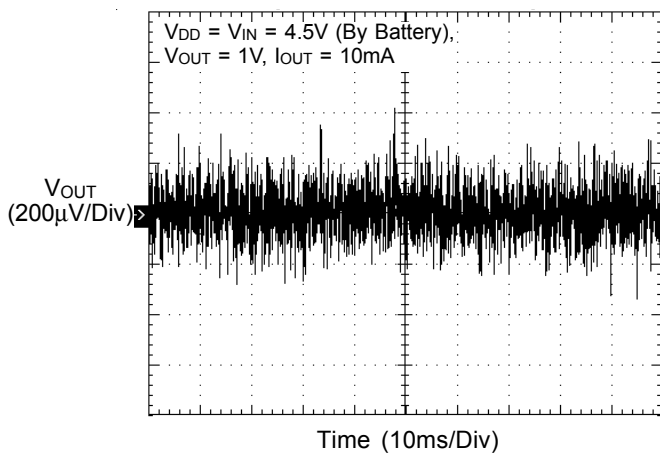
PSRR



Noise



Noise



Application Information

The RT9041C/D is a low voltage, low dropout linear regulator with an external bias supply input, capable of supporting an input voltage range from 1V to 5.5V with a fixed output voltage from 1V to 2V in 0.1V increments.

Supply Voltage Setting

The bias supply voltage (V_{DD}) operates from 3V to 5.5V. For better efficiency, it is suggested to operate V_{DD} at 5V when the output voltage is higher than 1V. Figure 1 shows the curves of the recommended $V_{DD} - V_{OUT}$ range vs. the dropout voltage ($V_{IN} - V_{OUT}$) values.

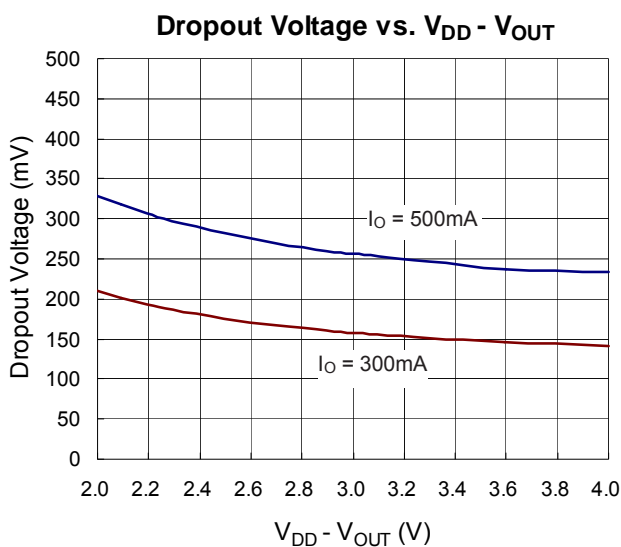


Figure 1. Dropout Voltage vs. $V_{DD} - V_{OUT}$

Output Voltage Setting

The RT9041D output voltage is also adjustable from 0.8V to 2.5V via the external resistive voltage divider. The voltage divider resistors can have values up to 800k Ω because of the very high impedance and low bias current of the sense comparator. The output voltage is set according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2} \right)$$

where V_{REF} is the reference voltage with a typical value of 0.8V.

Chip Enable Operation

The RT9041C/D goes into sleep mode when the EN pin is in a logic low condition. In this condition, the pass transistor, error amplifier, and band gap are all turned off, reducing the supply current to 1 μ A (typ.). The EN pin can be directly tied to V_{IN} to keep the part on.

Current Limit

The RT9041C/D contains an independent current limit circuitry, which monitors and controls the pass transistor's gate voltage, limiting the output current to 0.7A (typ.).

CIN and COUT Selection

Like any low dropout regulator, the external capacitors of the RT9041C/D must be carefully selected for regulator stability and performance. Using a capacitor of at least 10 μ F is suitable. The input capacitor must be located at a distance of not more than 0.5 inch from the input pin of the IC. Any good quality ceramic capacitor can be used. However, a capacitor with larger value and lower ESR (Equivalent Series Resistance) is recommended since it will provide better PSRR and line transient response.

The RT9041C/D is designed specifically to work with low ESR ceramic output capacitor for space saving and performance consideration. Using a ceramic capacitor with value at least 10 μ F and ESR larger than 2m Ω on the RT9041C/D output ensures stability. Nevertheless, the RT9041C/D can still work well with other types of output capacitors due to its wide range of stable ESR. Figure 2 shows the allowable ESR range as a function of load current for various output capacitance. Output capacitors with larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located at a distance of not more than 0.5 inch from the output pin of the RT9041C/D.

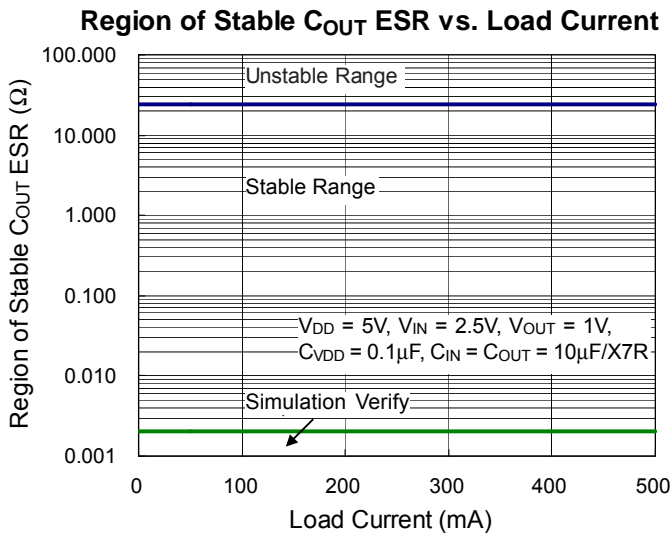


Figure 2. Region of Stable C_{OUT} ESR vs. the Load Current

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA} , is layout dependent. For SOT-23-6 packages, the thermal resistance, θ_{JA} , is 250°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by the following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (250^\circ\text{C}/\text{W}) = 0.400\text{W for}$$

SOT-23-6 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA} . The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

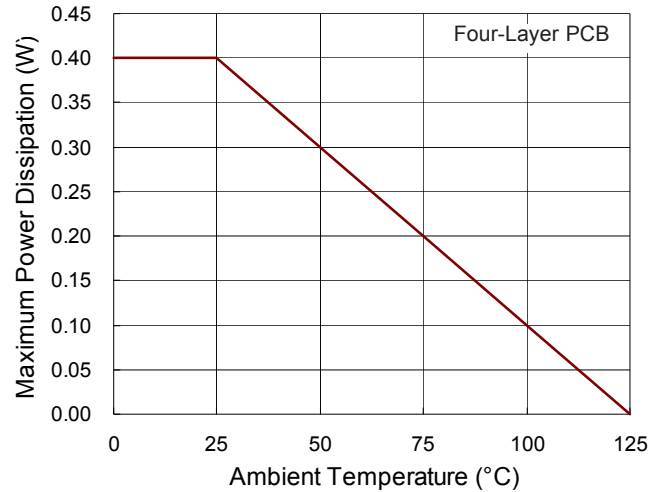
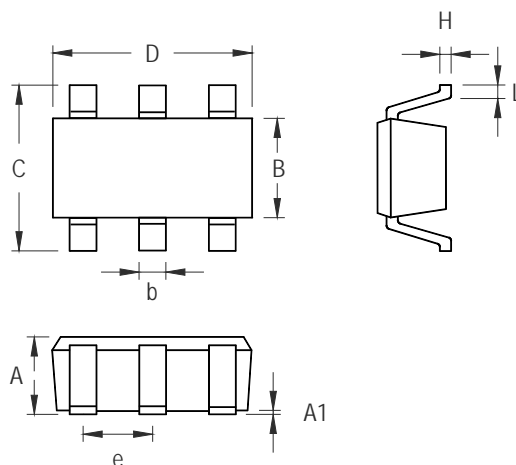


Figure 3. Derating Curve of Maximum Power Dissipation

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

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