Low-Dropout Linear Regulator Controller with PGOOD Indication

General Description

The RT9046 is a low-dropout voltage regulator controller designed specifically for use with an external N-MOSFET for various applications. The controller features a 2% reference, a high current driver capability of driving a high current/low $R_{DS(ON)}$ N-MOSFET, programmable output voltage, a power monitor with a 0.6ms delay, internal soft-start function, under voltage protection, and chip enable for power conservation. The device is also useful in other high current applications. The RT9046 is available in a small footprint package of SOT-23-6.

Ordering Information

RT9046 □□

- Package Type
  E : SOT-23-6
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

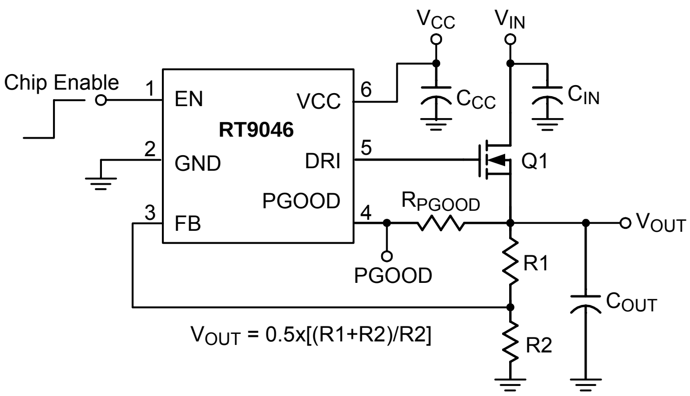
Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Typical Application Circuit



Features

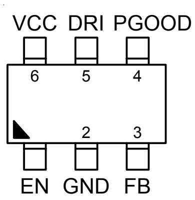
- **Programmable Output Voltage**
- **High Current Driver for High Current FET**
- **High Accuracy ±2% Voltage Reference**
- **Quick Line and Load Transient Response**
- **Power Good Monitor with Output Delay**
- **Internal Soft-Start Function to Reduce Inrush Current**
- **Enable Control and Under Voltage Protection**
- **Small Footprint Package SOT-23-6**
- **RoHS Compliant and Halogen Free**

Applications

- Large-scale, Telecom Blade Systems
- Large-scale, Mass Storage Blade Systems
- High Current Systems Requiring Sequencing
- High Current Systems Requiring Power Management

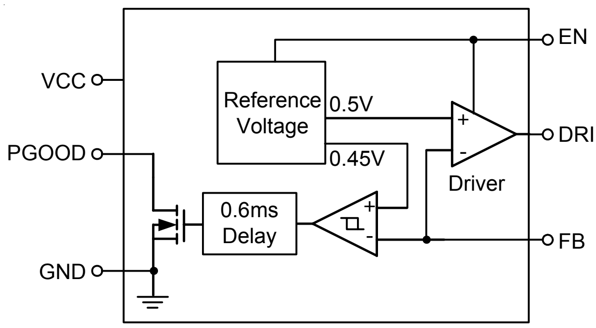
Pin Configurations

(TOP VIEW)



SOT-23-6

Function Block Diagram



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Chip Enable (Active High).
2	GND	Ground.
3	FB	Output Voltage Feedback.
4	PGOOD	Power Good Open Drain Output.
5	DRI	Driver Output.
6	VCC	Power Supply Input.

Test Circuit

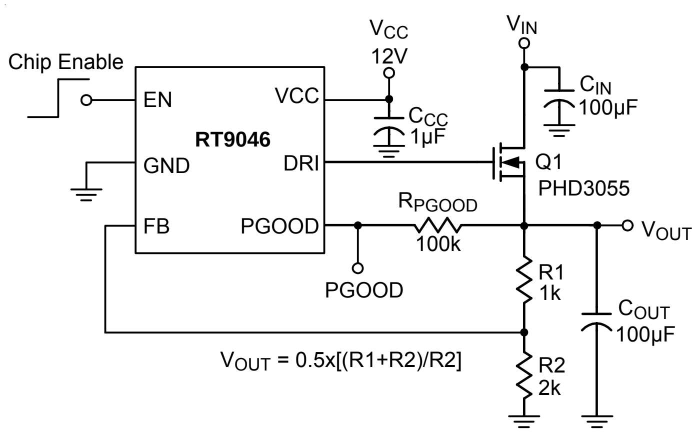


Figure 1. Typical Test Circuit

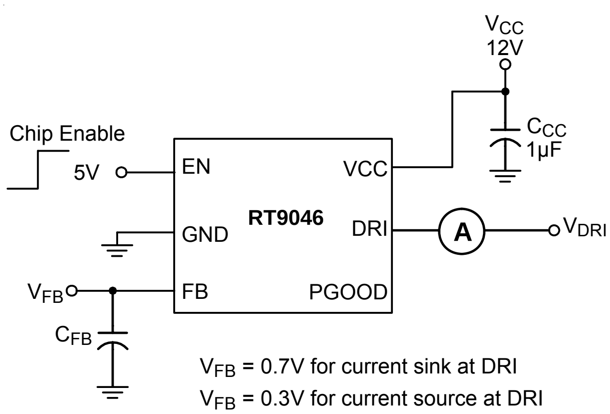


Figure 2. DRI Source/Sink Current Test Circuit

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{CC} ---------- 15V
- Enable Voltage ---------- 6.5V
- Power Good Output Voltage ---------- 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-6 ---------- 0.4W
- Package Thermal Resistance (Note 2)
  SOT-23-6, θ_{JA} ---------- 250°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- −65°C to 150°C

Recommended Operating Conditions (Note 3)

- Supply Input Voltage, V_{CC} ---------- 3.3V to 13.5V
- Enable Voltage ---------- 0V to 5.5V
- Junction Temperature Range ---------- −40°C to 125°C
- Ambient Temperature Range ---------- −40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V/12V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
POR Threshold			V_{CC} Rising	2.6	2.85	3.2	V
POR Hysteresis				–	0.2	--	V
V_{CC} Supply Current			V_{CC} = 12V	–	0.3	0.8	mA
Driver Source Current			V_{CC} = 12V, V_{DRI} = 6V	5	--	--	mA
Driver Sink Current			V_{CC} = 12V, V_{DRI} = 6V	5	--	--	mA
Reference Voltage (V_{FB})			V_{CC} = 12V, V_{DRI} = 5V	0.49	0.5	0.51	V
Reference Line Regulation (V_{FB})			V_{CC} = 4.5V to 15V	–	3	6	mV
Amplifier Voltage Gain			V_{CC} = 12V, No Load	–	70	--	dB
PSRR at 100Hz			V_{CC} = 12V, No Load	50	--	--	dB
Power Good							
Rising Threshold			V_{CC} = 12V	–	90	--	%
Hysteresis			V_{CC} = 12V	–	15	--	%
Sink Capability			V_{CC} = 12V @ 1mA	–	0.2	0.4	V
Delay Time			V_{CC} = 12V	0.2	0.6	2	ms
Falling Delay			V_{CC} = 12V	–	15	--	μs
Chip Enable							
EN Threshold	Logic-High Voltage	V_{IH}	V_{CC} = 12V	1.4	–	5.5	V
	Logic-Low Voltage	V_{IL}	V_{CC} = 12V	--	–	0.4	
Standby Current			V_{CC} = 12V, V_{EN} = 0V	--	–	5	μA

To be Continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Soft-Start Function						
Output Turn-On Rise Time		V_{CC} = 12V, V_{OUT} = 1.5V, C_{OUT} = 800μF	0.2	0.35	--	ms
UV Protection						
Under Voltage Protection		V_{CC} = 12V	40	50	60	%

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

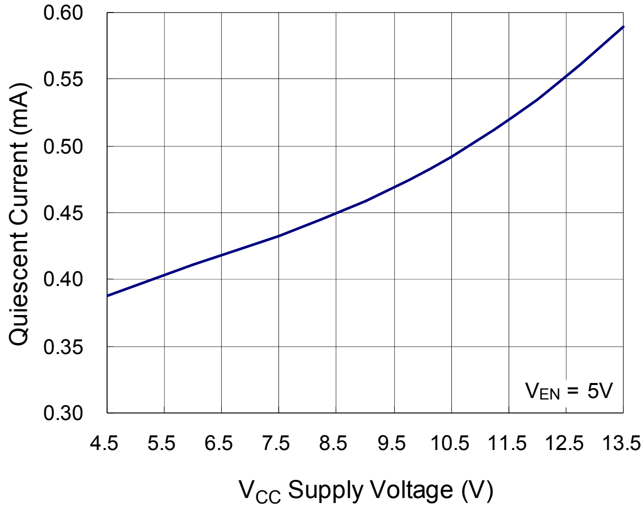
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3. The device is not guaranteed to function outside its operating conditions.

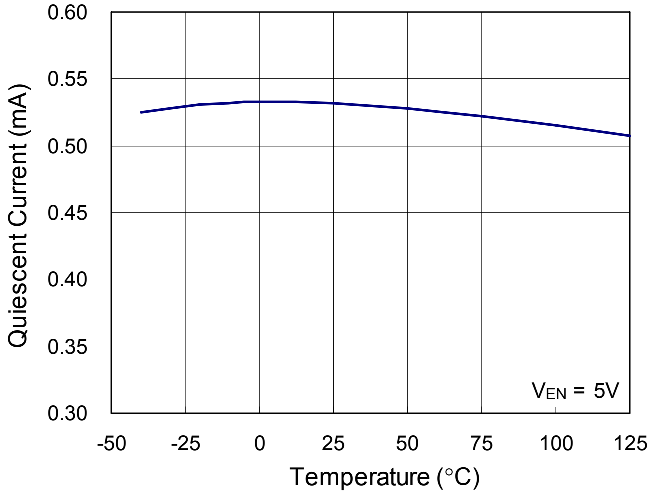
Typical Operating Characteristics

V_{IN} = 1.8V, V_{OUT} = 1.5V, V_{CC} = 12V, C_{IN} = C_{OUT} = 100µF, R1 = 4k, R2 = 2k, T_A = 25°C, unless otherwise specified.

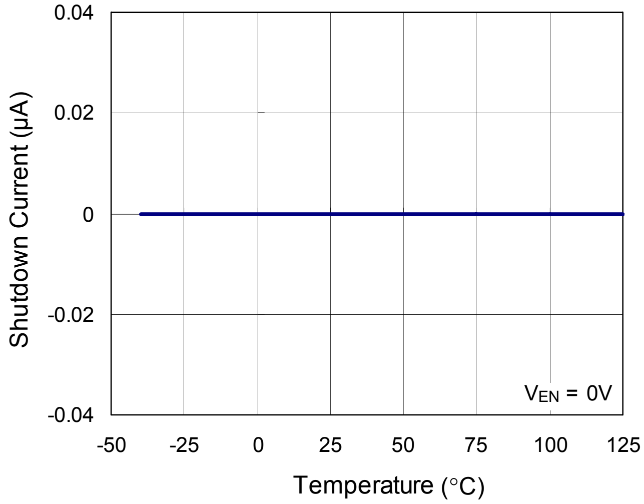
Quiescent Current vs. V_{CC} Supply Voltage



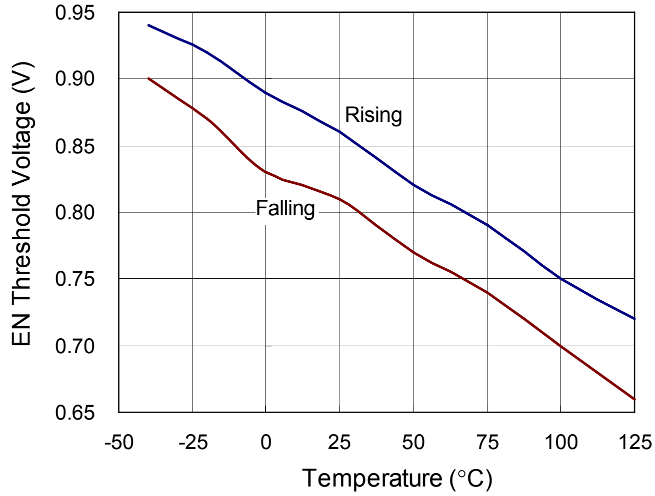
Quiescent Current vs. Temperature



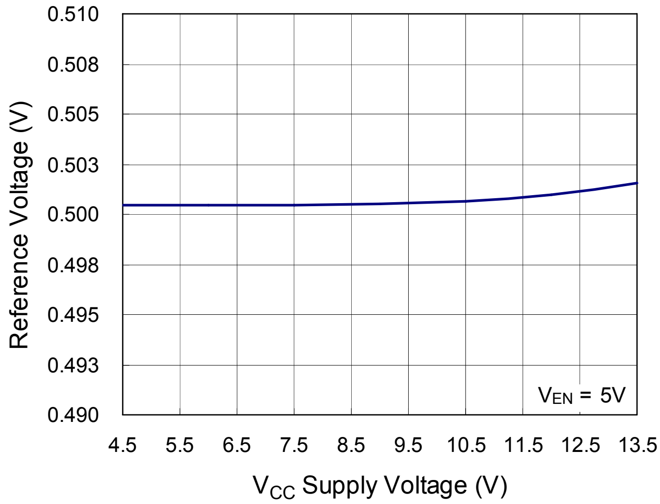
Shutdown Current vs. Temperature



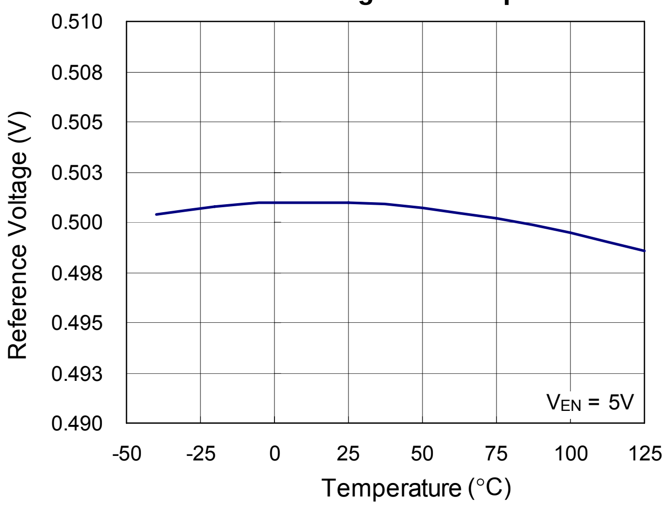
EN Threshold Voltage vs. Temperature



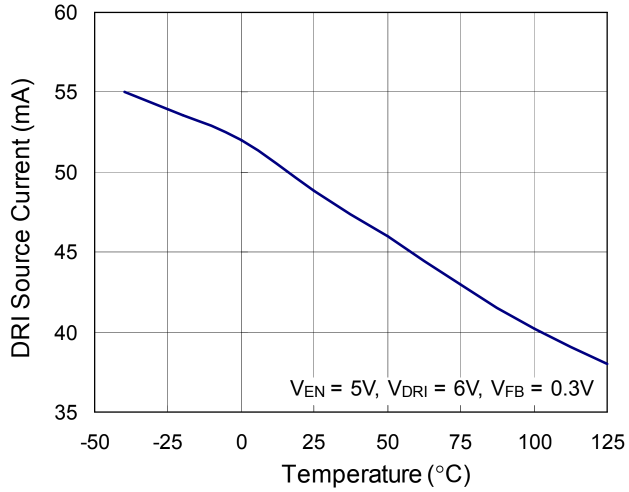
Reference Voltage vs. V_{CC} Supply Voltage



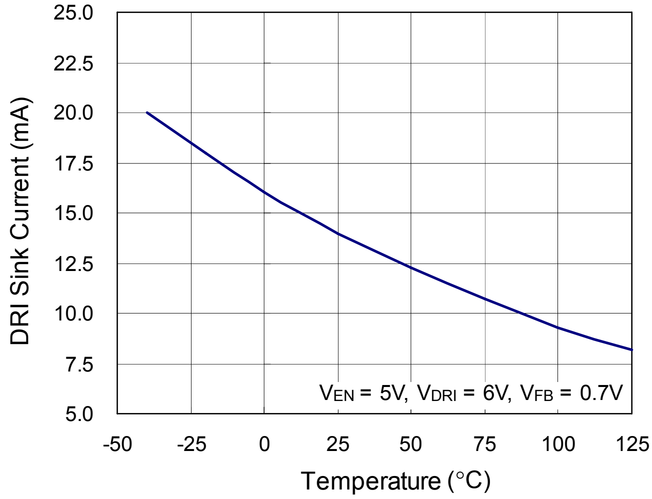
Reference Voltage vs. Temperature



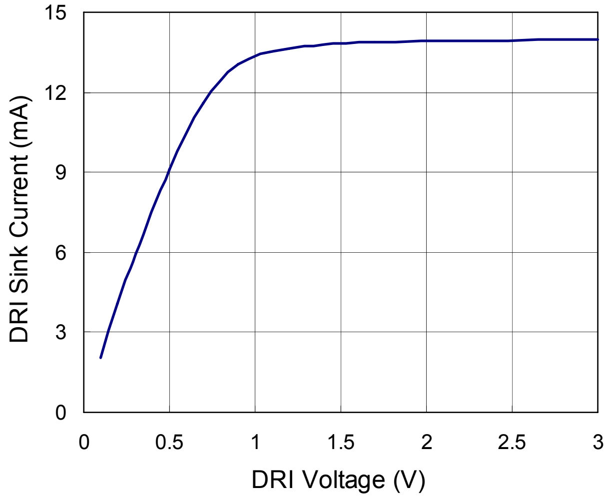
DRI Source Current vs. Temperature



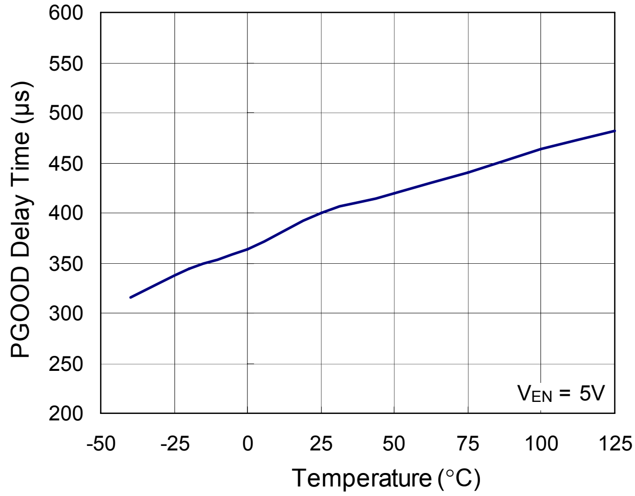
DRI Sink Current vs. Temperature



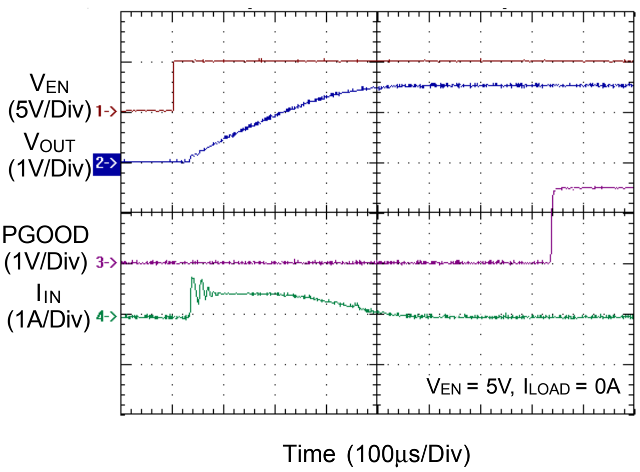
DRI Sink Current vs. DRI Voltage



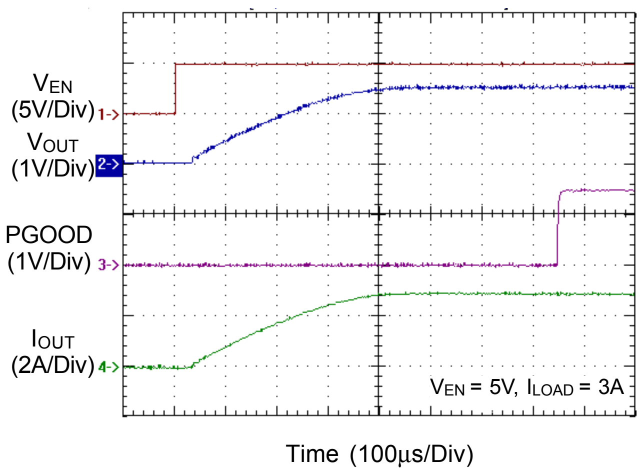
PGOOD Delay Time vs. Temperature



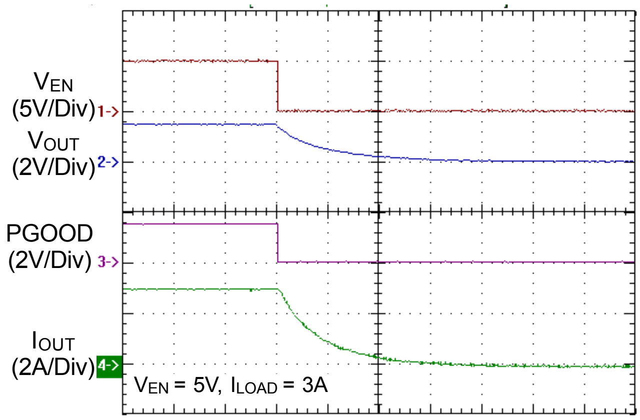
Start Up from EN and Inrush Current



Start Up from EN and PGOOD Delay

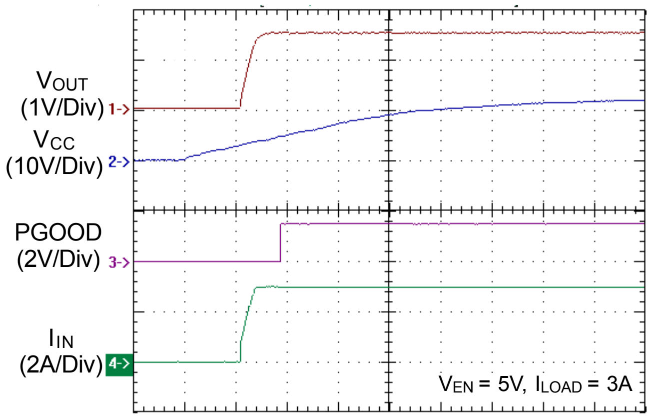


PGOOD Off



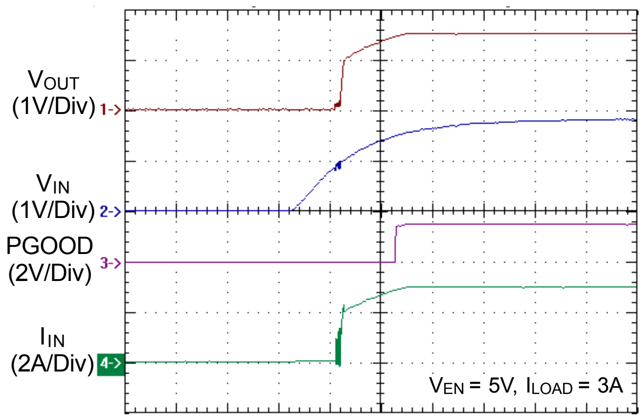
Time (50μs/Div)

Start Up from V_{CC}



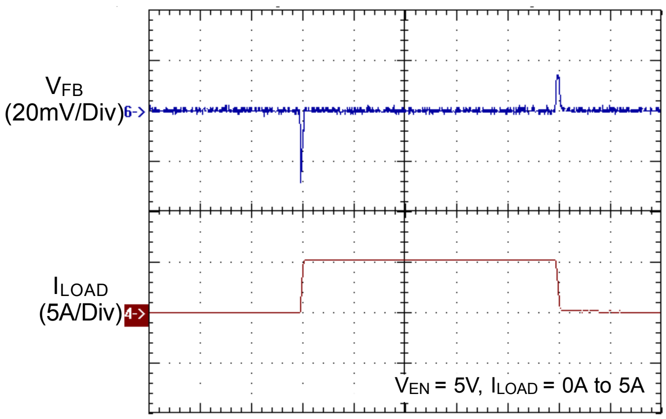
Time (1ms/Div)

Start Up from V_{IN}



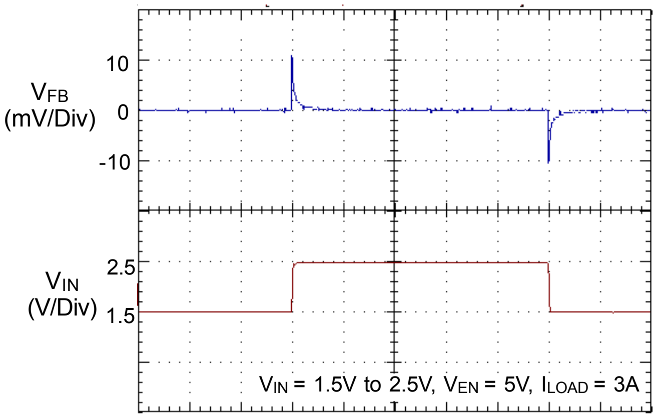
Time (2.5ms/Div)

Load Transient Response



Time (250μs/Div)

Line Transient Response



Time (100μs/Div)

Application Information

Capacitor Selection

External capacitors are necessary for the proper operation of the RT9046. The power supply, requires a 1μF ceramic capacitor between VCC and ground. This capacitor shunts power supply current transients to ground and stabilizes the input voltage to the RT9046. The capacitor should be placed as close to VCC as possible.

The power source for the pass transistor, V_{IN}, requires an input capacitor. A larger 100μF ceramic capacitor should be placed as close to the pass transistor's (Q1's) drain as possible to ensure the best PSRR and line transient response for V_{OUT}.

Again, it is necessary to place a 100μF capacitor between V_{OUT} and ground to reduce noise, and improve load transient response and PSRR.

Output Voltage Setting

The output voltage, is determined using a simple resistor divider and the internal 0.5V, 2% reference. The output can be programmed by the following equation :

$$V_{OUT} = 0.5 \times \frac{R1 + R2}{R2}$$

In order to achieve desired output voltage regulation, resistors must be selected for the accuracy of their nominal value. For a 5% accurate output voltage, 1% resistors should be employed in the design.

Power Good Function

The RT9046 has the power good function with 0.6ms delay. The power good output, is an open drain output. Connect a 100kΩ pull up resistor between VOUT and PGOOD, to sample the output voltage.

When the output voltage, reaches 90% of the desired value, the power good will output a logic high 0.6ms later. When the output voltage drops below 75% of the desired value, PGOOD will output a logic low 15μs later.

There are two exceptions : if the chip enable is pulled low or if VCC drops below the power-on reset (POR) value (2.65V @ 25°C), PGOOD will output a logic low.

Chip Enable Operation

The EN pin is the chip enable input. Pull the EN pin low (<0.4V) to shutdown the device. During shutdown mode, the RT9046 quiescent current drops below 5μA. The external capacitor and load current determine the output voltage decay rate (see Accelerating V_{OUT} Shutdown to improve shutdown speed). Drive the EN pin high (>1.4V) to turn the device on again.

Under Voltage Protection

The RT9046 provides V_{OUT} with under voltage protection, UVP. The UVP circuit begins monitoring V_{OUT} after it achieves 90% of the desired output voltage and the PGOOD pin has output a logic high. If V_{OUT} drops below 50% of its desired value, the PGOOD and DRI pins will be pulled low and the RT9046 will enter latch mode. The RT9046 can only be unlatched by cycling the VCC or EN pin low and then high again. This action will cause the RT9046 to exit the latch mode and restart.

MOSFET Selection

The RT9046 is designed to drive an external N-MOSFET. The MOSFET selection criteria include :

- Maximum continuous drain current, I_{DMAX}
- On-resistance, $R_{DS(ON)}$
- Threshold voltage, V_{GS_TH}
- Drain-to-source voltage, V_{DS}
- Package thermal resistance, θ_{JA}

The MOSFET must be able to carry the maximum current required by the load at V_{OUT}. MOSFET $I_{D(MAX)}$ should be greater than or equal to $I_{LOAD(MAX)}$ for V_{OUT}. Once we know $I_{LOAD(MAX)}$, we can calculate the maximum allowable MOSFET $R_{DS(ON)}$ as follows :

$$R_{DS(ON)} = \frac{(V_{IN} - V_{OUT})}{I_{LOAD(MAX)}}$$

For example, if the maximum load current, $I_{LOAD(MAX)}$, is 2A, V_{IN} is 1.5V, and V_{OUT} is 1.2V, then

$$R_{DS(ON)} = \frac{(1.5V - 1.2V)}{2A} = 150m\Omega$$

Thus, the MOSFET must have an $R_{DS(ON)}$ equal to or lower than 150mΩ when operating with V_{DS} of 0.3V at 2A.

The MOSFET must also have a V_{GS_TH} low enough to be turned on by the driver circuit at the driver output, V_{DRI}.

Finally, the MOSFET's junction to ambient temperature thermal resistance, θ_{JA}, must be considered. The MOSFET's junction temperature should be kept below its recommended maximum junction temperature; $T_{J(MAX)}$ = 125°C is a conservative maximum junction temperature. In the worst case example, the MOSFET will have to dissipate, 0.6W : $P_D = V_{DS} \times I_{DS(MAX)}$. In order to keep the junction temperature below the RT9046's guaranteed maximum operating ambient temperature specification ($T_{A(MAX)}$) of 85°C, we must select a MOSFET with a θ_{JA} of less than 67°C/W : $\theta_{JA} = (T_{J(MAX)} - T_{A(MAX)}) / P_D$.

A Philips PHD3055E N-MOSFET with a θ_{JA} of 50°C/W in the D-PAK package, maximum $R_{DS(ON)}$ of 150mΩ at V_{GS} = 10V, $I_{D(MAX)}$ = 10.3A, and V_{DSS} = 55V is a good choice.

Higher current and power applications may require the use of additional layout consideration, package selections, and PCB application in order to improve thermal performance of the MOSFET.

Accelerating V_{OUT} Shutdown

In order to accelerate the shutdown of V_{OUT}, a PNP transistor can be used. Given the sink capabilities of the RT9046's DRI output the KSB772 PNP transistor is a good choice. Figure 3 shows the implementation of this circuit with Q2 as the KSB772 PNP transistor. Shutdown delay will be determined by the load current.

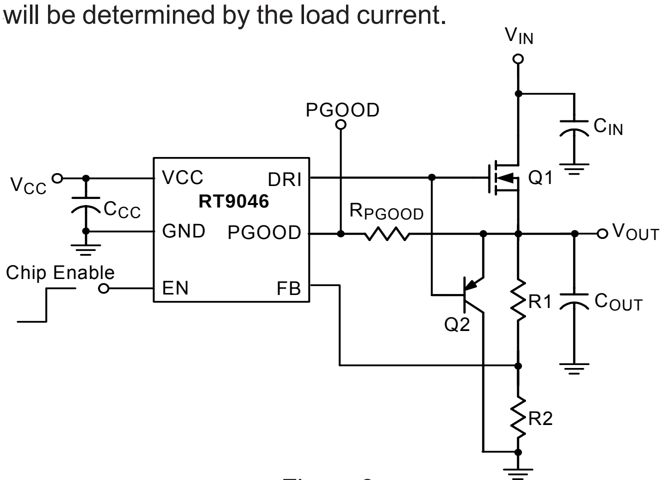


Figure 3

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT9046, the junction temperature is 125°Cand T_A is the maximum ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent. For SOT-23-6 packages, the thermal resistance θ_{JA} is 250°C/W on the standard JEDEC 51-3 single layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (250°C/W) = 0.4W for SOT-23-6 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT9046 package, the Figure 4 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

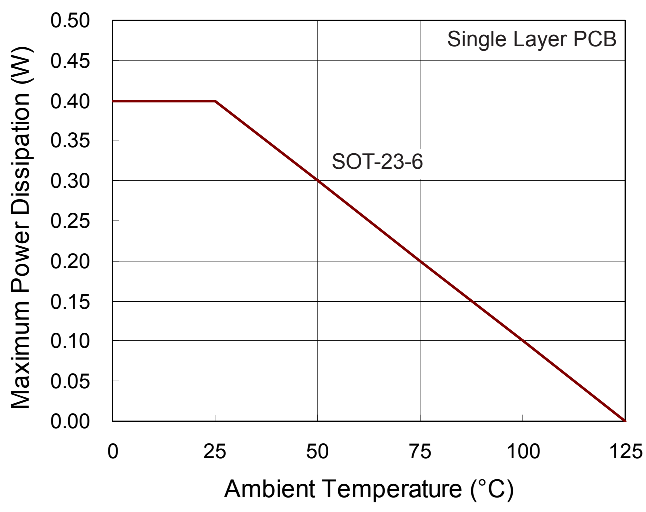


Figure 4. Derating Curves for RT9046 Packages

Layout Considerations

There are three critical layout considerations. The divider resistors, R1 and R2, should be mounted as close to the RT9046 FB pin as possible to minimize noise. Capacitor, C_{IN}, should be as close to the MOSFET's drain as possible, and output capacitor, C_{OUT}, as close to the MOSFET's source as possible. Finally, in cases where high load currents are required, designers will have to get creative. MOSFETs with mountable drains, increased copper in the layout, and fan generated air flow may be necessary to achieve workable designs. A layout example demonstrating passive placement and using increased copper area for the drain of a MOSFET pass transistor in the D-PAK package is illustrated by Figure 5.

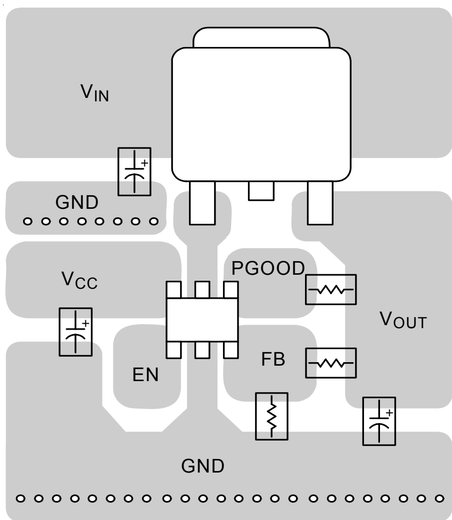
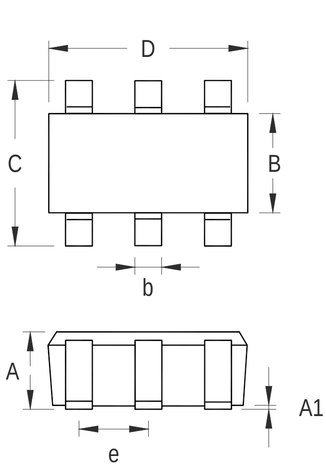


Figure 5

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

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