500mA, Low Dropout, Low Noise Ultra-Fast Without Bypass Capacitor CMOS LDO Regulator

General Description

The RT9049 is a high-performance, 500mA LDO regulator, offering extremely high PSRR and ultra-low dropout. The RT9049 is designed for portable RF and wireless applications with demanding performance and space requirements. The RT9049 quiescent current is as low as 115μA, further prolonging the battery life. The RT9049 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary which is critical for power applications in hand-held wireless devices. The RT9049 consumes typical 1.35μA in shutdown mode and has fast turn-on time less than 40μs. The other features include ultra-low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. The RT9049 is available in the SOT-23-5 package.

Ordering Information

RT9049-□□□□

- Package Type
  B : SOT-23-5
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- Fixed Output Voltage
  12 : 1.2V

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Features

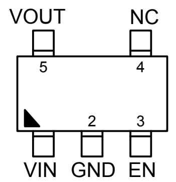
- **Wide Operating Voltage Ranges : 2.2V to 5.5V**
- **Low Dropout : 250mV at 500mA**
- **Ultra-Low-Noise for RF Application**
- **Ultra-Fast Response in Line/Load Transient**
- **Current Limiting Protection**
- **Thermal Shutdown Protection**
- **High Power Supply Rejection Ratio**
- **Only 10μF Output Capacitor Required for Stability**
- **1.35μA Shutdown Current**
- **TTL-Logic-Controlled Shutdown Input**
- **RoHS Compliant and Halogen Free**

Applications

- CDMA/GSM Cellular Handsets
- Portable Information Appliances
- Laptop, Palmtops, Notebook Computers
- HandHeld Instruments
- Mini PCI & PCI-Express Cards
- PCMCIA & New Cards

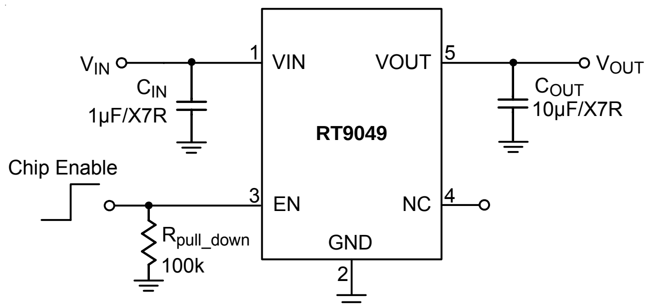
Pin Configurations

(TOP VIEW)

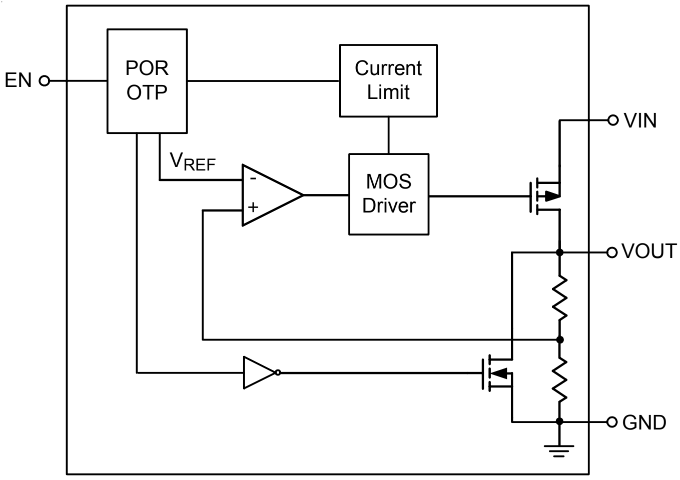


SOT-23-5

Typical Application Circuit



Function Block Diagram



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	Supply Input.
2	GND	Common Ground.
3	EN	Chip Enable (Active High). When the EN goes to a logic low, the device will be in shutdown mode.
4	NC	No Internal Connection.
5	VOUT	Regulator Output.

Absolute Maximum Ratings (Note 1)

- Input Voltage, V_{IN} ---------- 6V
- EN, V_{EN} ---------- 6V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-5 ---------- 0.4W
- Package Thermal Resistance (Note 2)
  SOT-23-5, θ_{JA} ---------- 250°C/W
  SOT-23-5, θ_{JC} ---------- 25°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 2.7V, V_{EN} = V_{IN}, C_{IN} = 1μF, C_{OUT} = 10μF(Ceramic, X7R), T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range		V_{IN}		2.2	--	5.5	V
Output Noise Voltage		V_{ON}		--	30	--	μV_{RMS}
Output Voltage Accuracy		ΔV_{OUT}	I_{OUT} = 10mA	–2	0	+2	%
Quiescent Current (Note 5)		I_Q	I_{OUT} = 0mA	--	115	125	μA
Shutdown Current		I_{SHDN}	V_{EN} = 0V	--	1.35	2	μA
Current Limit		I_{LIM}	R_{LOAD} = 0Ω	0.5	0.6	0.85	A
Load Regulation (Note 6)		ΔV_{LOAD}	1mA < I_{OUT} < 400mA V_{IN} = 2.5V	--	--	0.6	%
EN Threshold Voltage	Logic-High	V_{IH}		1.6	--	--	V
	Logic-Low	V_{IL}		--	--	0.6	
Enable Pin Current		I_{EN}		--	0.1	1	μA
Power Supply Rejection Rate		PSRR	I_{OUT} = 100mA, f = 10kHz	--	–50	--	dB
Line Regulation		ΔV_{LINE}	V_{IN} = 2.2V to 5.5V, I_{OUT} = 1mA	--	0.01	0.2	%/V
Thermal Shutdown Temperature		T_{SD}		--	170	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	30	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity single layer test board of JEDEC 51-3 thermal measurement standard. The case position of θ_{JC} is on the package top of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

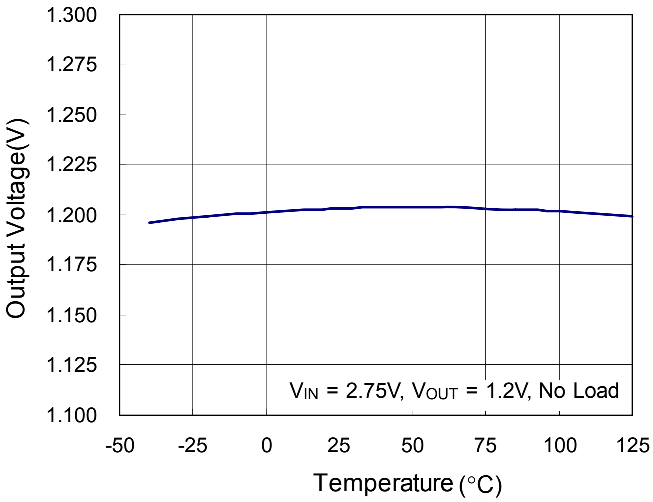
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Quiescent, or ground current, is the difference between input and output currents. It is defined by $I_Q = I_{IN}-I_{OUT}$ under no load condition (I_{OUT} = 0mA). The total current drawn from the supply is the sum of the load current plus the ground pin current.

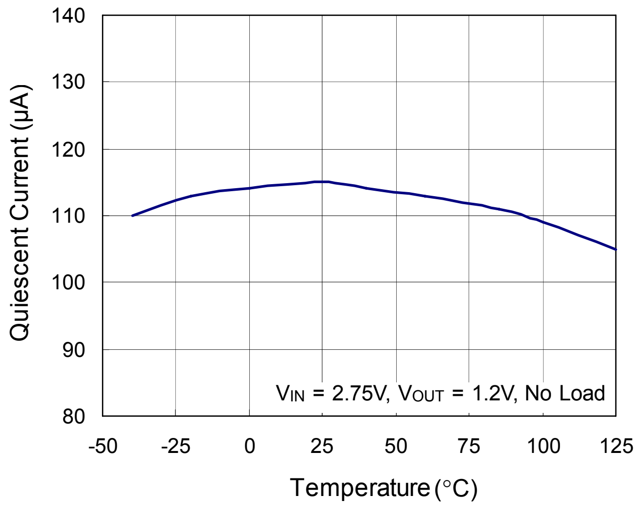
Note 6. Regulation is measured at constant junction temperature by using a 2ms current pulse. Devices are tested for loadregulation in the load range from 10mA to 500mA.

Typical Operating Characteristics

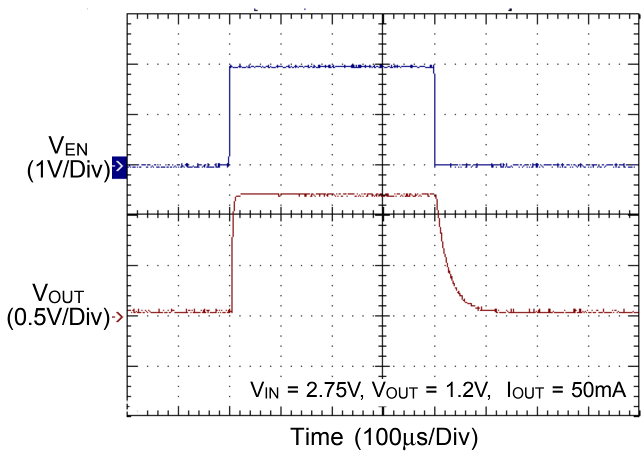
Output Voltage vs. Temperature



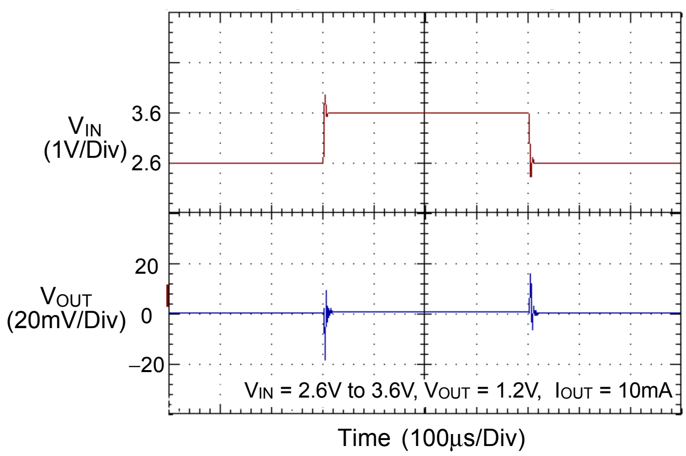
Quiescent Current vs. Temperature



Power On-Off from EN



Line Transient Response



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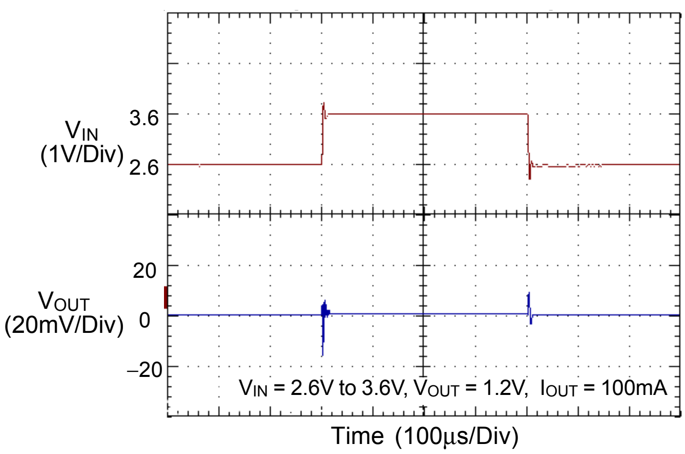
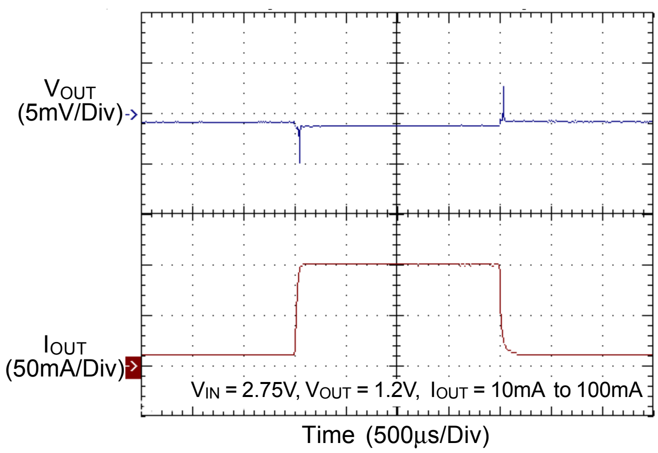
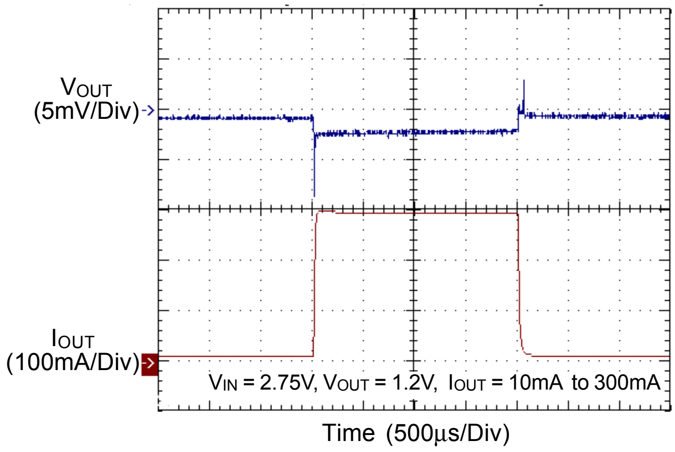


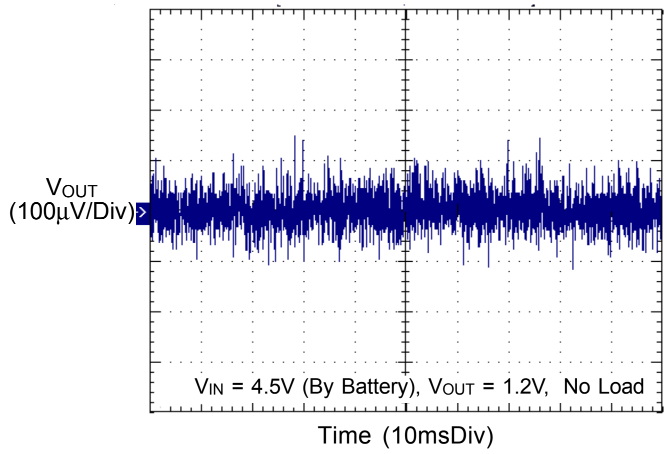
Load Transient Response



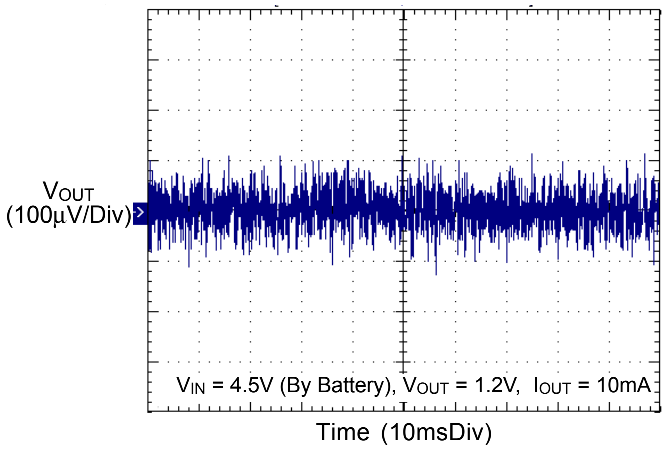
Load Transient Response



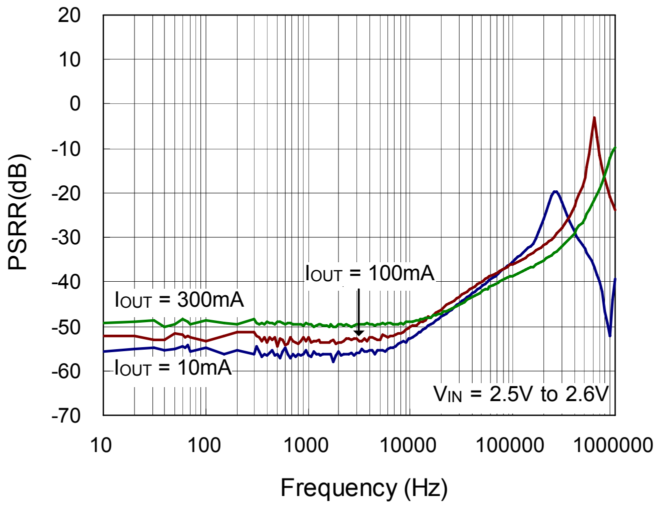
Noise



Noise



PSRR



Applications Information

Like any low-dropout regulator, the external capacitors used with the RT9049 must be carefully selected for regulator stability and performance. Using a capacitor more than 1μF on the RT9049 is suitable. The input capacitor must be located at a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum capacitance and ESR in all LDOs application. The RT9049 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 10μF with ESR is > 45mΩ on the RT9049 output ensures stability. The RT9049 still works well with output capacitor of other types due to the wide stable ESR range. Figure 1. shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located at less than 0.5 inch from the VOUT pin of the RT9049 and returned to a clean analog ground.

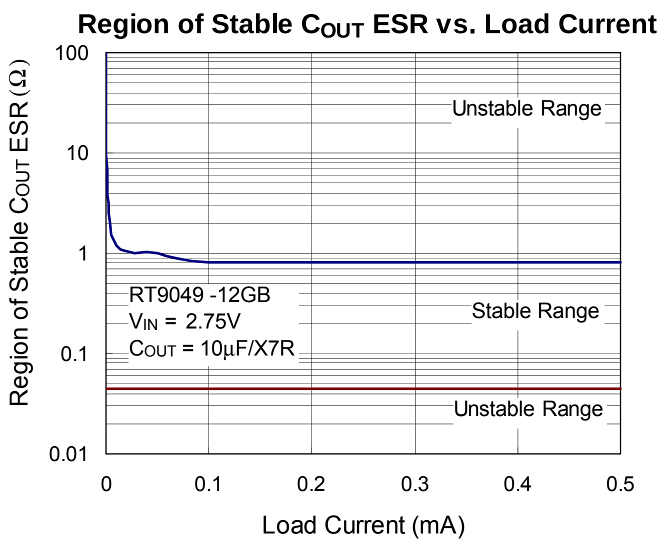


Figure 1.Region of Stable C_{OUT} ESR vs. Load Current

Enable

The RT9049 goes into sleep mode when the Enable pin is in a logic low condition. During this condition, the pass transistor, error amplifier, and bandgap are turned off, reducing the supply current to 1.35μA typical. The Enable pin may be directly tied to V_{IN} to keep the part on. The Enable input is CMOS logic and cannot be left floating.

PSRR

The power supply rejection ratio (PSRR) is defined as the gain from the input to output divided by the gain from the supply to the output. The PSRR is found to be

$$PSRR = 20 \times \log\left(\frac{\Delta \text{Gain Error}}{\Delta \text{Supply}}\right)$$

Note that when heavy load measuring, Δsupply will cause Δtemperature. And Δtemperature will cause Δoutput voltage. So the heavy load PSRR measuring is includes temperature effect.

Current Limit

The RT9049 contains an independent current limiter, which monitors and controls the pass transistor's gate voltage, limiting the output current to 0.6A (typ.). The output can be shorted to ground indefinitely without damaging the part.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT9049, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For SOT-23-5 package, the thermal resistance

θ_{JA} is 250°C/W on the standard JEDEC 51-3 single layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (250°C/W) = 0.4W for SOT-23-5 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT9049 package, the Figure 2 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

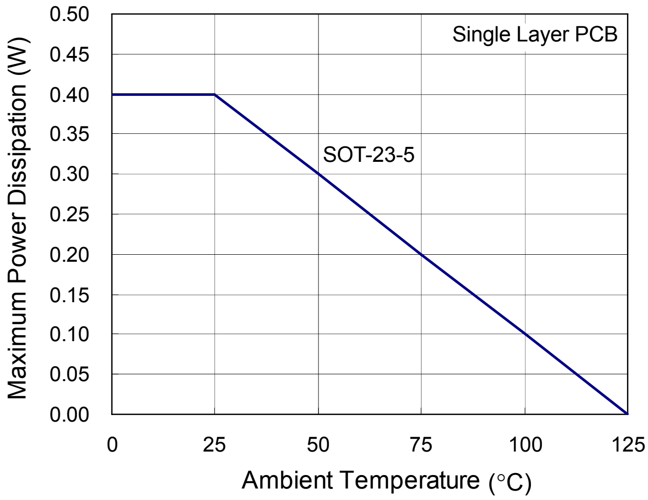
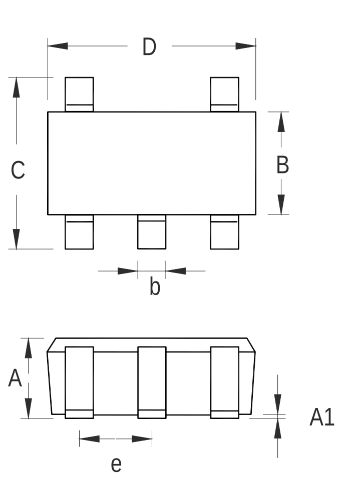


Figure 2. Derating Curves for RT9049 Package

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5 Surface Mount Package

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