RICHTEK®

RT9053A

Low Dropout, 400mA Adjustable Linear Regulator

1 General Description

The RT9053A is a high-performance, 400mA LDO regulator with ultra-low dropout. The quiescent current is as low as 35μA (typical), which helps to further prolong battery life. The RT9053A is also compatible with low ESR ceramic capacitors, reducing the amount of board space necessary for power applications, which is critical for handheld wireless devices. In shutdown mode, the RT9053A typically consumes only 0.7μA. Other features include low dropout voltage, high output accuracy, and current-limit protection. The RT9053A is available in SOT-23-5 and WDFN-6L 2x2 package options. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Ordering Information

RT9053A□□

Package Type(1)
B : SOT-23-5
QW : WDFN-6L 2x2 (W-Type)

Lead Plating System
G: Richtek Green Policy Compliant(2)
Z : ECO (Ecological Element with Halogen Free and Pb free)(3)
(for WDFN-6L 2x2 Only)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.
- Marked with (3) indicated: Suitable for use in SnPb or Pb-free soldering processes.

3 Features

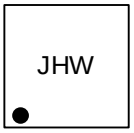
- **Adjustable Output Voltage Down to 0.8V**
- **Wide Operating Voltage Ranges: 2.2V to 5.5V**
- **Low Dropout: 230mV at 400mA**
- **Ultra-Fast Response in Line/Load Transient**
- **Current-Limit Protection**
- **Over-Temperature Protection**
- **Output Only 1μF Capacitor Required for Stability**

4 Applications

- Mega Sim Card
- CDMA/GSM Cellular Handsets
- Portable Information Appliances
- Laptop, Palmtops, Notebook Computers
- Hand-Held Instruments
- Mini PCI and PCI-Express Cards
- PCMCIA and New Cards

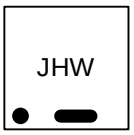
5 Marking Information

RT9053AGQW



JH=: Product Code
W: Date Code

RT9053AZQW



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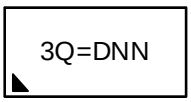
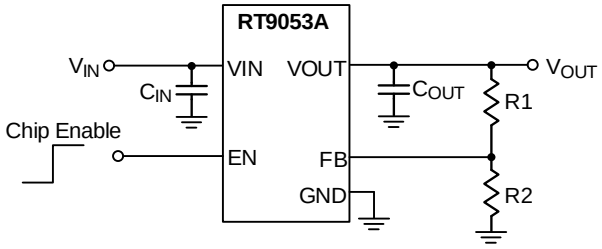
RT9053AGB



3Q=: Product Code
DNN: Date Code

6 Simplified Application Circuit



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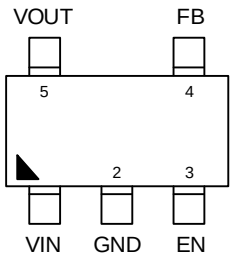
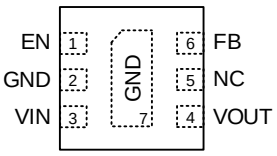
7 Pin Configuration

(TOP VIEW)



SOT-23-5

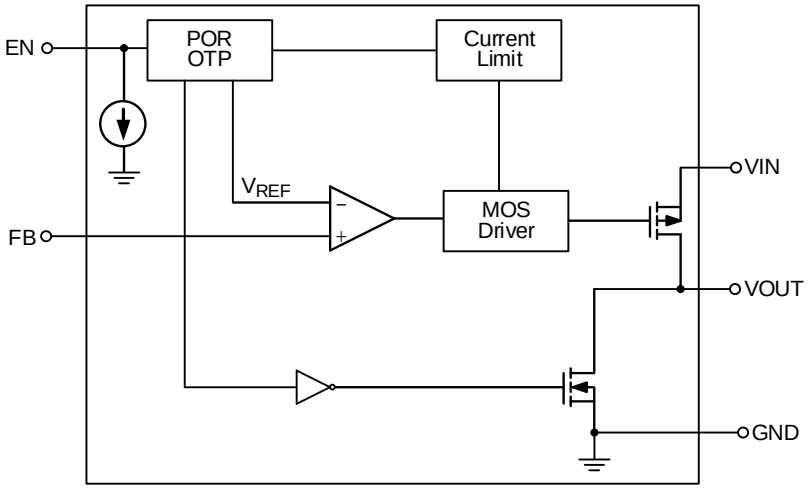


WDFN-6L 2x2

8 Functional Pin Description

Pin No.		Pin Name	Pin Function
SOT-23-5	WDFN-6L 2x2		
1	3	VIN	Supply input. A general 1μF ceramic capacitor should be placed as close as possible to this pin for better noise rejection.
2	2, 7 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
3	1	EN	Chip Enable (Active High). When the EN goes to a logic low, the device will be in shutdown mode.
4	6	FB	Feedback voltage input. This pin is used to set the desired output voltage using an external resistive divider. The typical feedback reference voltage is 0.8V.
5	4	VOUT	LDO output pins. A ceramic capacitor of 2.2μF or larger (with 1μF or greater effective capacitance) is required for stability. The output capacitor should be placed as close to the device as possible, and the impedance between the VOUT pin and the load should be minimized.
--	5	NC	No Internal Connection.

9 Functional Block Diagram



10 Absolution Maximum Ratings

(Note 2)

- Supply Input Voltage, VIN ---------- 6V
- EN Input Voltage ---------- 6V
- Power Dissipation, P_D @ T_A = 25°C

  SOT-23-5 ---------- 0.4W

  WDFN-6L 2x2 ---------- 0.606W
- Package Thermal Resistance (Note 3)

  SOT-23-5, θ_{JA} ---------- 250°C/W

  WDFN-6L 2x2, θ_{JA} ---------- 165°C/W

  WDFN-6L 2x2, θ_{JC} ---------- 8.2°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3.θ_{JA} is measured at T_A = 25°C on a low effective thermal conductivity single-layer test board per JEDEC 51-3. θ_{JC} is measured at the exposed pad of the package

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VIN ---------- 2.2V to 5.5V
- Junction Temperature Range ---------- −40°C to 125°C
- Ambient Temperature Range ---------- −40°C to 85°C

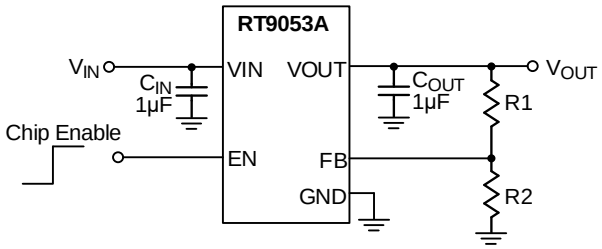
Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{IN} = 3.7V, C_{IN} = C_{OUT} = 1μF, I_{OUT} = 20mA, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
FB Voltage	V_{FB}		0.792	0.8	0.808	V
Output Voltage Accuracy	V_{OUT_ACC}	I_{OUT} = 10mA	−1	0	1	%
Quiescent Current	I_Q	I_{OUT} = 0mA	--	35	50	μA
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	0.7	1.5	μA
Current Limit	I_{LIM}	R_{LOAD} = 0Ω, 2.2V ≤ V_{IN} < 5.5V	400	650	1000	mA
Dropout Voltage	V_{DROP}	I_{OUT} = 400mA	--	230	350	mV
Load Regulation	V_{LOAD_REG}	1mA < I_{OUT} < 400mA 2.2V ≤ V_{IN} < 5.5V	--	--	1	%
Line Regulation	V_{LINE_REG}	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{OUT} = 1mA	--	0. 01	0.2	%/V
EN Input Voltage Rising Threshold	V_{EN_R}		1.6	--	5.5	V
EN Input Voltage Falling Threshold	V_{EN_F}		0	--	0.6	V
EN Input Current	I_{EN}		--	1	2	μA
FB Pin Current	I_{FB}		--	0.1	1	μA
Over-Temperature Protection Threshold	V_{OTP}		--	150	--	°C
Power Supply Rejection Ratio	PSRR	f = 1kHz, I_{OUT} = 10mA	--	−56	--	dB
		f = 10kHz, I_{OUT} = 10mA	--	−35	--	
Output Noise	V_n	V_{OUT} = 1.5V, C_{OUT} = 1μF, I_{OUT} = 0mA	--	30	--	μV_{RMS}

13 Typical Application Circuit



Note 6.

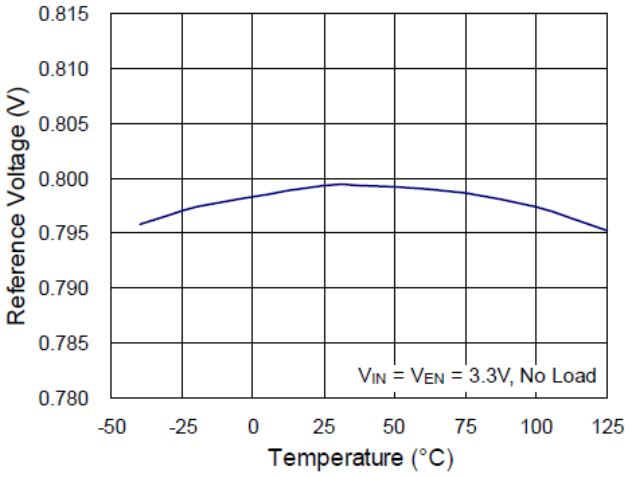
- For Stability Requirement, C_{OUT} must have a minimum value of 1µF for the RT9053A, and this capacitance must be maintained across the entire expected operating temperature range. It should also be located as close as possible to the regulator.
- All input and output capacitive parameters recommended here refer to effective capacitance. It is necessary to account for any derating effects, such as DC bias, when considering the effective capacitance.

Table 1. Recommended External Components

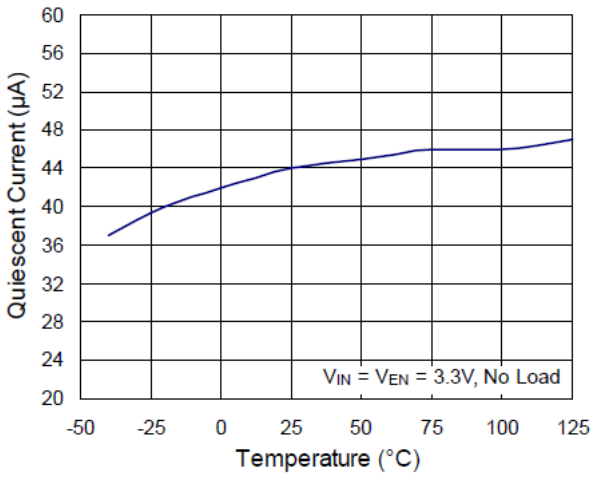
Component	Description	Vendor P/N
C_{IN}, C_{OUT}	1µF, 16V, X7R, 0603	GXT188R71C105KE13 (Murata)

14 Typical Operating Characteristics

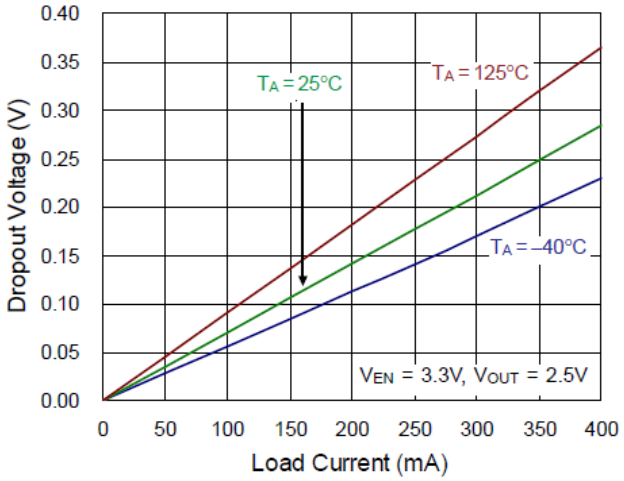
Reference Voltage vs. Temperature



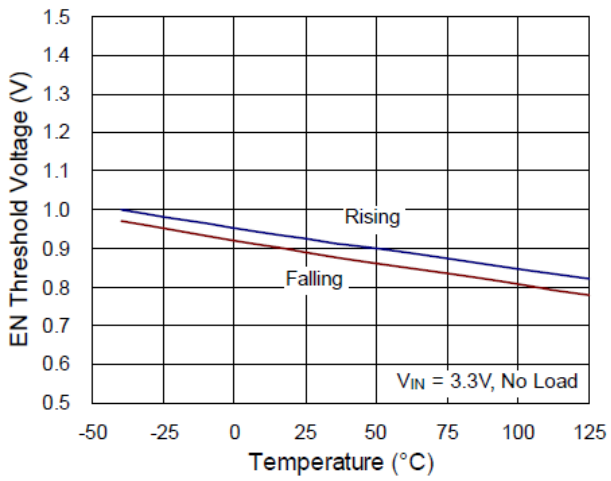
Quiescent Current vs. Temperature



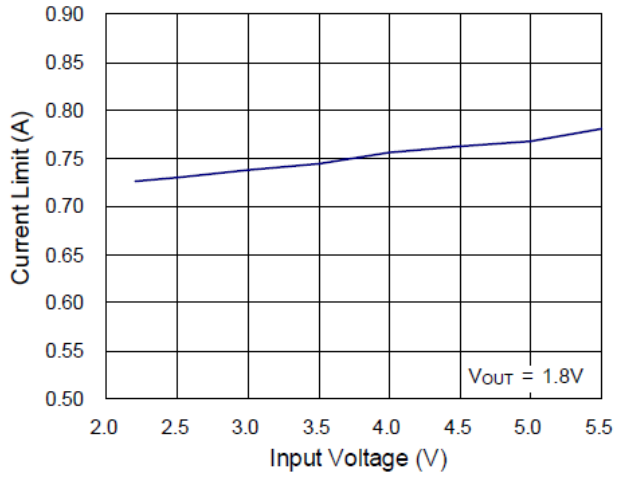
Dropout Voltage vs. Load Current



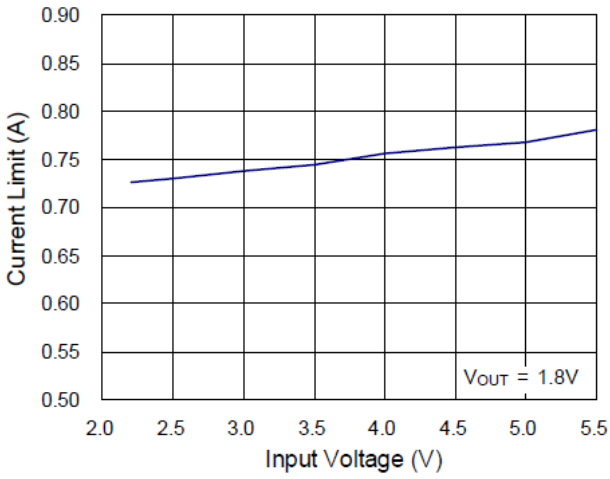
EN Threshold Voltage vs. Temperature



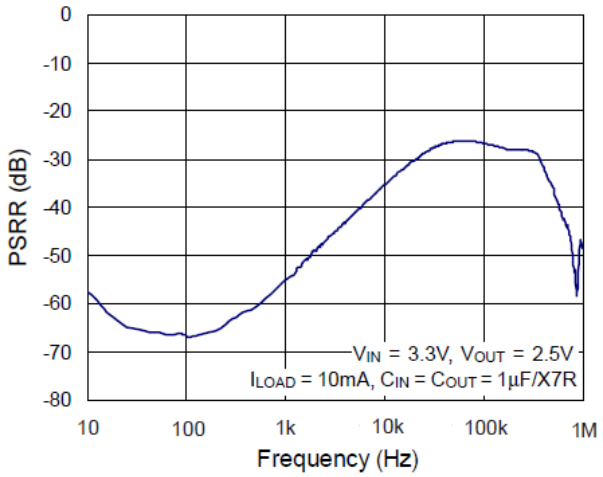
Current Limit vs. Input Voltage



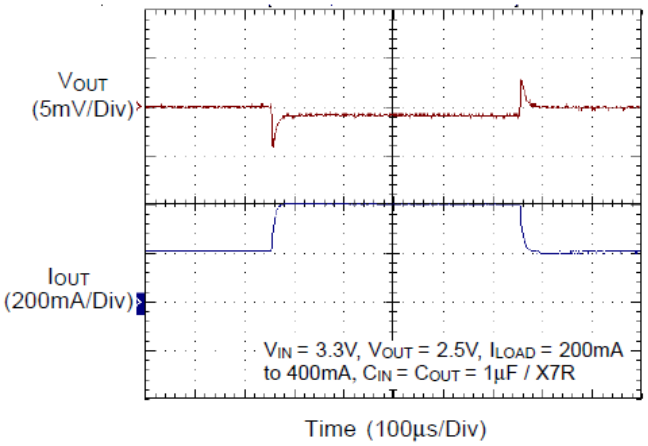
Current Limit vs. Input Voltage



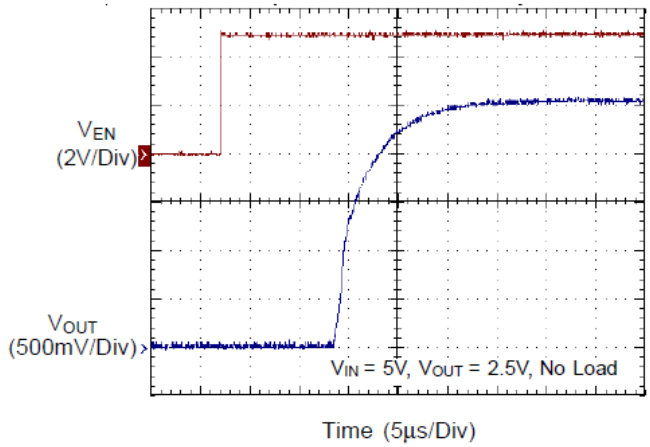
PSRR vs. Frequency



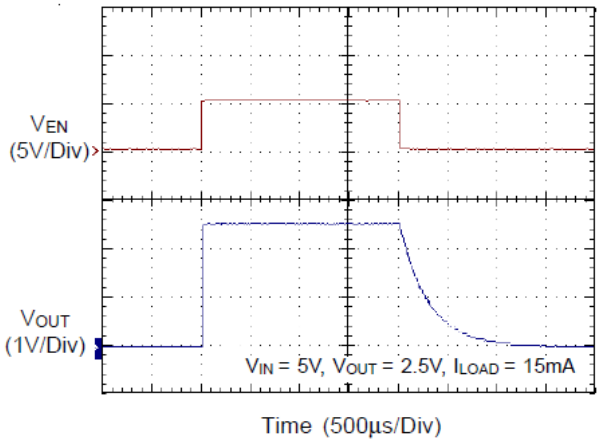
Load Transient Response



Power On from EN



Enable/Shutdown Response



15 Operation

The RT9053A is designed to operate with a single supply input ranging from 2.2V to 5.5V and is capable of delivering up to 0.4A of current to the output. The device features high PSRR (Power Supply Rejection Ratio) and low noise, ensuring a clean power supply for the application. It includes a low-noise reference and error amplifier to minimize the device's noise. The high PSRR of the RT9053A effectively minimizes the transfer of input supply noise to the output.

15.1 Enable and Shutdown

The RT9053A features an EN pin that serves as an external chip enable control, allowing the device to be enabled or disabled. When VEN is below 0.6V, the regulator turns off and initiates shutdown mode, while V_{EN} above 1.6V turns on the regulator. If the EN pin is not being utilized, it should be connected as close as possible to the largest input capacitance to prevent the enable circuit from being inadvertently triggered by voltage dips on the VIN line.

15.2 Current-Limit Protection

The RT9053A features a current-limit function to prevent damage during output overload or short-circuit conditions. The output current is monitored by an internal sensing transistor.

16 Application Information

(Note 7)

16.1 Input Capacitor Selection

Like any low-dropout linear regulator, the external capacitors used with the RT9053A must be carefully selected for stability and performance. It is recommended that the input capacitance be at least 1μF, and it may be increased without limitation. The input capacitor should be placed within a distance of less than 0.5 inch from the IC's input pin and connected to a clean ground plane. Any high-quality ceramic or tantalum capacitor can be used for the input capacitor. Using an input capacitor with a larger capacitance and lower ESR (Equivalent Series Resistance) can achieve better PSRR and line transient response.

16.2 Output Capacitor Selection

The RT9053A is specifically designed to work with a low ESR ceramic output capacitor to save board space and achieve better performance. The output capacitor should be at least 1μF. Using a larger capacitance can reduce noise and improve load transient response, the stability and PSRR. The RT9053A can operate with other types of output capacitors due to its wide range of stable operation. The output capacitor should be placed less than 0.5 inch from the VOUT pin and connected to a clean ground plane.

16.3 Output Voltage Setting

The output voltage divider R1 and R2 allow adjustment of the output voltage for various applications, as shown in Figure 1.

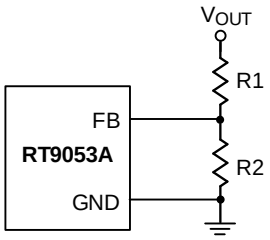


Figure 1. Output Voltage Setting

The output voltage is set according to the following equation:

$$V_{OUT} = V_{FB}\left(1+\frac{R1}{R2}\right)$$

where V_{FB} is the feedback reference voltage (0.8V, typically).

16.4 Enable Function

The RT9053A features enable/shutdown function. The voltage at the EN pin determines the enable/shutdown state of the regulator. To ensure the regulator will switch on, the enable control voltage must be greater than 1.6V. The regulator will enter shutdown mode when the voltage at the EN pin falls below 0.6V. If the enable function is not needed, the EN pin should be pulled high or simply tied to VIN to keep the regulator in an on state.

16.5 PSRR

The RT9053A features a high Power Supply Rejection Ratio (PSRR), which is defined as the ratio of output voltage change to input voltage change.

$$PSRR = 20 \times \log\left(\frac{\Delta V_{OUT}}{\Delta V_{IN}}\right)$$

A low dropout regulator with a higher PSRR can provide better line transient performance.

16.6 Current Limit

The RT9053A implements an independent current limit circuit, which monitors and controls the pass element's gate voltage to limit the output current at 650mA (typical). If the current limit condition lasts for a long time, the regulator temperature may increase high enough to damage the regulator itself. Therefore, the RT9053A implements current-limit function and thermal protection function to prevent the regulator from damage when the output is shorted to ground.

16.7 Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT9053A, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent.

For WDFN-6L 2x2 packages, the thermal resistance, θ_{JA}, is 165°C/W on a standard JEDEC 51-3 single-layer thermal test board.

For SOT-23-5 packages, the thermal resistance, θ_{JA}, is 250°C/W on a standard JEDEC 51-3 single-layer thermal test board.

The maximum power dissipation at T_A = 25°C can be calculated by the following formulas:

$P_{D(MAX)}$ = (125°C – 25°C) / (165°C/W) = 0.606W for WDFN-6L 2x2 package

$P_{D(MAX)}$ = (125°C – 25°C) / (250°C/W) = 0.400W for SOT-23-5 package

The thermal resistance θ_{JA} is determined by the package architecture design and the PCB layout design. However, the package architecture design had been already designed. If possible, it is useful to increase thermal performance by the PCB layout copper design. The thermal resistance θ_{JA} can be decreased by adding copper area under the exposed pad of WDFN series package.

As shown in Figure 2, we can find the relation between the copper area and the thermal resistance θ_{JA}. The thermal resistance will be reduced by adding more copper area. When the IC is mounted to the standard footprint, the thermal resistance θ_{JA} is 165°C/W. Adding copper area of pad to 15mm^2 under the package reduces the θ_{JA} to 150°C/W. Even further, increasing the copper area of pad to 70mm^2 reduces the θ_{JA} to 130°C/W.

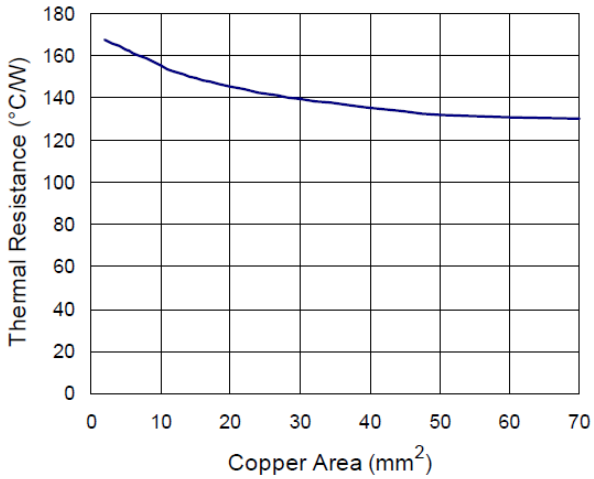


Figure 2. WDFN-6L 2x2 Thermal Resistance θ_{JA} vs. PCB Copper Area

As shown in Figure 3, we can also find the WDFN-6L 2x2 maximum power dissipation improvement by different copper area designs at ambient temperature T_A = 25°C operation.

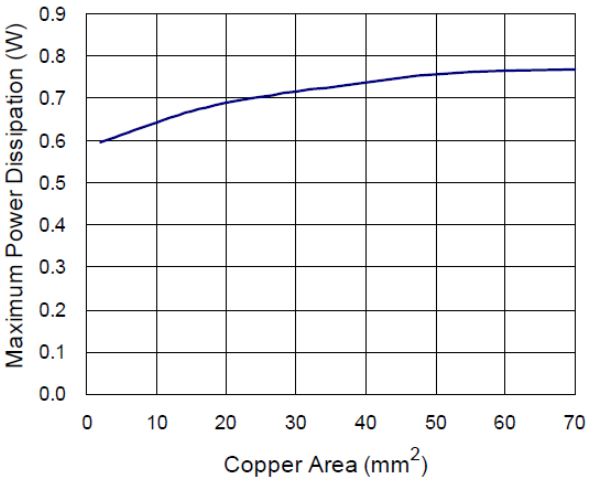


Figure 3. Maximum Power Dissipation PD vs. PCB Copper Area

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT9053A packages, the derating curves in Figure 4 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

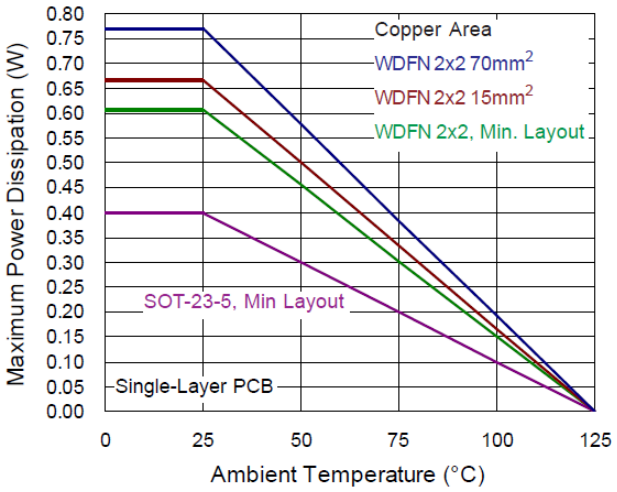
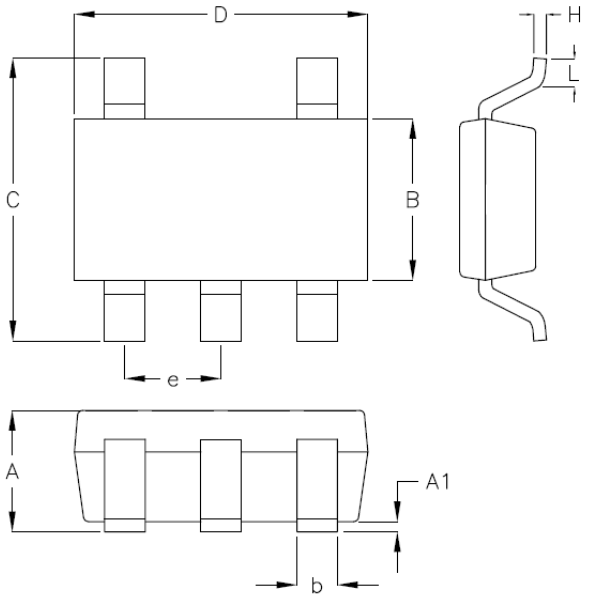


Figure 4. Derating Curves for RT9053A Packages

Note 7. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

17 Outline Dimension

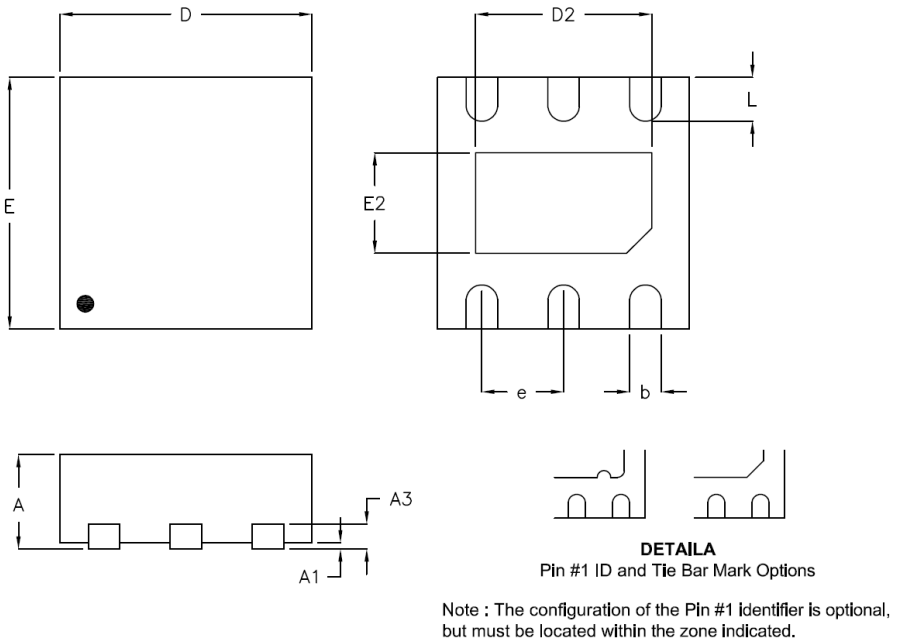
17.1 SOT-23-5 Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5 Surface Mount Package

17.2 WDFN-6L 2x2 Package

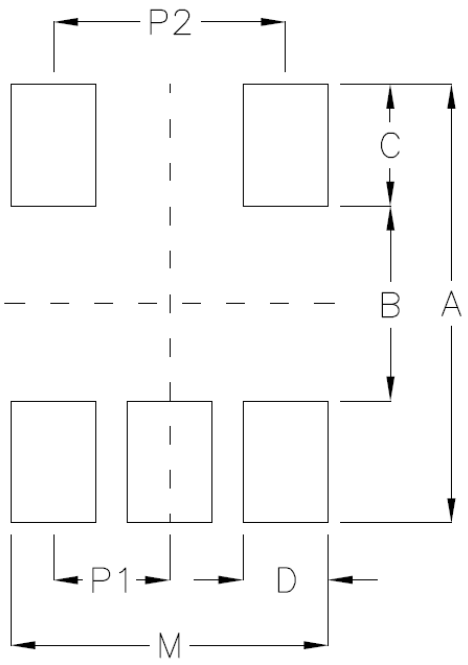


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.350	0.008	0.014
D	1.950	2.050	0.077	0.081
D2	1.000	1.450	0.039	0.057
E	1.950	2.050	0.077	0.081
E2	0.500	0.850	0.020	0.033
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

W-Type 6L DFN 2x2 Package

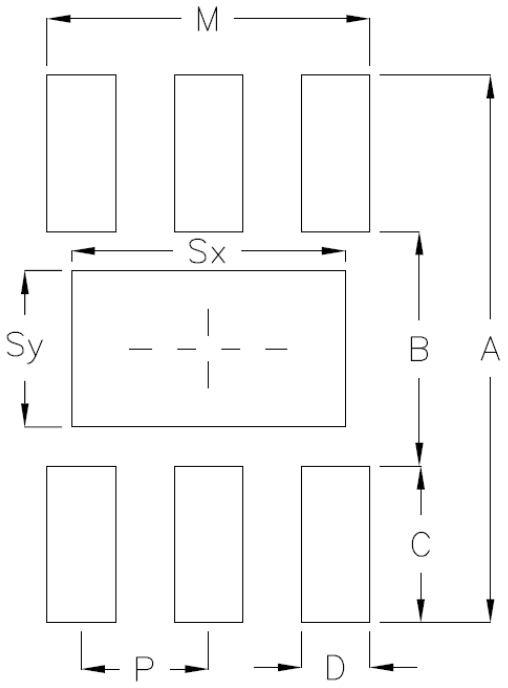
18 Footprint Information

18.1 SOT-23-5 Package



Package	Number of Pin	Footprint Dimension (mm)							Tolerance
		P1	P2	A	B	C	D	M	
TSOT-25/TSOT-25(FC)/SOT-25	5	0.95	1.90	3.60	1.60	1.00	0.70	2.60	±0.10

18.2 WDFN-6L 2x2 Package



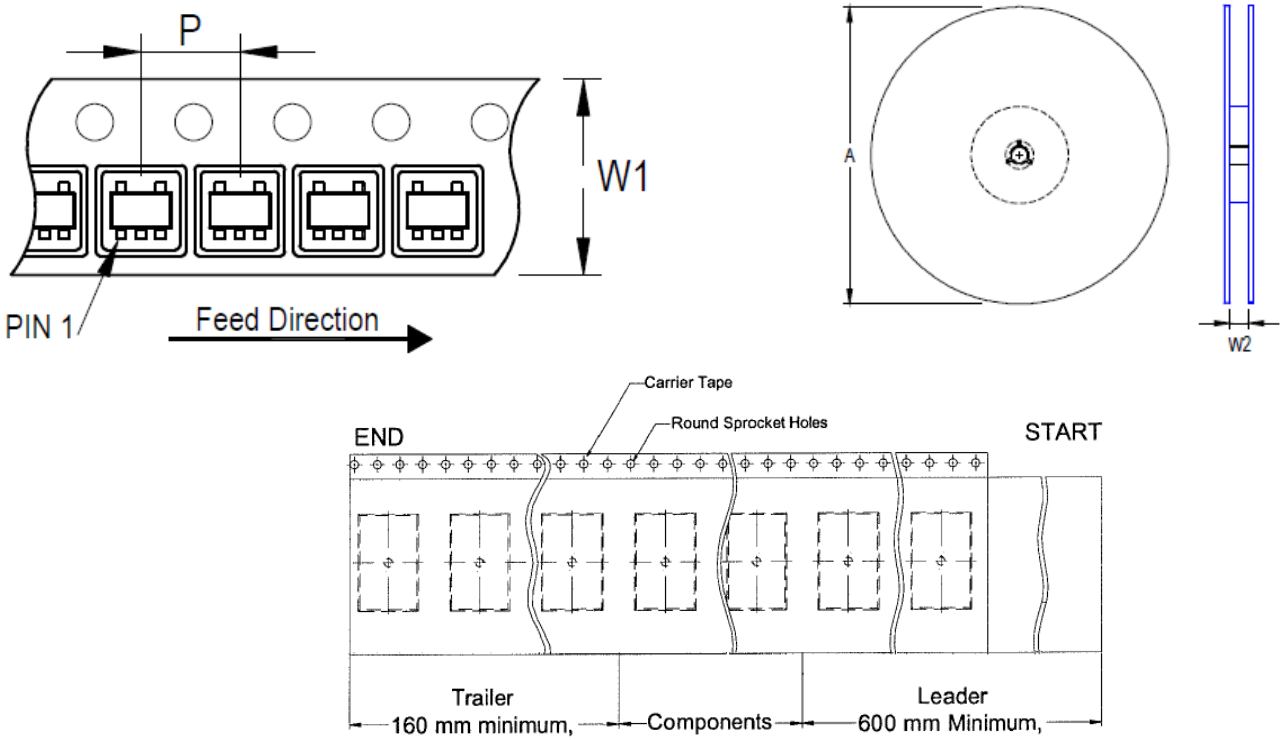
Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2*2-6	6	0.65	2.80	1.20	0.80	0.35	1.40	0.80	1.65	±0.05

19 Packing Information

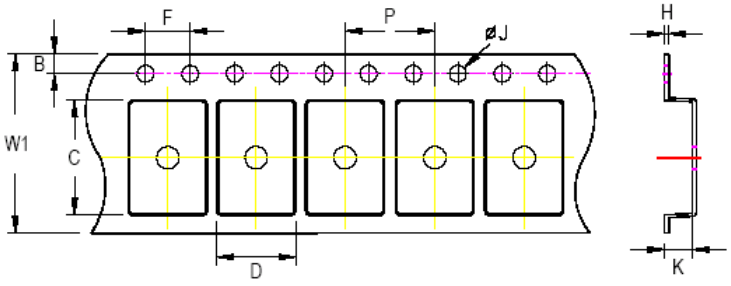
19.1 Tape and Reel Data

19.1.1 SOT-23-5 Package

SOT/TSOT-23-5



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
SOT-23-5	8	4	180	7	3,000	160	600	8.4/9.9

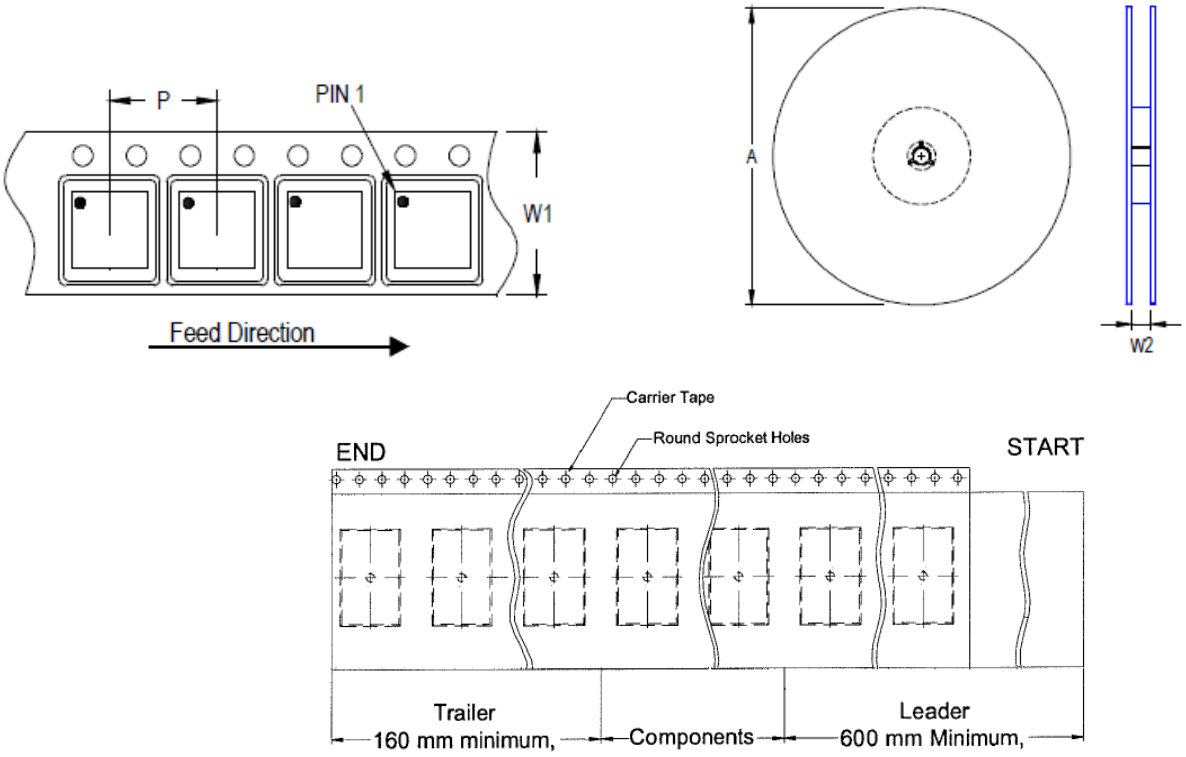


C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

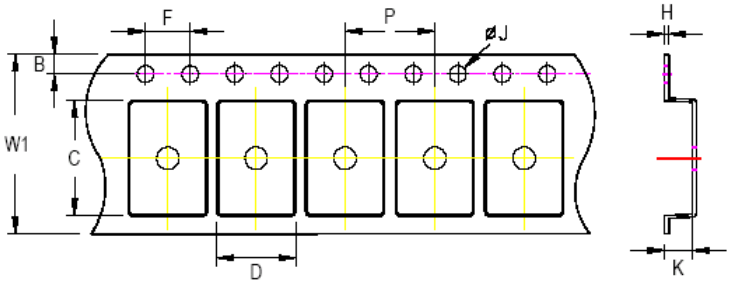
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.3mm	1.7mm	0.6mm

19.1.2 WDFN-6L 2x2 Package



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 2x2	8	4	180	7	2,500	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

19.2 Tape and Reel Packing

19.2.1 SOT-23-5 Package

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
SOT-23-5	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

19.2.2 WDFN-6L 2x2 Package

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 2x2	7”	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description	Item
04	2025/5/19	Modify	*General Description on page 1* *Features on page 1* *Simplified Application Circuit on page 1* *Ordering Information on page 1* *Marking Information on page 1* *Functional Pin Description on page 3* *Electrical Characteristics on page 5* *Typical Application Circuit on page 6* *Operation on page 9* - Added Operation *Application Information on page 10 to 13* *Footprint Information on page 16, 17* - Added Footprint Information *Packing Information on page 17 to 22* - Added packing information