3A, Ultra-Low Dropout Voltage Regulator

General Description
The RT9059 is a high performance positive voltage regulator designed for use in applications requiring very low input voltage and very low dropout voltage at up to 3A. It operates with a VIN as low as 1V and VDD voltage 3V with programmable output voltage as low as 0.8V. The RT9059 features ultra low dropout, ideal for applications where VOUT is very close to VIN. Additionally, it has an enable pin to further reduce power dissipation while shutdown. The RT9059 provides excellent regulation over variations in line, load and temperature. The RT9059 provides a power good signal to indicate if the voltage level of VO reaches 90% of its rating value.

Features
- Output Current up to 3A
- High Accuracy ADJ Voltage 1.5%
- Dropout Voltage 350mV @ 3A Typically
- VOUT Power Good Signal
- VOUT Pull Low Resistance when Disable
- Current Limiting Protection
- Thermal Shutdown Protection
- RoHS Compliant and Halogen Free

Applications
- Notebook PC Applications
- Motherboard Applications

Ordering Information
RT9059(-       )

Package Type
SP : SOP-8 (Exposed Pad-Option 1)
QW : WDFN-10L 3x3 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

None : Adjustable Output
Fixed Output Voltage Code
15 : 1.5V
18 : 1.8V
25 : 2.5V

Note :
Richtek products are :
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information
For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

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DS9059-10 February 2016 www.richtek.com
Typical Application Circuit

![Typical Application Circuit](image)

\[ V_{OUT} = 0.8 \times \frac{(R1+R2)}{R2} \]

Figure 1. Adjustable Voltage Regulator

Figure 2. Fixed Voltage Regulator

Functional Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Adjustable Output Voltage</td>
<td>Fixed Output Voltage</td>
<td>Adjustable Output Voltage</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>6</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>7, 8, 9</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>10</td>
</tr>
<tr>
<td>5</td>
<td>5, 7</td>
<td>--</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>1, 2, 3</td>
</tr>
<tr>
<td>7</td>
<td>--</td>
<td>4</td>
</tr>
<tr>
<td>8, 9 (Exposed Pad)</td>
<td>8, 9 (Exposed Pad)</td>
<td>11</td>
</tr>
</tbody>
</table>
Functional Block Diagram

- EN
- VDD
- VIN
- VOUT
- ADJ
- GND
- PGoods
- RSENSE
- 150Ω
- EA
- MOS Driver
- Thermal Protection
- Soft-Start
- DELAY
- Comparator
- VREF
- UVLO
- OCP
- DE%

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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN to GND
  DC: -0.3V to 6V
  < 10ms: -0.3V to 7V
- Control Voltage, VDD to GND
  DC: -0.3V to 6V
  < 10ms: -0.3V to 7V
- Output Voltage, VOUT
- Chip Enable Voltage, EN
- Adjust Voltage, ADJ
- Power Good Voltage, VPGOOD
- Power Dissipation, PD @ T_A = 25°C
  SOP-8 (Exposed Pad): 2.96W
  WDFN-10L 3x3: 2.95W
- Package Thermal Resistance (Note 2)
  SOP-8 (Exposed Pad), \( \theta_{JA} \): 33.7°C/W
  SOP-8 (Exposed Pad), \( \theta_{JC} \): 5.4°C/W
  WDFN-10L 3x3, \( \theta_{JA} \): 33.8°C/W
  WDFN-10L 3x3, \( \theta_{JC} \): 8.9°C/W
- Junction Temperature: 150°C
- Lead Temperature (Soldering, 10 sec.): 260°C
- Storage Temperature Range: -65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model): 2kV
  MM (Machine Model): 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN: 1V to 5.5V
- Control Voltage, VDD: 3V to 5.5V
- Junction Temperature Range: -40°C to 125°C
- Ambient Temperature Range: -40°C to 85°C

Electrical Characteristics

\( V_{DD} = 5V, C_{IN} = C_{OUT} = 10\mu F, C_{VDD} = 1\mu F, T_A = 25°C, \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD Operation Range</td>
<td>( V_{DD} )</td>
<td></td>
<td>3</td>
<td>--</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>VDD POR Threshold</td>
<td>( V_{POR_VDD} )</td>
<td>( V_{DD} ) Rising</td>
<td>2.4</td>
<td>2.7</td>
<td>3</td>
<td>V</td>
</tr>
<tr>
<td>VDD POR Falling Hysteresis</td>
<td>( \Delta V_{POR_VDD} )</td>
<td>( V_{DD} ) Falling</td>
<td>0.15</td>
<td>0.2</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>( V_{IN} )</td>
<td></td>
<td>1</td>
<td>--</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>VIN POR Threshold</td>
<td>( V_{POR_VIN} )</td>
<td>( V_{IN} ) Rising</td>
<td>0.7</td>
<td>0.8</td>
<td>0.9</td>
<td>V</td>
</tr>
<tr>
<td>VIN POR Falling Hysteresis</td>
<td>( \Delta V_{POR_VIN} )</td>
<td>( V_{IN} ) Falling</td>
<td>0.15</td>
<td>0.2</td>
<td>0.25</td>
<td>V</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>( I_Q )</td>
<td>( \text{EN On, No Load} )</td>
<td>--</td>
<td>0.6</td>
<td>1.2</td>
<td>mA</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Conditions</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>---------------------------------</td>
<td>--------------</td>
<td>----------------------------------------------------------------------------------</td>
<td>------</td>
<td>------</td>
<td>------</td>
<td>------</td>
</tr>
<tr>
<td>Reference Voltage</td>
<td>$V_{\text{REF}}$</td>
<td></td>
<td>0.788</td>
<td>0.8</td>
<td>0.812</td>
<td>V</td>
</tr>
<tr>
<td>Fixed Output Voltage Accuracy</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOUT Load Regulation</td>
<td>$\Delta V_{\text{LOAD}}$</td>
<td>$I_{\text{OUT}} = 1\text{mA to } 3\text{A, } V_{\text{IN}} = V_{\text{OUT}+1\text{V}}$</td>
<td>--</td>
<td>0.5</td>
<td>1</td>
<td>%</td>
</tr>
<tr>
<td>OUT Line Regulation</td>
<td>$\Delta V_{\text{LINE}}$</td>
<td>$V_{\text{DD}} = 3.6\text{V to } 5.5\text{V, } V_{\text{IN}} = V_{\text{OUT}+1\text{V}}$ to $5\text{V, } I_{\text{OUT}} = 1\text{mA}$</td>
<td>--</td>
<td>0.2</td>
<td>0.6</td>
<td>%</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>$V_{\text{DROP}}$</td>
<td>$I_{\text{OUT}} = 2\text{A}$</td>
<td>--</td>
<td>250</td>
<td>350</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{\text{OUT}} = 3\text{A}$</td>
<td>--</td>
<td>350</td>
<td>450</td>
<td>mV</td>
</tr>
<tr>
<td>Current Limit</td>
<td>$I_{\text{LIM}}$</td>
<td>$V_{\text{IN}} = 3.6\text{V}$</td>
<td>3.1</td>
<td>3.6</td>
<td>4.2</td>
<td>A</td>
</tr>
<tr>
<td>Short Circuit Current</td>
<td>$I_{\text{SC}}$</td>
<td>$V_{\text{OUT}} &lt; 0.2\text{V}$</td>
<td>1</td>
<td>1.4</td>
<td>1.8</td>
<td>A</td>
</tr>
<tr>
<td>VOUT Pull Low Resistance</td>
<td>$R_{\text{PULL}}$</td>
<td>$V_{\text{EN}} = 0\text{V}$</td>
<td>--</td>
<td>150</td>
<td>--</td>
<td>Ω</td>
</tr>
<tr>
<td>Thermal Shutdown Temperature</td>
<td>$T_{\text{SD}}$</td>
<td></td>
<td>--</td>
<td>160</td>
<td>--</td>
<td>°C</td>
</tr>
<tr>
<td>Thermal Shutdown Recovery</td>
<td>$T_{\text{SDR}}$</td>
<td></td>
<td>--</td>
<td>90</td>
<td>--</td>
<td>°C</td>
</tr>
<tr>
<td>PGOOD Rising Threshold</td>
<td>$V_{\text{TH_PGOOD}}$</td>
<td>$V_{\text{OUT}}$ Rising</td>
<td>--</td>
<td>90</td>
<td>--</td>
<td>%</td>
</tr>
<tr>
<td>PGOOD Hysteresis</td>
<td>$\Delta V_{\text{TH_PGOOD}}$</td>
<td>$V_{\text{OUT}}$ Falling</td>
<td>--</td>
<td>10</td>
<td>--</td>
<td>%</td>
</tr>
<tr>
<td>PGOOD Delay Time</td>
<td></td>
<td></td>
<td>--</td>
<td>1</td>
<td>1.5</td>
<td>ms</td>
</tr>
<tr>
<td>PGOOD Sink Capability</td>
<td>$V_{\text{PGOOD}}$</td>
<td>$I_{\text{SINK}} = 10\text{mA}$</td>
<td>--</td>
<td>0.2</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>EN Input Voltage</td>
<td>Logic-High $V_{\text{IH}}$</td>
<td></td>
<td>1.2</td>
<td>--</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Logic-Low $V_{\text{IL}}$</td>
<td></td>
<td>--</td>
<td>--</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>EN Delay Time</td>
<td></td>
<td></td>
<td>0.3</td>
<td>0.85</td>
<td>1.4</td>
<td>ms</td>
</tr>
<tr>
<td>EN Pin Bias Current</td>
<td>$I_{\text{EN}}$</td>
<td>$V_{\text{EN}} = 5\text{V}$</td>
<td>--</td>
<td>12</td>
<td>--</td>
<td>μA</td>
</tr>
<tr>
<td>VDD Pin Shutdown Current</td>
<td>$I_{\text{SHDN_VDD}}$</td>
<td>$V_{\text{EN}} = 0\text{V}$</td>
<td>--</td>
<td>--</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td>VIN Pin Shutdown Current</td>
<td>$I_{\text{SHDN_VIN}}$</td>
<td>$V_{\text{EN}} = 0\text{V, } V_{\text{IN}} = 5\text{V}$</td>
<td>--</td>
<td>--</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td>Inrush Current</td>
<td>$I_{\text{INRUSH}}$</td>
<td>$V_{\text{OUT}} = 1.8\text{V, } C_{\text{OUT}} = 10\mu\text{F, } I_{\text{LOAD}} = 1\text{A}$</td>
<td>--</td>
<td>0.5</td>
<td>--</td>
<td>A</td>
</tr>
<tr>
<td>Soft-Start Time</td>
<td>$I_{\text{SS}}$</td>
<td></td>
<td>1.9</td>
<td>2.8</td>
<td>3.75</td>
<td>ms</td>
</tr>
</tbody>
</table>

**Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** $\theta_{\text{JA}}$ is measured at $T_{\text{A}} = 25^\circ\text{C}$ on a high effective thermal conductivity four-layer test board per JEDEC 51-7. $\theta_{\text{JC}}$ is measured at the exposed pad of the package.

**Note 3.** Devices are ESD sensitive. Handling precaution recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.
Typical Operating Characteristics

1. **Quiescent Current vs. Temperature**
   - Graph showing quiescent current (mA) versus temperature (°C)
   - $V_{DD} = 5V, V_{IN} = 3V$

2. **Current Limit vs. Temperature**
   - Graph showing current limit (A) versus temperature (°C)
   - $V_{DD} = 5V, V_{IN} = 3V$

3. **EN Threshold Voltage vs. Temperature**
   - Graph showing EN voltage (V) versus temperature (°C)
   - Rising and Falling curves

4. **Current Limit vs. Temperature**
   - Graph showing current limit (A) versus temperature (°C)
   - $V_{DD} = 5V, V_{IN} = 3V$

5. **VREF Voltage vs. Temperature**
   - Graph showing VREF voltage (V) versus temperature (°C)
   - $V_{DD} = 5V, V_{IN} = 3V$

6. **PGOOD Delay Time vs. Temperature**
   - Graph showing PGOOD delay time (µs) versus temperature (°C)
   - $V_{DD} = 5V, V_{IN} = 2V$

7. **EN Threshold Voltage vs. Temperature**
   - Graph showing EN voltage (V) versus temperature (°C)
   - Rising and Falling curves

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VDD POR Threshold Voltage vs. Temperature

VDD Voltage (V) vs. Temperature (°C)

- Rising
- Falling

PSRR vs. Frequency

PSRR (dB) vs. Frequency (Hz)

VIN Line Transient Response

VIN (1V/Div)

VDD = 5V, COUT = 10μF

VOUT (20mV/Div)

Time (200μs/Div)

VIN = 2.2V, VDD = 5V
VOUT = 1.2V, COUT = 10μF

Load Transient Response

IOUT (1A/Div)

Time (1ms/Div)

VDD Line Transient Response

VDD (1V/Div)

VIN = 2V, COUT = 10μF

VOUT (20mV/Div)

Time (200μs/Div)

Dropout Voltage vs. Load Current

Dropout Voltage (mV) vs. Load Current (A)

VDD POR Threshold Voltage vs. Temperature

VDD Voltage (V) vs. Temperature (°C)

- Rising
- Falling

PSRR vs. Frequency

PSRR (dB) vs. Frequency (Hz)

VIN Line Transient Response

VIN (1V/Div)

VDD = 5V, COUT = 10μF

VOUT (20mV/Div)

Time (200μs/Div)

VIN = 2.2V, VDD = 5V
VOUT = 1.2V, COUT = 10μF

Load Transient Response

IOUT (1A/Div)

Time (1ms/Div)

VDD Line Transient Response

VDD (1V/Div)

VIN = 2V, COUT = 10μF

VOUT (20mV/Div)

Time (200μs/Div)
**Start Up from V\text{DD}**

- **V\text{DD}**: 2V/div
- **PGOOD**: 1V/div
- **V\text{OUT}**: 1V/div

Time (2ms/Div)

VIN = 3V, I\text{OUT} = 0A, C\text{OUT} = 10\mu F

**Start Up from V\text{IN}**

- **V\text{IN}**: 1V/div
- **PGOOD**: 1V/div
- **V\text{OUT}**: 1V/div

Time (2ms/Div)

V\text{DD} = 5V, I\text{OUT} = 0A, C\text{OUT} = 10\mu F

**Start Up from Enable and PGOOD Delay**

- **EN**: 2V/div
- **PGOOD**: 1V/div
- **V\text{OUT}**: 1V/div
- **I\text{OUT}**: 1A/div

Time (1ms/Div)

VIN = 3V, V\text{DD} = 5V, I\text{OUT} = 1.5A, C\text{OUT} = 10\mu F
Applications Information

Adjustable Mode Operation
The output voltage of RT9059 is adjustable from 0.8V to VIN by external voltage divider resistors as shown in Typical Application Circuit (Figure 1). The value of resistors R1 and R2 should be more than 10kΩ to reduce the power loss. The output voltage can be calculated by the following equation:

\[ V_{OUT} = V_{REF} \times \left( 1 + \frac{R1}{R2} \right) \]

where \( V_{REF} \) is the reference voltage (0.8V typical).

Enable
The RT9059 goes into shutdown mode when the EN pin is in the logic low condition. During this condition, the pass transistor, error amplifier, and band gap are turned off, reducing the supply current to 1\( \mu \text{A} \) typical. The RT9059 goes into operation mode when the EN pin is in the logic high condition. If the EN pin is floating, please notice the RT9059 internal initial logic level. For RT9059, the EN pin function pulls low level internally. So the regulator will be turned off when EN pin is floating.

Input Capacitor
Good bypassing is recommended from input to ground to improve AC performance. A 10\( \mu \text{F} \) input capacitor or greater located as close as possible to the IC is recommended.

Output Capacitor
The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The RT9059 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor which value is at least 10\( \mu \text{F} \) on the RT9059 output ensures stability. The RT9059 still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the RT9059 and returned to a clean analog ground.

Current Limit
The RT9059 contains an independent current limit and the short circuit current protection to prevent unexpected applications. The current limit monitors and controls the pass transistor's gate voltage, minimum limiting the output current to 3.1A typical. When the output voltage is less than 0.2V, the short circuit current protection starts the current fold back function and maintains the loading current at maximum 1.8A. The output can be shorted to ground indefinitely without damaging the part.

Power Good
The power good function is an open-drain output. Connect 100kΩ pull up resistor to VOUT to obtain an output voltage. The PGOOD pin will output high immediately after the output voltage arrives 90% of normal output voltage.

Thermal Shutdown Protection
Thermal protection limits power dissipation to prevent IC over temperature in RT9059. When the operation junction temperature exceeds 160°C, the over temperature protection circuit starts the thermal shutdown function and turns the pass transistor off. The pass transistor turns on again after the junction temperature cools by 70°C.

Thermal Considerations
For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

\[ P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A})}{\theta_{JA}} \]

where \( T_{J(MAX)} \) is the maximum junction temperature, \( T_{A} \) is the ambient temperature, and \( \theta_{JA} \) is the junction to ambient thermal resistance.
For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, $\theta_{JA}$, is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance, $\theta_{JA}$, is 33.7°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WDFN-10L 3x3 package, the thermal resistance, $\theta_{JA}$, is 33.8°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at $T_A = 25^\circ$C can be calculated by the following formula:

$$P_{D(MAX)} = \frac{(125^\circ\text{C} - 25^\circ\text{C})}{(33.7^\circ\text{C/W})} = 2.96\text{W} \text{ for SOP-8 (Exposed Pad) package}$$

$$P_{D(MAX)} = \frac{(125^\circ\text{C} - 25^\circ\text{C})}{(33.8^\circ\text{C/W})} = 2.95\text{W} \text{ for WDFN-10L 3x3 package}$$

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, $\theta_{JA}$. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

![Figure 3. Derating Curve of Maximum Power Dissipation](image)
Outline Dimension

8-Lead SOP (Exposed Pad) Plastic Package

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Dimensions In Millimeters</th>
<th>Dimensions In Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>4.801 - 5.004</td>
<td>0.189 - 0.197</td>
</tr>
<tr>
<td>B</td>
<td>3.810 - 4.000</td>
<td>0.150 - 0.157</td>
</tr>
<tr>
<td>C</td>
<td>1.346 - 1.753</td>
<td>0.053 - 0.069</td>
</tr>
<tr>
<td>D</td>
<td>0.330 - 0.510</td>
<td>0.013 - 0.020</td>
</tr>
<tr>
<td>F</td>
<td>1.194 - 1.346</td>
<td>0.047 - 0.053</td>
</tr>
<tr>
<td>H</td>
<td>0.170 - 0.254</td>
<td>0.007 - 0.010</td>
</tr>
<tr>
<td>I</td>
<td>0.000 - 0.152</td>
<td>0.000 - 0.006</td>
</tr>
<tr>
<td>J</td>
<td>5.791 - 6.200</td>
<td>0.228 - 0.244</td>
</tr>
<tr>
<td>M</td>
<td>0.406 - 1.270</td>
<td>0.016 - 0.050</td>
</tr>
<tr>
<td>Option 1</td>
<td>X 2.000 - 2.300</td>
<td>0.079 - 0.091</td>
</tr>
<tr>
<td></td>
<td>Y 2.000 - 2.300</td>
<td>0.079 - 0.091</td>
</tr>
<tr>
<td>Option 2</td>
<td>X 2.100 - 2.500</td>
<td>0.083 - 0.098</td>
</tr>
<tr>
<td></td>
<td>Y 3.000 - 3.500</td>
<td>0.118 - 0.138</td>
</tr>
</tbody>
</table>
Note: The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Dimensions In Millimeters</th>
<th>Dimensions In Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>A</td>
<td>0.700</td>
<td>0.800</td>
</tr>
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W-Type 10L DFN 3x3 Package

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