RICHTEK®

RT9078

2μA I_Q, 300mA Low-Dropout Linear Regulator

1 General Description

The RT9078 series is a low-dropout (LDO) voltage regulator with an enable function that operates from a 1.2V to 5.5V supply. It provides up to 300mA of output current in miniaturized packaging.

The device features a 2μA low quiescent current and 0.5μA shutdown current, making it ideal for battery-powered applications requiring extended service life. Additional features include a current limit function, over-temperature protection, and output discharge function.

The recommended junction temperature range is –40°C to 125°C.

2 Ordering Information

RT9078-□□□□□

Pin 1 Orientation
Empty: Quadrant 1
(2): Quadrant 2, Follow EIA-481
(For ZQFN-4L 1x1 only)

Package Type(1)
J5: TSOT-23-5
QZ: ZQFN-4L 1x1 (Z-Type)
(ZDFN-4L 1x1)

Lead Plating System
G: Richtek Green Policy Compliant(2)

Output Voltage
08 : 0.8V
:
18 : 1.8V
20 : 2.0V
:
33 : 3.3V
1B : 1.25V
1H : 1.85V
2H : 2.85V
1K : 1.05V
3D : 3.45V (ZQFN-4L 1x1 only)
Special Request: Any voltage between 0.8V and 3.3V under specific business agreement

Pin Function
RT9078: Without SNS Pin
RT9078N: With SNS Pin(3)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.
- Marked with (3) indicated: Available for output target adjustment (For example: The RT9078N-08GJ5 with 0.8V reference level for output target adjustment)

3 Features

- **Input Voltage Range: 1.2V to 5.5V**
- **2μA Ground Current (I_Q) at no Load**
- **PSRR = 75dB at 1kHz**
- **Adjustable Output Voltage Range:**
  - **0.8V to 5V (TSOT-23-5 Package with SNS Pin Only)**
- **±2% Output Accuracy**
- **Low (0.1μA) Shutdown Current**
- **Dropout Voltage: 0.15V at 300mA when V_{OUT} ≥ 3V**
- **Support Fixed Output Voltage: 0.8V, 1.0V, 1.05V, 1.1V, 1.2V, 1.25V, 1.3V, 1.5V, 1.8V, 1.85V, 1.9V, 2V, 2.5V, 2.8V, 2.85V, 3V, 3.1V, 3.3V, 3.45V**
- **Current-Limit Protection**
- **Over-Temperature Protection**
- **Output Active Discharge Function**
- **Available in TSOT-23-5 and ZQFN-4L 1x1 (ZDFN-4L 1x1) Packages**

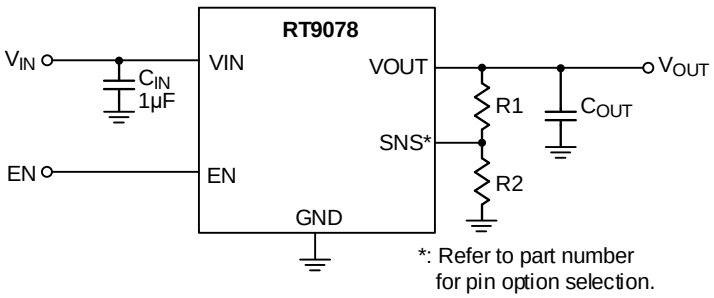
4 Applications

- Portable, Battery Powered Equipment
- Ultra Low Power Microcontrollers
- Notebook Computers

5 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

6 Simplified Application Circuit



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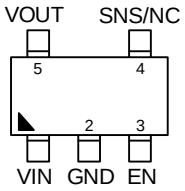
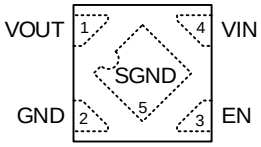
7 Pin Configuration

(TOP VIEW)



TSOT-23-5

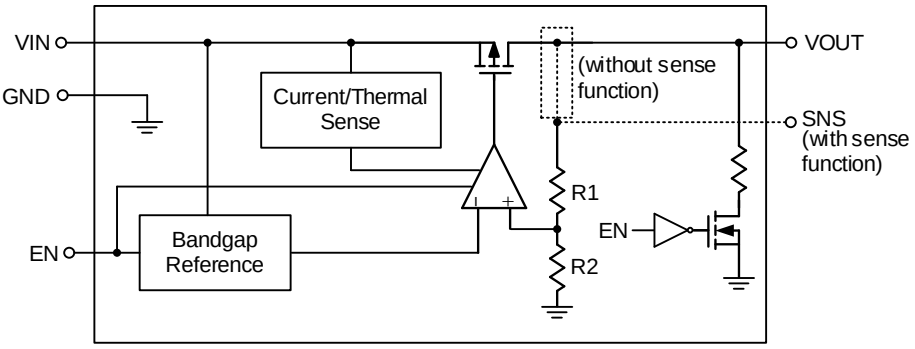


ZQFN-4L 1x1 (ZDFN-4L 1x1)

8 Functional Pin Description

Pin No.		Pin Name	Pin Function
TSOT-23-5	ZQFN-4L 1x1 (ZDFN-4L 1x1)		
1	4	VIN	Supply input. A general 1μF ceramic capacitor should be placed as close as possible to this pin to improve noise suppression.
2	2	GND	Ground. The exposed pad must be soldered to a large PCB area and connected to GND to optimize power dissipation.
3	3	EN	Enable control input. Connecting this pin to a logic high signal enables the regulator. Pulling this pin below 0.4V turns the regulator off, significantly reducing the quiescent current to a fraction of its operating value.
4	--	SNS	Output voltage sense pin for the RT9078N only. This pin sets the desired output voltage using an external resistive divider. The typical voltage at the SNS pin is 0.8V.
		NC	No internal connection. These pins can be left unconnected without affecting device functionality. Alternatively, connecting these pins to GND can help increase the GND copper coverage on the PCB top layer, which may improve heat dissipation through conduction.
5	1	VOUT	LDO output pins. A 1μF or larger ceramic capacitor (0.7μF or greater effective capacitance) is required for stability. Place the output capacitor as close to the device as possible and minimize the impedance between the VOUT pin and the load.
--	5 (Exposed Pad)	SGND	Substrate of chip. Connect to the GND plane to enhance thermal dissipation.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VIN, VOUT, SNS, EN to GND ---------- –0.3V to 6.5V
- VOUT to VIN ---------- –6.5V to 0.3V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility
  HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Input Voltage, VIN ---------- 1.2V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		TSOT-23-5	ZQFN-4L 1x1 (ZDFN-4L 1x1)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	189.4	291.4	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	75.9	163	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	55.8	90.7	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	100.7	236	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	21.6	52.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	67.2	189.1	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(Top)}$, and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

(V_{OUT} + 1 < V_{IN} < 5.5V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OUT}		0.8	--	3.45	V
Output Voltage Accuracy	V_{OUT_ACC}	I_{LOAD} = 1mA	–2	--	2	%
Reference Voltage (For RT9078N-08GJ5 Only)	V_{REF}	I_{LOAD} = 1mA	0.784	0.8	0.816	V
Dropout Voltage (Note 7)	V_{DROP}	0.8V ≤ V_{OUT} < 1.05V, I_{LOAD} = 300mA	--	0.7	0.97	V
		1.05V ≤ V_{OUT} < 1.2V, I_{LOAD} = 300mA	--	0.5	0.92	
		1.2V ≤ V_{OUT} < 1.5V, I_{LOAD} = 300mA	--	0.4	0.57	
		1.5V ≤ V_{OUT} < 1.8V, I_{LOAD} = 300mA	--	0.3	0.47	
		1.8V ≤ V_{OUT} < 2.1V, I_{LOAD} = 300mA	--	0.24	0.33	
		2.1V ≤ V_{OUT} < 2.5V, I_{LOAD} = 300mA	--	0.21	0.3	
		2.5V ≤ V_{OUT} < 2.8V, I_{LOAD} = 300mA	--	0.18	0.25	
		2.8V ≤ V_{OUT} < 3V, I_{LOAD} = 300mA	--	0.16	0.23	
		3V ≤ V_{OUT}, I_{LOAD} = 300mA	--	0.15	0.2	
Dropout Voltage (Note 8)	V_{DROP}	1.8V ≤ V_{OUT} < 2.1V, I_{LOAD} = 200mA	--	0.16	0.2	V
Quiescent Current	I_Q	I_{LOAD} = 0mA, V_{OUT} ≤ 5.5V V_{IN} ≥ V_{OUT} + V_{DROP}	--	2	4	µA
Shutdown Current (Note 9)	I_{SHDN}	V_{EN} = 0V	--	0.1	0.5	µA
		V_{EN} = 0V, V_{OUT} = 0V	--	0.1	0.5	µA
EN Input Current	I_{EN}	V_{EN} = 5.5V	--	--	0.1	µA
Line Regulation	V_{LINE_REG}	I_{LOAD} = 1mA, 1.2V ≤ V_{IN} < 1.5V	--	0.3	0.6	%
		I_{LOAD} = 1mA, 1.5V ≤ V_{IN} < 1.8V	--	0.15	0.3	
		I_{LOAD} = 1mA, 1.8V ≤ V_{IN} ≤ 5.5V	--	0.13	0.35	
Load Regulation	V_{LOAD_REG}	1mA < I_{LOAD} < 300mA	--	0.5	1	%
Power Supply Rejection Ratio	PSRR	V_{IN} = 3V, I_{LOAD} = 50mA, C_{OUT} = 1µF, V_{OUT} = 2.5V, f = 1kHz	--	75	--	dB
Output Voltage Noise	V_n	C_{OUT} = 1µF, I_{LOAD} = 150mA, BW = 10Hz to 100kHz, V_{IN} = V_{OUT} + 1V, V_{OUT} = 0.8V	--	38	--	µVRMS
		V_{OUT} = 1.2V	--	46	--	
		V_{OUT} = 1.8V	--	48	--	
		V_{OUT} = 3.3V	--	51	--	
Current Limit	I_{LIM}	V_{OUT} = 90% of $V_{OUT\ (NOM)}$	350	600	--	mA
EN Input Voltage Rising Threshold	V_{EN_R}	V_{IN} = 5V	0.5	0.7	0.9	V
EN Input Voltage Falling Threshold	V_{EN_F}	V_{IN} = 5V	0.4	0.65	0.85	
Over-Temperature Protection Threshold	T_{OTP}	I_{LOAD} = 30mA, V_{IN} ≥ 1.5V	--	150	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C
Discharge Resistor	R_{DISCHG}	EN = 0V, V_{OUT} = 0.1V	--	80	--	Ω

Note 7. The dropout voltage is defined as $V_{IN} - V_{OUT}$, when V_{OUT} is 98% of the normal value of V_{OUT}.

Note 8. For the application under the following condition $1.8V \leq V_{OUT} < 2.1V$, $I_{LOAD} = 200mA$, $T_A = 85°C$, the maximum dropout voltage is guaranteed by design to not exceed 0.28V.

Note 9. The specification is tested at wafer stage and guaranteed by design after assembly.

15 Typical Application Circuit

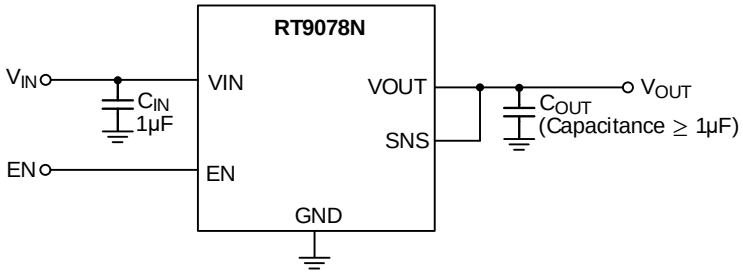


Figure 1. Application with Sense Function

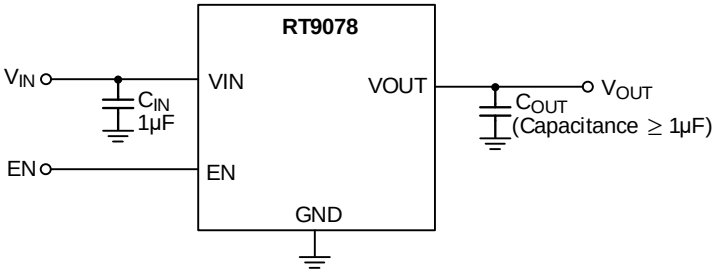


Figure 2. Application without Sense Function

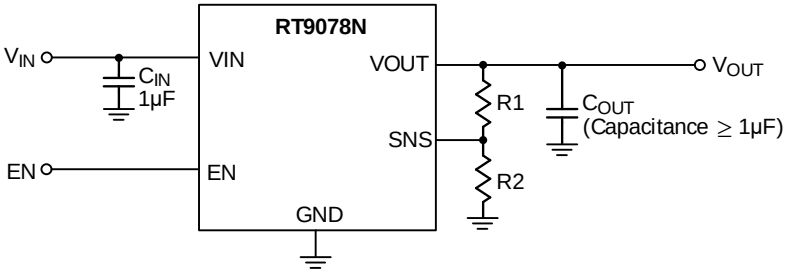


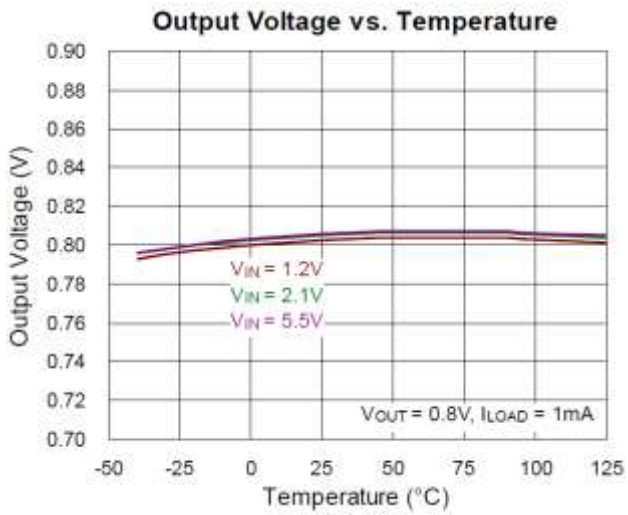
Figure 3. Adjustable Output Voltage Application Circuit

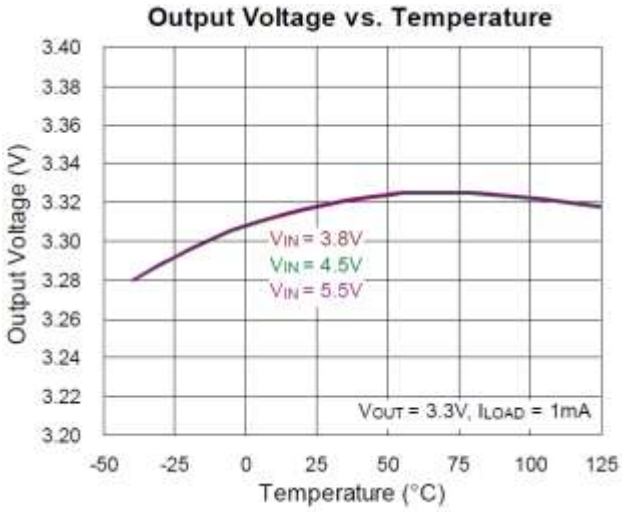
Table 1. Recommended External Components

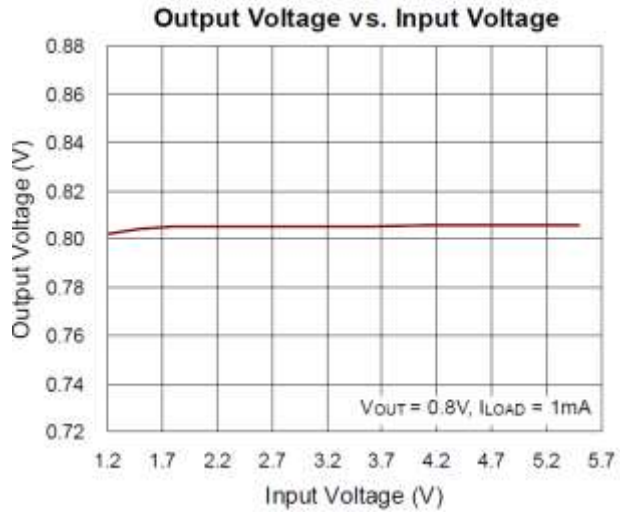
Component	Description	Vendor P/N
C_{IN}	1µF, 10V, X5R, 0402	GRM155R61A105KE15 (Murata)
C_{OUT}(1)	1µF, 6.3V, X5R, 0402	GRM153R60J105ME95(Murata) CGB2A3X5R0J105M033BB(TDK)
	2.2µF, 6.3V, X5R, 0402	GRM153R60J225ME95 (Murata) C1005X5R0J225M050BC (TDK)
	4.7µF, 6.3V, X5R, 0402	GRM153R60J475ME15 (Murata) C1005X5R0J475K050BE(TDK)

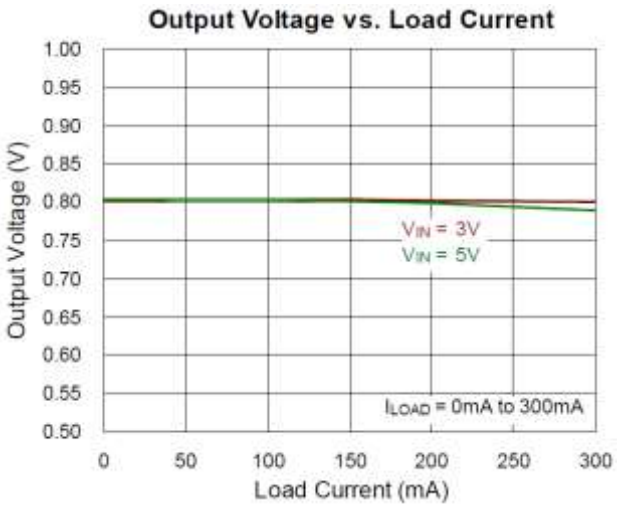
Note 10. Marked with (1): Considering the effective capacitance derated with biased voltage level, the C_{OUT} component needs satisfy the effective capacitance at least 0.7µF or above at targeted output level for stable and normal operation.

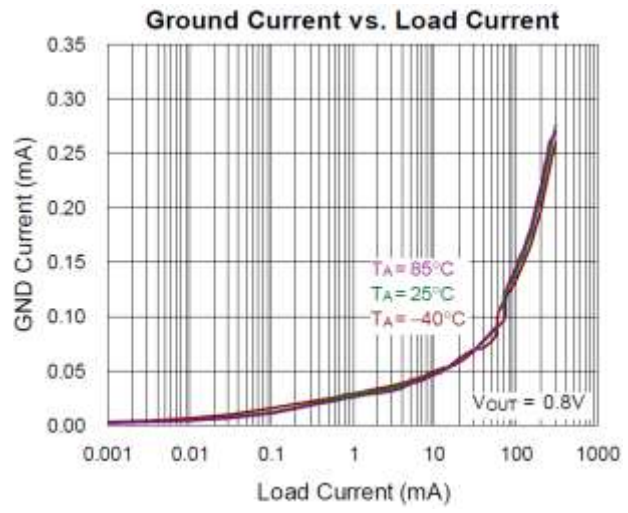
16 Typical Operating Characteristics

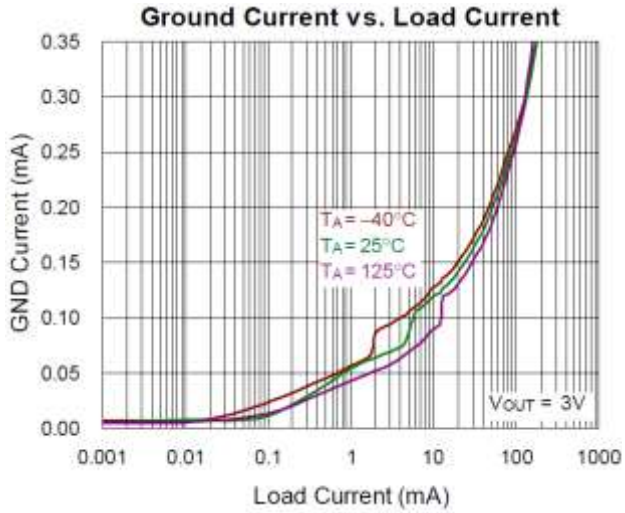




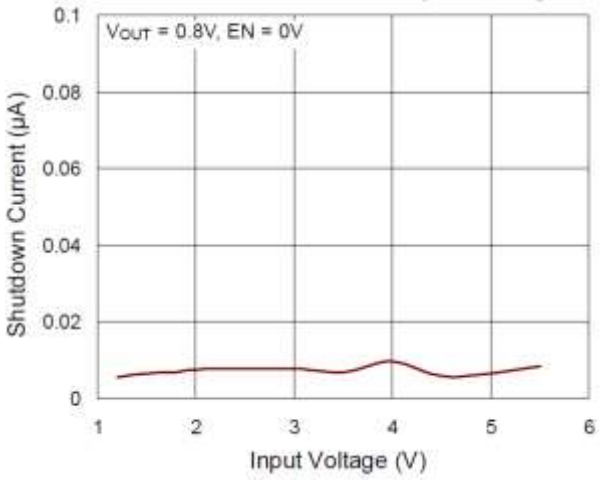




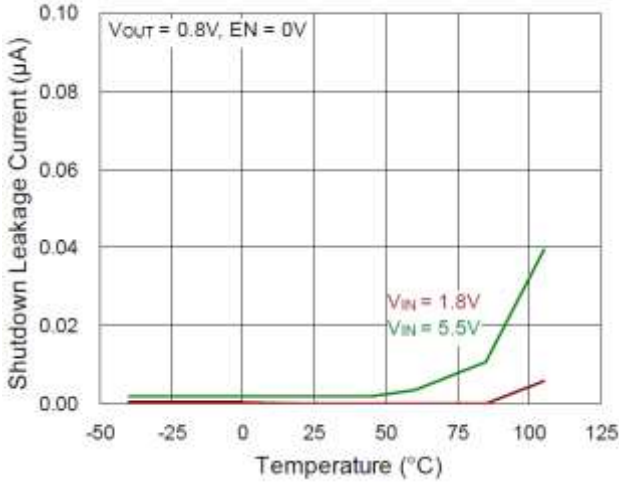




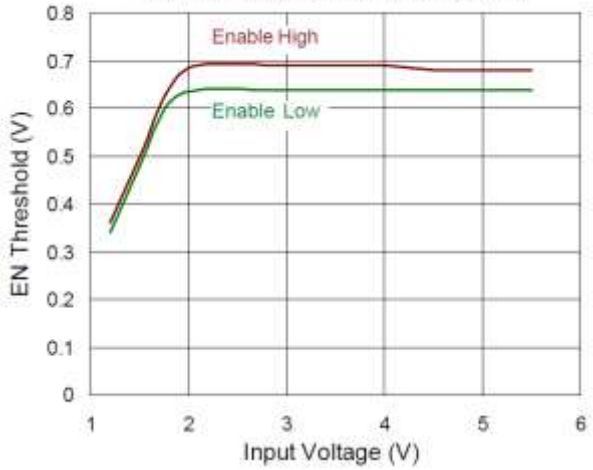
Shutdown Current vs. Input Voltage



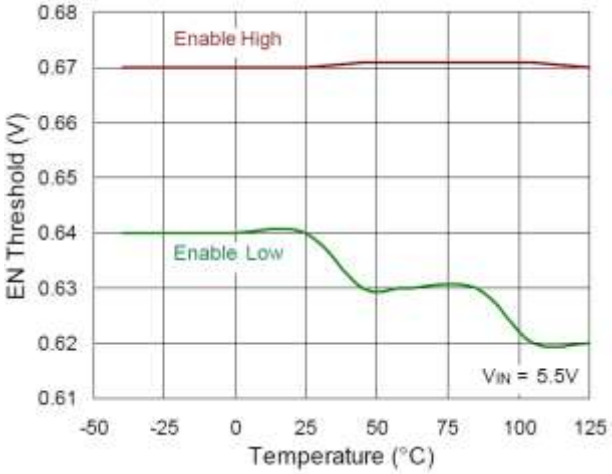
Shutdown Leakage Current vs. Temperature



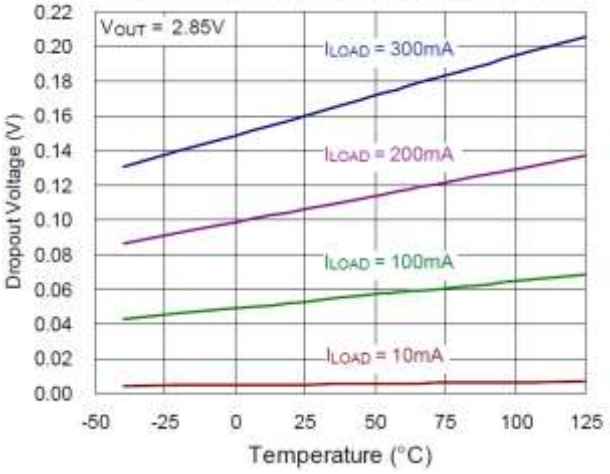
EN Threshold vs. Input Voltage



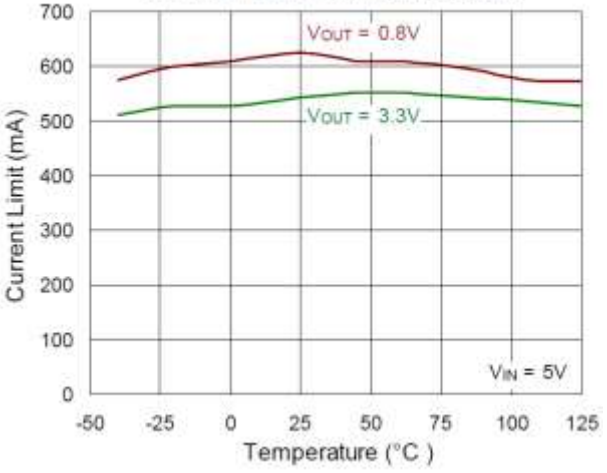
EN Threshold vs. Temperature



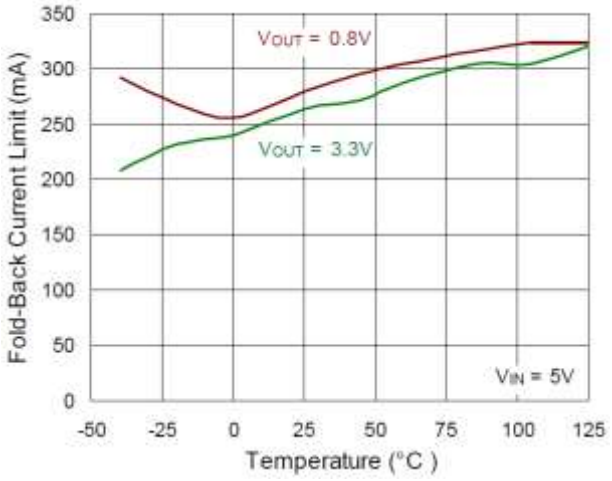
Dropout Voltage vs. Temperature



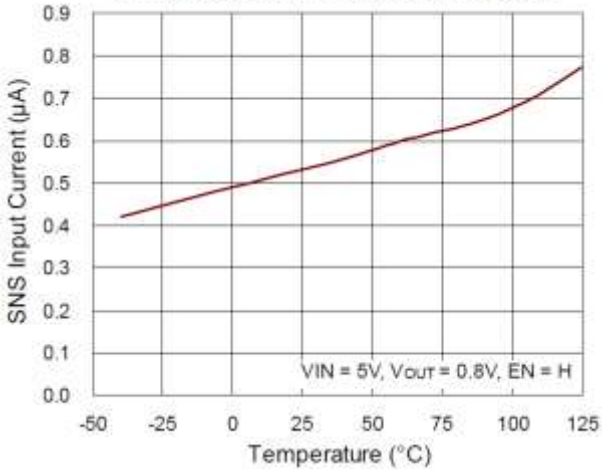
Current Limit vs. Temperature



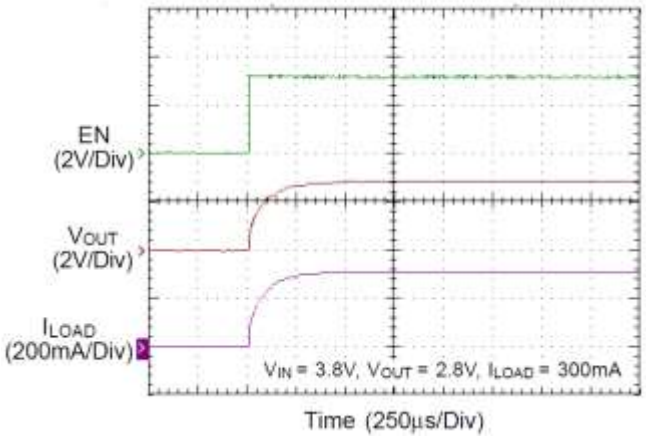
Fold-Back Current Limit vs. Temperature



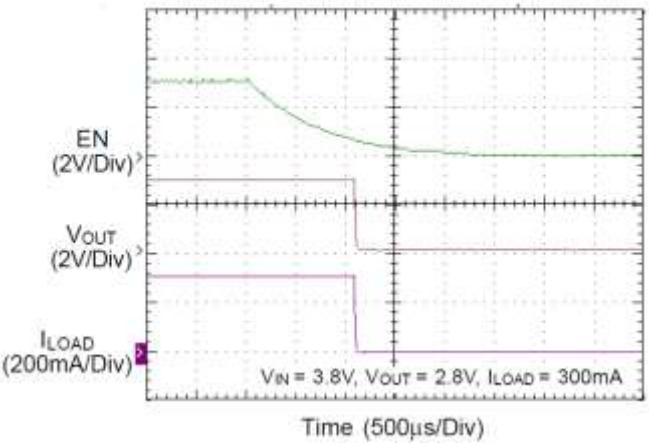
SNS Input Current vs. Temperature



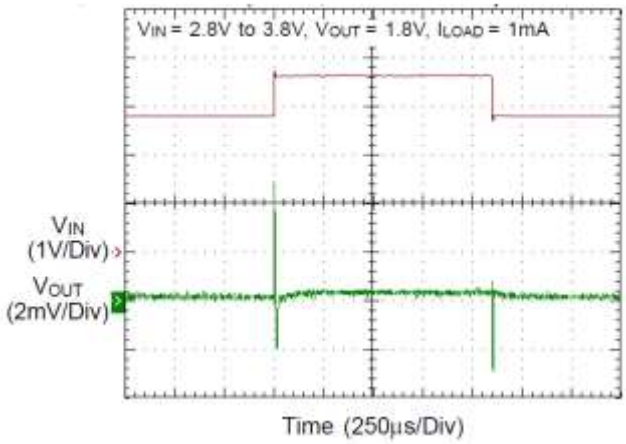
Power On from EN



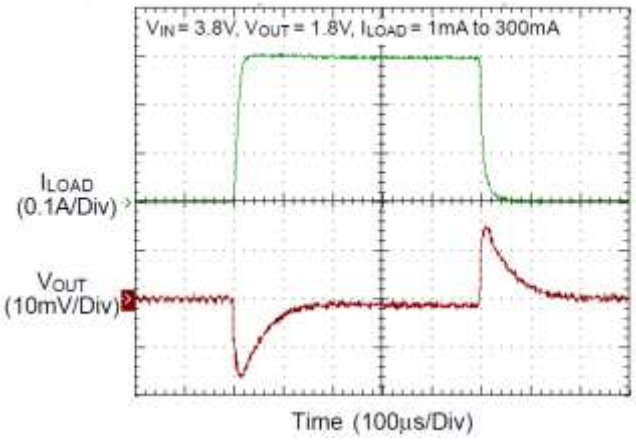
Power Off from EN

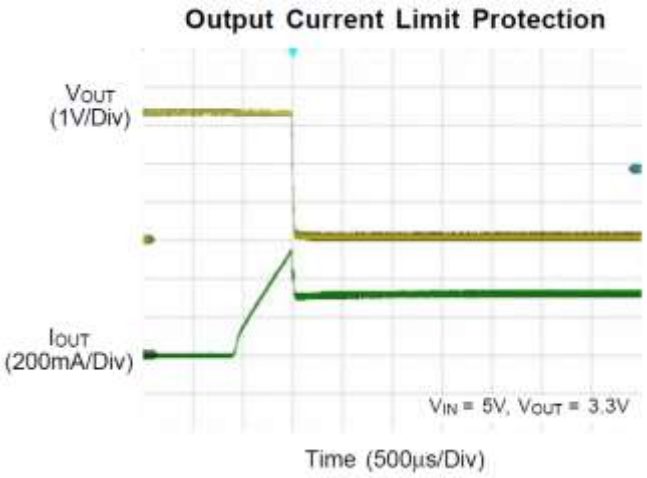


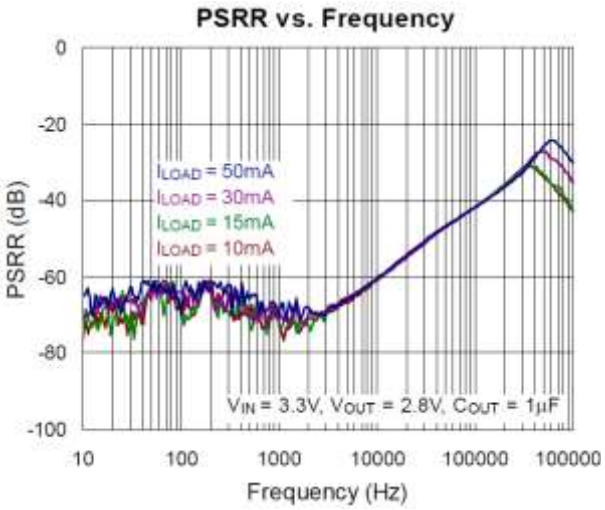
Line Transient

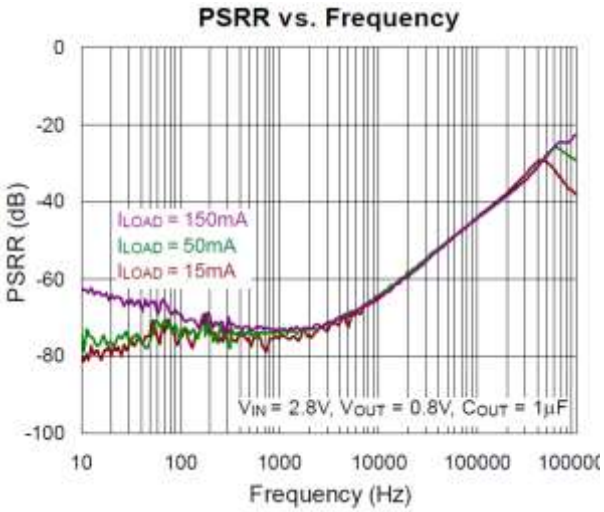


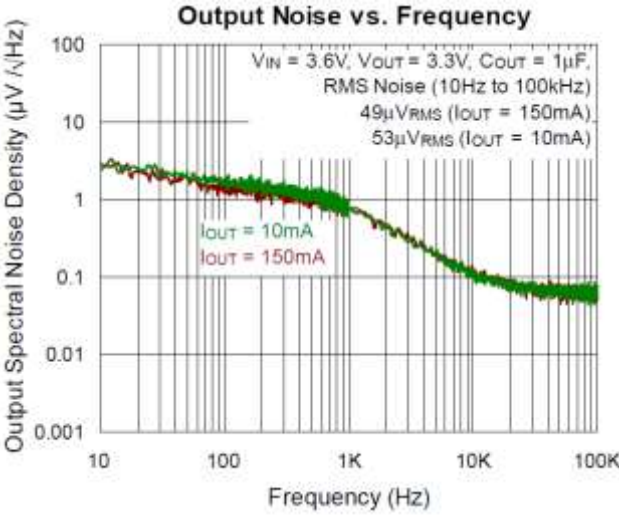
Load Transient











17 Operation

17.1 Basic Operation

The RT9078 is a low quiescent current linear regulator optimized for systems that require minimal external components. It supports an input voltage range from 1.2V to 5.5V.

To maintain stable operation, a minimum output capacitance of 1μF is required, considering the temperature variations and voltage coefficient of the capacitor.

17.2 Pass Transistor

The RT9078 incorporates a P-MOSFET pass transistor, which provides low on-resistance for low dropout voltage applications.

17.3 Error Amplifier

The Error Amplifier compares the internal reference voltage with the output feedback voltage from the internal divider and controls the gate voltage of the P-MOSFET.

17.4 IC Enable and Shutdown

The RT9078 provides an EN pin, as an external IC enable control, to enable or disable the device. If V_{EN} is below 0.4V, it turns the regulator off and the device enters shutdown mode. While V_{EN} is above 0.9V, the regulator is enabled. When the regulator is shutdown, the ground current is reduced to a maximum of 0.5μA.

17.5 Current-Limit Protection

The RT9078 includes an independent current limiter that monitors and controls the pass transistor's gate voltage, restricting the output current to 0.6A (typical). The current limiting level drops to approximately 0.3A, referred to as fold-back current limiting when the output voltage decreases further. The output can be shorted to ground indefinitely without damaging the device.

17.6 Over-Temperature Protection

The over-temperature protection function turns off the P-MOSFET when the junction temperature exceeds 150°C (typical) and the output current exceeds 30mA. Once the junction temperature decreases by approximately 20°C, the regulator automatically resumes operation.

17.7 Output Active Discharge

When the RT9078 operates in shutdown mode, the device features an internal active pull-down circuit that connects the output to GND via a resistor, facilitating output discharging.

18 Application Information

(Note 11)

Like any low dropout linear regulator, the RT9078's external input and output capacitors must be properly selected to ensure stability and performance. Utilize a 1μF or larger input capacitor and place it close to the IC's VIN and GND pins. An output capacitor with the minimum 1mΩ ESR (Equivalent Series Resistance) and a capacitance greater than 1μF is recommended. Place the output capacitor close to the IC's VOUT and GND pins. Enhancing capacitance and reducing ESR can improve the circuit's PSRR and line transient response.

18.1 Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at a specific output current. The dropout voltage (V_{DROP}) can also be expressed as the voltage drop across the pass-FET at a specific output current (I_{RATED}) while the pass-FET is operating fully in the ohmic region. Thus, the pass-FET can be characterized as a resistance (R_{ON}). Thus, the dropout voltage can be defined as $V_{DROP} = V_{IN} - V_{OUT} = R_{ON} \times I_{RATED}$. For normal operation, the suggested LDO operating range is $V_{IN} > V_{OUT} + V_{DROP}$ for good transient response and PSRR ability. Conversely, operating in the ohmic region will severely degrade the performance.

18.2 Adjustable Output Voltage Setting

Due to the small input current at the SNS pin, the RT9078N with the SNS pin can function as an adjustable output voltage LDO. Figure 3 illustrates the connections for the adjustable output voltage application. The resistor divider from VOUT to SNS determines the output voltage during regulation. The voltage on the SNS pin determined by the values of R1 and R2, sets the output voltage. The adjustable output voltage is calculated using the formula provided in the following Equation:

$$V_{OUT} = \frac{R1 + R2}{R2} \times V_{SNS}$$

where V_{SNS} is determined by the output voltage selection in the ordering information of the RT9078N (for example, for the RT9078N-08GJ5, V_{SNS} is 0.8V). The maximum adjustable output voltage can reach up to the input voltage minus the dropout voltage. The total value of the resistive divider R1 and R2 should not exceed 50kΩ.

18.3 Thermal Considerations

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent.

For TSOT-23-5 package, the thermal resistance, θ_{JA}, is 100.7°C/W on a standard JEDEC 51-7 four-layer thermal test board.

For ZQFN-4L 1x1 (ZDFN-4L 1x1) package, the thermal resistance, θ_{JA}, is 236°C /W on a two-layer Richtek evaluation board.

The maximum power dissipation at T_A = 25°C can be calculated by the following formula:

$P_{D(MAX)}$ = (125°C – 25°C) / (100.7°C/W) = 0.99W for TSOT-23-5 package.

$P_{D(MAX)}$ = (125°C – 25°C) / (236°C/W) = 0.42W for ZQFN-4L 1x1 (ZDFN-4L 1x1) package.

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curves in Figure 4 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

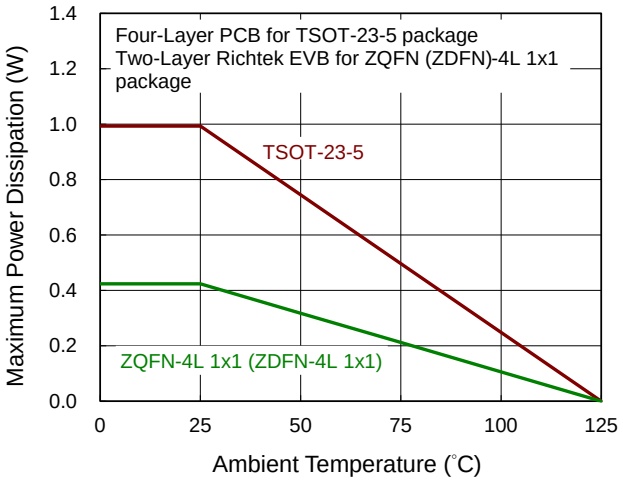


Figure 4. Derating Curves of Maximum Power Dissipation

18.4 Layout Considerations

For best performance of the RT9078, follow the PCB layout recommendations below:

- Input capacitors must be placed as close as possible to the IC to minimize the power loop area.
- Minimize the power trace length and avoid using vias for the input and output capacitors connection.

Figure 5 and Figure 6 show layout reference examples, which help minimize parasitic inductance, reduce load transients, and ensure circuit stability.

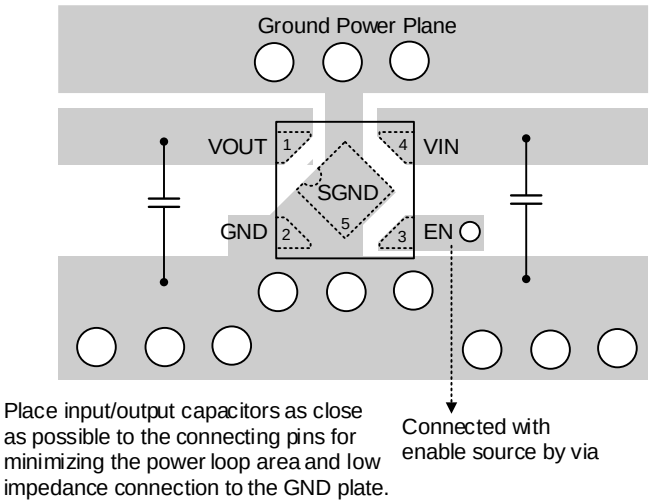


Figure 5. PCB Layout Guide for ZQFN-4L 1x1 Package

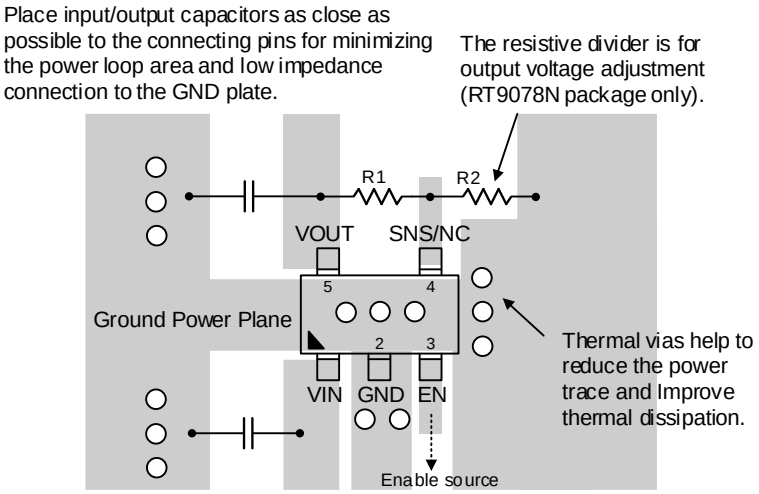
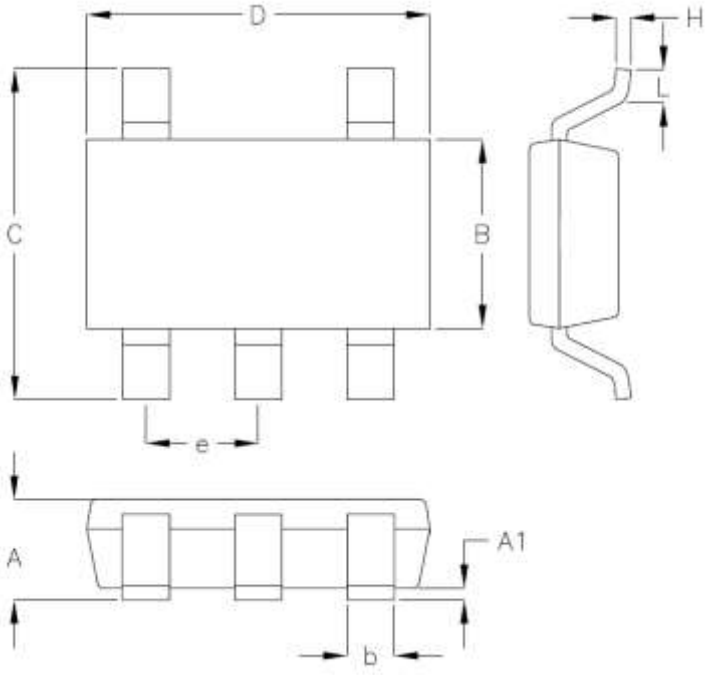


Figure 6. PCB Layout Guide for TSOT-23-5 Package

Note 11. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

19 Outline Dimension

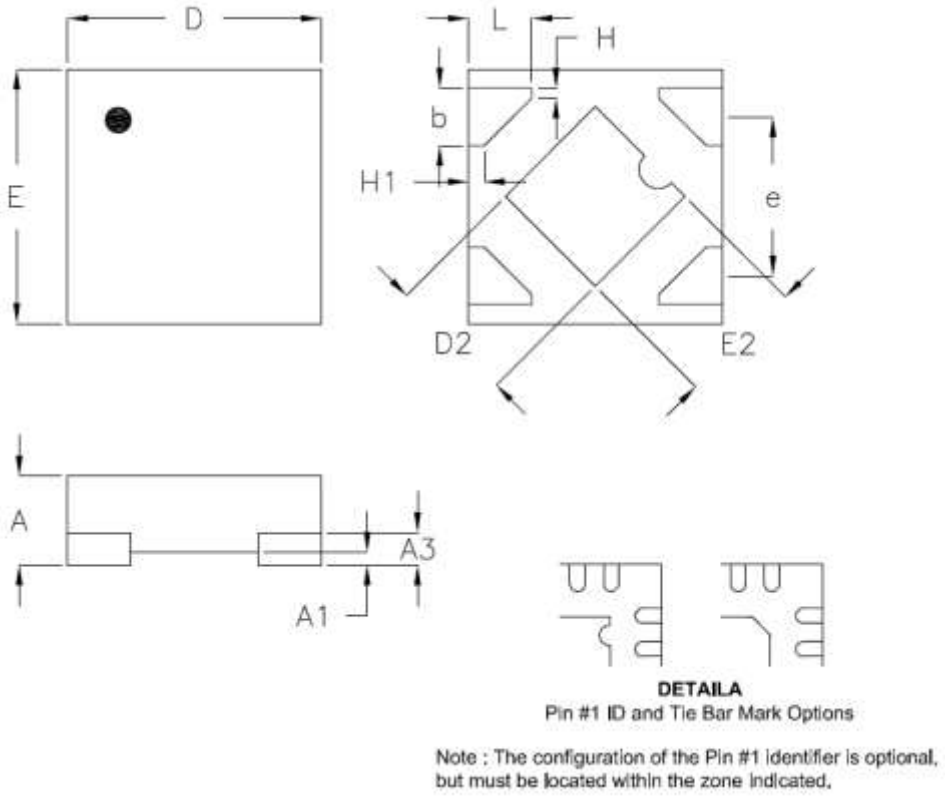
19.1 TSOT-23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.300	0.559	0.012	0.022
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-5 Surface Mount Package

19.2 ZQFN-4L 1x1 Package

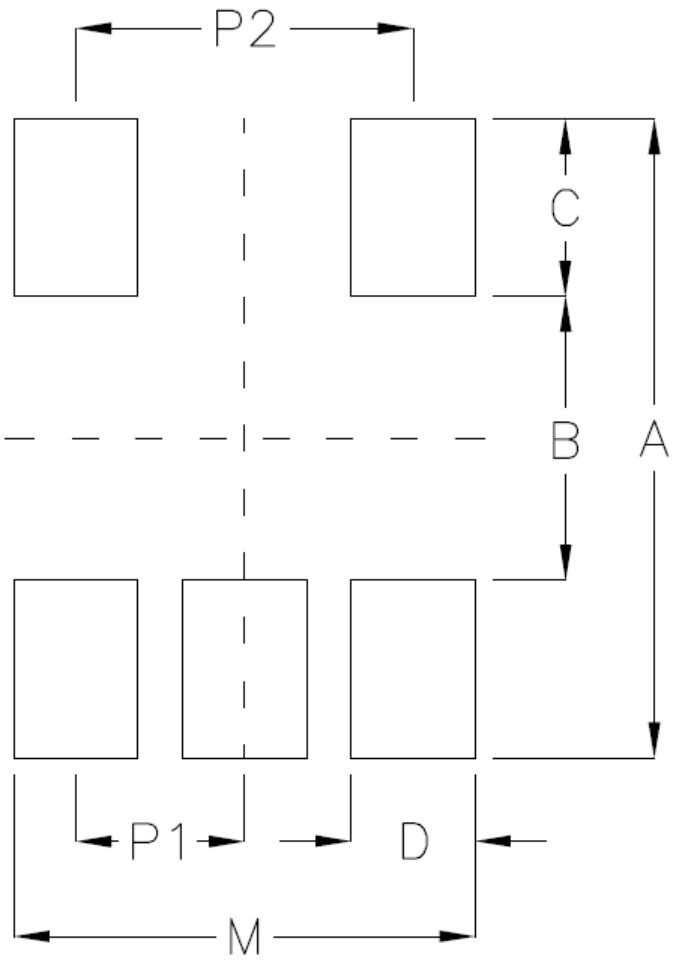


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.300	0.400	0.012	0.016
A1	0.000	0.050	0.000	0.002
A3	0.117	0.162	0.005	0.006
b	0.175	0.275	0.007	0.011
D	0.900	1.100	0.035	0.043
D2	0.450	0.550	0.018	0.022
E	0.900	1.100	0.035	0.043
E2	0.450	0.550	0.018	0.022
e	0.625		0.025	
L	0.200	0.300	0.008	0.012
H	0.039		0.002	
H1	0.064		0.003	

Z-Type 4L QFN 1x1 Package

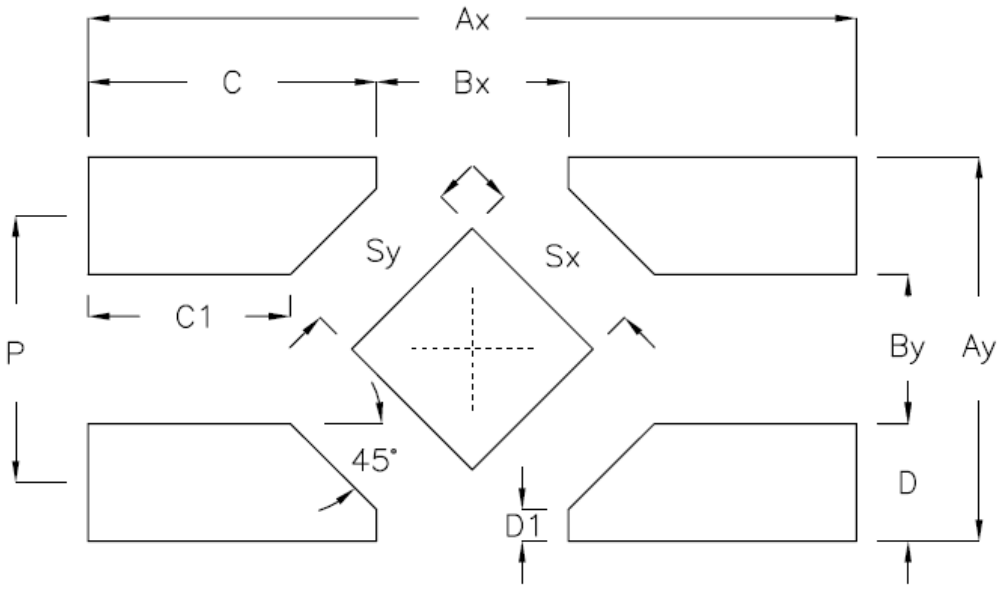
20 Footprint Information

20.1 TSOT-23-5 Package



Package	Number of Pin	Footprint Dimension (mm)							Tolerance
		P1	P2	A	B	C	D	M	
TSOT-25/TSOT-25(FC)/SOT-25	5	0.95	1.90	3.60	1.60	1.00	0.70	2.60	±0.10

20.2 ZQFN-4L 1x1 Package



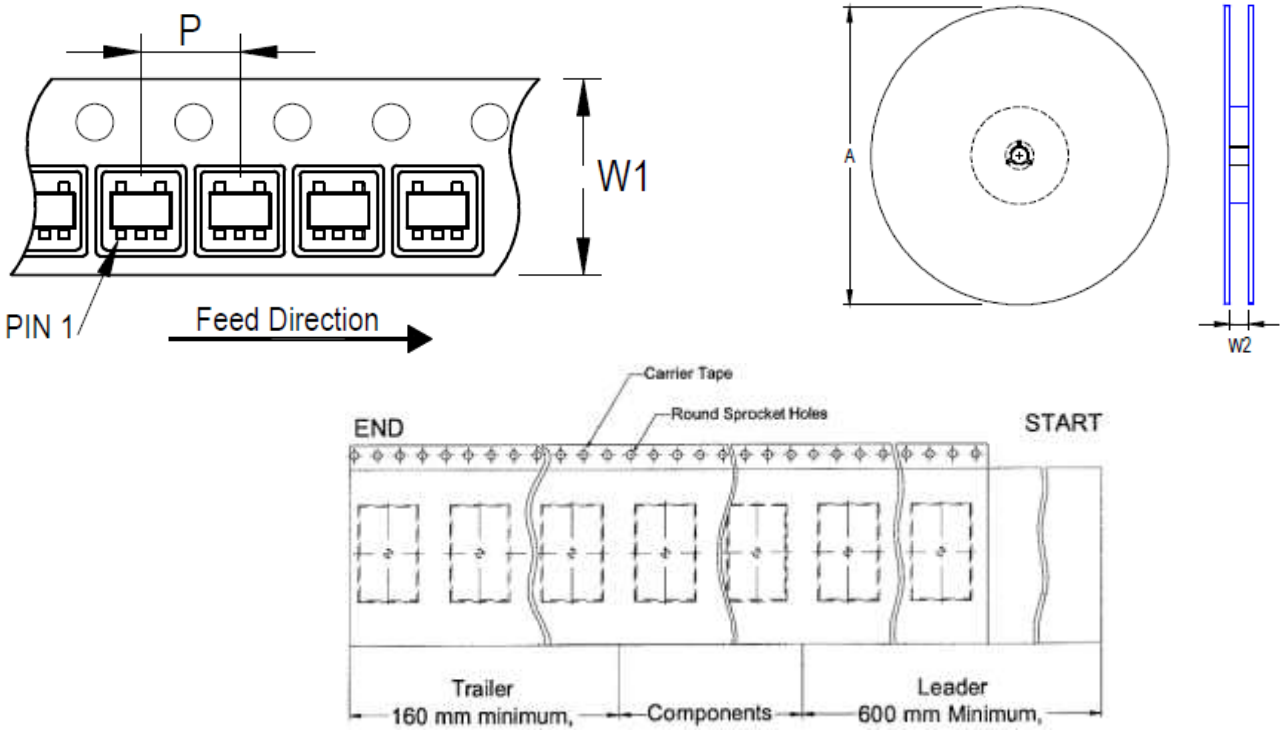
Package	Number of Pin	Footprint Dimension (mm)											Tolerance
		P	Ax	Ay	Bx	By	C	C1	D	D1	Sx	Sy	
U/X/ZQFN1x1-4	4	0.625	1.800	0.900	0.450	0.350	0.675	0.474	0.275	0.074	0.400	0.400	±0.050

21 Packing Information

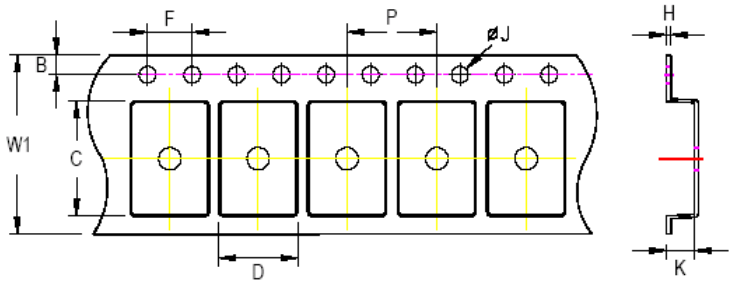
21.1 Tape and Reel Data

21.1.1 TSOT-23-5

SOT/TSOT-23-5



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader(mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
TSOT-23-5	8	4	180	7	3,000	160	600	8.4/9.9

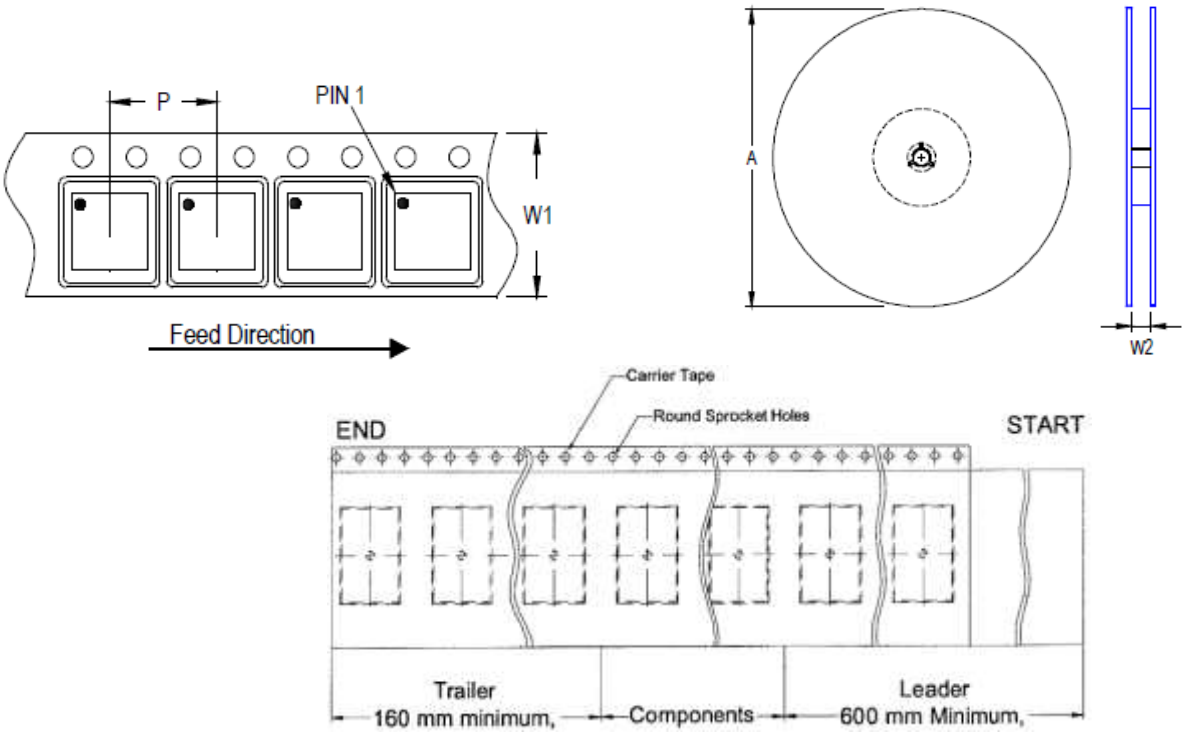


C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 8mm carrier tape: 0.5mm maximum

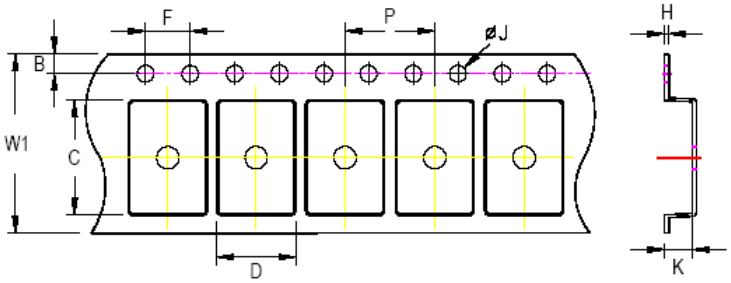
Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.2mm	0.6mm

21.1.2 ZQFN-4L 1x1

21.1.2.1 Quadrant 1



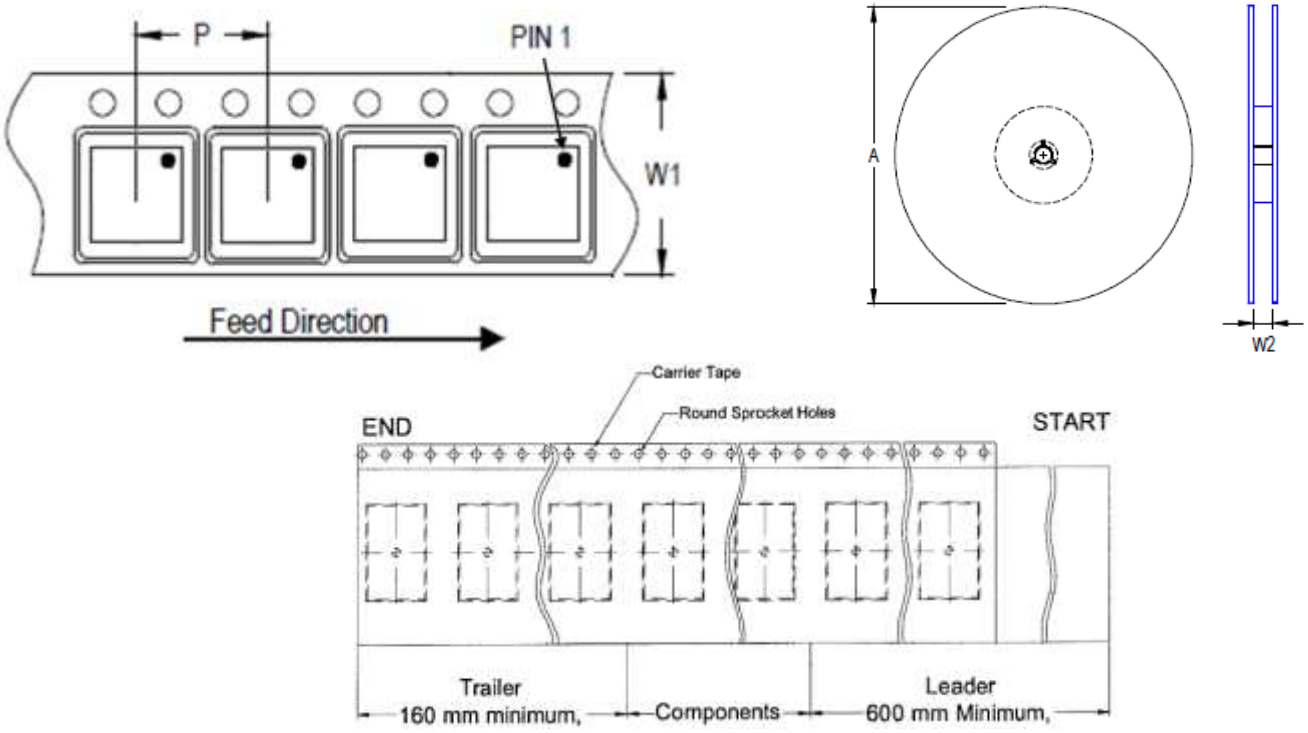
Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(Z) QFN/DFN 1x1	8	4	180	7	2,500	160	600	8.4/9.9



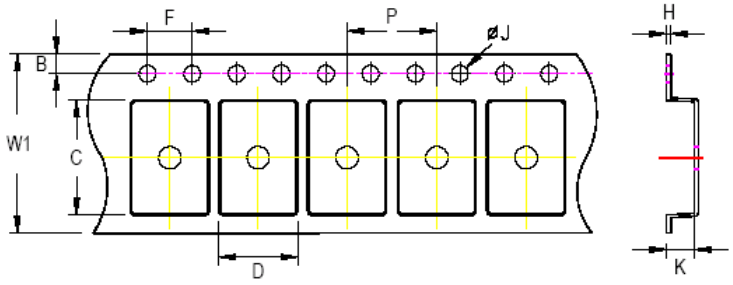
C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 8mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.5mm	0.6mm	0.6mm

21.1.2.2 Quadrant 2



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader(mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(Z) QFN/DFN 1x1	8	4	180	7	2,500	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.5mm	0.6mm	0.6mm

21.2 Tape and Reel Packing

21.2.1 TSOT-23-5

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
TSOT-23-5	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

21.2.2 ZQFN-4L 1x1

21.2.2.1 Quadrant 1

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(Z) QFN/DFN 1x1	7”	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

21.3.1.1 Quadrant 2

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(Z) QFN/DFN 1x1	7”	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

21.4 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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22 Datasheet Revision History

Version	Date	Description
20	2024/4/15	Rewrite
21	2025/6/30	Features Ordering Information Pin Configuration Functional Pin Description Electrical Characteristics Application Information Packing Information - Added ZQFN-4L 1x1 Quadrant 1 - Added Tape Size “K”