DDR Termination Regulator

1 General Description

The RT9088A is a sink/source tracking termination regulator. It is specifically designed for low-cost and low-external component count systems. The RT9088A features a high-speed operational amplifier that provides a fast load transient response and only requires a minimum 30μF ceramic output capacitor. The RT9088A supports remote sensing functions and includes all features required to power the DDRIII and Low Power DDRIII/DDRIV VTT bus termination according to the JEDEC specification. In addition, the RT9088A provides an open-drain PG signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3 (suspend to RAM) for DDR applications.

The RT9088A is available in the thermal efficient package, WDFN-10L 3x3. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Ordering Information

RT9088A □□

Package Type(1)
QW: WDFN-10L 3x3 (W-Type)

Lead Plating System
G: Richtek Green Policy Compliant(2)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

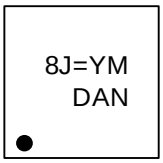
3 Features

- **VIN Input Voltage Range: 1.1V to 3.5V**
- **VCNTL Input Voltage Range: 2.9V to 5.5V**
- **Support Ceramic Capacitors**
- **Power-Good Indicator**
- **10mA Source/Sink Reference Output**
- **Meet DDRI, DDRII JEDEC Spec**
- **Support DDRIII, Low Power DDRIII/DDRIV VTT Applications**
- **Soft-Start Function**
- **UVLO (Undervoltage Lockout) and OCP (Overcurrent Protection)**
- **Over-Temperature Protection**

4 Applications

- Notebooks/Desktops/Servers
- Telecom/Datacom Systems
- GSM Base Stations
- LCD-TVs/PDP-TVs
- Copiers/Printers
- Set-Top Boxes

5 Marking Information



8J=: Product Code
YMDAN: Date Code

6 Simplified Application Circuit

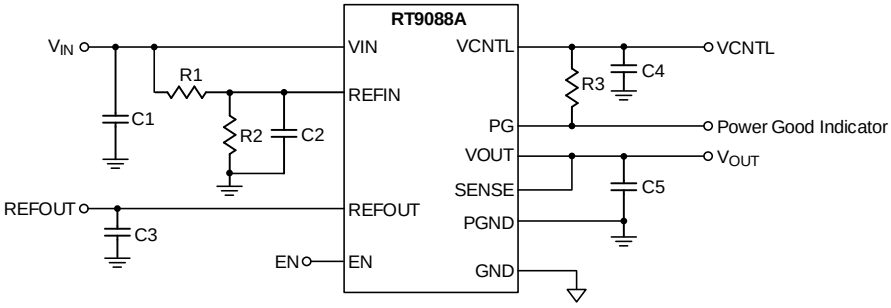
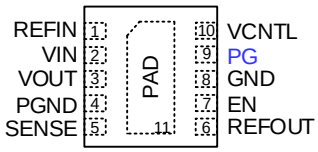


Table of Contents

7 Pin Configuration

(TOP VIEW)

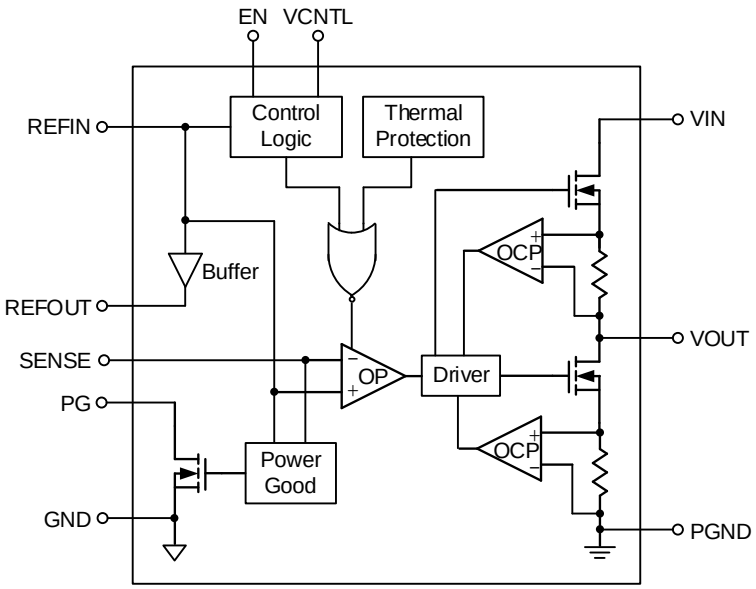


WDFN-10L 3x3

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	REFIN	Reference input.
2	VIN	Power input of the regulator.
3	VOUT	Power output of the regulator.
4	PGND	Power ground of the regulator.
5	SENSE	Voltage sense input for the regulator. Connect to the positive terminal of the output capacitor or the load.
6	REFOUT	Reference output. Connect to GND through a 0.1μF ceramic capacitor.
7	EN	Enable control input. For DDR VTT applications, connect EN to SLP_S3. For other applications, use EN as the ON/OFF function.
8	GND	Analog ground. Connect to the negative terminal of the output capacitor.
9	PG	Power good open-drain output. Connect a pull-up resistor between this pin and VCNTL pin.
10	VCNTL	Control voltage input. Connect this pin to the 3.3V or 5V power supply. A 4.7μF ceramic decoupling capacitor is required.
11 (Exposed Pad)	PAD	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large PGND plane. Connect this PGND plane to other layers with thermal vias to help dissipate heat from the device.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, VIN, VCNTL ---------- –0.3V to 6V
- Input Voltage, EN, REFIN, SENSE ---------- –0.3V to 6V
- Output Voltage, VOUT, REFOUT, PG ---------- –0.3V to 6V
- Package Thermal Resistance
- Power Dissipation, P_D @ T_A = 25°C

  WDFN-10L 3x3---------- 3.27W
- Package Thermal Resistance (Note 3)

  WDFN-10L 3x3, θ_{JA}---------- 30.5°°C/W

  WDFN-10L 3x3, θ_{JC}---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model)---------- ±2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Control Input Voltage, VCNTL ---------- 2.9V to 5.5V
- Supply Input Voltage, VIN ---------- 1.1V to 3.5V
- Ambient Temperature Range ---------- –40°C to 125°C
- Junction Temperature Range ---------- –40°C to 85°C

Note 5. The device is not guaranteed to function outside its operating conditions.

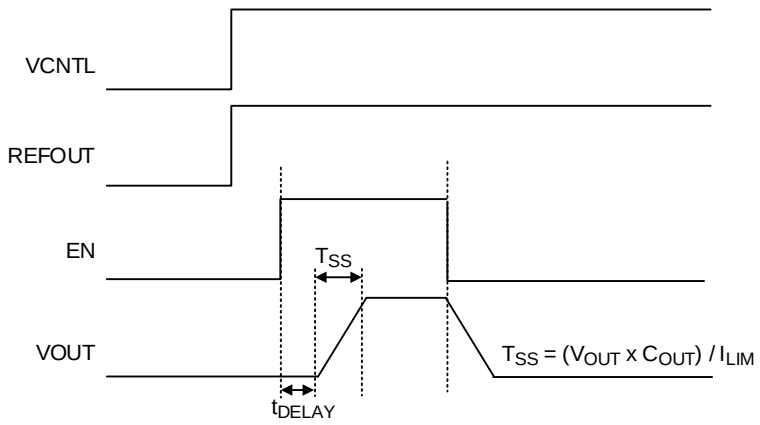
12 Electrical Characteristics

(V_{IN} = 1.5V, V_{EN} = V_{CNTL} = 3.3V, V_{REFIN} = V_{SENSE} = 0.75V, C_{OUT} = 10µF x 3, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
VCNTL Supply Current	I_{VCNTL}	V_{EN} = V_{CNTL}, No Load	--	0.7	1	mA
VCNTL Shutdown Current	I_{SHDN_VCNTL}	V_{EN} = 0V, V_{REFIN} = 0V, No Load	--	65	80	µA
		V_{EN} = 0V, V_{REFIN} > 0.4V, No Load	--	200	400	µA
VIN Supply Current	I_{VIN}	V_{EN} = V_{CNTL}, No Load	--	1	50	µA
VIN Shutdown Current	I_{SHDN_VIN}	V_{EN} = 0V, No Load	--	0.1	50	µA
Output						
VTT Output Voltage	V_{OUT}	V_{IN} = 1.5V, V_{REFIN} = 0.75V, I_{OUT} = 0A	--	0.75	--	V
		V_{IN} = 1.35V, V_{REFIN} = 0.675V, I_{OUT} = 0A	--	0.675	--	V
		V_{IN} = 1.2V, V_{REFIN} = 0.6V, I_{OUT} = 0A	--	0.6	--	V
REFIN, VTT Output Voltage Offset	V_{OFFSET}	I_{OUT} = ±2A, V_{LDOIN} = 1.5V, V_{REFOUT} = 0.75V	–25	--	25	mV
		I_{OUT} = ±2A, V_{LDOIN} = 1.35V, V_{REFOUT} = 0.675V	–25	--	25	
		I_{OUT} = ±2A, V_{LDOIN} = 1.2V, V_{REFOUT} = 0.6V	–25	--	25	
VOUT Source Current Limit	$I_{LIM\_VOUT\_SR}$	VOUT in PG Window	3.5	--	5.5	A
VOUT Sink Current Limit	$I_{LIM\_VOUT\_SK}$	VOUT in PG Window	3.5	--	5.5	A
VOUT Discharge Resistance	R_{DISCHG}	V_{REFIN} = 0V, V_{OUT} = 0.3V, V_{EN} = 0V	--	18	25	Ω
Power-Good Comparator						
PG Threshold	V_{PG}	V_{SENSE} lower threshold with respect to REFOUT	–25	–20	–15	%
		V_{SENSE} upper threshold with respect to REFOUT	15	20	25	
		PG Hysteresis	--	5	--	
PG Start-Up Delay	t_{DLY_PG1}	Start-up rising delay, V_{SENSE} within PG range	--	2	--	ms
Output Low Voltage	V_{LOW_PG}	I_{PG} = 4mA	--	--	0.4	V
PG Falling Delay	t_{DLY_PG2}	Falling delay, V_{SENSE} is out of PG range	--	10	--	µs
Leakage Current	I_{LK_PG}	V_{SENSE} = V_{REFIN} (PG high impedance), V_{PG} = V_{IN} + 0.3V	--	--	1	µA
REFIN and REFOUT						
REFIN Input Current	I_{REFIN}	V_{EN} = V_{CNTL}	--	--	1	µA
REFIN Voltage Range	V_{REFIN}		0.5	--	1.8	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
REFIN Undervoltage-Lockout	V_{UVLO_REFIN}	REFIN Rising	360	390	420	mV
		Hysteresis	--	20	--	
REFOUT Voltage Tolerance to VREFIN	V_{TOL_REFOUT}	−10mA < I_{REFOUT} < 10mA, V_{REFIN} = 0.75V	−15	--	15	mV
		−10mA < I_{REFOUT} < 10mA, V_{REFIN} = 0.675V	−13.5	--	13.5	
		−10mA < I_{REFOUT} < 10mA, V_{REFIN} = 0.6V	−12	--	12	
REFOUT Source Current Limit	$I_{LIM\_REFOUT\_SR}$	V_{REFOUT} = 0V	10	40	--	mA
REFOUT Sink Current Limit	$I_{LIM\_REFOUT\_SK}$	V_{REFOUT} = REFIN + 1V	10	40	--	mA
UVLO/EN						
UVLO Threshold	V_{UVLO_VCNTL}	Rising	2.5	2.7	2.85	V
		Hysteresis	--	120	--	mV
EN Input Voltage Rising Threshold	V_{EN_R}		1.7	--	--	V
EN Input Voltage Falling Threshold	V_{EN_F}		--	--	0.3	V
EN Turn-On Delay	t_{DLY}	EN turn on to V_{OUT} rising (see Note 6)	--	--	7	μs
Over-Temperature Protection						
Over-Temperature Protection	T_{OTP}	Shutdown Temperature	--	160	--	°C
		Hysteresis	--	15	--	

Note 6. t_{DLY} is the period from when EN is turned on to when V_{OUT} begins to rise, as shown in the following diagram. T_{SS} is the rising period of V_{OUT}. The formula used to calculate this rising period is T_{SS} = (V_{OUT} x C_{OUT})/I_{LIM}. It is based on the value of the output capacitor C_{OUT}, the settled output voltage V_{OUT}, and the output current limit I_{LIM}.



13 Typical Application Circuit

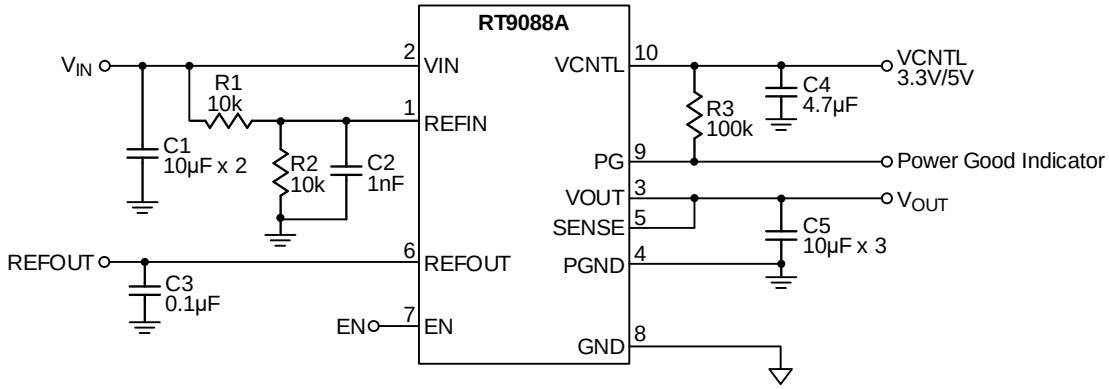
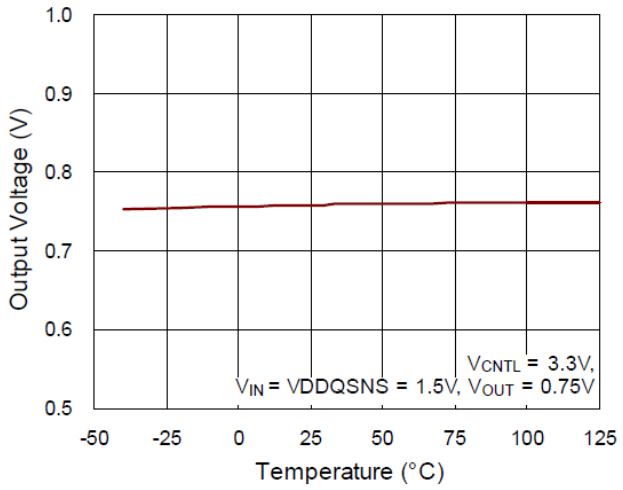


Table 1. Boost Converter Mode (P Type Isolation MOSFET)

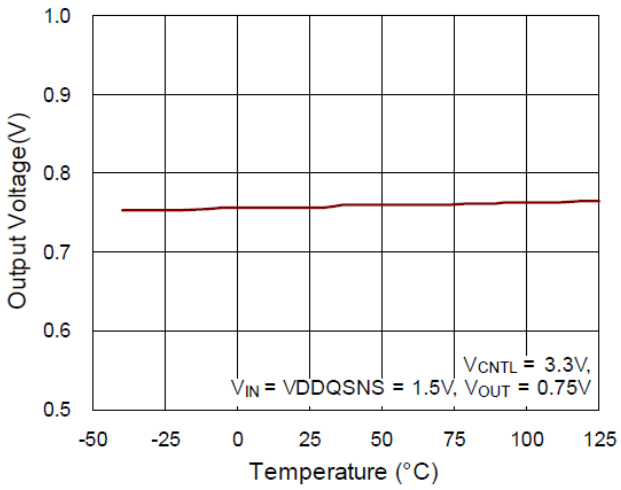
Component	Description	Vendor P/N
C1, C5	10µF, 6.3V, X7R, 0805	GRM21BR70J106KE76L (Murata) CGA4J1X7R0J106K125AC (TDK)
C2	1nF, 50V, X7R, 0603	GCD188R71H102KA01D (Murata) CGA3E2X7R1H102K080AA (TDK)
C3	0.1µF, 16V, X7R, 0603	GCJ188R71C104KA01D (Murata)
C4	4.7µF, 6.3V, X5R, 0603	GRT188R60J475ME01D (Murata) CGB3B3X5R0J475M055AB(TDK)

14 Typical Operating Characteristics

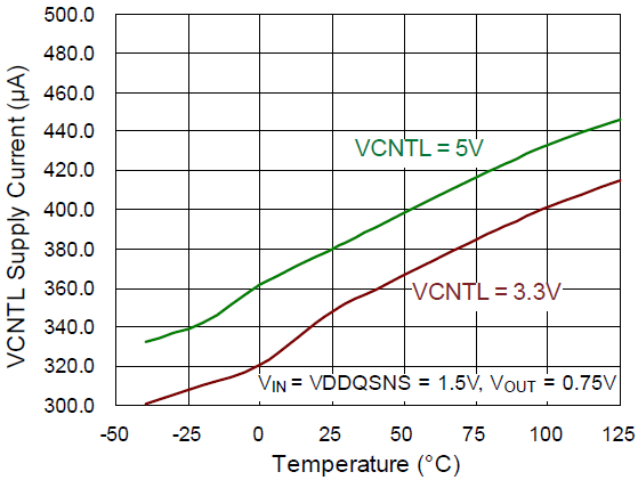
Output Voltage vs. Temperature



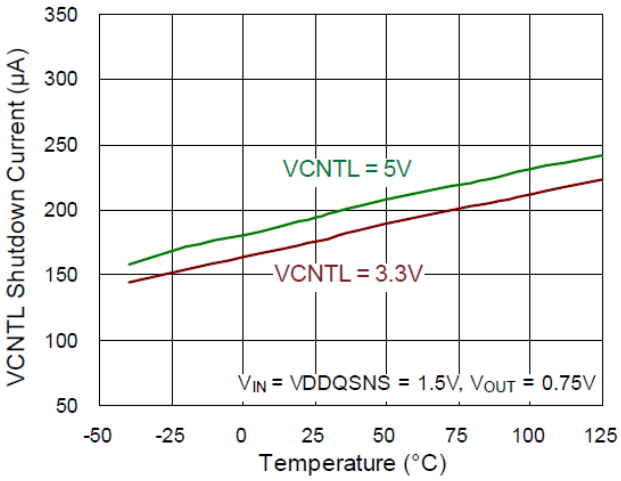
REFOUT Voltage vs. Temperature



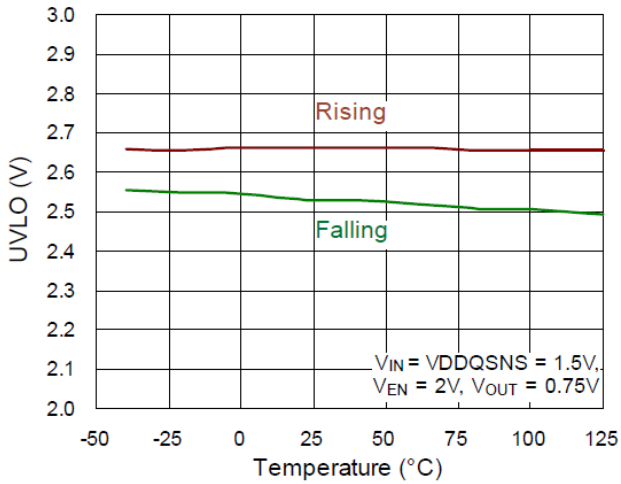
VCNTL Supply Current vs. Temperature



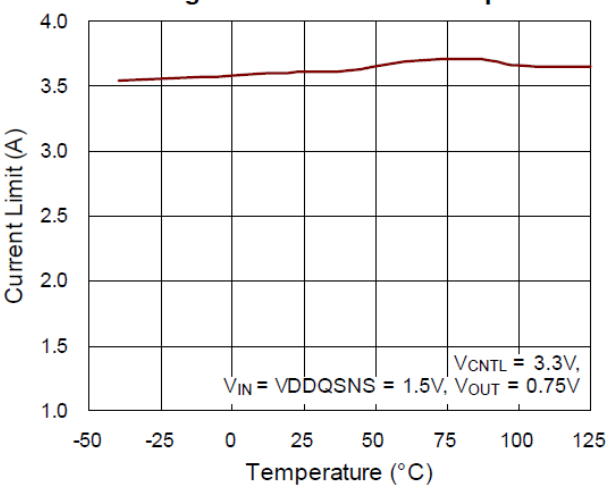
VCNTL Shutdown Current vs. Temperature



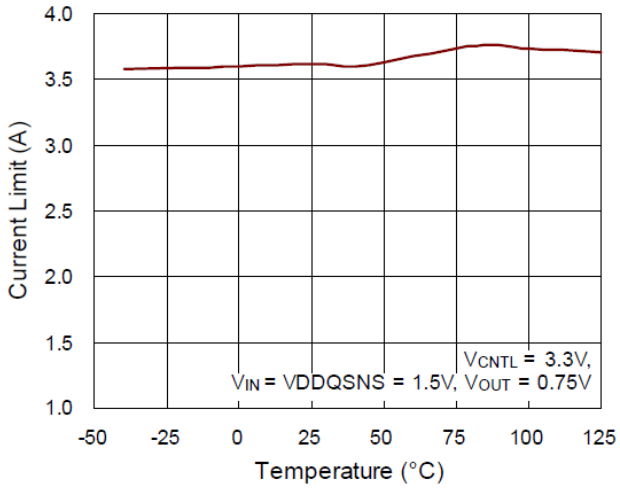
UVLO vs. Temperature



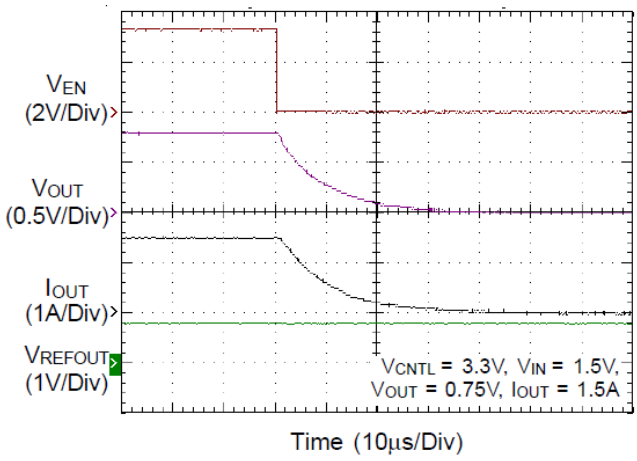
Sourcing Current Limit vs. Temperature



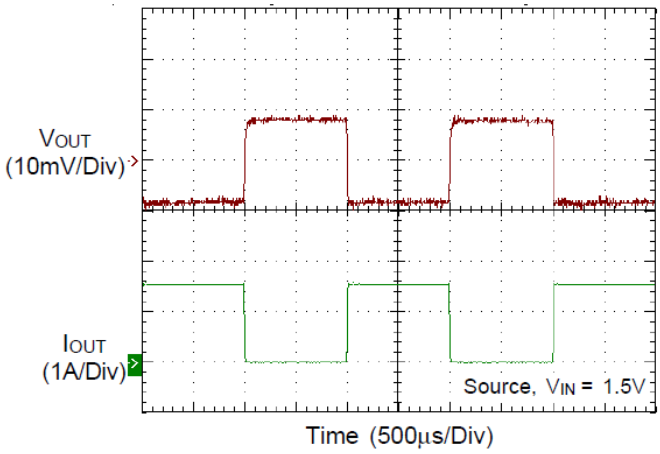
Sinking Current Limit vs. Temperature



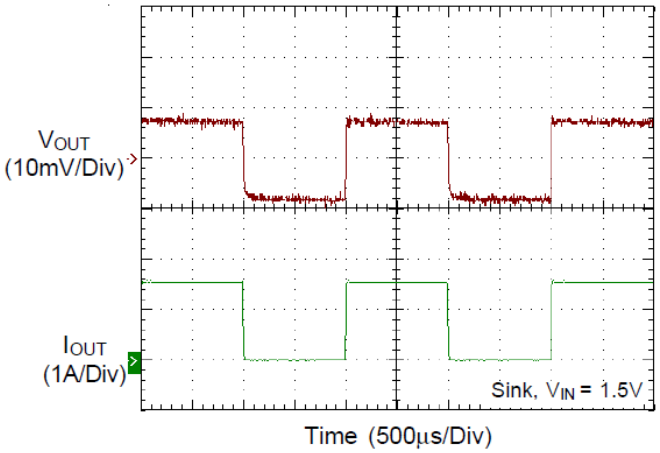
Power Off from EN



0.75V_{OUT} @ 1.5A Transient Response



0.75V_{OUT} @ 1.5A Transient Response



15 Operation

The RT9088A is a linear sink/source DDR termination regulator with current capability up to 3A. The RT9088A builds in a high-side N-MOSFET which provides current sourcing and a low-side N-MOSFET for current sinking. All the control circuits are supplied by the power VCNTL. In normal operation, the error amplifier OP adjusts the gate driving voltage of the power MOSFET to achieve the SENSE voltage well tracks the REFIN voltage.

15.1 Current Monitoring and Overcurrent Protection

Both the source and sink currents are detected by the internal sensing resistor, and the OCP function limits the current to a designed value when overload happens. Furthermore, the current will be reduced to half if VOUT is out of the power-good window.

15.2 Buffer

This function provides a REFOUT output level equal to the REFIN level, with 10mA source/sink current capability.

15.3 Power-Good Indicator

When the SENSE voltage is in the power-good window and lasts for a certain delay time, then the PG pin will be high impedance and the PG voltage will be pulled high by the external resistor.

15.4 Control Logic

This block includes VCNTL UVLO, REFIN UVLO, and Enable/Disable functions, and provides logic control to the whole chip.

15.5 Thermal Protection

Both the high-side and low-side power MOSFETs will be turned off when the junction temperature is higher than typically 160°C and be released to normal operation when junction temperature falls below 120°C typically.

16 Application Information

(Note 7)

The RT9088A is a 3A sink/source tracking termination regulator. It is specifically designed for low-cost systems with minimal external components, such as notebook or PC applications. The RT9088A features a high-speed operational amplifier that provides a fast load transient response and only requires two 10μF ceramic input capacitors and three 10μF ceramic output capacitors.

16.1 Capacitor Selection

Good bypassing from VIN to GND is recommended to improve AC performance. A 10μF or larger input capacitor should be placed as close as possible to the IC, ideally within 0.5 inches of the VIN pin.

The 1μF ceramic capacitor should be added close to the VCNTL pin and kept free away from any parasitic impedance from the supply power. For stable operation, the total capacitance of the ceramic capacitors at the VOUT output terminal must be larger than 30μF. The RT9088A is designed to work specifically with low ESR ceramic output capacitors for space-saving and performance consideration. Larger output capacitance can reduce the noise and improve load transient response, stability, and PSRR. The output capacitor should be located as close as possible to the VOUT output terminal pin.

16.2 Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-10L 3x3 package, the thermal resistance, θ_{JA}, is 30.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula:

$P_{D(MAX)}$ = (125°C − 25°C) / (30.5°C/W) = 3.27W for WDFN-10L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

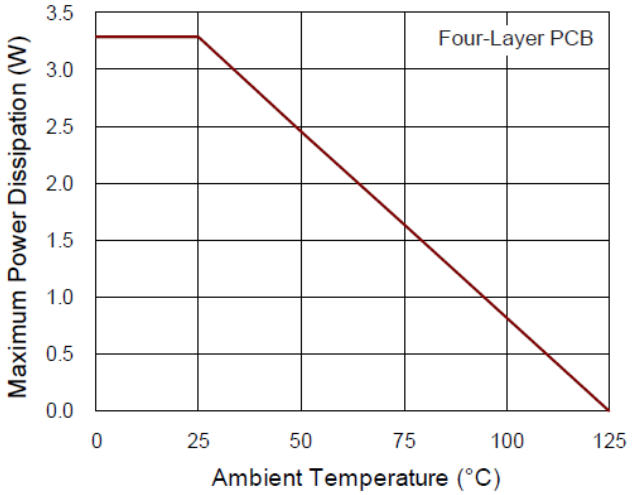
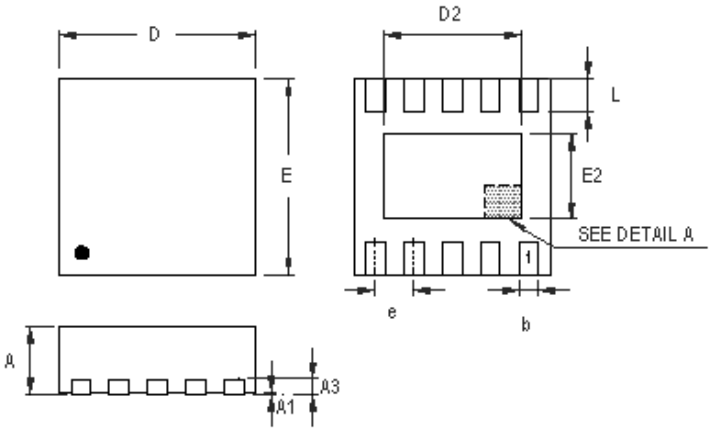
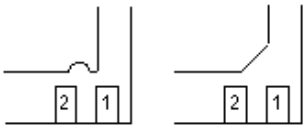


Figure 1. Derating Curve of Maximum Power Dissipation

Note 7. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

17 Outline Dimension





DETAIL A

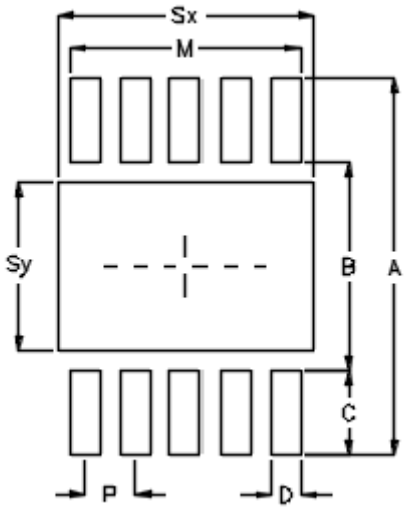
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

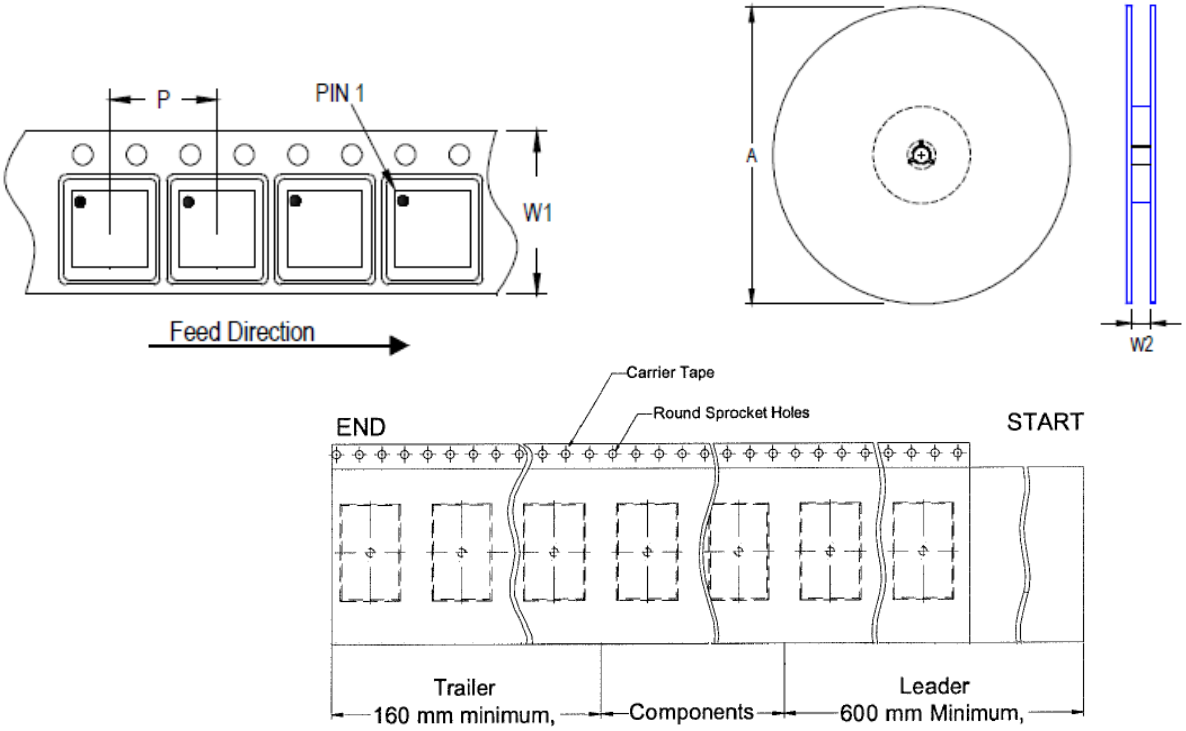
18 Footprint Information



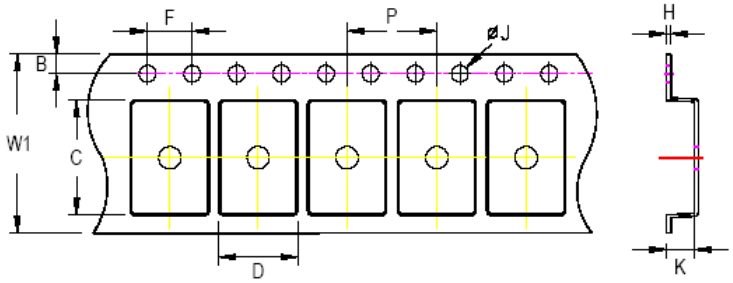
Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/X/ZDFN3*3-10	10	0.50	3.80	2.10	0.85	0.30	2.55	1.70	2.30	±0.05

19 Packing Information

19.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 3x3	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description	Item
06	2025/6/24	Modify	*Changed the names PGOOD to PG* *General Description on page 1* *Features on page 1* *Ordering Information on page 2* *Electrical Characteristics on page 5, 6* *Footprint Information on page 14* - Added Footprint Information *Packing Information on page 15 to 17* - Added packing information