DDR Termination Regulator

General Description

The RT9088B is a sink/source tracking termination regulator. It is specifically designed for low-cost and low-external component count systems. The RT9088B possesses a high speed operating amplifier that provides fast load transient response and only requires a minimum 30μF ceramic output capacitor. The RT9088B supports remote sensing functions and all features required to power the DDRIII and Low Power DDRIII / DDRIV VTT bus termination according to the JEDEC specification. In addition, the RT9088B provides an open-drain PGOOD signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3 (suspend to RAM) for DDR applications.

The RT9088B is available in the thermal efficient package, WDFN-10L 2x2.

Ordering Information

RT9088B □□

Package Type
QW : WDFN-10L 2x2 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

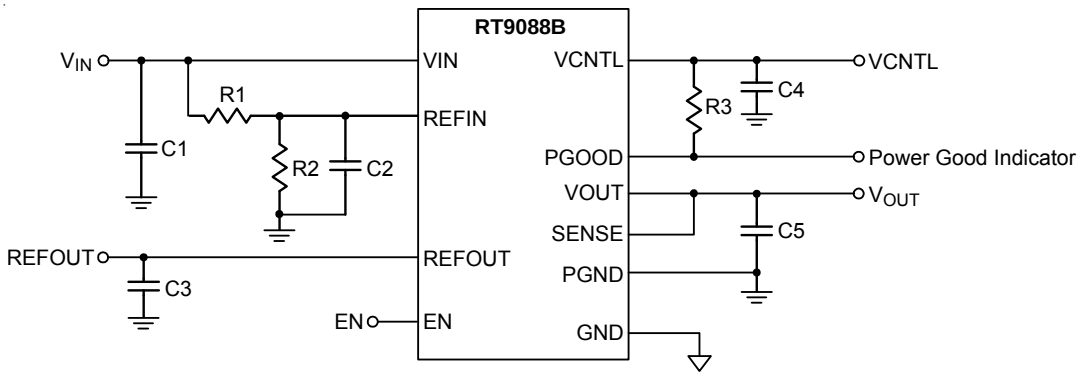
Features

- **VIN Input Voltage Range: 1.1V to 3.5V**
- **VCNTL Input Voltage Range: 2.9V to 5.5V**
- **Support Ceramic Capacitors**
- **Power Good Indicator**
- **10mA Source/Sink Reference Output**
- **Meet DDRI, DDRII JEDEC Spec**
- **Support DDRIII, Low Power DDRIII/DDRIV VTT Applications**
- **Soft-Start Function**
- **UVLO and OCP Protection**
- **Thermal Shutdown**

Applications

- Notebook/Desktop/Server
- Telecom/Datacom, GSM Base Station, LCD-TV/PDP-TV, Copier/Printer, Set-Top Box

Simplified Application Circuit



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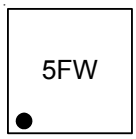
Marking Information

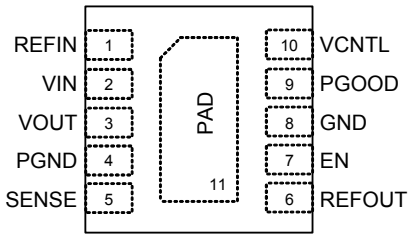


5F : Product Code

W : Date Code

Pin Configuration

(TOP VIEW)



WDFN-10L 2x2

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	REFIN	Reference input.
2	VIN	Power input of the regulator.
3	VOUT	Power output of the regulator.
4	PGND	Power ground of the regulator.
5	SENSE	Voltage sense input for the regulator. Connect to positive terminal of the output capacitor or the load.
6	REFOUT	Reference output. Connect to GND through a 0.1μF ceramic capacitor.
7	EN	Enable control input. For DDR VTT application, connect EN to SLP_S3. For other applications, use EN as the ON/OFF function.
8	GND	Analog ground. Connect to negative terminal of the output capacitor.
9	PGOOD	Power good open-drain output. Connect a pull-up resistor between this pin and VCNTL pin.
10	VCNTL	Control voltage input. Connect this pin to the 3.3V or 5V power supply. A 4.7μF ceramic decoupling capacitor is required.
11 (Exposed Pad)	PAD	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large PGND plane. Connect this PGND plane to other layers with thermal vias to help dissipate heat from the device.

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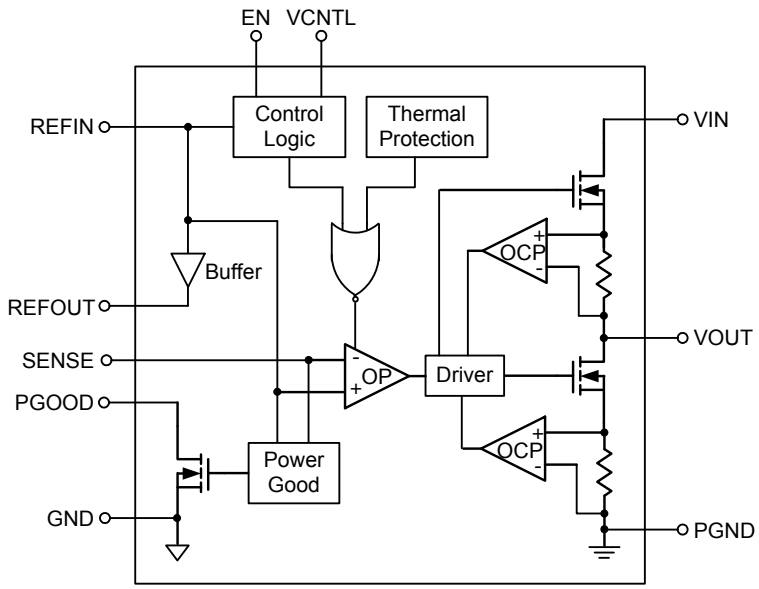
Functional Block Diagram



Operation

The RT9088B is a linear sink/source DDR termination regulator with current capability up to 3A. The RT9088B builds in a high-side N-MOSFET which provides current sourcing and a low-side N-MOSFET which provides current sinking. All the control circuits are supplied by the power VCNTL. In normal operation, the error amplifier OP adjusts the gate driving voltage of the power MOSFET to achieve SENSE voltage well tracking the REFIN voltage.

Both the source and sink currents are detected by the internal sensing resistor, and the OCP function will work to limit the current to a designed value when overload happens. Furthermore, the current will be folded back to be one half if VOUT is out of the power good window.

Buffer

This function provides REFOUT output level which is equal to REFIN level with 10mA source/sink current capability.

Power Good

When the SENSE voltage is in the power good window and lasts for a certain delay time, then the PGOOD pin will be high impedance and the PGOOD voltage will be pulled high by the external resistor.

Control Logic

This block includes VCNTL UVLO, REFIN UVLO and Enable/Disable functions, and provides logic control to the whole chip.

Thermal Protection

Both the high-side and low-side power MOSFETs will be turned off when the junction temperature is higher than typically 160°C, and be released to normal operation when junction temperature falls below 120°C typically.

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Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN, VCNTL ---------- –0.3V to 6V
- Input Voltage, EN, REFIN, SENSE ---------- –0.3V to 6V
- Output Voltage, VOUT, REFOUT, PGOOD ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-10L 2x2 ---------- 2.91W
- Package Thermal Resistance (Note 2)
  WDFN-10L 2x2, θ_{JA} ---------- 34.3°C/W
  WDFN-10L 2x2, θ_{JC} ---------- 9°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Control Input Voltage, VCNTL ---------- 2.9V to 5.5V
- Supply Input Voltage, VIN ---------- 1.1V to 3.5V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 1.5V, V_{EN} = V_{CNTL} = 3.3V, V_{REFIN} = V_{SENSE} = 0.75V, C_{OUT} = 10µF x 3, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
VCNTL Supply Current	I_{VCNTL}	V_{EN} = V_{CNTL}, No Load	--	0.7	1	mA
VCNTL Shutdown Current	I_{SHDN_VCNTL}	V_{EN} = 0V, V_{REFIN} = 0V, No Load	--	65	80	µA
		V_{EN} = 0V, V_{REFIN} > 0.4V, No Load	--	200	400	µA
VIN Supply Current	I_{VIN}	V_{EN} = V_{CNTL}, No Load	--	1	50	µA
VIN Shutdown Current	I_{SHDN_VIN}	V_{EN} = 0V, No Load	--	0.1	50	µA
Output						
VTT Output Voltage	V_{OUT}	V_{IN} = 1.5V, V_{REFIN} = 0.75V, I_{OUT} = 0A	--	0.75	--	V
		V_{IN} = 1.35V, V_{REFIN} = 0.675V, I_{OUT} = 0A	--	0.675	--	V
		V_{IN} = 1.2V, V_{REFIN} = 0.6V, I_{OUT} = 0A	--	0.6	--	V
REFIN, VTT Output Voltage Offset	V_{OUT_OS}	I_{OUT} = ±2A, V_{LDOIN} = 1.5V, V_{REFOUT} = 0.75V	–25	--	25	mV
		I_{OUT} = ±2A, V_{LDOIN} = 1.35V, V_{REFOUT} = 0.675V	–25	--	25	
		I_{OUT} = ±2A, V_{LDOIN} = 1.2V, V_{REFOUT} = 0.6V	–25	--	25	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VOUT Source Current Limit	$I_{LIM_VOUT_SR}$	VOUT in PGOOD Window	3.5	--	5.5	A
VOUT Sink Current Limit	$I_{LIM_VOUT_SK}$	VOUT in PGOOD Window	3.5	--	5.5	A
VOUT Discharge Resistance	$R_{DISCHARGE}$	V_{REFIN} = 0V, V_{OUT} = 0.3V, V_{EN} = 0V	--	18	25	Ω
Power Good Comparator						
PGOOD Threshold	V_{TH_PGOOD}	V_{SENSE} lower threshold with respect to REFOUT	−25	−20	−15	%
		V_{SENSE} upper threshold with respect to REFOUT	15	20	25	
		PGOOD Hysteresis	--	5	--	
PGOOD Start-Up Delay	$T_{PGDELAY1}$	Start-up rising delay, V_{SENSE} within PGOOD range	--	2	--	ms
Output Low Voltage	V_{LOW_PGOOD}	I_{PGOOD} = 4mA	--	--	0.4	V
PGOOD Falling Delay	$t_{PGDELAY2}$	Falling delay, V_{SENSE} is out of PGOOD range	--	10	--	μs
Leakage Current	$I_{LEAKAGE_PGOOD}$	V_{SENSE} = V_{REFIN} (PGOOD high impedance), V_{PGOOD} = V_{IN} + 0.3V	--	--	1	μA
REFIN and REFOUT						
REFIN Input Current	I_{REFIN}	V_{EN} = V_{CNTL}	--	--	1	μA
REFIN Voltage Range	V_{REFIN}		0.5	--	1.8	V
REFIN Under-Voltage Lockout	V_{UVLO_REFIN}	REFIN Rising	360	390	420	mV
		Hysteresis	--	20	--	
REFOUT Voltage Tolerance to VREFIN	V_{TOL_REFOUT}	−10mA < I_{REFOUT} < 10mA, V_{REFIN} = 0.75V	−15	--	15	mV
		−10mA < I_{REFOUT} < 10mA, V_{REFIN} = 0.675V	−15	--	15	
		−10mA < I_{REFOUT} < 10mA, V_{REFIN} = 0.6V	−15	--	15	
REFOUT Source Current Limit	$I_{LIM_REFOUT_SR}$	V_{REFOUT} = 0V	10	40	--	mA
REFOUT Sink Current Limit	$I_{LIM_REFOUT_SK}$	V_{REFOUT} = REFIN + 1V	10	40	--	mA
UVLO/EN						
UVLO Threshold	V_{UVLO_VCNTL}	Rising	2.5	2.7	2.85	V
		Hysteresis	--	120	--	mV
EN Input Voltage Logic-High	V_{IN_H}		1.7	--	--	V
EN Input Voltage Logic-Low	V_{IN_L}		--	--	0.3	
EN Turn-On Delay	t_{DELAY}	EN turn on to V_{OUT} rising (reference Note 5)	--	--	7	μs
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}	Shutdown Temperature	--	160	--	°C
		Hysteresis	--	15	--	

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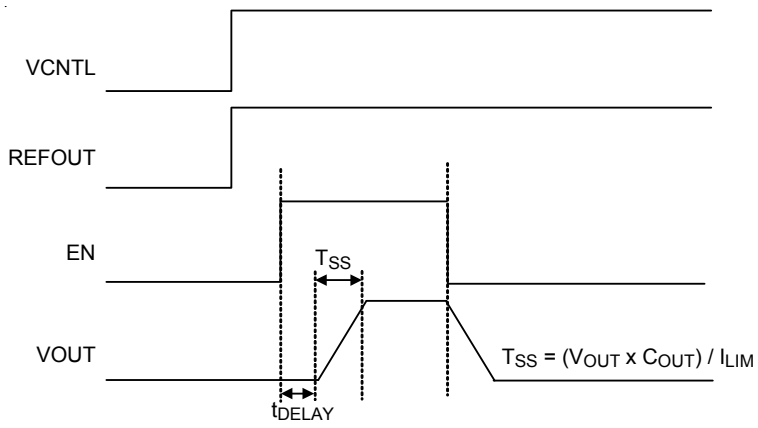
Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. t_{DELAY} is the period from EN turn on to V_{OUT} rising as shown in below diagram. While T_{SS} is the rising period of V_{OUT}, the formula used to calculated this rising period is $T_{SS} = (V_{OUT} \times C_{OUT})/I_{LIM}$. It's base on the value of output capacitor C_{OUT}, the settled output voltage V_{OUT} and the output current limit I_{LIM}.



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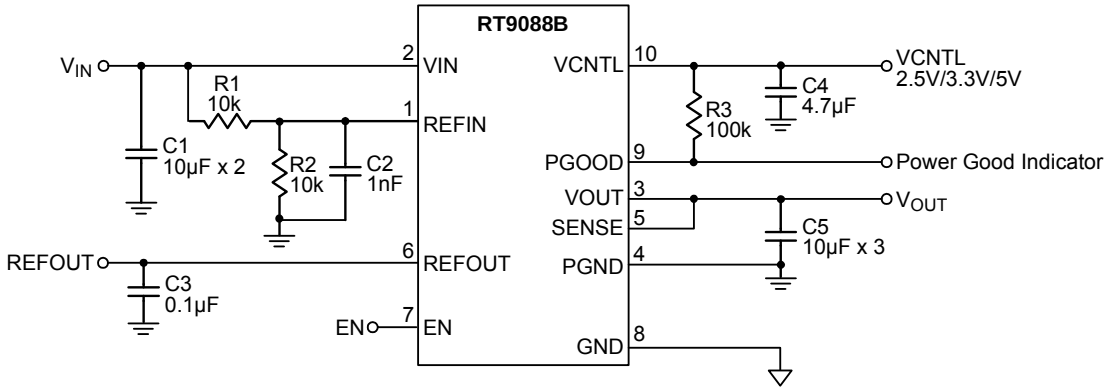
Typical Application Circuit



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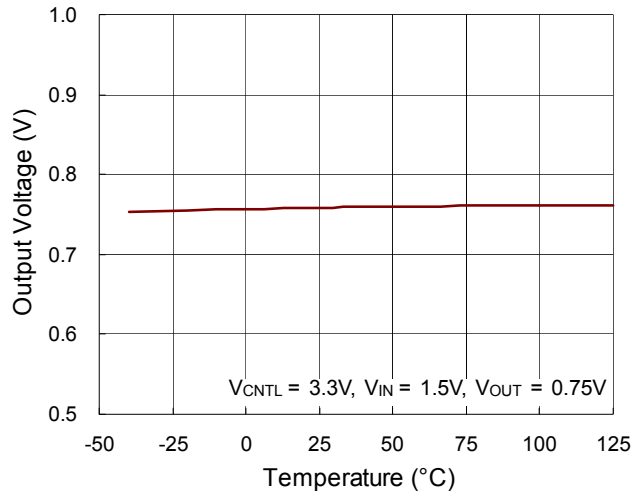
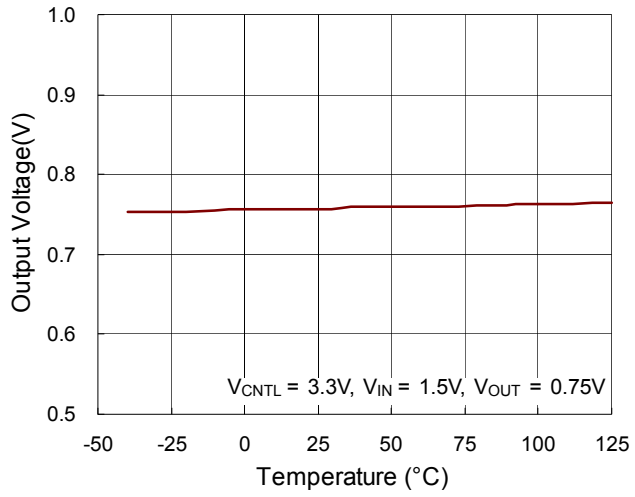
Typical Operating Characteristics

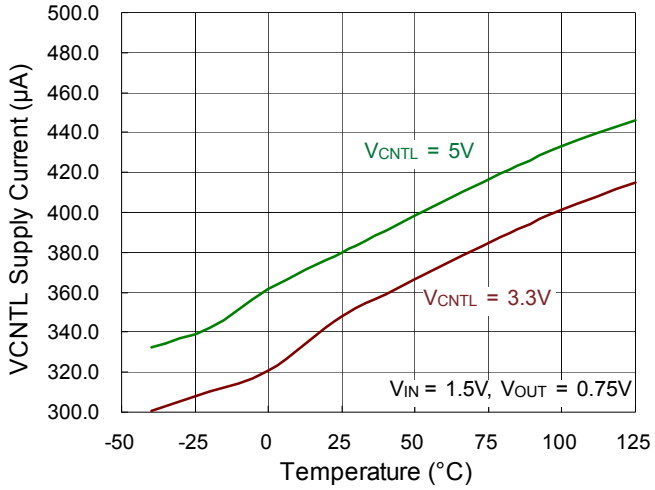
Output Voltage vs. Temperature



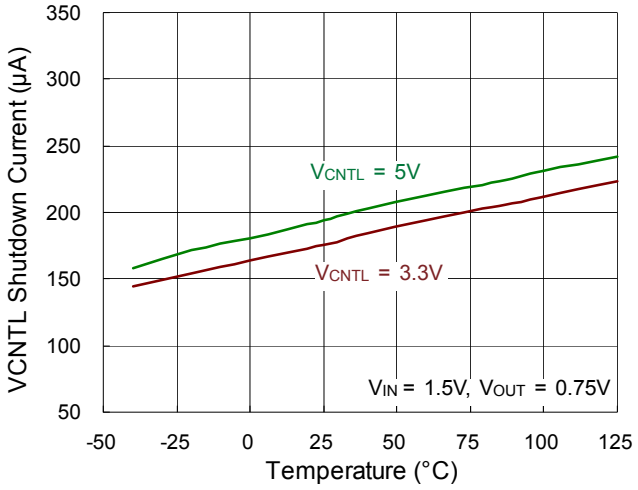
REFOUT Voltage vs. Temperature



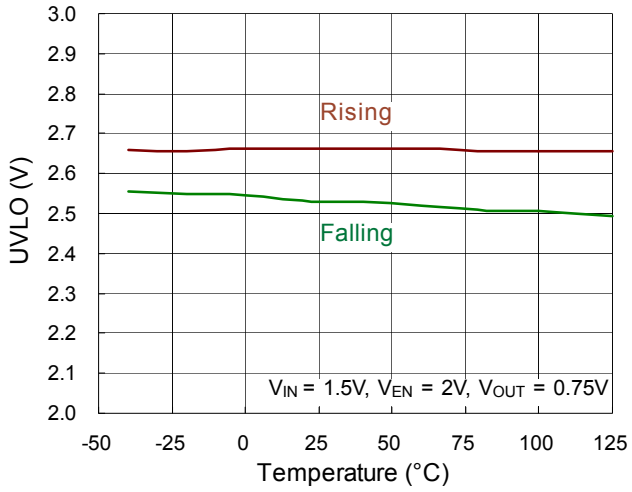
VCNTL Supply Current vs. Temperature



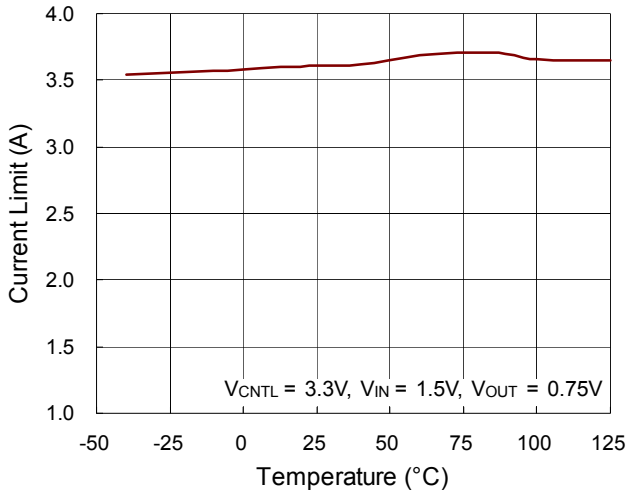
VCNTL Shutdown Current vs. Temperature



UVLO vs. Temperature



Sourcing Current Limit vs. Temperature



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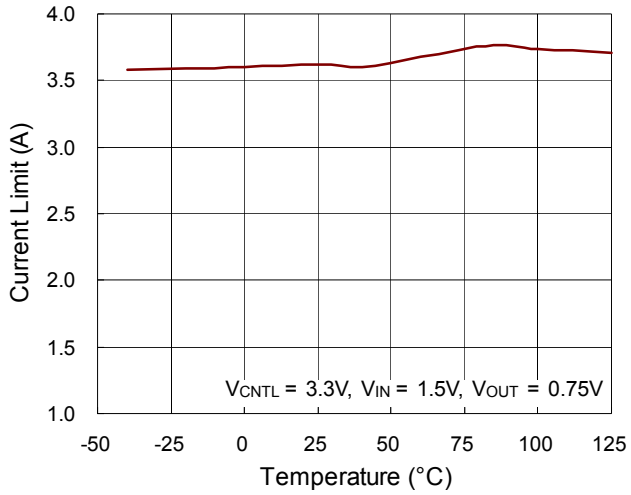
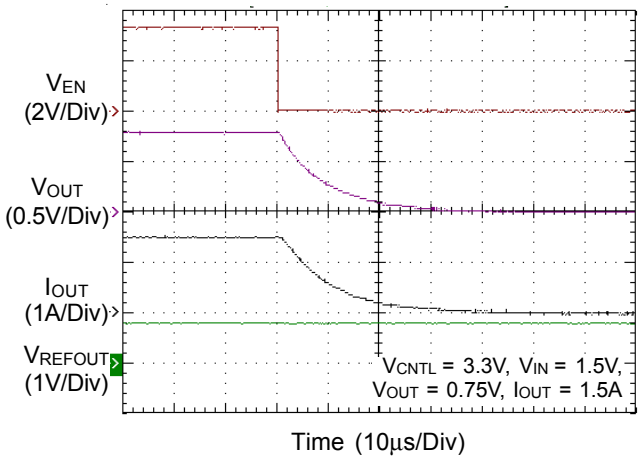
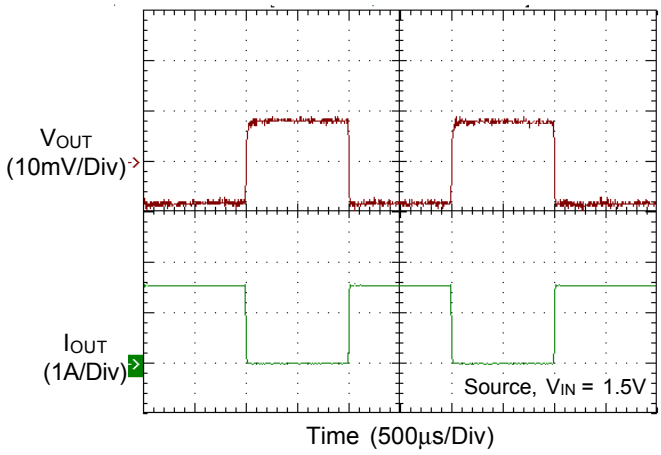
Sinking Current Limit vs. Temperature



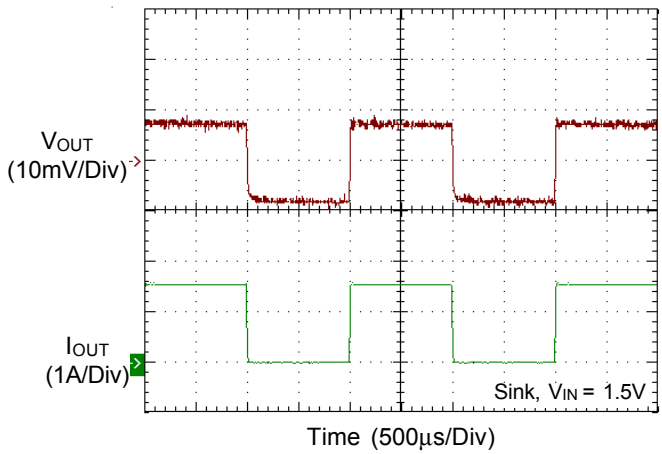
Power Off from EN



0.75V_{OUT} @ 1.5A Transient Response



0.75V_{OUT} @ 1.5A Transient Response



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Application Information

The RT9088B is a 3A sink/source tracking termination regulator. It is specifically designed for low-cost and low-external component count system such as notebook PC applications. The RT9088B possesses a high speed operating amplifier that provides fast load transient response.

Capacitor Selection

Good bypassing is recommended from VIN to GND to help improve AC performance. A 10μF or greater input capacitor placed as close as possible to the IC is recommended. The input capacitor must be placed at a distance of less than 0.5 inches from the VIN pin of the IC.

The 1μF ceramic capacitor added close to the VCNTL pin should be kept away from any parasitic impedance from the supply power. For stable operation, the total capacitance of the ceramic capacitor at the VOUT output terminal must be larger than 30μF. The RT9088B is designed specifically to work with low ESR ceramic output capacitor in space saving and performance consideration. Larger output capacitance can reduce the noise and improve load transient response, stability and PSRR. The output capacitor should be located near the VOUT output terminal pin as close as possible.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-10L 2x2, the thermal resistance, θ_{JA}, is 34.3°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (34.3°C/W) = 2.91W for a WDFN-10L 2x2 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

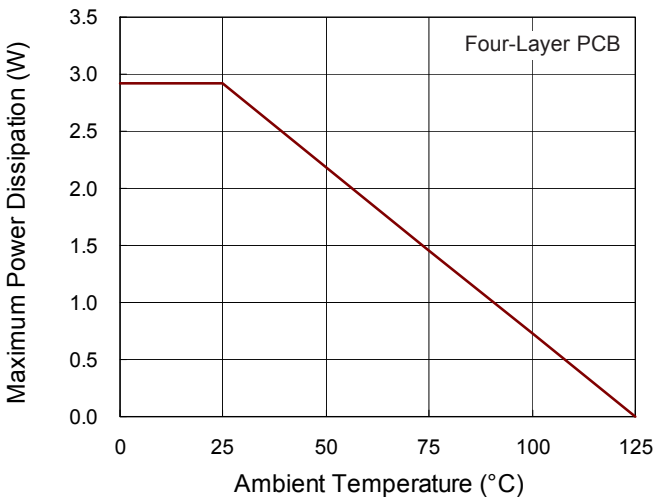

Figure 1. Derating Curve of Maximum Power Dissipation

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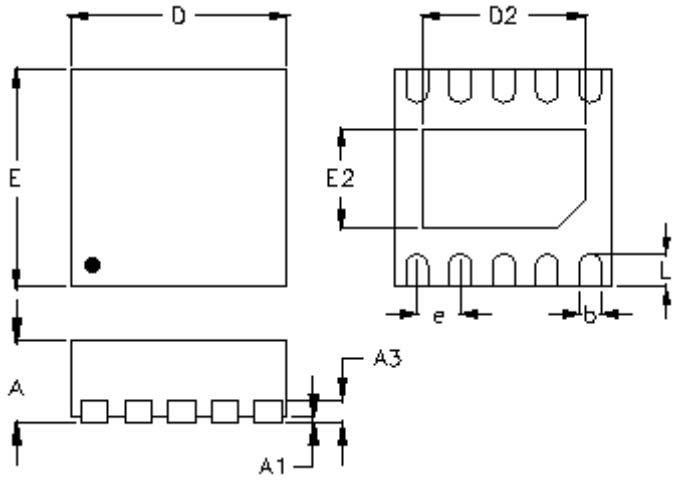
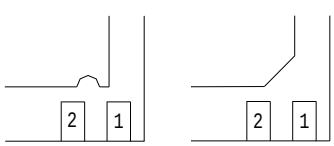
Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	1.900	2.100	0.075	0.083
D2	1.450	1.550	0.057	0.061
E	1.900	2.100	0.075	0.083
E2	0.850	0.950	0.033	0.037
e	0.400		0.016	
L	0.250	0.350	0.010	0.014

W-Type 10L DFN 2x2 Package

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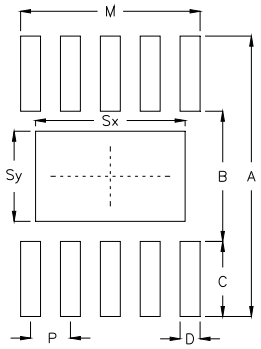
Footprint Information



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2x2-10	10	0.40	2.80	1.30	0.75	0.20	1.50	0.90	1.80	±0.05

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