250mA, Ultra-Low Noise, Low Quiescent Current, LDO Regulator

General Description

The RT9092 is a high performance positive low dropout (LDO) regulator designed for applications requiring very low dropout voltage and ultra-high Power Supply Ripple Rejection (PSRR) low noise, low quiescent current, and the IC can supply up to 250mA output current. The input voltage range is from 2.2V to 5.5V. The device is designed to work with a 1μF input and a 1μF output ceramic capacitor (no separate noise bypass capacitor is required).

The RT9092 features a precise 2% output regulation over line, load, and temperature variations in WL-CSP-4B 0.67x0.67 (BSC), ZQFN-4L 1x1 and SOT-23-5 packages. The output voltage is available from 1.2V to 4.5V in 25mV steps.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

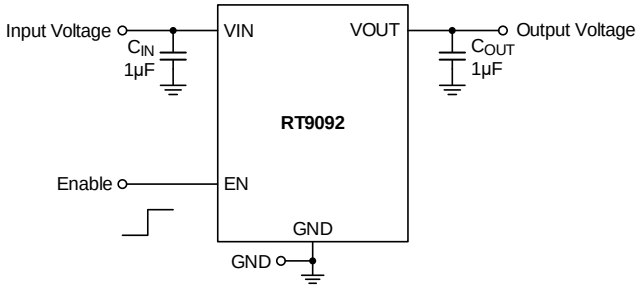
Applications

- Mobile Phones, Tablets
- Digital Cameras and Audio Devices
- Portable and Battery-Powered Equipment
- Portable Medical Equipment
- Smart Meters
- IP Cameras
- Drones
- Telecom/Networking Cards
- Wireless Infrastructures
- Medical Equipment

Features

- **Input Voltage Range: 2.2V to 5.5V**
- **Adjustable Output Voltage: 1.2V to 4.5V**
- **PSRR**
  - **80dB @ 1kHz (20mA)**
  - **70dB @ 10kHz (20mA)**
- **Output Current: 250mA**
- **Very Low Dropout: 120mV**
- **Very Low I_Q (Enabled): 16μA**
- **Virtually Zero I_Q (Disable): < 1μA**
- **Very Low I_G (Enabled): 16μA**
- **Start-Up Time: 250μs**
- **−40°C to 125°C Operating Junction Temperature Range**
- **Excellent Noise Immunity**
- **Fast Response Over Load and Line Transient**
- **Stable with a 1μF Input and Output Ceramic Capacitors**
- **Accurate Output Voltage 2% Over Load, Line, Process, and Temperature Variations**
- **Overcurrent Protection**
- **Over-Temperature Protection**

Simplified Application Circuit



Ordering Information

RT9092□-□□

- Packing
  A: Standrad
- Output Voltage
  (Refer to Output Voltage Table)
- Package Type
  P: WL-CSP-4B 0.67x0.67 (BSC)
  N: ZQFN-4L 1x1
  D: SOT-23-5

Note:

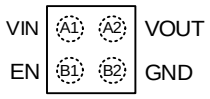
Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

Marking Information

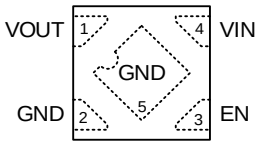
For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Pin Configuration

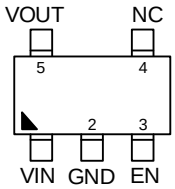
(TOP VIEW)



WL-CSP-4B 0.67x0.67 (BSC)



ZQFN-4L 1x1



SOT-23-5

Functional Pin Description

Pin No.			Pin Name	Pin Function
WL-CSP-4B 0.67x0.67 (BSC)	ZQFN-4L 1x1	SOT-23-5		
A1	4	1	VIN	Supply input. A minimum of 1μF ceramic capacitor should be placed as close as possible to this pin for better noise rejection.
A2	1	5	VOUT	Output of the regulator. Decouple this pin to GND with at least 1μF for stability.
B1	3	3	EN	Enable control input. Connecting this pin to logic high enables the regulator or driving this pin low puts it into shutdown mode. EN can be connected to GND if not used.
B2	2	2	GND	Common ground.
--	--	4	NC	No internal connection.
--	5 (Exposed Pad)	--	GND	Thermal pad for ZQFN-4L 1x1 package, connect to GND.

RT9092 Output Voltage Table

VOUT = 1.2V to 1.575V	
VOUT	Output Voltage Code
1.2	AA
1.225	AB
1.25	AC
1.275	AD
1.3	AE
1.325	AF
1.35	AG
1.375	AH
1.4	AI
1.425	AJ
1.45	AK
1.475	AL
1.5	AM
1.525	AN
1.55	AO
1.575	AP

VOUT = 1.6V to 1.975V	
VOUT	Output Voltage Code
1.6	AQ
1.625	AR
1.65	AS
1.675	AT
1.7	AU
1.725	AV
1.75	AW
1.775	AX
1.8	AY
1.825	AZ
1.85	BA
1.875	BB
1.9	BC
1.925	BD
1.95	BE
1.975	BF

VOUT = 2V to 2.375V	
VOUT	Output Voltage Code
2	BG
2.025	BH
2.05	BI
2.075	BJ
2.1	BK
2.125	BL
2.15	BM
2.175	BN
2.2	BO
2.225	BP
2.25	BQ
2.275	BR
2.3	BS
2.325	BT
2.35	BU
2.375	BV

VOUT = 2.4V to 2.775V	
VOUT	Output Voltage Code
2.4	BW
2.425	BX
2.45	BY
2.475	BZ
2.5	CA
2.525	CB
2.55	CC
2.575	CD
2.6	CE
2.625	CF
2.65	CG
2.675	CH
2.7	CI
2.725	CJ
2.75	CK
2.775	CL

VOUT = 2.8V to 3.175V	
VOUT	Output Voltage Code
2.8	CM
2.825	CN
2.85	CO
2.875	CP
2.9	CQ
2.925	CR
2.95	CS
2.975	CT
3	CU
3.025	CV
3.05	CW
3.075	CX
3.1	CY
3.125	CZ
3.15	DA
3.175	DB

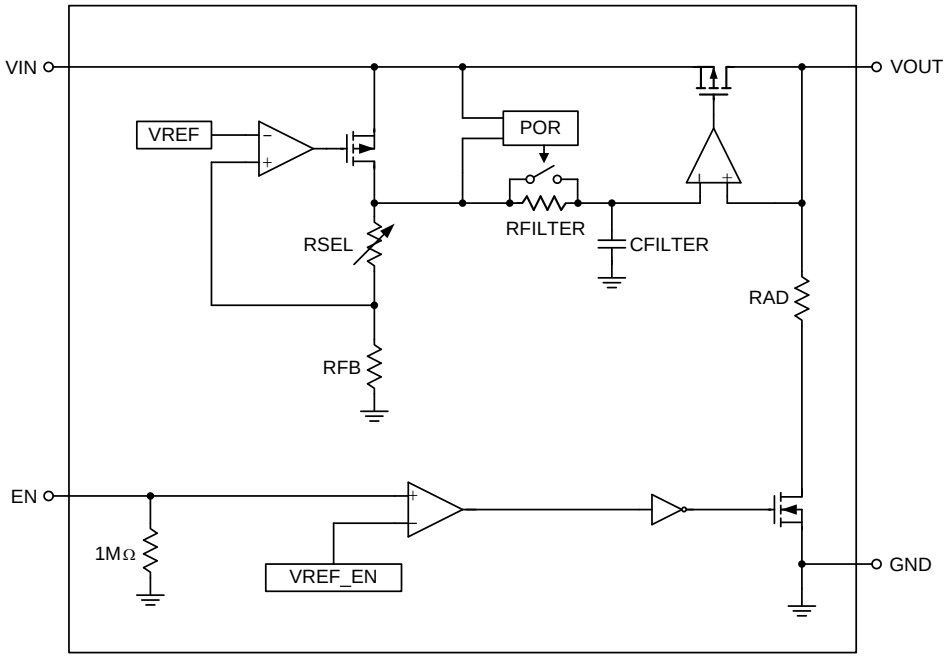
VOUT = 3.2V to 3.575V	
VOUT	Output Voltage Code
3.2	DC
3.225	DD
3.25	DE
3.275	DF
3.3	DG
3.325	DH
3.35	DI
3.375	DJ
3.4	DK
3.425	DL
3.45	DM
3.475	DN
3.5	DO
3.525	DP
3.55	DQ
3.575	DR

VOUT = 3.6V to 3.975V	
VOUT	Output Voltage Code
3.6	DS
3.625	DT
3.65	DU
3.675	DV
3.7	DW
3.725	DX
3.75	DY
3.775	DZ
3.8	FA
3.825	FB
3.85	FC
3.875	FD
3.9	FE
3.925	FF
3.95	FG
3.975	FH

VOUT = 4V to 4.375V	
VOUT	Output Voltage Code
4	FI
4.025	FJ
4.05	FK
4.075	FL
4.1	FM
4.125	FN
4.15	FO
4.175	FP
4.2	FQ
4.225	FR
4.25	FS
4.275	FT
4.3	FU
4.325	FV
4.35	FW
4.375	FX

VOUT = 4.4V to 4.5V	
VOUT	Output Voltage Code
4.4	FY
4.425	FZ
4.45	GA
4.475	GB
4.5	GC

Functional Block Diagram



Operation

Basic Operation

The RT9092 is a high performance positive low dropout (LDO) regulator designed for applications requiring very low dropout voltage, ultra-high Power Supply Ripple Rejection (PSRR), low noise and low quiescent current that can supply up to 250mA output current. The input voltage range is from 2.2V to 5.5V. The RT9092 features a precise 2% output regulation over line, load, and temperature variations. The output voltage is available from 1.2V to 4.5V in 25mV steps. The minimum required output capacitance for stable operation is 1μF (X5R or X7R) effective capacitance after consideration of the temperature and voltage coefficient of the capacitor.

Enable and Shutdown Operation

The RT9092 goes into shutdown mode when the EN pin is in a logic low condition. In this condition, the pass transistor, error amplifier, and bandgap are all turned off, reducing the supply current to only 1μA (max.). If the shutdown mode is not required, the EN pin can be directly tied to VIN pin to keep the LDO on.

Over-Temperature Protection (OTP)

The over-temperature protection function will turn off the P-MOSFET when the junction temperature exceeds 160°C (typ.), and the output current exceeds 250mA. Once the junction temperature cools down by approximately 26°C (typ.), the regulator will automatically resume operation.

Current-limit Protection

The RT9092 provides current limit function to prevent the device from damages during overload or shorted-circuit condition. This current is detected by an internal sensing transistor.

Error Amplifier

The Error Amplifier compares the internal reference voltage with the output feedback voltage from the internal divider, and controls the Gate voltage of P-MOSFET to support good line regulation and load regulation at output voltage.

Output Automatic Discharge

The RT9092 output employs an internal 10Ω (typ.) pull down resistance to discharge the output when the EN pin is low, and the device is disabled.

Absolute Maximum Ratings (Note 1)

- VIN, EN to GND ---------- –0.3V to 6V
- VOUT to GND ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  - WL-CSP-4B 0.67x0.67 (BSC) ---------- 1.08W
  - ZQFN-4L 1x1 ---------- 1.11W
  - SOT-23-5 ---------- 0.57W
- Package Thermal Resistance (Note 2)
  - WL-CSP-4B 0.67x0.67 (BSC), θ_{JA} ---------- 91.8°C/W
  - ZQFN-4L 1x1, θ_{JA} ---------- 89.8°C/W
  - ZQFN-4L 1x1, θ_{JC} ---------- 34°C/W
  - SOT-23-5, θ_{JA} ---------- 174.5°C/W
  - SOT-23-5, θ_{JC} ---------- 76.8°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage Range ---------- 2.2V to 5.5V
- Output Current ---------- 0mA to 250mA
- EN Voltage ---------- 0V to V_{IN}
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = V_{OUT} + 1V, V_{EN} = 1.2V, I_{OUT} = 1mA, C_{IN} = 1μF, C_{OUT} = 1μF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage	V_{IN}	V_{IN} = V_{OUT} + 1V	2.2	--	5.5	V
Output Voltage Accuracy (Note 5)	V_{OUT_ACC}	V_{IN} = (V_{OUT} + 1V) to 5.5V, I_{OUT} = 1 mA to 250mA, package: WL-CSP-4B 0.67x0.67 (BSC)	–2	--	2	%V_{OUT}
		V_{IN} = (V_{OUT} + 1V) to 5.5V, I_{OUT} = 1 mA to 250mA, package: ZQFN-4L 1x1 and SOT-23-5	–3	--	3	
Line Regulation	$V_{OUT\_LineReg}$	V_{IN} = (V_{OUT} + 1V) to 5.5V, I_{OUT} = 1mA	--	0.02	--	%/V
Load Regulation	$V_{OUT\_LoadReg}$	I_{OUT} = 1mA to 250mA	--	0.001	--	%/mA
LOAD Current	I_{OUT}	Operation in stable and regulated output voltage	0	--	250	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Output Current	I_{OUT_MAX}		250	--	--	mA
Quiescent Current (Note 6)	I_Q	V_{EN} = 1.2V, I_{OUT} = 0mA	--	16	25	µA
		V_{EN} = 1.2V, I_{OUT} = 250mA (Note 7)	--	300	425	
		V_{EN} = 0.3V (Disable)	--	0.2	1	
Ground Current (Note 8)	I_G	V_{EN} = 1.2V, I_{OUT} = 0mA	--	16	--	µA
Dropout Voltage (Note 9)	V_{DROP}	$V_{OUT} \geq$ 2.2V, I_{OUT} = 100mA	--	50	--	mV
		$V_{OUT} \geq$ 2.2V, I_{OUT} = 250mA (WL-CSP-4B 0.67x0.67 (BSC) and SOT-23-5 package)	--	120	200	
		$V_{OUT} \geq$ 2.2V, I_{OUT} = 250mA (ZQFN-4L 1x1 package)	--	--	250	
Power Supply Rejection Ration (Note 7)	PSRR	f = 100Hz, I_{OUT} = 20mA	--	80	--	dB
		f = 1kHz, I_{OUT} = 20mA	--	80	--	
		f = 10kHz, I_{OUT} = 20mA	--	70	--	
		f = 100kHz, I_{OUT} = 20mA	--	60	--	
Output Noise Voltage (Note 7)	e_N	BW = 10Hz to 100kHz, I_{OUT} = 1mA	--	10	--	µVrms
		BW = 10Hz to 100kHz, I_{OUT} = 250mA	--	6.5	--	
Output Automatic Discharge Pulldown Resistance	R_{AD}	V_{EN} < 0.3V	--	10	--	Ω
EN Pin Logic Input Threshold						
Low Input Threshold	V_{IL}	V_{IN} = 2.2 to 5.5V, V_{EN} falling until the output is disabled	--	--	0.4	V
High Input Threshold	V_{IH}	V_{IN} = 2.2 to 5.5V, V_{EN} rising until the output is enabled	1.2	--	--	V
Input Current at EN PIN	I_{EN}	V_{EN} = 5.5V and V_{IN} = 5.5V	--	5.5	--	µA
		V_{EN} = 0V and V_{IN} = 5.5V	--	0.001	--	
Transient Characteristics						
Line Transient (Note 7)	ΔV_{OUT_Line}	V_{IN} = V_{OUT} + 1V to V_{OUT} + 1.6V in 30µs	–1	--	--	mV
		V_{IN} = V_{OUT} + 1.6V to V_{OUT} + 1V in 30µs	--	--	1	
Load Transient (Note 7)	ΔV_{OUT_Load}	I_{OUT} = 1mA to 250mA in 10µs	–40	--	--	mV
		I_{OUT} = 250mA to 1mA in 10µs	--	--	40	
Overshoot on Start-Up (Note 7)	$\Delta V_{OUT\_Startup}$	Stated as a percentage of $V_{OUT(NOM)}$	--	--	5	%
Set Up Time	t_{SETUP}	From V_{EN} > V_{IH} to V_{OUT} start rising	--	250	--	µs
Soft-Start Time	t_{SS}	Time from 10% rising to 90% of V_{OUT} setting	50	--	700	µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Protection						
Short Circuit Current Limit	I_{SC}	Temp = 25°C	250	500	--	mA
Thermal Shutdown	T_{SD}		--	160	--	°C
Thermal Hysteresis	T_{SD_H}		--	26	--	°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the ZQFN-4L 1x1 package and at the case top of the SOT-23-5 package.

Note 3. Devices are ESD sensitive.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Maximum available load $I_{OUT\_SUPPORT}$ with different V_{IN} due to thermal consideration refers to the curves at Typical Operating Characteristics.

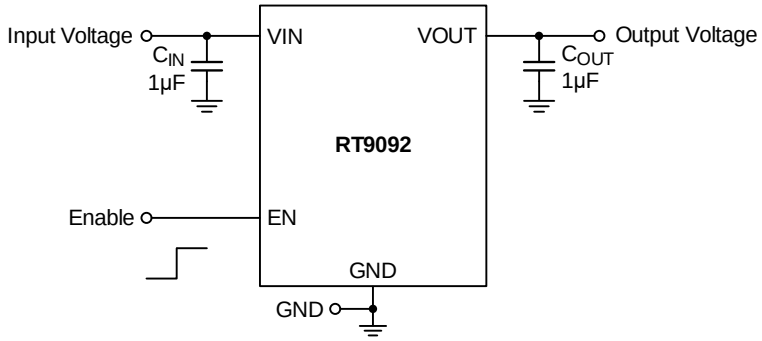
Note 6. Quiescent current is defined here as the difference in current between the input voltage source and the load at VOUT.

Note 7. This specification is guaranteed by design.

Note 8. Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.

Note 9. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100mV below its nominal value.

Typical Application Circuit

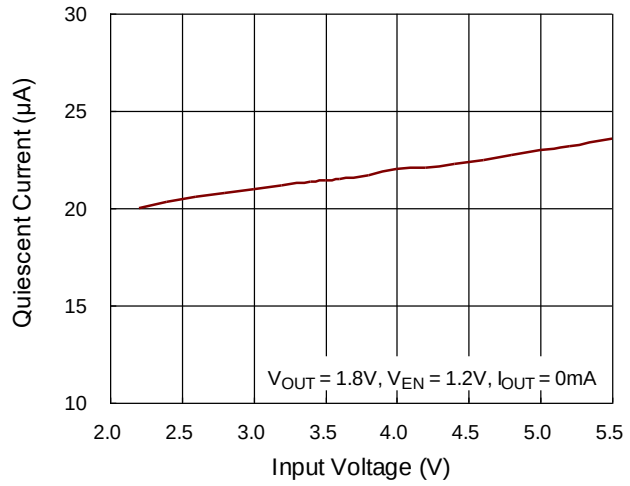


BOM List

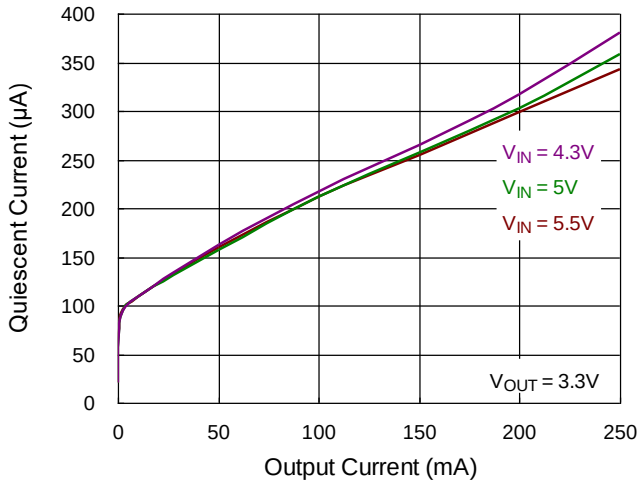
Reference	Part Number	Value	Package	Manufacturer
CIN, COUT	GRM155R61A105KE01	1µF/10V/X5R	0402	MURATA

Typical Operating Characteristics

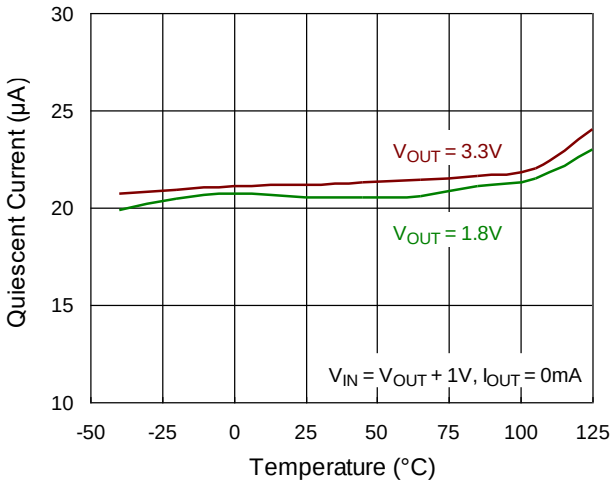
Quiescent Current vs. Input Voltage



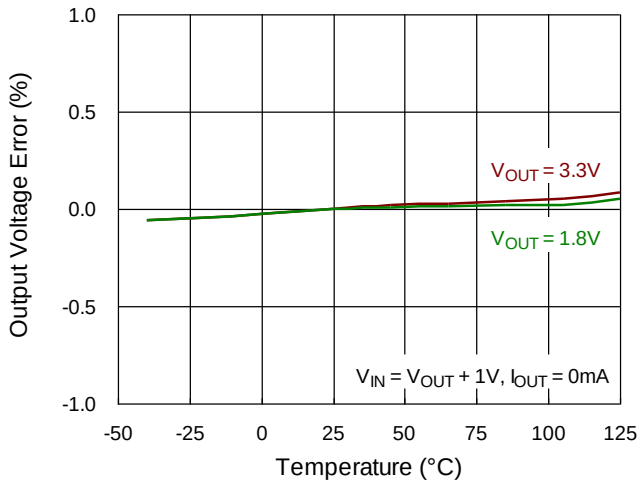
Quiescent Current vs. Output Current



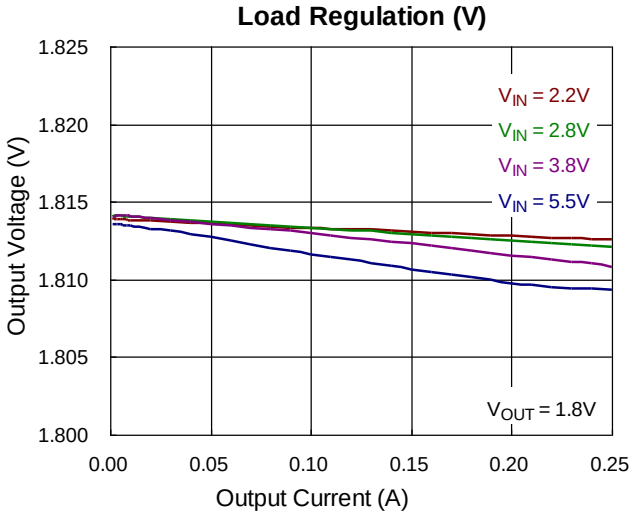
Quiescent Current vs. Temperature



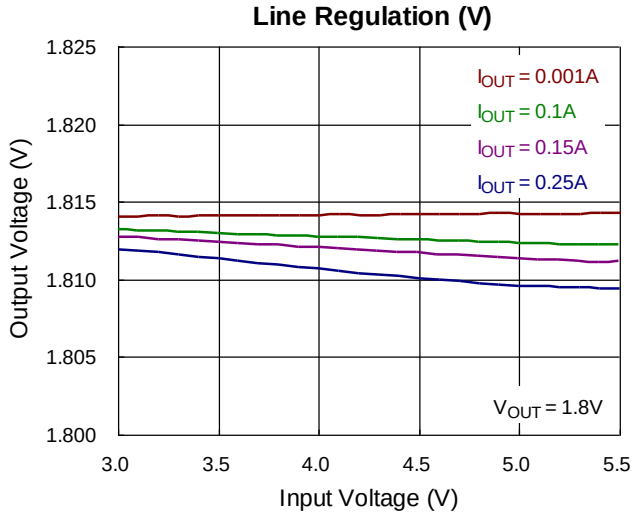
Output Voltage Error vs. Temperature



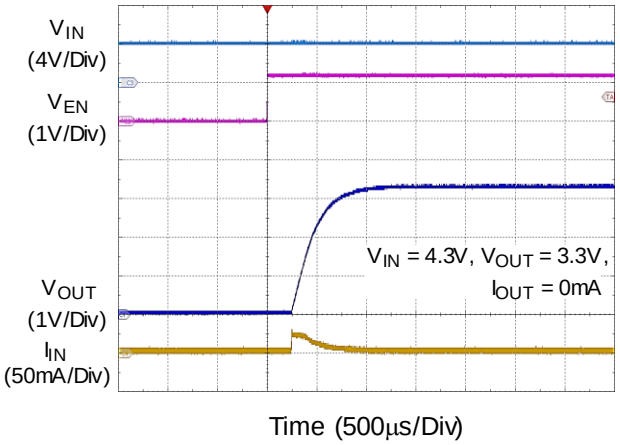
Load Regulation (V)



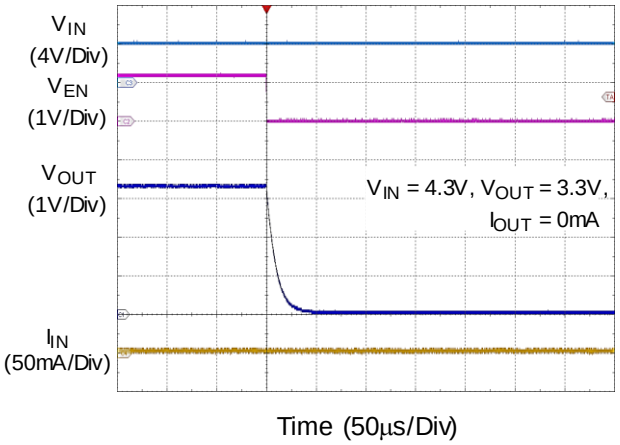
Line Regulation (V)



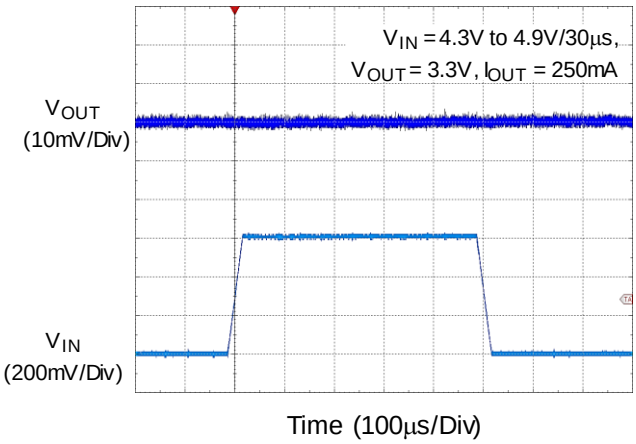
Power On from EN



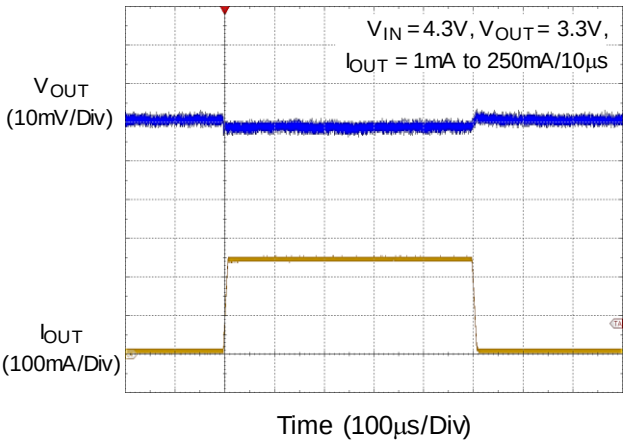
Power Off from EN



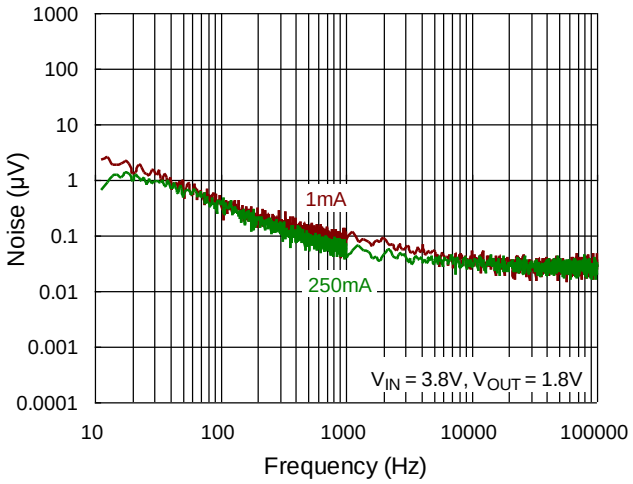
Line Transient



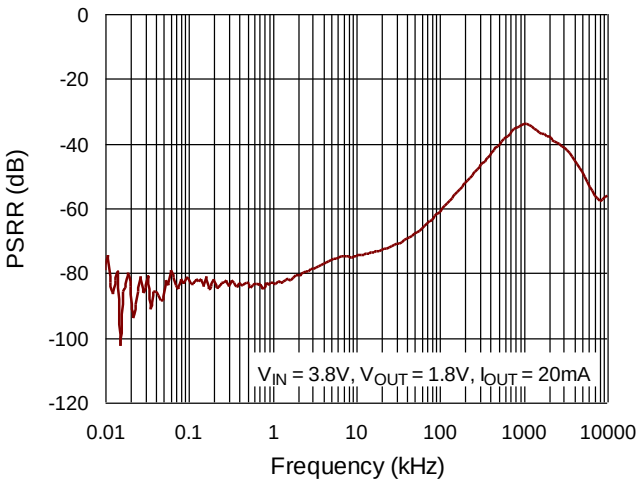
Load Transient



Noise Density Test



PSRR Loads Averaged 10Hz to 10MHz



Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

Like any low dropout linear regulator, the RT9092's external input and output capacitors must be properly selected for stability and performance. Use a 1μF (X5R or X7R) or larger input capacitor and place it close to the IC's VIN and GND pins. Output capacitor effective capacitance larger than 1μF (X5R or X7R) requirement may be used. Place the output capacitor close to the IC's VOUT and GND pins. Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

Chip Enable Operation

The RT9092 EN pin internal resistor is 1MΩ to GND The EN pin is the chip enable input. Pulling the EN pin low (< 0.4V) will shut down the device. During shutdown mode, the RT9092 quiescent current drops to lower than 1μA. Driving the EN pin to high (> 1.2V, < 5.5V) will turn on the device again.

Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage V_{DROP} can also be expressed as the voltage drop on the pass-FET at specific output current (I_{RATED}) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized as an resistance $R_{DS(ON)}$. Thus the dropout voltage can be defined as ($V_{DROP} = V_{VIN} - V_{VOUT} = R_{DS(ON)} \times I_{RATED}$). For normal operation, the suggested LDO operating range is ($V_{VIN} > V_{VOUT} + 0.2V$) for good transient response and PSRR ability. Conversely, operating at the ohmic region will degrade these performance severely. Additionally, the output of RT9092 is automatically discharged through an internal 10Ω pull-down resistance when the EN pin is low and the device is disabled.

C_{IN} and C_{OUT} Selection

Like any low dropout regulator, the external capacitors of the RT9092 must be carefully selected for regulator stability and performance. Using a capacitor of at least 1μF (X5R or X7R) is suitable. With a reasonable PCB layout, the ceramic output capacitor can be placed up to 5cm and the ceramic input capacitor can be placed up to 1cm of the chip. Any good quality ceramic capacitor can be used. However, a capacitor with larger value and lower ESR (Equivalent Series Resistance) is recommended since it will provide better PSRR and line transient response.

The RT9092 is designed specifically to work with low ESR ceramic output capacitor for space saving and performance consideration. Using a ceramic capacitor with capacitance of at least 1μF (X5R or X7R) on the RT9092 output ensures stability.

Minimum Operating Input Voltage (V_{IN})

The RT9092 does not include any dedicated UVLO circuitry. The RT9092 internal circuitry is not fully functional until V_{IN} is at least 2.2V. The output voltage is not regulated until V_{IN} has reached at least the greater of 2.2 V or (V_{OUT} + 0.2V).

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-4B 0.67x0.67 (BSC) package, the thermal resistance, θ_{JA}, is 91.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a ZQFN-4L 1x1 package, the thermal resistance, θ_{JA}, is 89.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a SOT-23-5 package, the thermal resistance, θ_{JA}, is 174.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (91.8°C/W) = 1.08W for a WL-CSP-4B 0.67x0.67 (BSC) package.

$P_{D(MAX)}$ = (125°C - 25°C) / (89.8°C/W) = 1.11W for a ZQFN-4L 1x1 package.

$P_{D(MAX)}$ = (125°C - 25°C) / (174.5°C/W) = 0.57W for a SOT-23-5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

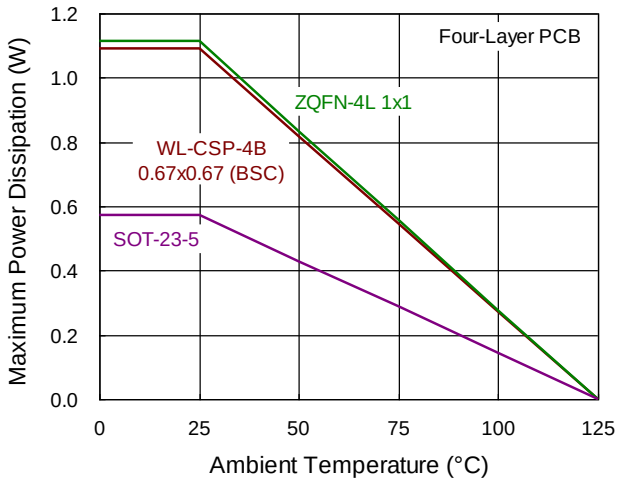


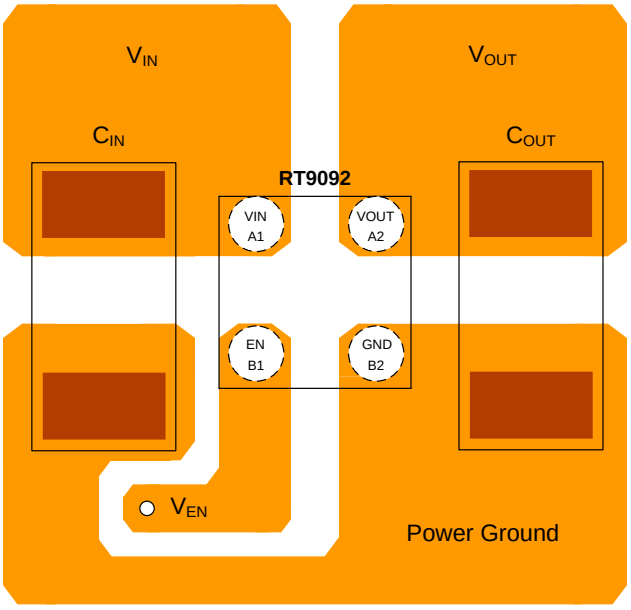
Figure 1. Derating Curve of Maximum Power Dissipation

Layout Considerations

The dynamic performance of the RT9092 is dependent on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the RT9092.

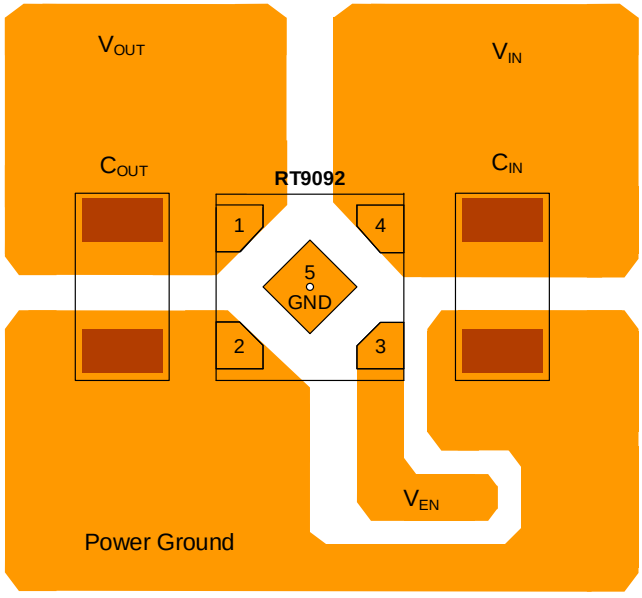
Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the RT9092, and as close to the package as possible is practical. The ground connections for C_{IN} and C_{OUT} must be back to the RT9092 ground pin using a copper trace as wide and short as possible.

Connections using long trace lengths, narrow trace widths, and/or connections through vias must be avoided. These added parasitic inductances and resistance may result in inferior performance especially during transient conditions.



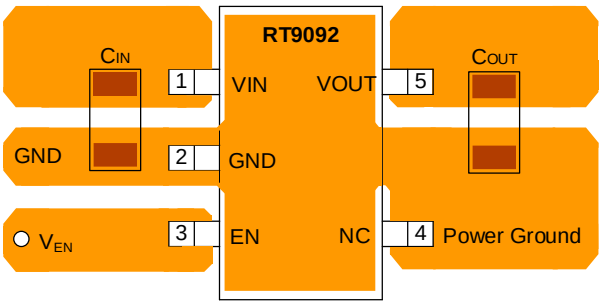
GND ball (B2) connect to second layer ground path by Via to increase cooling area directly.

Figure 2. WL-CSP-4B 0.67x0.67 (BSC) Layout Guide



GND Pad (2) and (5) connect to second layer ground path by Via to increase cooling area directly.

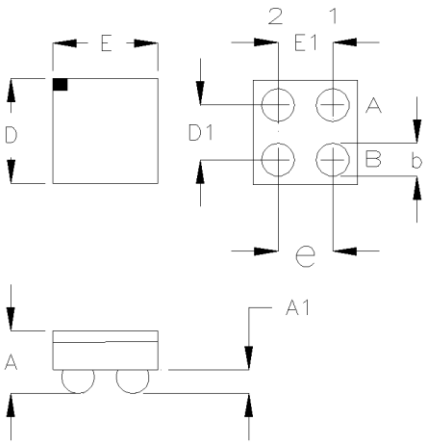
Figure 3. ZQFN-4L 1x1 Layout Guide



GND Pin (2) connect to second layer ground path by Via to increase cooling area directly.

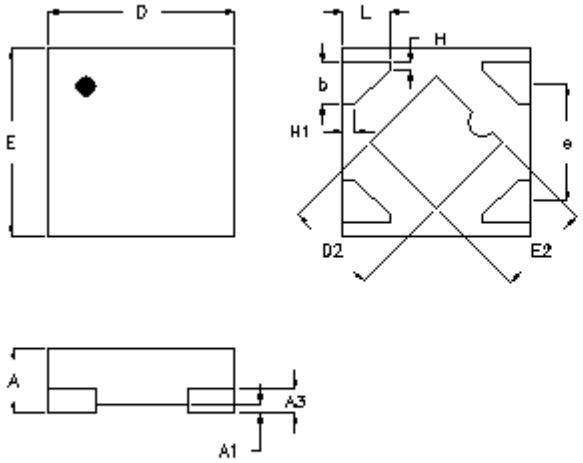
Figure 4. SOT-23-5 Layout Guide

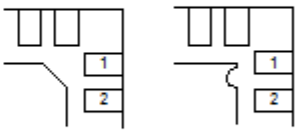
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.355	0.445	0.014	0.018
A1	0.145	0.175	0.006	0.007
b	0.190	0.230	0.007	0.009
D	0.630	0.710	0.025	0.028
D1	0.350		0.014	
E	0.630	0.710	0.025	0.028
E1	0.350		0.014	
e	0.350		0.014	

4B WL-CSP 0.67x0.67 Package (BSC)





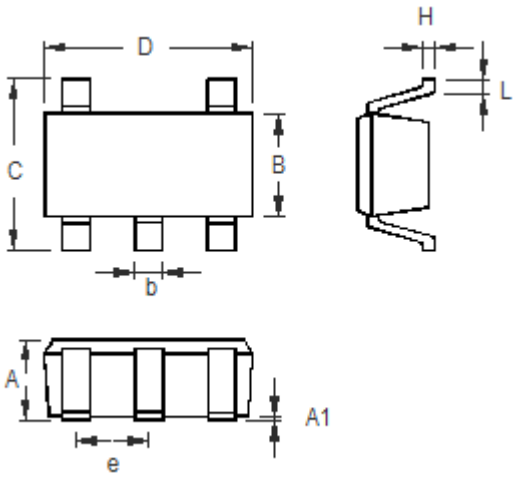
DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.300	0.400	0.012	0.016
A1	0.000	0.050	0.000	0.002
A3	0.117	0.162	0.005	0.006
b	0.175	0.275	0.007	0.011
D	0.900	1.100	0.035	0.043
D2	0.450	0.550	0.018	0.022
E	0.900	1.100	0.035	0.043
E2	0.450	0.550	0.018	0.022
e	0.625		0.025	
L	0.200	0.300	0.008	0.012
H	0.039		0.002	
H1	0.064		0.003	

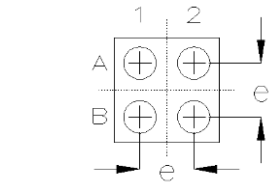
Z-Type 4L QFN 1x1 Package

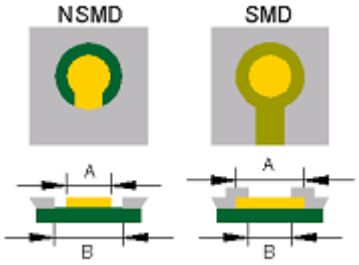


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

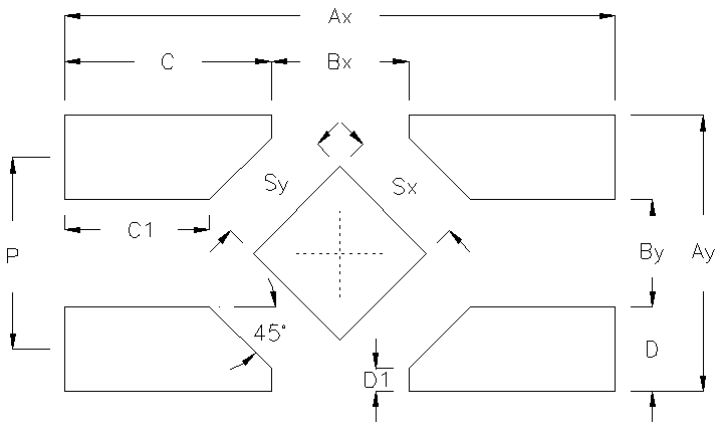
SOT-23-5 Surface Mount Package

Footprint Information

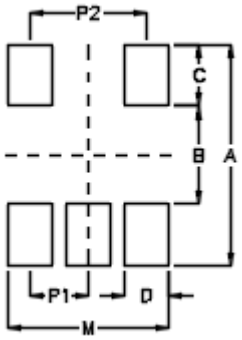




Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP0.67x0.67-4(BSC)	4	NSMD	0.350	0.180	0.280	±0.025
		SMD		0.210	0.180	



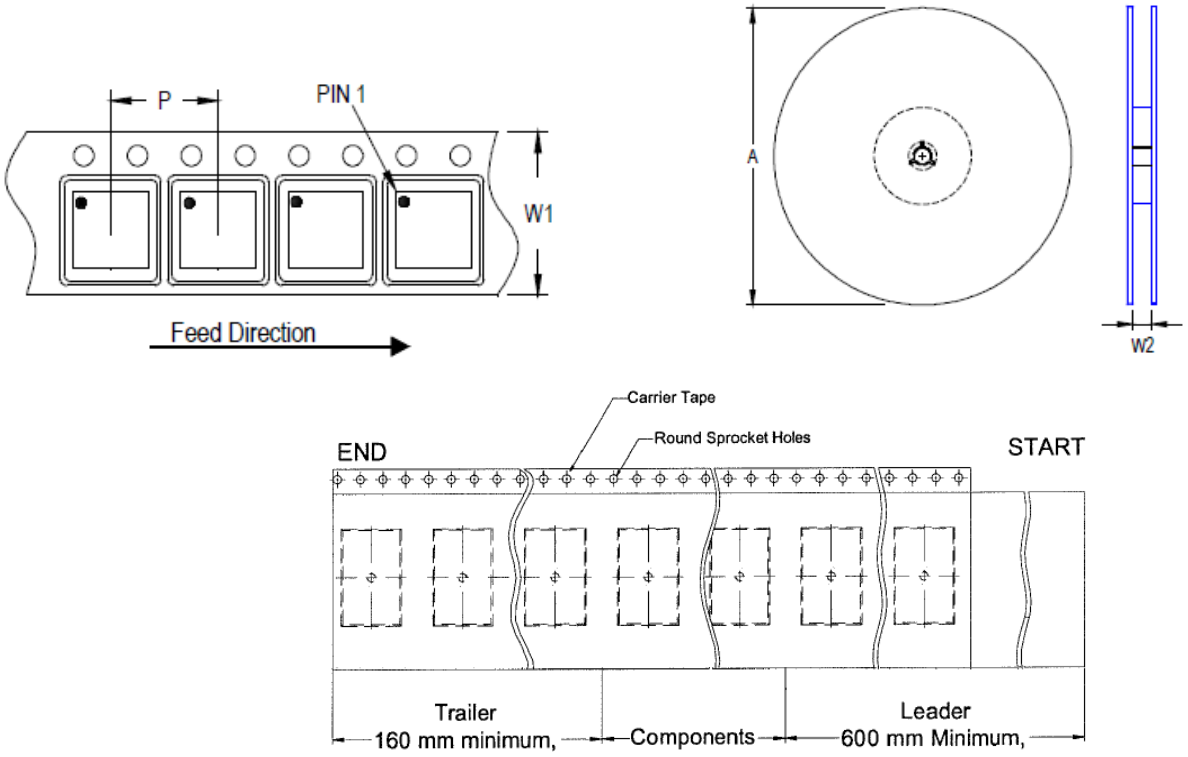
Package	Number of Pin	Footprint Dimension (mm)											Tolerance
		P	Ax	Ay	Bx	By	C	C1	D	D1	Sx	Sy	
U/X/ZQFN1x1-4	4	0.625	1.800	0.900	0.450	0.350	0.675	0.474	0.275	0.074	0.400	0.400	±0.050



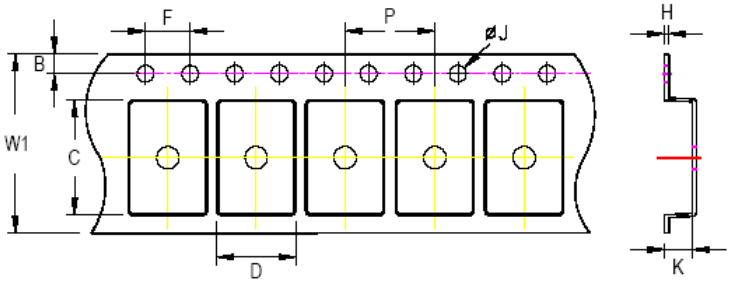
Package	Number of Pin	Footprint Dimension (mm)							Tolerance
		P1	P2	A	B	C	D	M	
TSOT-25/TSOT-25(FC)/SOT-25	5	0.95	1.90	3.60	1.60	1.00	0.70	2.60	±0.10

Packing Information

Tape and Reel Data (WL-CSP 0.67x0.67)



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 0.67x0.67	8	2	180	7	10,000	160	600	8.4/9.9

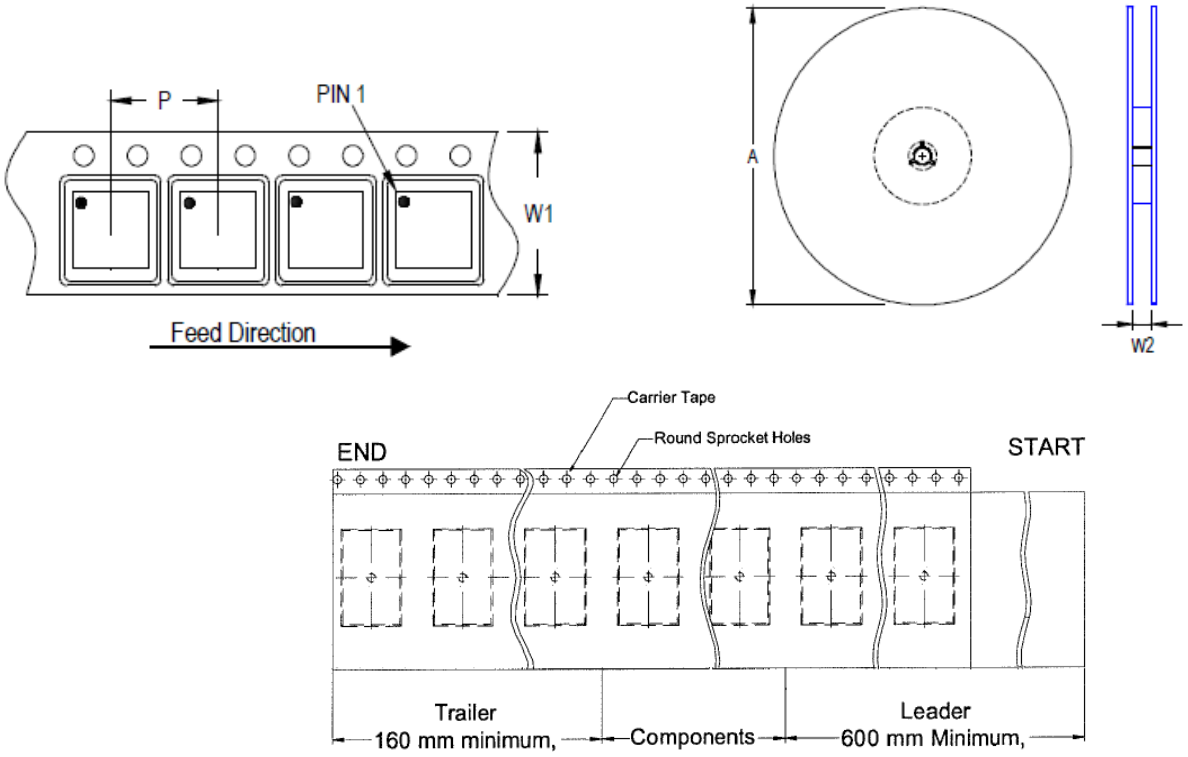


C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

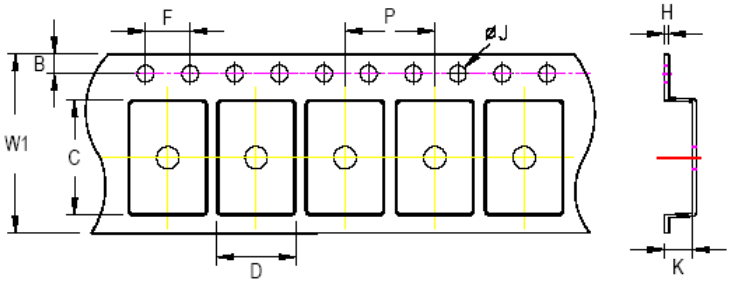
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Data (QFN/DFN 1x1)



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 1x1	8	4	180	7	2,500	160	600	8.4/9.9

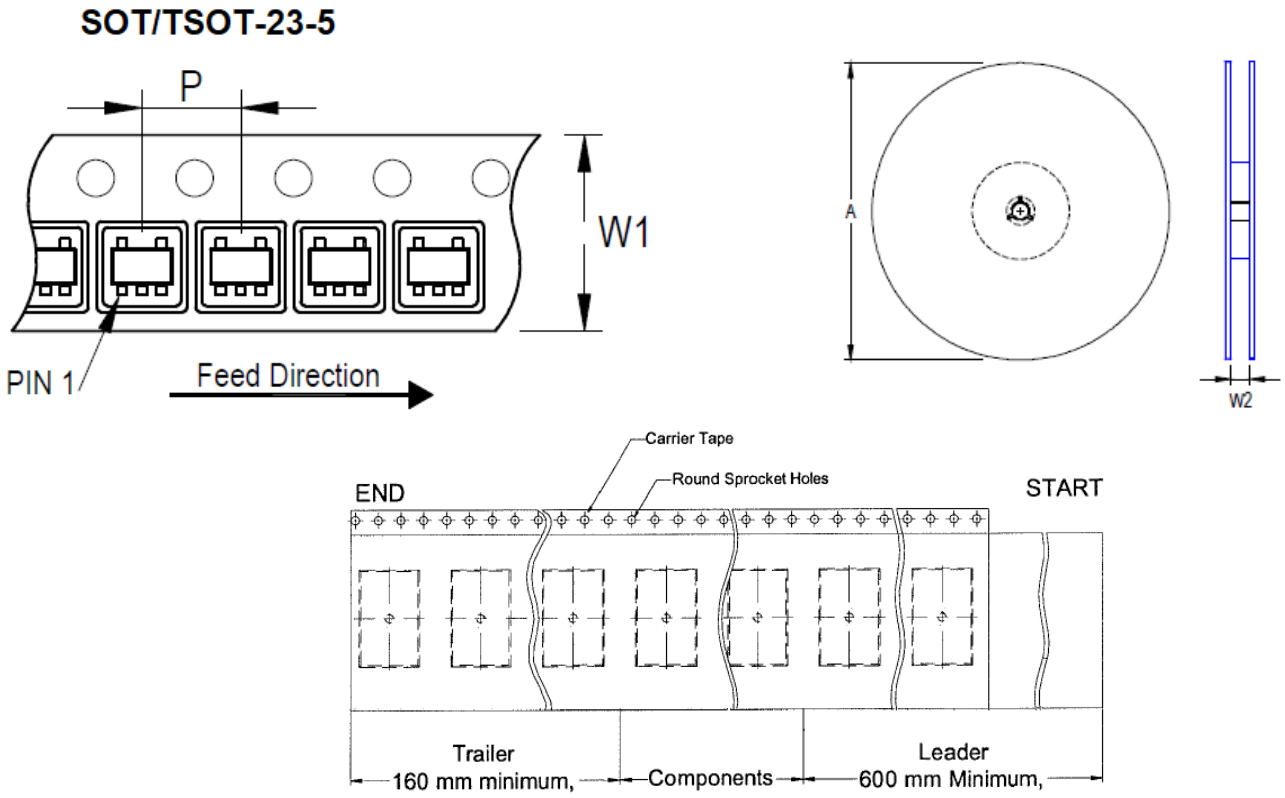


C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

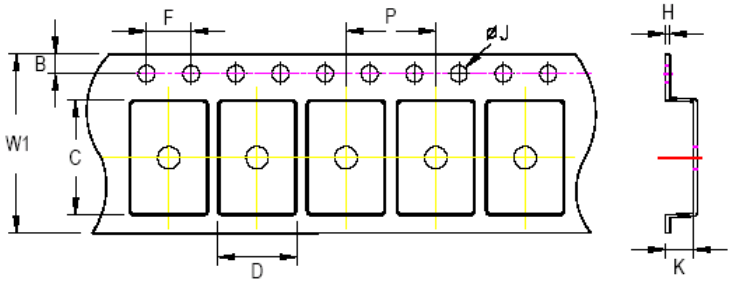
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Data (SOT/TSOT-23-5)



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
SOT/TSOT-23-5	8	4	180	7	3,000	160	600	8.4/9.9



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing (WL-CSP 0.67x0.67)

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
WL-CSP 0.67x0.67	7”	10,000	Box A	18.3*18.3*8.0	3	30,000	Carton A	38.3*27.2*38.3	12	360,000
			Box E	18.6*18.6*3.5	1	10,000	For Combined or Partial Reel.			

Tape and Reel Packing (QFN/DFN 1x1)

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN & DFN 1x1	7”	2,500	Box A	18.3*18.3*8.0	3	7,500	Carton A	38.3*27.2*38.3	12	90,000
			Box E	18.6*18.6*3.5	1	2,500	For Combined or Partial Reel.			

Tape and Reel Packing (SOT/TSOT-23-5)

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
SOT/TSOT-23-5	7”	3,000	Box A	18.3*18.3*8.0	3	9,000	Carton A	38.3*27.2*38.3	12	108,000
			Box E	18.6*18.6*3.5	1	3,000	For Combined or Partial Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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Datasheet Revision History

Version	Date	Description	Item
00	2023/2/20	Final	Ordering Information on P2 Application Information on P12 Packing Information on P16, 17, 18
01	2023/6/12	Modify (Added ZQFN-4L 1x1 and SOT-23-5 Package)	General Description on P1 Ordering Information on P1 Pin Configuration on P2 Functional Pin Description on P2 RT9092 Output Voltage Table on P3, 4 Absolute Maximum Ratings on P7 Electrical Characteristics on P7, 8 Note 2 on P9 Typical Application Circuit on P10 Application Information on P13, 14, 15 Outline Dimension on P17, 18 Footprint Information on P20, 21 Packing Information on P23, 24, 26, 27
02	2023/10/24	Modify	General Description on P1 Recommended Operating Conditions on P7 Application Information on P13
03	2023/11/13	Modify	Electrical Characteristics on P8