# 700mA, 5.5V, Low Noise Low Dropout Regulator

## General Description

The RT9095 is a low-noise, high accuracy, low-dropout linear regulator (LDO), and is capable of sourcing 700mA. The device supports single input supply voltage as low to 1.7V, which makes it easy to use.

The RT9095 is designed with high PSRR and low noise, which can meet the requirements of noise-sensitive applications such as RF, PLL, Clocking and analog circuits. The regulator control circuitry includes a programmable soft-start circuit and short circuit, reverse current, and over-temperature protection. Other features include an enable input and a power-OK output. The device is fully specified over the temperature range of $T_J$ = –40°C to 105°C and is offered in a WDFN-8SL 2x2 package.

## Ordering Information

RT9095 □□

- Package Type
  QW : WDFN-8SL 2x2 (W-Type)
  (Exposed Pad-Option1)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

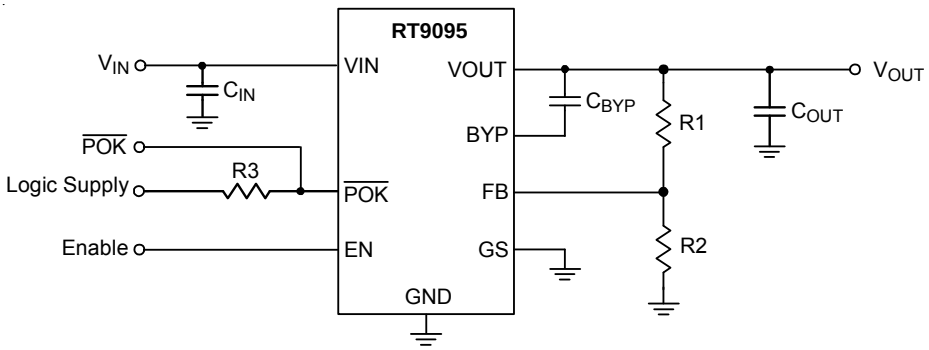
## Features

- **Input Voltage Range : 1.7V to 5.5V**
- **Output Voltage Range : 0.6V to 5.3V**
- **Accurate Voltage Reference**
  - **0.6V ±1.5%, Over –40°C to 105°C**
- **Ultra High PSRR : 48dB at 500kHz**
- **Excellent Noise Immunity : 25μ$V_{RMS}$**
- **Ultra Low Dropout Voltage : 150mV at 500mA**
- **Enable Control**
- **Short-Circuit Protection**
- **Output-to-Input Reverse Current Protection**
- **Support Power-OK Output Indicator Function**
- **RoHS Compliant and Halogen Free**

## Applications

- Portable Electronic Device
- Optical Modules
- Camera Modules
- PLL/Synthesizer, Clocking
- Sensors
- Medium-Current, Noise Sensitive Applications

## Simplified Application Circuit

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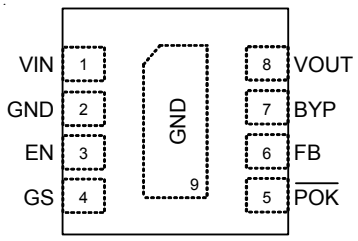
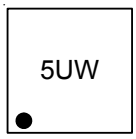
## Pin Configuration

(TOP VIEW)




WDFN-8SL 2x2

## Marking Information




5U : Product Code

W : Date Code

## Functional Pin Description

| aPin No. | Pin Name | Pin Function |
|---|---|---|
| 1 | VIN | Supply input. A 10μF or larger ceramic capacitor is recommended for good noise bypass and should be placed as close as possible to this pin. |
| 2, 9 (Exposed Pad) | GND | Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. |
| 3 | EN | Enable control input. Connecting this pin to logic high enables the regulator, and driving this pin low puts it into shutdown mode. The device can have VIN and $V_{EN}$ sequenced in any order without causing damage to the device. |
| 4 | GS | Internally Used. Connect GS to GND. |
| 5 | $\overline{POK}$ | Power-OK Output. Open-drain output that goes low when the output is above 91% of the nominal regulation voltage. $\overline{POK}$ is high impedance in shutdown or when the output is below the regulation voltage. |
| 6 | FB | Feedback voltage input. This pin is used to set the desired output voltage via an external resistive divider. The feedback reference voltage is 0.6V typically. |
| 7 | BYP | Bypass Input. Connecting a 0.01μF to this output further reduces output noise. Slew rate = (5V / ms) x (0.01μF / $C_{BYP}$). |
| 8 | VOUT | LDO output pin. A 10μF or larger ceramic capacitor (above 4.7μF effective capacitance) ensures the stability requirement. Place the output capacitor as close as possible to the device and minimize the impedance between the VOUT pin and the load. |

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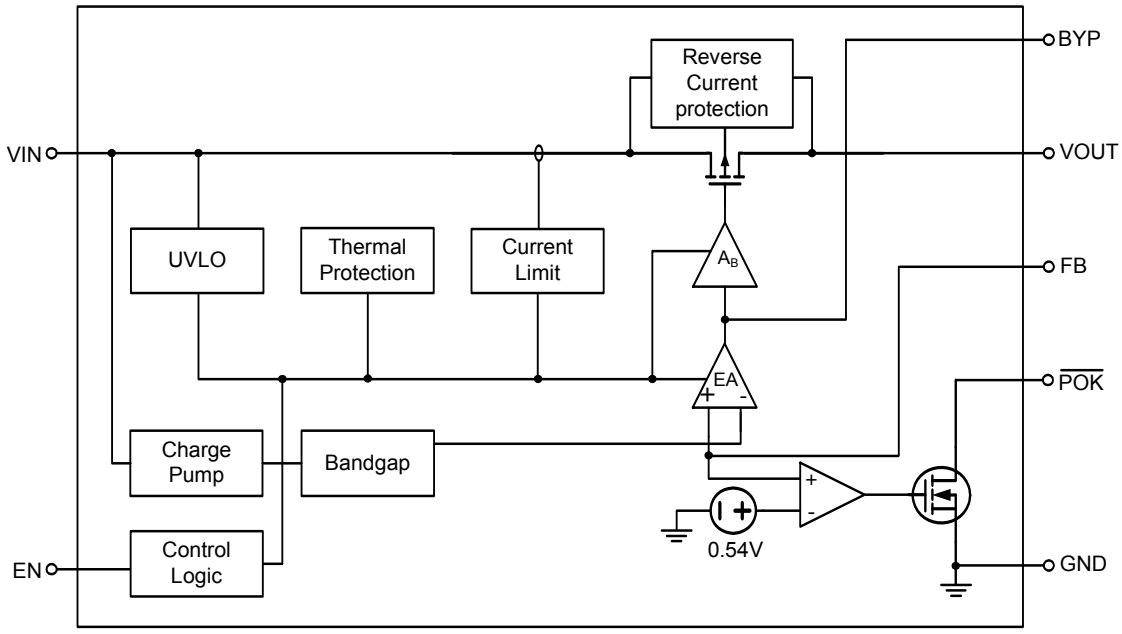
## Functional Block Diagram




## Operation

The RT9095 operates with single supply input ranging from 1.7V to 5.5V and is capable of delivering up to 700mA current to the output. The high PSRR and low noise features provides a clean supply to the application.

A low-noise reference and error amplifier are included to reduce device noise. The BYP capacitor filters the noise from the reference, and the feed-forward capacitor filters the noise from the error amplifier. The high power-supply rejection ratio (PSRR) of the RT9095 minimizes the coupling of input supply noise to the output.

### Enable

The RT9095 provides an EN pin, as an external chip enable control, to enable or disable the device. Pull the EN pin low to turn-off the regulator and enters the shutdown mode, while pull the EN pin high to turn-on the regulator. When the regulator is shutdown, the ground current is reduced to a maximum of 1μA. The enable circuitry has hysteresis (typically 100mV) for use with relatively slowly ramping analog signals.

If not used, connect the EN pin as close as possible to the largest capacitance on the input to prevent voltage droops on the VIN line from triggering the enable circuit.

### Bypass (BYP)

The capacitor connected from VOUT to BYP filters the reference noise above the 100Hz range and provides a high-speed feedback path for improved transient response.

The slew rate of the output voltage during startup is determined by the BYP capacitor. A 0.01μF capacitor sets the slew rate to 5V / ms. This startup rate results in a 50mA slew current drawn from the input at startup to charge the output capacitance.

The BYP capacitor value can be adjusted from 4.7nF to 0.1μF to change the startup slew rate according to the following formula :

Startup slew rate = (5V / ms) x (0.01μF / $C_{BYP}$)

Note that this slew rate applies only at startup, and that recovery from a short circuit occurs with a slew rate approximately 100 times slower.

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Also note that, being a low-frequency filter node, BYP is sensitive to leakage.

### Power OK

The RT9095 monitors the feedback pin voltage and indicates the status of the output voltage on the open-drain $\overline{POK}$ pin. The $\overline{POK}$ pin requires an external pull-up resistor to an external supply, and any downstream device can receive $\overline{POK}$ as a logic signal that can be used for sequencing. A pull-up resistor from 10kΩ to 100kΩ is recommended. Make sure that the external pull-up supply voltage results in a valid logic signal for the receiving device or devices.

During startup, $\overline{POK}$ stays high until the output voltage rises to 91% (typical) of its regulation level. If an overload occurs at the output or the output is shutdown, $\overline{POK}$ goes high.

### Internal Current Limit ($I_{LIM}$)

The RT9095 continuously monitors the output current to protect the pass transistor against abnormal operations. When an overload or short circuit is encountered, the current limit circuitry limits the output current to 0.8A (typical).

Thermal shutdown can be activated during a current limit event because of the high power dissipation typically found in these conditions. To ensure proper operation of the current limit, minimize the inductances at the input and load. Continuous operation in current limit is not recommended.

Because of the build-in body diode, the pass transistor conducts current when the output voltage exceeds the input voltage. Since the current is not limited, external current protection should be added if the device may work at reverse voltage state.

### Over-Temperature Protection (OTP)

The RT9095 implements thermal shutdown protection. The device is disabled when the junction temperature ($T_J$) exceeds 160°C (typical). The LDO automatically turns on again when the temperature falls below 140°C (typical).

For reliable operation, limit the junction temperature to a maximum of 125°C. Continuously running the RT9095 into thermal shutdown or above a junction temperature of 125°C reduces long-term reliability.

### Output Active Discharge

When EN and UVLO are lower than the respective threshold voltage during over-temperature protection, the RT9095 discharges the LDO output (via VOUT pins) through an internal current sink to ground. Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply collapses because reverse current can possibly flow from the output to the input. External current protection should be added if the device work at reverse voltage state.

### Reverse Current Protection

The reverse current protection circuit stops the reverse current from VOUT pin to VIN pin when the output voltage is higher than the input.

When VIN drops 10mV below VOUT, the RT9095 will shut off the regulator and open the PMOS body diode connection, preventing any reverse current.

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## Absolute Maximum Ratings (Note 1)

- All Pins ---------- –0.3V to 7V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

## ESD Ratings (Note 2)

- ESD Susceptibility
  HBM (Human Body Model) ---------- 2kV

## Recommended Operating Conditions (Note 3)

- Supply Input Voltage, VIN ---------- 1.7V to 5.5V
- Junction Temperature Range ---------- –40°C to 105°C

## Thermal Information (Note 4 and Note 5)

| Thermal Parameter | | WDFN-8SL 2x2 | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance (JEDEC standard) | 52.2 | °C/W |
| $\theta_{JC(Top)}$ | Junction-to-case (top) thermal resistance | 160.1 | °C/W |
| $\theta_{JC(Bottom)}$ | Junction-to-case (bottom) thermal resistance | 23.1 | °C/W |
| $\theta_{JA(EVB)}$ | Junction-to-ambient thermal resistance (specific EVB) | 61.6 | °C/W |
| $\Psi_{JC(Top)}$ | Junction-to-top characterization parameter | 5.61 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 36.5 | °C/W |

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## Electrical Characteristics

Over operating temperature range ($T_A$ = 25°C), (1.7V ≤ $V_{IN}$ < 5.5V and $V_{IN}$ ≥ $V_{OUT(TARGET)}$ + 0.5V, $V_{OUT(TARGET)}$ = 0.6V, $V_{EN}$ = $V_{IN}$= 5V, $C_{IN}$ = 10µF, $C_{OUT}$ = 10µF, $C_{BYP}$ = 0.01µF, unless otherwise noted. (Note 6)

| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input Voltage Range | $V_{IN}$ | | | 1.7 | -- | 5.5 | V |
| Input Under Voltage Lockout | $V_{IN-UVLO}$ | VIN rising, 100mV typical hysteresis | | 1.45 | 1.6 | 1.7 | V |
| Output Voltage Range | $V_{OUT}$ | $V_{IN}$ ≥ $V_{OUT}$ + 0.1V | | 0.6 | -- | 5.3 | V |
| Output Voltage Accuracy | | 1.7V ≤ $V_{IN}$ ≤ 5.5V for $V_{OUT}$ ≤1.4 V, $V_{OUT}$ + 0.3V ≤ $V_{IN}$ ≤ 5.5V for $V_{OUT}$ > 1.4V, 0.1mA ≤ $I_{OUT}$ ≤ 500mA | | −1.5 | -- | 1.5 | % |
| Load Regulation | $\Delta V_{OUT}/\Delta I_{OUT}$ | 0.1mA ≤ $I_{OUT}$ ≤ 700mA | | -- | 0.02 | -- | %/A |
| Line Regulation | $\Delta V_{OUT}/\Delta V_{IN}$ | 1.7V ≤ $V_{IN}$ ≤ 5.5V for $V_{OUT}$ ≤1.4V, $V_{OUT}$ + 0.3V ≤ $V_{IN}$ ≤ 5.5V for $V_{OUT}$ > 1.4V, $I_{OUT}$ = 200mA | | -- | 0.04 | -- | %/V |
| Dropout Voltage | $V_{DO}$ | $I_{OUT}$ = 700mA | $V_{IN}$ ≥ 3.6V | -- | 70 | 140 | mV |
| | | | $V_{IN}$ = 1.7V | -- | 210 | -- | |
| Output Current Limit | $I_{LIM}$ | $V_{OUT}$ = 95% of regulation, $V_{IN}$ = $V_{OUT}$ + 0.5V | | 700 | 800 | 900 | mA |
| Output Noise | $V_N$ | $I_{OUT}$ = 100mA, f = 10Hz to 100kHz, $V_{OUT}$ = 0.6V, $C_{BYP}$ = 0.01µF | | -- | 25 | -- | µ$V_{RMS}$ |
| Power Supply Rejection Ratio | PSRR | $I_{OUT}$ = 10mA | f = 1kHz | -- | 60 | -- | dB |
| | | | f = 10kHz | -- | 55 | -- | |
| | | | f = 100kHz | -- | 63 | -- | |
| | | | f = 500kHz | -- | 48 | -- | |
| Threshold Accuracy | $V_{FB}$ | 1.7V ≤ $V_{IN}$ ≤ 5.5V for 0.1mA ≤ $I_{OUT}$ ≤ 700mA | | 0.591 | 0.6 | 0.609 | V |
| Input Bias current | | $V_{FB}$ = 0.6 V | | −0.1 | 0.02 | 0.1 | µA |
| $C_{BYP}$ | BYPASS | $C_{BYPASS}$ | | 4.7 | -- | 100 | nF |
| BYP Startup Current | | From BYP to GND during startup | | -- | 50 | -- | µA |
| GND Supply Current | GND | $I_{OUT}$ = 0mA | | -- | 130 | 200 | µA |
| GND Shutdown Current | | $V_{IN}$ = 5.5V, EN = 0 V | | -- | 0.001 | +1 | µA |
| Enable Input Threshold | Enable | 1.7V ≤ $V_{IN}$ ≤ 5.5V | EN rising | -- | 0.8 | 1.2 | V |
| | | | EN falling | 0.4 | 0.7 | -- | |
| Enable Input Bias Current | | 1.7V ≤ $V_{EN}$ ≤ 5.5V | EN falling | −1 | 0.001 | 1 | µA |

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| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{POK}$ Threshold | $\overline{POK}$ | $V_{OUT}$ when $\overline{POK}$ switches | $V_{OUT}$ rising | 86 | 91 | 95 | % |
| | | | $V_{OUT}$ falling | -- | 88 | -- | % |
| $\overline{POK}$ Voltage Low | | $I_{\overline{POK}}$ = 1mA | | -- | 10 | 100 | mV |
| $\overline{POK}$ Leakage Current | | $\overline{POK}$ = 5.5V, $V_{EN}$ = 0V | | –1 | 0.001 | 1 | μA |
| Thermal Shutdown Threshold | Thermal Shutdown | $T_J$ rising | | -- | 165 | -- | °C |
| | | $T_J$ falling | | -- | 150 | -- | |
| Load Transient | Output Transient | $I_{OUT}$ = 50mA to 500mA to 50mA, $t_{RISE}$ = $t_{FALL}$ = 1μs | | -- | 50 | -- | mV/P–P |
| Line Transient | | $V_{IN}$ = 5V to 5.5V to 5V, $t_{RISE}$ = $t_{FALL}$ = 5μs, $I_{OUT}$ = 500mA | | -- | 3 | -- | mV/P–P |
| IN-to-OUT Reverse Voltage Turnoff Threshold | | $V_{IN}$ falling below $V_{OUT}$ | | -- | 10 | -- | mV |

**Note 1.** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** Devices are ESD sensitive. Handling precautions are recommended.

**Note 3.** The device is not guaranteed to function outside its operating conditions.

**Note 4.** $\theta_{JA}$ and $\theta_{JC}$ are measured or simulated at $T_A$ = 25°C based on the JEDEC 51-7 standard.

**Note 5.** $\theta_{JA(EVB)}$, $\Psi_{JC(Top)}$ and $\Psi_{JB}$ are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

**Note 6.** All devices are production tested at $T_A$ = 25°C. Specifications over the operating temperature range are guaranteed by design and characterization.

**Note 7.** External resistor tolerance is not taken into account.

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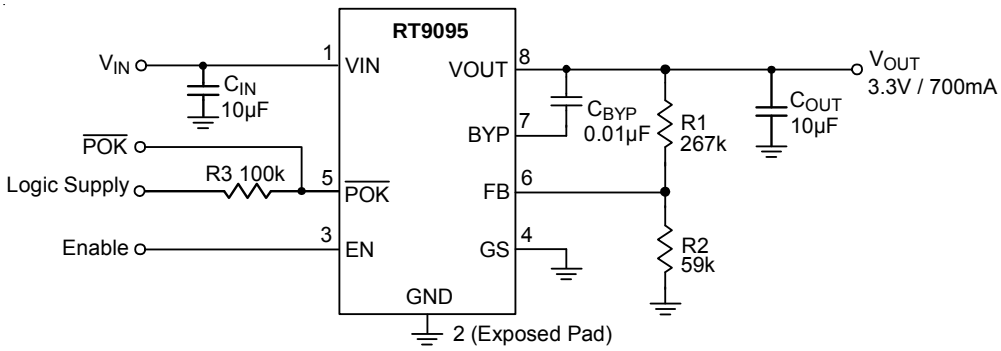
## Typical Application Circuit




$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) = 0.6V \times \left(1 + \frac{267k}{59k}\right) = 3.3V$$

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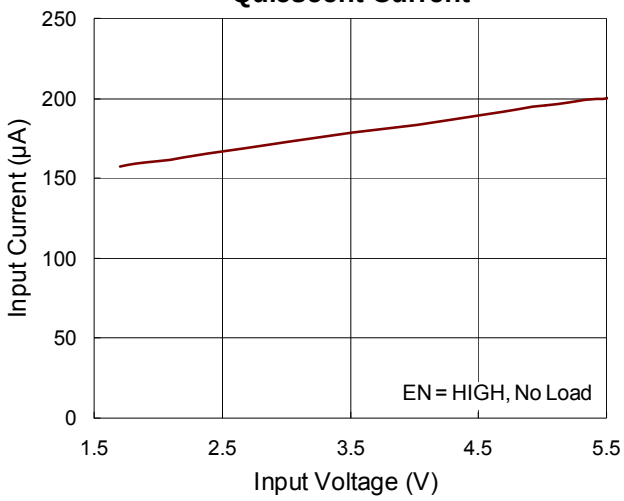
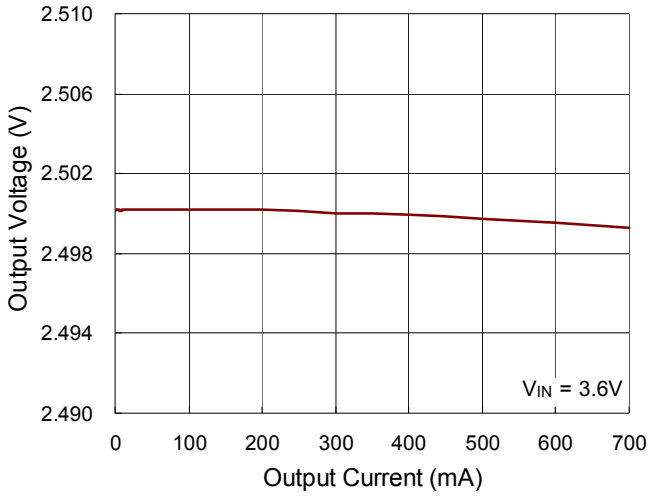
## Typical Operating Characteristics

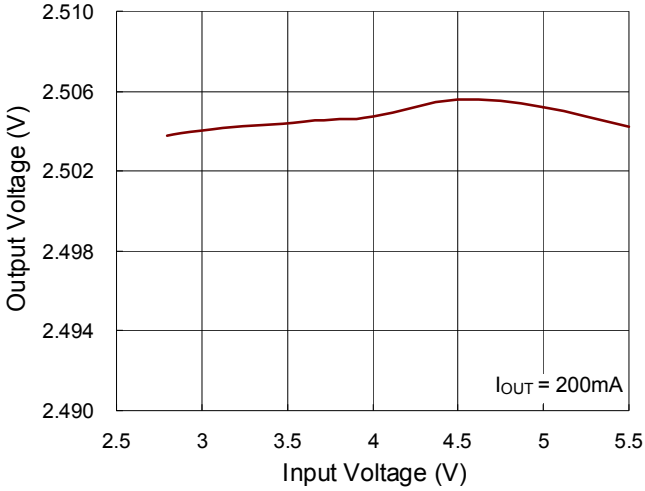
### Quiescent Current



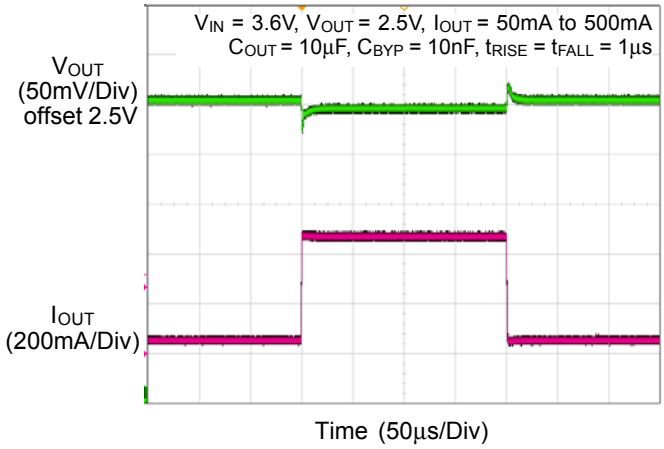

### Load Regulation



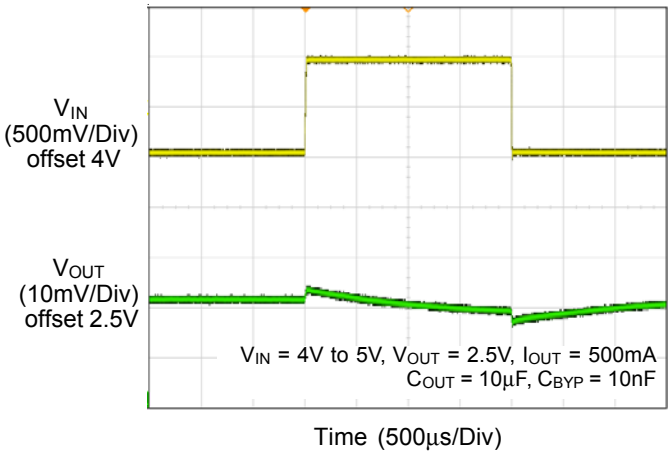

### Line Regulation



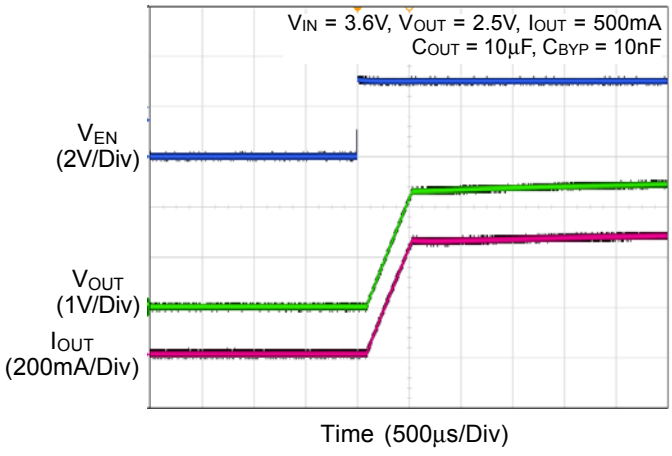

### Load Transient Response




### Line Transient Response




### Power Up Response

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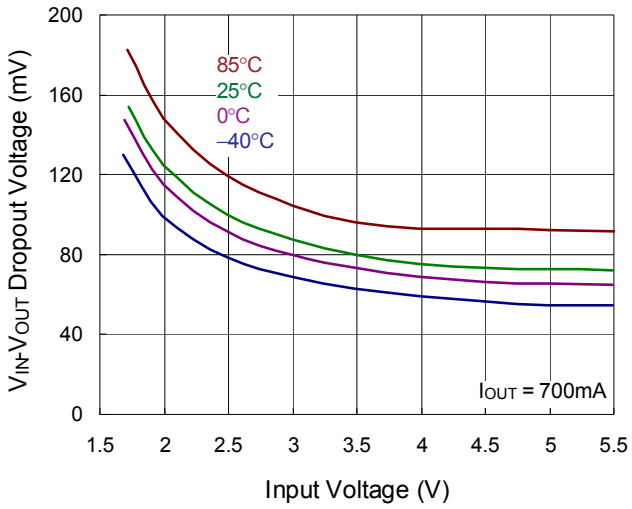
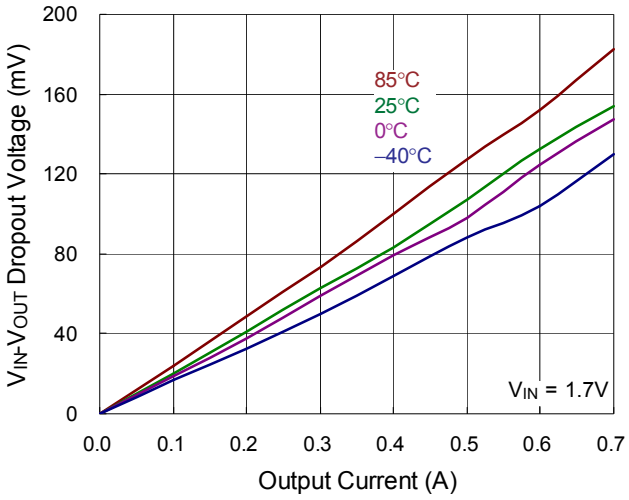
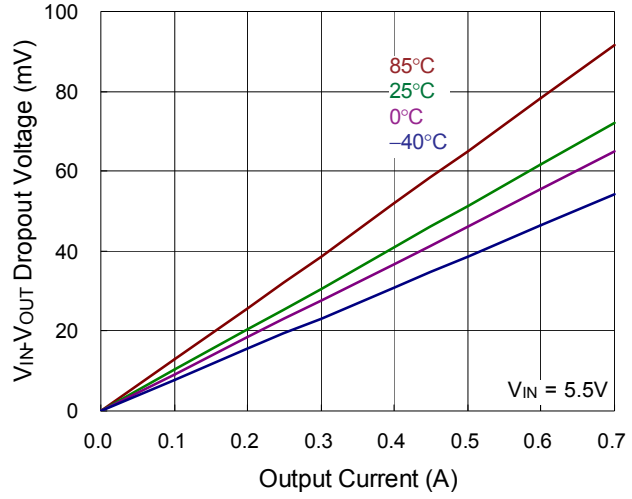
**Dropout Voltage vs. Input Voltage**



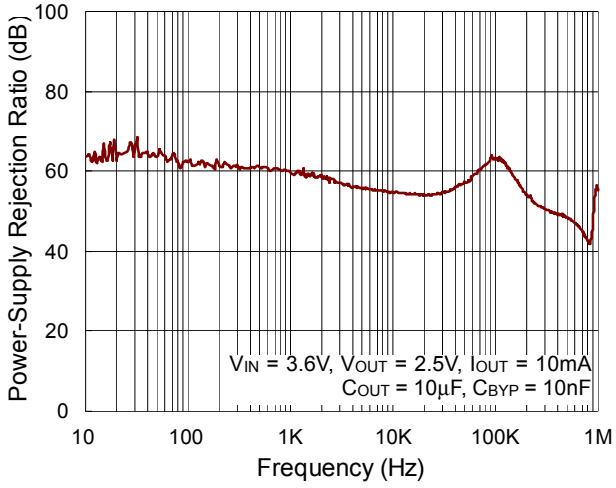

**Dropout Voltage vs. Output Current**



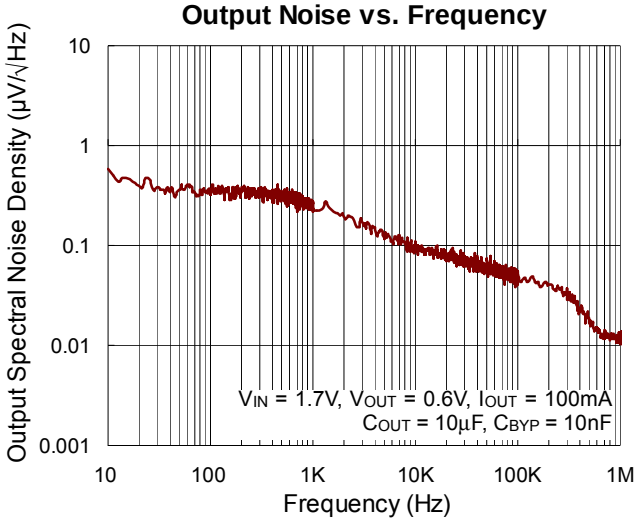

**Dropout Voltage vs. Output Current**




**PSRR vs. Frequency**




**Output Noise vs. Frequency**

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## Application Information

The RT9095 is a low-noise, high accuracy, low-dropout linear regulator which is capable of sourcing with maximum dropout of 210mV. The input voltage operating range is from 1.7V to 5.5V and the adjustable output voltage is from 0.6V to ($V_{IN}$ – $V_{DROP}$) according to the external resistor setting.

### Output Voltage Setting

The output voltage of the RT9095 can be set by external resistors.

By using external resistors, the output voltage is determined by the values of R1 and R2 as shown in Figure 1. The values of R1 and R2 can be calculated for any voltage value using the following formula :

$$V_{OUT} = 0.6 \times \frac{R1 + R2}{R2}$$

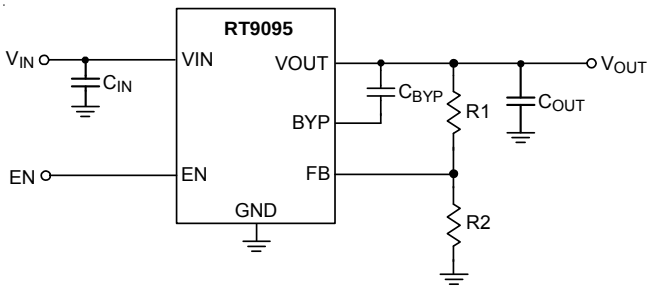


Figure 1. Output Voltage Set by External Resistors

Set the lower feedback resistor (R2) to 60kΩ or less to minimize FB input bias current error.

### Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at a specific output current. The dropout voltage $V_{DROP}$ also can be expressed as the voltage drop on the pass-FET at a specific output current ($I_{RATED}$) while the pass-FET is fully operating in the ohmic region and the pass-FET can be characterized as a resistance $R_{DS(ON)}$. Thus, the dropout voltage can be defined as ($V_{DROP}$ = $V_{IN}$ – $V_{OUT}$ = $R_{DS(ON)}$ x $I_{RATED}$). For normal operation, the suggested LDO operating range is ($V_{IN}$ > $V_{OUT}$ + $V_{DROP}$) for good transient response and PSRR performance. However, operation in the ohmic region will degrade the performance severely.

### $C_{IN}$ and $C_{OUT}$ Selection

The RT9095 is designed to support low-series-resistance (ESR) ceramic capacitors. X7R, X5R, and COG-rated ceramic capacitors are recommended due to its good capacitive stability across different temperatures, whereas the use of Y5V-rated capacitors is not recommended because of large capacitance variations.

However, ceramic capacitance varies with operating voltage and temperature, and the design engineer must be aware of these characteristics. Input capacitance is selected to minimize transient input drop during load current steps. For general applications, an input capacitor of 10μF is highly recommended for minimal input impedance. If the trace inductance between the RT9095 input pin and power supply is high, a fast load transient can cause VIN voltage level ringing above the absolute maximum voltage rating which damages the device. Adding more input capacitors is available to restrict the ringing and keep it below the device absolute maximum ratings.

A 10μF or larger ceramic capacitor (above 4.7μF effective capacitance) ensures the stability requirement at output terminal. Generally, a 10μF 0805-sized ceramic capacitor ensures the minimum effective capacitance at temperature and DC bias requirement. Place these capacitors as close as possible to the pins for performance and stability.

### Input Inrush Current

During start-up, the input Inrush current into the VIN pin consists of the sum of load current and the charging current of the output capacitor. The inrush current is difficult to measure because the input capacitor must be removed, which is not recommended. Generally, the soft-start inrush current can be estimated by Equation b1, where $V_{OUT}(t)$ is the instantaneous output voltage of the power-on ramp, $dV_{OUT}(t)$ / dt is the slope of the $V_{OUT}$ ramp and $R_{LOAD}$ is the resistive load impedance.

$$I_{OUT}(t) = \frac{\left(C_{OUT} \times dV_{OUT}(t)\right)}{dt} + \left(\frac{V_{OUT}(t)}{R_{LOAD}}\right) \quad (b1)$$

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### Thermal Considerations

Thermal protection limits power dissipation in the RT9095. When power dissipation on the pass element ($P_{DIS}$ = ($V_{IN}$ – $V_{OUT}$) x $I_{OUT}$) is too high and raises the junction operation temperature over 160°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turns on again after the junction temperature cools down by 20°C.

The output is shorted to ground when there as short circuit at the output. This procedure can reduce the chip temperature and provides maximum safety to end users when output short circuit occurs.

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating

Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a WDFN-8SL 2x2 package, the thermal resistance, $\theta_{JA(EVB)}$, is 61.6°C/W on a standard high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A$ = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (61.6°C/W) = 1.62W for a WDFN-8SL 2x2 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA}$. The derating curves in Figure 2 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

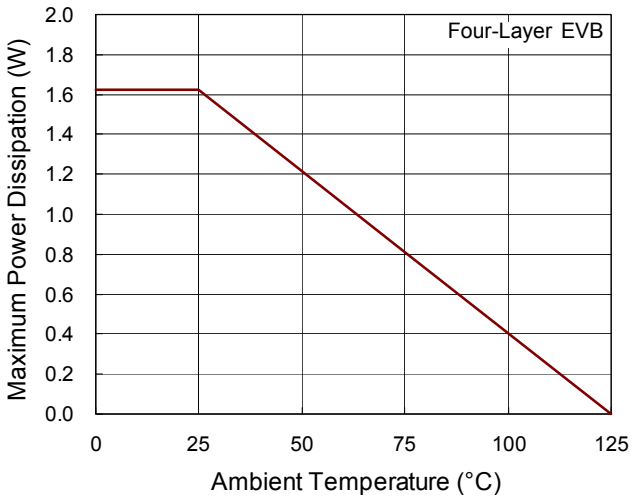


Figure 2. Derating Curve of Maximum Power Dissipation

### Layout Considerations

For best performance of the RT9095, the PCB layout suggestions below are highly recommended. All circuit components should be placed on the same side and as close to the respective LDO pin as possible. Place the ground return path connection to the input and output capacitor. Connect the ground plane with a wide copper surface for good thermal dissipation. Using vias and long power traces for the input and output capacitors connections is not recommended and has negative effects on performance. Figure 3 shows a layout example that reduces conduction trace loops, helping to minimize inductive parasitics and load transient effects while improving the circuit stability.

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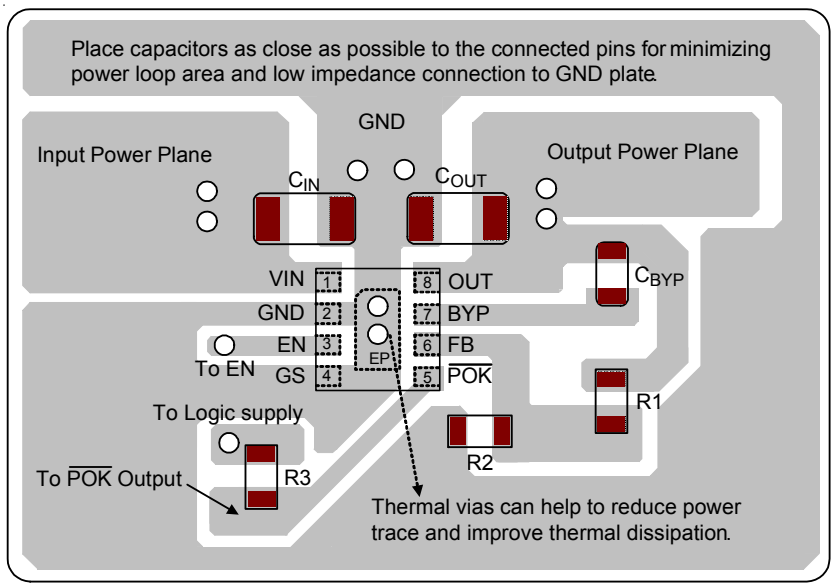


Figure 3. PCB Layout Guide

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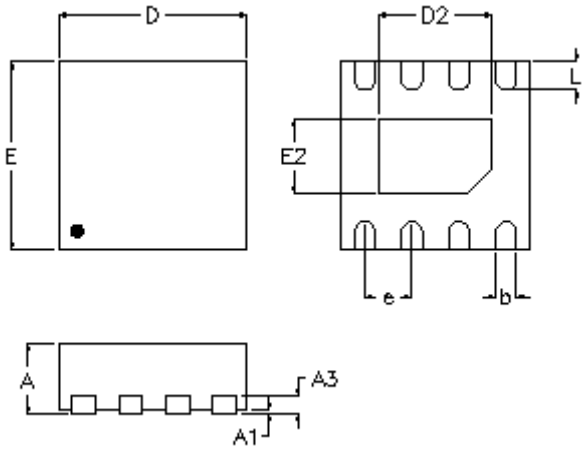
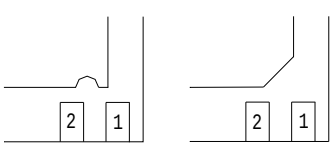
## Outline Dimension




**DETAIL A**

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|---|
| | | Min | Max | Min | Max |
| A | | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | | 0.175 | 0.250 | 0.007 | 0.010 |
| b | | 0.200 | 0.300 | 0.008 | 0.012 |
| D | | 1.900 | 2.100 | 0.075 | 0.083 |
| D2 | Option1 | 1.150 | 1.250 | 0.045 | 0.049 |
| | Option2 | 1.550 | 1.650 | 0.061 | 0.065 |
| E | | 1.900 | 2.100 | 0.075 | 0.083 |
| E2 | Option1 | 0.750 | 0.850 | 0.030 | 0.033 |
| | Option2 | 0.850 | 0.950 | 0.033 | 0.037 |
| e | | 0.500 | | 0.020 | |
| L | | 0.250 | 0.350 | 0.010 | 0.014 |

**W-Type 8SL DFN 2x2 Package**

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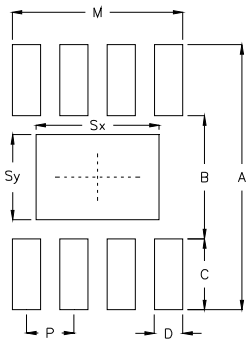
## Footprint Information




| Package | | Number of Pin | Footprint Dimension (mm) | | | | | | | | Tolerance |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | P | A | B | C | D | Sx | Sy | M | |
| V/W/U/XDFN2*2-8S | Option1 | 8 | 0.50 | 2.80 | 1.30 | 0.75 | 0.30 | 1.30 | 0.90 | 1.80 | ±0.05 |
| | Option2 | | | | | | | 1.60 | 0.90 | | |

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