2μA I_Q, 600mA, Low-Dropout Linear Voltage Regulator

1 General Description

The RT9096/RT9096N is a low-dropout (LDO) linear voltage regulator capable of operating with input voltages ranging from 1.2V to 5.5V and supplying up to 600mA of output current. The output voltage is designed to operate in two modes for different purposes. In the adjustable mode, the RT9093 output voltage can be set from 0.8V to 3.3V. In the fixed mode, the output voltage is also available from 0.8V to 3.3V without the need for an external resistive voltage divider, saving on the bill of materials (BOM) costs in conditions where the PCB area is limited.

This device implements the EN pin for system sequencing. It also integrates input undervoltage-lockout (UVLO), overcurrent protection (OCP), and over-temperature protection (OTP) to prevent fault conditions.

The RT9096/RT9096N is available in the TSOT-23-5 package with both fixed and adjustable output voltage options facilitating easy use in various applications. It is also offered in the ZQFN-4L 1x1 package without an external resistive voltage divider. The device is fully specified for operation over the temperature range of T_J = -40°C to 125°C.

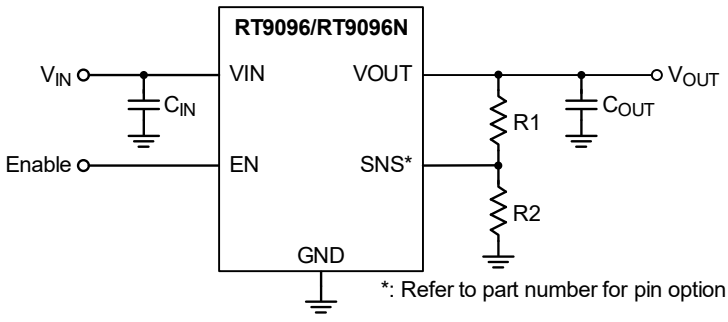
2 Features

- **Input Voltage Range: 1.2V to 5.5V**
- **Optional Fixed or Adjustable Output Voltage: 0.8V to 3.3V**
- **Output Current: 600mA (V_{IN} ≥ 2.3V)**
- **Low Quiescent Current: 2μA (Typical)**
- **Low Shutdown Current: 0.1μA (Typical)**
- **Output Voltage Accuracy: ±2%**
- **Low Dropout Voltage: 310mV (Typical) at 600mA when V_{OUT} ≥ 3V**
- **High PSRR: 75dB at 1kHz**
- **Active Output Discharge**
- **Stable with Output 1μF Ceramic Capacitance**
- **Overcurrent Protection**
- **Over-Temperature Protection**
- **Junction Temperature Range: –40°C to 125°C**
- **Available in TSOT-23-5 & ZQFN-4L 1x1 Packages**

3 Applications

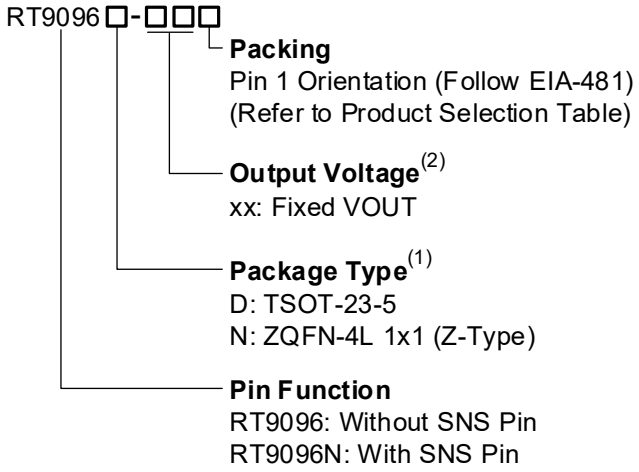
- Portable, Battery Powered Equipment
- Ultra Low Power Microcontrollers
- Notebook Computers

4 Simplified Application Circuit



5 Ordering Information

5.1 Product Number Information



5.2 Product Selection Table

Orderable Product Number	Output Voltage	EN(*)	SNS(*)	Package(1)	Pin 1 Quadrant
RT9096ND-08A	0.8V to 3.3V	O	O	TSOT-23-5	Q3
RT9096ND-18A	1.8V to 3.3V	O	O		
RT9096ND-33A	3.3	O	O		
RT9096N-08B	0.8V	O	–	ZQFN-4L 1x1	Q2
RT9096D-09A	0.9V	O	–	TSOT-23-5	Q3
RT9096N-09B		O	–	ZQFN-4L 1x1	Q2
RT9096N-10B	1V	O	–	ZQFN-4L 1x1	Q2
RT9096N-1KB	1.05V	O	–	ZQFN-4L 1x1	Q2
RT9096N-11A	1.1V	O	–	ZQFN-4L 1x1	Q1
RT9096N-11B		O	–	ZQFN-4L 1x1	Q2
RT9096ND-12A	1.2V	O	–	TSOT-23-5	Q3
RT9096N-12A		O	–	ZQFN-4L 1x1	Q1
RT9096N-12B		O	–	ZQFN-4L 1x1	Q2
RT9096N-1BB	1.25V	O	–	ZQFN-4L 1x1	Q2
RT9096N-13B	1.3V	O	–	ZQFN-4L 1x1	Q2
RT9096N-14B	1.4V	O	–	ZQFN-4L 1x1	Q2
RT9096D-15A	1.5V	O	–	TSOT-23-5	Q3
RT9096N-15B		O	–	ZQFN-4L 1x1	Q2

Orderable Product Number	Output Voltage	EN(*)	SNS(*)	Package(1)	Pin 1 Quadrant
RT9096N-16B	1.6V	O	–	ZQFN-4L 1x1	Q2
RT9096N-17B	1.7V	O	–	ZQFN-4L 1x1	Q2
RT9096D-18A	1.8V	O	–	TSOT-23-5	Q3
RT9096N-18A		O	–	ZQFN-4L 1x1	Q1
RT9096N-18B		O	–	ZQFN-4L 1x1	Q2
RT9096N-1HB	1.85V	O	–	ZQFN-4L 1x1	Q2
RT9096N-19B	1.9V	O	–	ZQFN-4L 1x1	Q2
RT9096N-20B	2V	O	–	ZQFN-4L 1x1	Q2
RT9096N-21B	2.1V	O	–	ZQFN-4L 1x1	Q2
RT9096N-22B	2.2V	O	–	ZQFN-4L 1x1	Q2
RT9096N-23B	2.3V	O	–	ZQFN-4L 1x1	Q2
RT9096N-24B	2.4V	O	–	ZQFN-4L 1x1	Q2
RT9096D-25A	2.5V	O	–	TSOT-23-5	Q3
RT9096N-25B		O	–	ZQFN-4L 1x1	Q2
RT9096N-26B	2.6V	O	–	ZQFN-4L 1x1	Q2
RT9096N-27B	2.7V	O	–	ZQFN-4L 1x1	Q2
RT9096D-28A	2.8V	O	–	TSOT-23-5	Q3
RT9096N-28A		O	–	ZQFN-4L 1x1	Q1
RT9096N-28B		O	–	ZQFN-4L 1x1	Q2
RT9096N-2HB	2.85V	O	–	ZQFN-4L 1x1	Q2
RT9096N-29B	2.9V	O	–	ZQFN-4L 1x1	Q2
RT9096D-30A	3V	O	–	TSOT-23-5	Q3
RT9096N-30B		O	–	ZQFN-4L 1x1	Q2
RT9096N-31B	3.1V	O	–	ZQFN-4L 1x1	Q2
RT9096N-32B	3.2V	O	–	ZQFN-4L 1x1	Q2
RT9096D-33A	3.3V	O	–	TSOT-23-5	Q3
RT9096N-33A		O	–	ZQFN-4L 1x1	Q1
RT9096N-33B		O	–	ZQFN-4L 1x1	Q2

*: O indicated function supported; - indicated function not supported.

Note 1.

- Marked with (1) indicates that Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicates that for output voltage within 0.8V to 3.3V that are not described in the product selection table, contact our sales representative directly or through a Richtek distributor located in your area.

6 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

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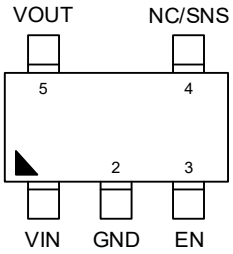
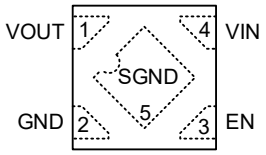
7 Pin Configuration

(TOP VIEW)



TSOT-23-5



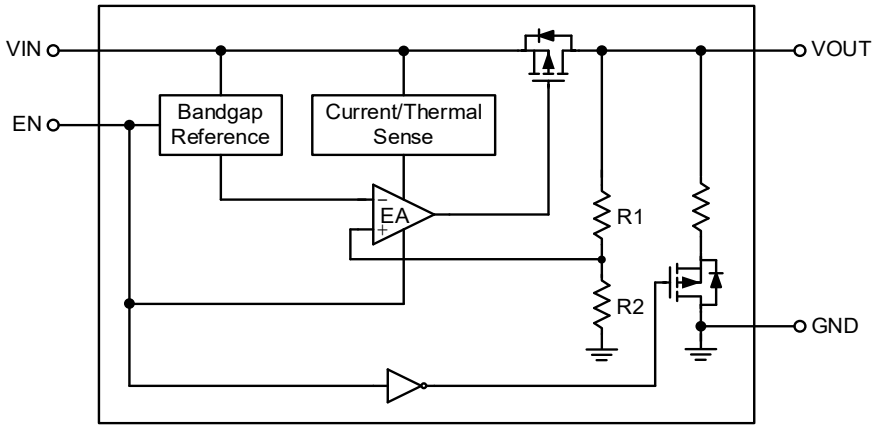
ZQFN-4L 1x1

8 Functional Pin Description

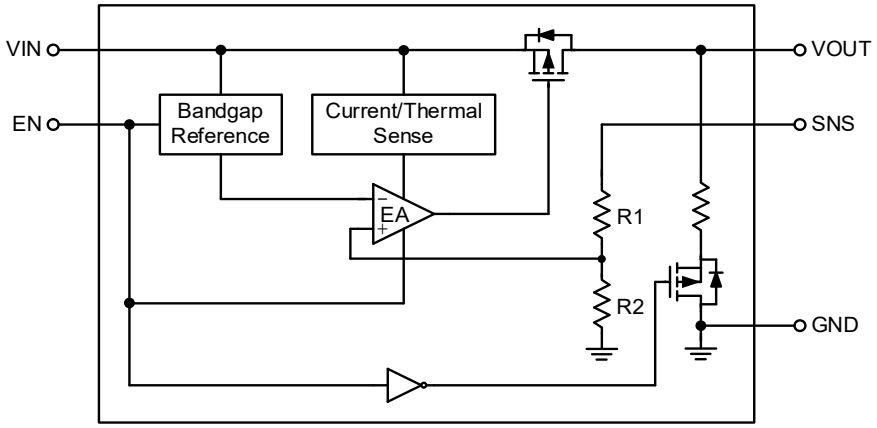
Pin No.		Pin Name	Pin Function
TSOT-23-5	ZQFN-4L 1x1		
1	4	VIN	Supply voltage input. The input voltage range is from 1.2V to 5.5V. Connect a ceramic capacitor with an effective capacitance of at least 1μF as close as possible from this pin to GND to minimize the input impedance
2	2	GND	Ground. Connect this pin to a large PCB copper area for maximum power dissipation.
3	3	EN	Enable control input. A logic-high enables the regulator, while a logic-low forces the device into shutdown mode. Connect this pin to the VIN pin to conserve the system's power rail and connect this pin to the external power rail for power sequence control. It is recommended to apply the enable voltage after the VIN pin voltage is ready for correct soft-start function. Do not leave this pin floating.
4	--	NC/SNS	• No internal connection. Connect this pin to GND plane of top layer to extend GND copper area to enhance the thermal performance. • Output voltage sense input. This pin is used to set the output voltage via an external resistive voltage divider. The feedback reference voltage is 0.8V (typical). Place the resistive voltage divider as close to the SNS pin as possible. Do not leave this pin floating.
5	1	VOUT	LDO output pin. Connect a ceramic capacitor with an effective capacitance of at least 0.7μF as close as possible to this pin and GND to minimize the output impedance.
--	5	SGND	Exposed pad. The exposed pad must be soldered to a large PCB copper area for maximum power dissipation.

9 Functional Block Diagram

9.1 Without SNS Pin



9.2 With SNS Pin



10 Absolute Maximum Ratings

(Note 2)

- VIN, VOUT, EN, SNS ---------- –0.3V to 6.5V
- VOUT to VIN ---------- –6.5V to –0.3V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility

  HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage, VIN ---------- 1.2V to 5.5V
- Fixed Output Voltage, VOUT ---------- 0.8V to 3.3V
- Adjustable Output Voltage, VOUT ---------- 0.8V to 3.3V
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		TSOT-23-5	ZQFN-4L 1x1	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	189.4	291.4	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	75.9	163	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	55.8	90.7	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (Specific EVB)	100.7	236	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	21.6	52.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	67.2	189.1	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are measured on a high effective-thermal-conductivity two-layer test board which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

(V_{OUT} + 1V < V_{IN} < 5.5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Range and Operating Current						
VIN Supply Input Voltage	V_{IN}		1.2	--	5.5	V
Quiescent Current	I_Q	$V_{IN} \geq V_{OUT} + V_{DROP}$, $V_{OUT} \leq 5.5V$, I_{OUT} = 0mA	--	2	4	µA
Shutdown Current (Note 7)	I_{SHDN}	V_{EN} = 0V	--	0.1	0.5	µA
		V_{EN} = 0V, V_{OUT} = 0V	--	0.1	0.5	
EN Input Voltage Rising Threshold	V_{EN_R}	V_{IN} = 5V	0.84	--	--	V
EN Input Voltage Falling Threshold	V_{EN_F}	V_{IN} = 5V	--	--	0.36	
EN Input Current	I_{EN}	V_{EN} = 5.5V	--	--	0.1	µA
Output Operation						
Output Voltage	V_{OUT}	Fixed mode	0.8	--	3.3	V
		Adjustable mode	0.8	--	3.3	
Output Voltage Accuracy (Note 8)	V_{OUT_ACC}	I_{OUT} = 1mA	–2	--	2	%
Reference Voltage	V_{REF}	I_{OUT} = 1mA	--	0.8	--	V
Dropout Voltage (Note 9)	V_{DROP}	0.8V ≤ V_{OUT} < 1.05V, I_{OUT} = 600mA (TSOT-23-5)	--	1.05	1.33	V
		0.8V ≤ V_{OUT} < 1.05V, I_{OUT} = 600mA (ZQFN-4L 1x1)	--	1.05	1.63	
		1.05V ≤ V_{OUT} < 1.2V, I_{OUT} = 600mA	--	0.8	1.13	
		1.2V ≤ V_{OUT} < 1.5V, I_{OUT} = 600mA	--	0.71	1.03	
		1.5V ≤ V_{OUT} < 1.8V, I_{OUT} = 600mA	--	0.57	0.93	
		1.8V ≤ V_{OUT} < 2.1V, I_{OUT} = 600mA	--	0.57	0.83	
		2.1V ≤ V_{OUT} < 2.5V, I_{OUT} = 600mA	--	0.41	0.73	
		2.5V ≤ V_{OUT} < 3V, I_{OUT} = 600mA	--	0.36	0.63	
		3V ≤ V_{OUT}, I_{OUT} = 600mA	--	0.31	0.53	
Line Regulation	V_{LINE_REG}	1.2V ≤ V_{IN} < 1.5V, I_{OUT} = 1mA	--	0.3	0.6	%
		1.5V ≤ V_{IN} < 1.8V, I_{OUT} = 1mA	--	0.15	0.3	
		1.8V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 1mA	--	0.13	0.35	
Load Regulation	V_{LOAD_REG}	I_{OUT} = 1mA to 600mA	--	0.5	1	%
Current Limit	I_{LIM}	V_{OUT} = 90% of $V_{OUT(NOM)}$	610	1100	--	mA
Discharge Resistor	R_{DISCHG}	V_{EN} = 0V, V_{OUT} = 0.1V	--	80	--	Ω

Note 7. The specification is tested at wafer stage and guaranteed by design after assembly.

Note 8. The external resistor tolerance is not taken into account.

Note 9. The dropout voltage is defined as $V_{IN} - V_{OUT}$, when V_{OUT} is 98% of the normal value of V_{OUT}.

14.1 System Characteristics

(The following specifications are guaranteed by design and are not performed in production testing. (V_{OUT} + 1V < V_{IN} < 5.5V, T_A = 25°C, unless otherwise specified.))

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Power Supply Rejection Ratio	PSRR	f = 1kHz, V_{IN} = 3V, V_{OUT} = 2.5V, I_{OUT} = 50mA, C_{OUT} = 1μF		--	75	--	dB
Output Noise Voltage	V_n	BW = 10Hz to 100kHz, V_{IN} = V_{OUT} + 1V, I_{OUT} = 150mA, C_{OUT} = 1μF	V_{OUT} = 0.8V	--	26	--	μV_{RMS}
			V_{OUT} = 1.2V	--	37	--	
			V_{OUT} = 1.8V	--	39	--	
			V_{OUT} = 3.3V	--	42	--	
Over-Temperature Protection Threshold	T_{OTP}	$V_{IN} \geq$ 1.5V, I_{OUT} = 30mA		--	150	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}			--	20	--	

15 Typical Application Circuit

15.1 SOT-23-5 Package

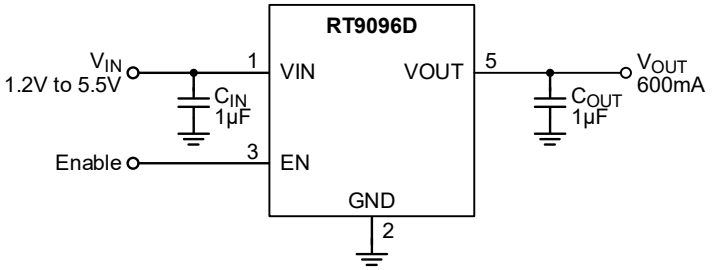


Figure 1. Configuration Circuit without SNS Pin

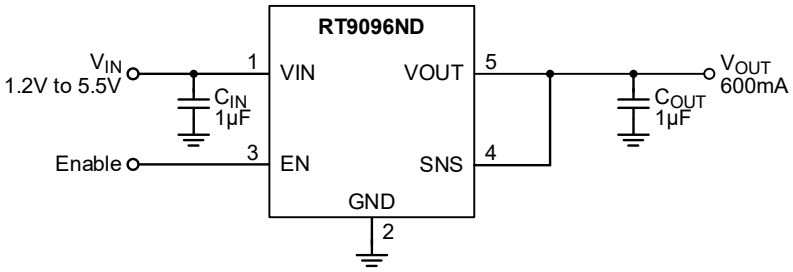


Figure 2. Configuration Circuit with SNS Pin for Fixed VOUT

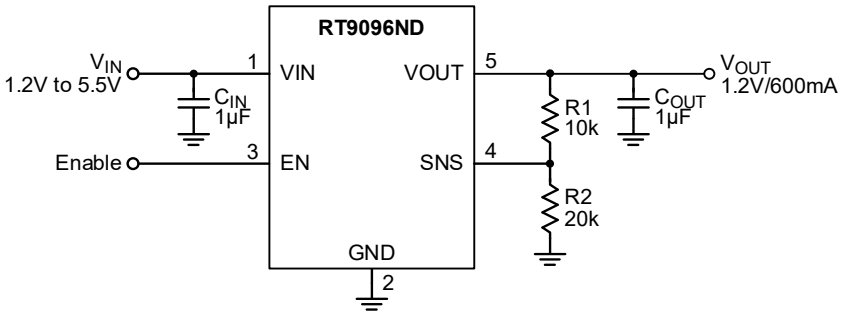


Figure 3. Configuration Circuit with SNS Pin for Adjustable VOUT

15.2 ZQFN-4L 1x1 Package

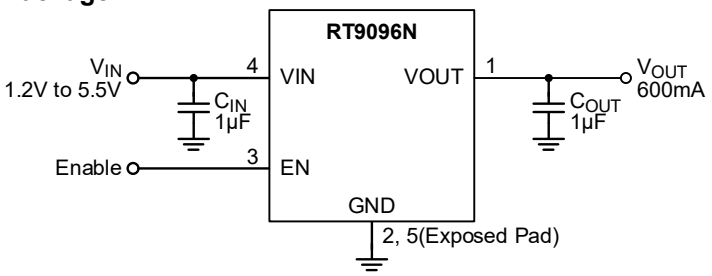


Figure 4. Configuration Circuit

15.3 Recommended Components

Table 1. Recommended Feedback-Resistor Values for V_{SNS} = 0.8V

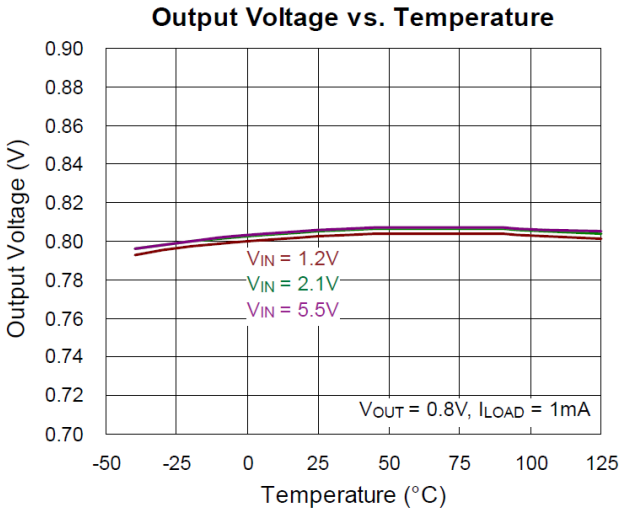
Output Voltage (V)	External Resistor Divider Combination	
	R1 (Ω)	R2 (Ω)
0.8	Short	Open
1.2	10k	20k
1.5	10k	11.5k
1.8	10k	8.06k
2.5	10k	4.75k
3.3	10k	3.16k
5	10k	1.91k

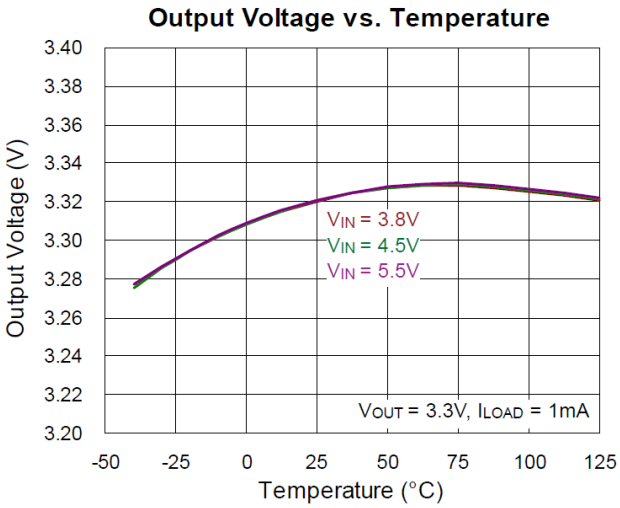
Table 2. Recommended External Components

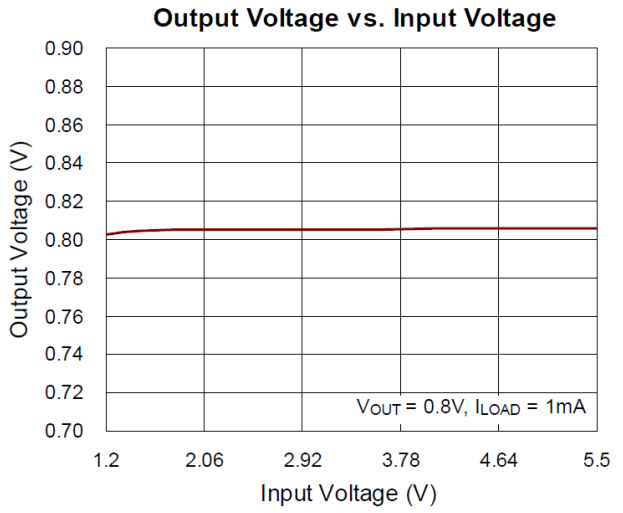
Reference	Qty	Part Number	Description	Package	Manufacture
IC	1	RT9096/RT9096N	Linear Regulator	SOT-23-5 ZQFN-4L 1x1	RICHTEK
C_{IN}	1	GRM155R61A105KE15	1μF/10V/X5R	C-0402	MURATA
C_{OUT} (Note 10)	1	GRM153R60J105ME95	1μF/6.3V/X5R	C-0402	MURATA
		CGB2A3X5R0J105M033BB			TDK
		GRM153R60J225ME95	2.2μF/6.3V/X5R	C-0402	MURATA
		C1005X5R0J225M050BC			TDK
		GRM153R60J475ME15	4.7μF/6.3V/X5R	C-0402	MURATA
		C1005X5R0J475K050BE			TDK

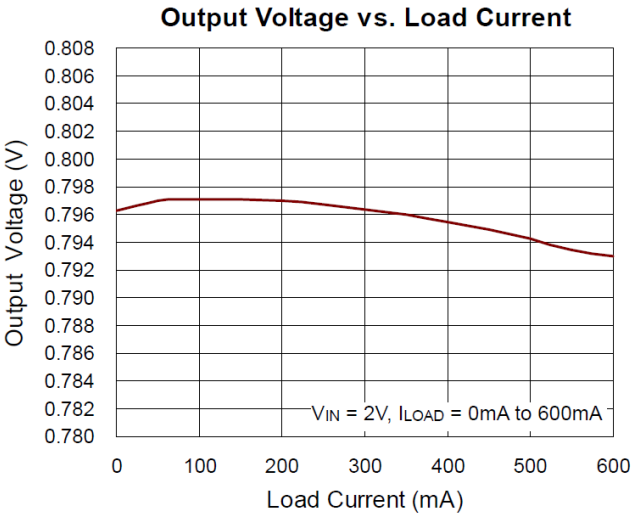
Note 10. Considering the effective capacitance de-rated with the biased voltage level, the COUT component must have an effective capacitance of at least 0.7μF or above at the targeted output level to ensure stable and normal operation.

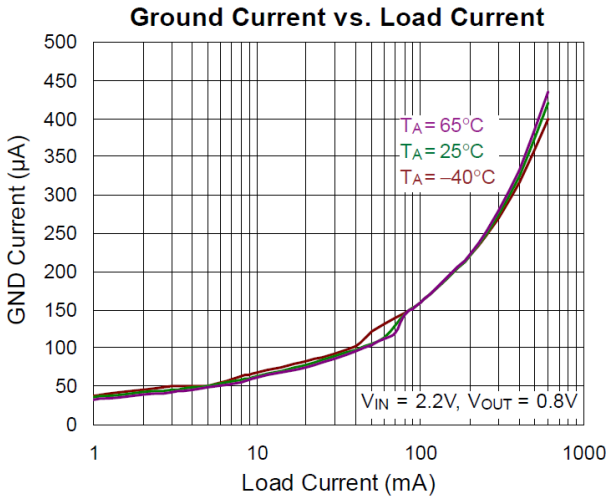
16 Typical Operating Characteristics

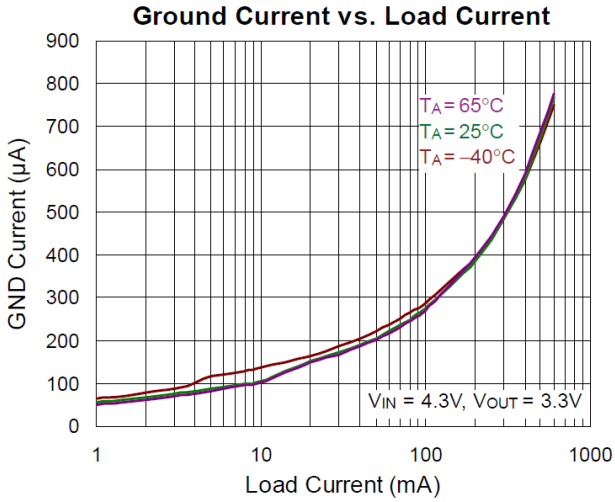




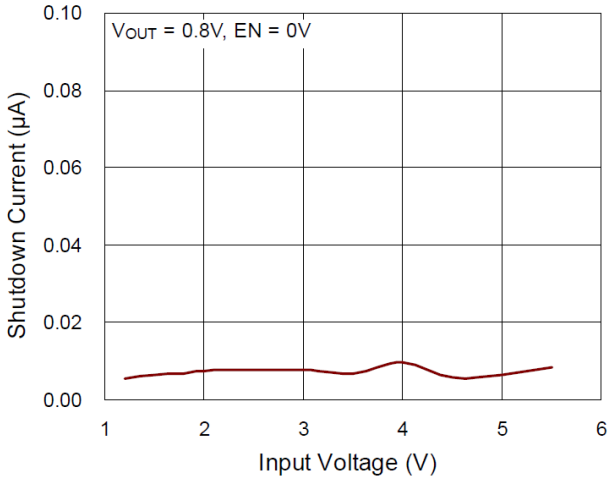




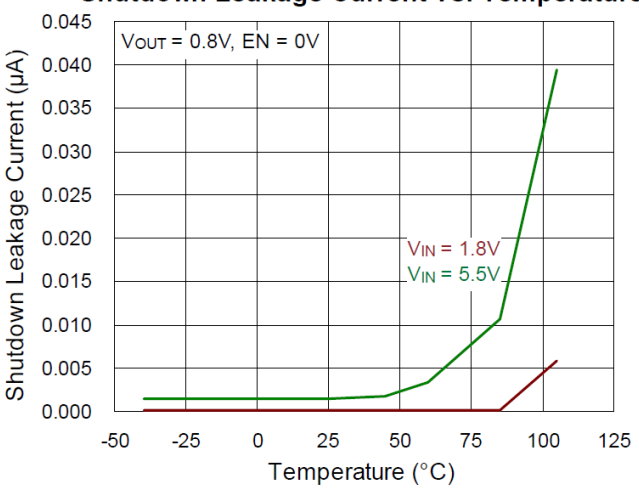




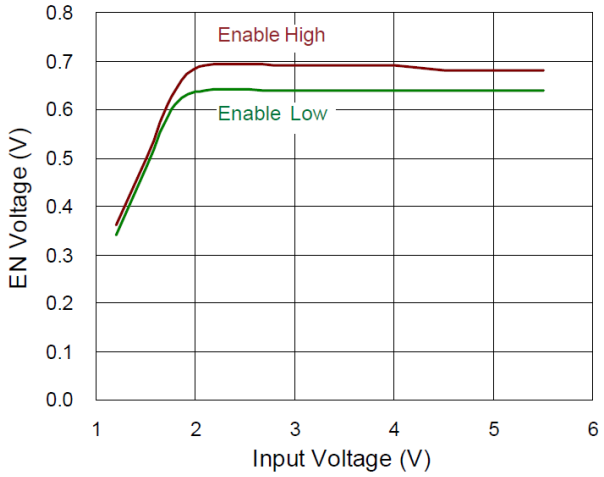
Shutdown Current vs. Input Voltage



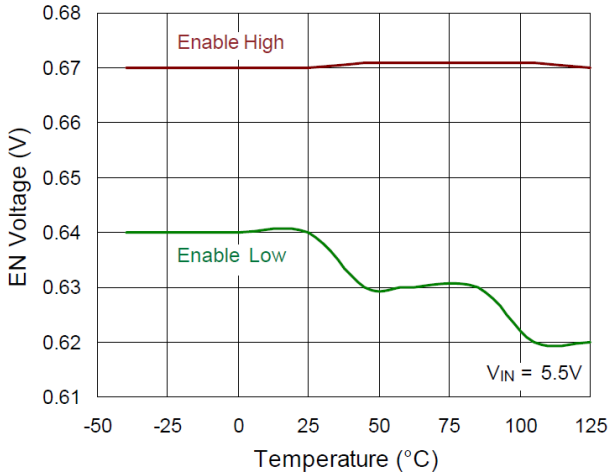
Shutdown Leakage Current vs. Temperature



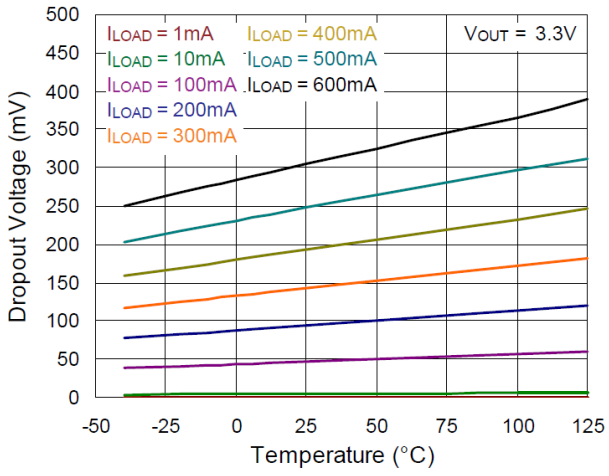
Enable Threshold vs. Input Voltage



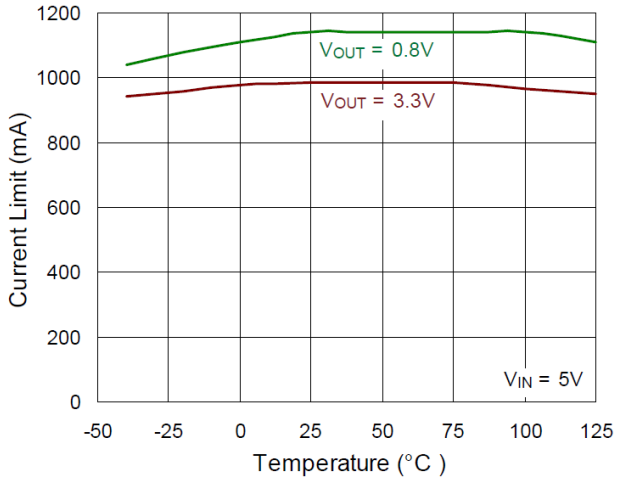
Enable Threshold vs. Temperature



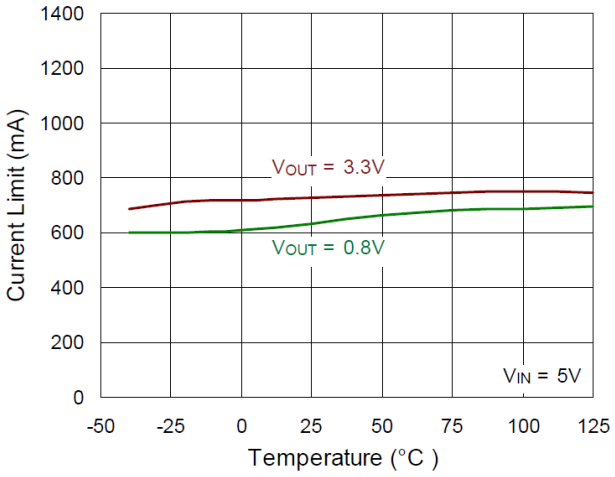
Dropout Voltage vs. Temperature



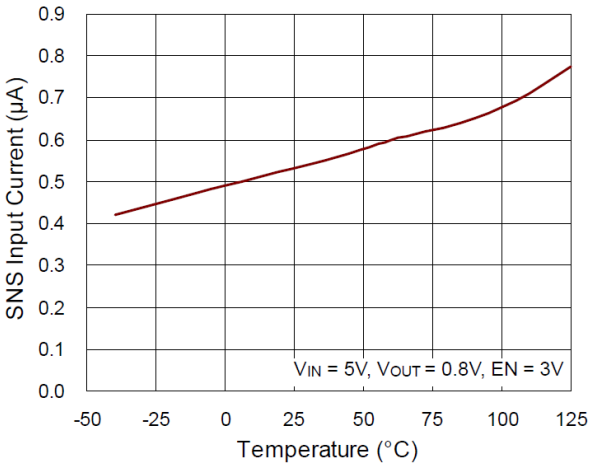
Current Limit vs. Temperature



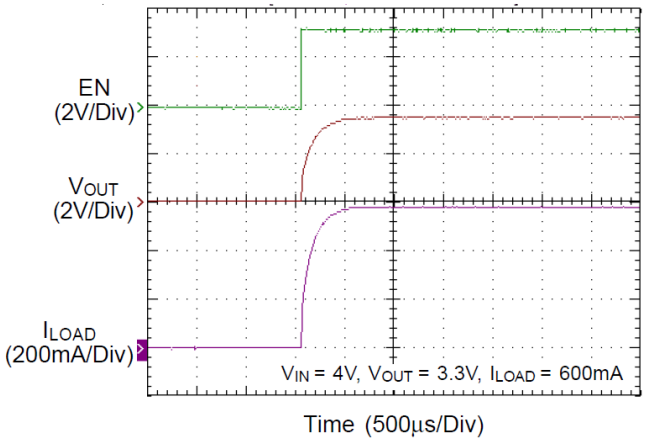
Fold-Back Current Limit vs. Temperature



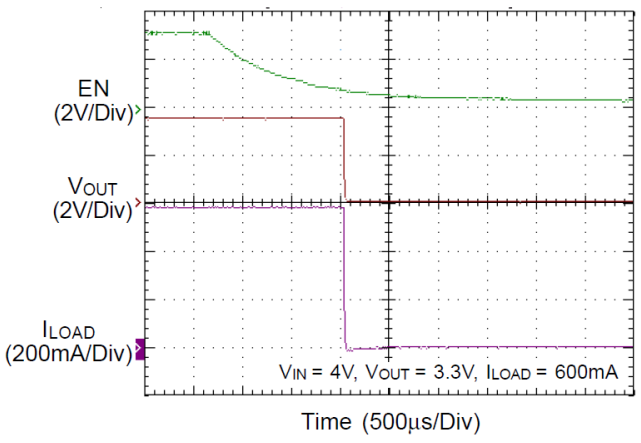
SNS Input Current vs. Temperature



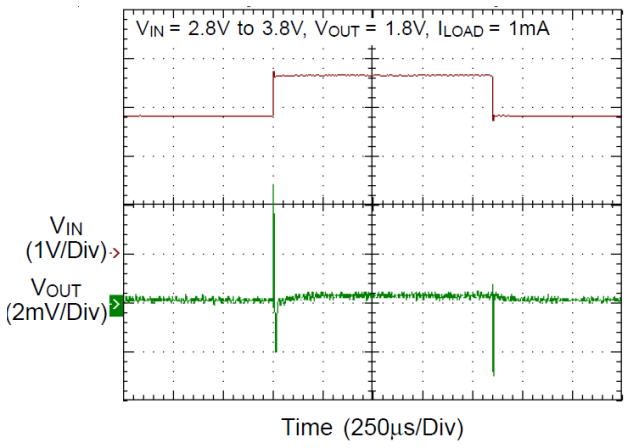
Power On from EN



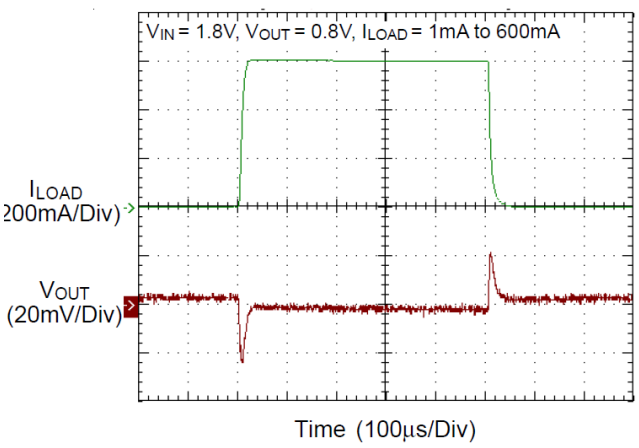
Power Off from EN

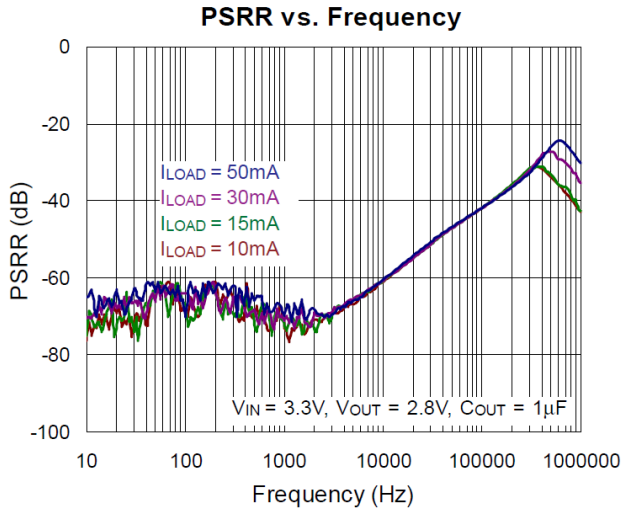


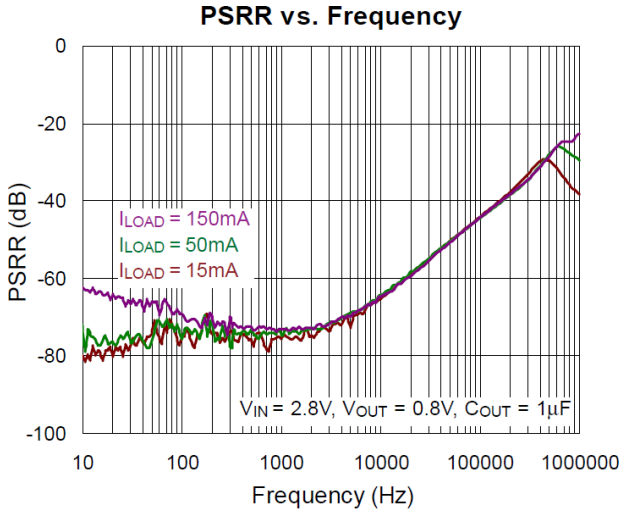
Line Transient

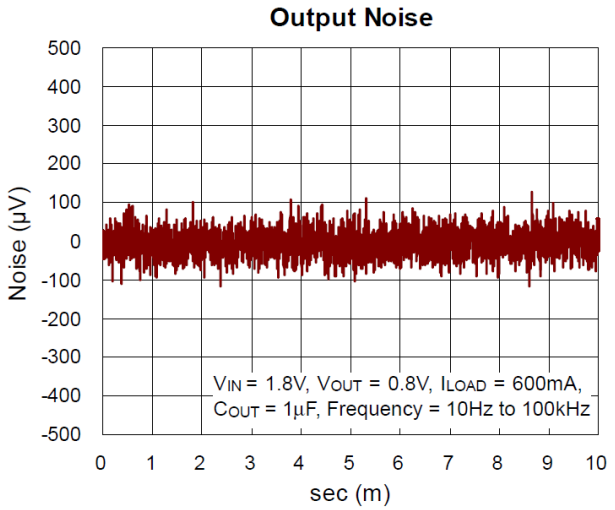


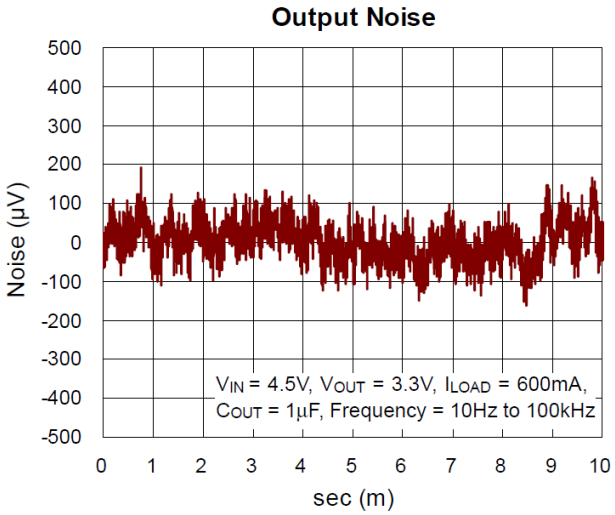
Load Transient











17 Operation

The RT9096/RT9096N is a 600mA low-quiescent low-dropout (LDO) linear regulator with a single supply input ranging from 1.2V to 5.5V. The output voltage is designed to operate in two modes for different purposes. In the adjustable mode, the RT9093 output voltage can be set from 0.8V to 3.3V. In the fixed mode, the output voltage is also available from 0.8V to 3.3V without the need for an external resistive voltage divider, saving on the bill of materials (BOM) counts in conditions where the PCB area is limited.

The RT9096/RT9096N integrates EN pin for system sequencing. It also features comprehensive protection, including input undervoltage lockout (UVLO), overcurrent protection (OCP), and over-temperature protection (OTP).

17.1 Undervoltage-Lockout (UVLO)

The RT9096/RT9096N implements undervoltage lockout (UVLO) circuitry to prevent operation under insufficient input voltage by constantly monitoring the VIN pin. Figure 5 illustrates the internal UVLO circuit's response to three different input voltage events (duration a, b, and c), assuming the EN pin voltage remains above the rising threshold (V_{EN_R}) at all times. During duration "a", as V_{IN} starts to rise, V_{OUT} begins to ramp up after V_{IN} exceeds the UVLO rising threshold voltage. Then V_{OUT} reaches the target level with the internal fixed soft-start time and remains in regulation. During duration "b", there is a voltage drop in the power line, but it does not fall below the UVLO falling threshold. The device continues normal operation, and V_{OUT} stays in regulation. During duration "c", V_{IN} drops below the UVLO falling threshold, causing the control loop to be disabled and regulation to cease. Consequently, V_{OUT} also drops.

In general applications, the instantaneous power line transients at the VIN pin will become worse due to longer power traces. As illustrated during duration "c", it leads to a collapse of V_{OUT}. To effectively enhance input power stabilization, it is recommended to add additional input capacitance or to improve the input trace layout on the PCB.

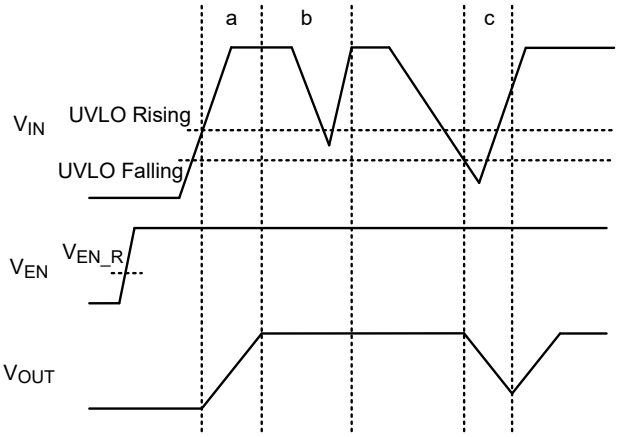


Figure 5. Undervoltage-Lockout Trigger Conditions and Output Variation

17.2 Enable and Shutdown

The RT9096/RT9096N provides an EN pin to enable or disable the device externally. When the EN pin voltage falls below the falling threshold (V_{EN_F}), the RT9096/RT9096N enters shutdown mode, even if the VIN pin voltage is above the UVLO rising threshold (V_{UVLO_R}). In shutdown mode, the supply current is reduced to a maximum of 0.5μA (I_{SHDN}). Once the EN pin voltage rises above the rising threshold (V_{EN_R}) and the VIN pin voltage is higher than the UVLO threshold, the internal digital circuit is enabled for normal operation. Additionally, the EN pin can be directly connected to the VIN pin to save the system's power rail.

17.3 Output Voltage Setting

Based on the typical application circuit, the RT9096/RT9096N offers two methods for output voltage setting, allowing adjustments within a range from 0.8V to 3.3V. Using the fixed mode for output voltage setting eliminates the need for an external resistive voltage divider, thereby saving on the bill of materials (BOM) count. In contrast, the adjustable mode allows the output voltage to be set by connecting a resistive voltage divider between VOUT and GND. The output voltage in this mode is calculated using the following equation:

$$V_{OUT} = V_{SNS} \times \frac{R1 + R2}{R2}$$

where V_{SNS} is the feedback reference voltage as determined in the Product Selection Table.

The current of the resistive voltage divider greater than 50μA is recommended to obtain a good temperature coefficient for the output voltage. As shown in Figure 6, the output voltage is approximately 3.35V with good temperature coefficient when SNS pin voltage is 0.8V and R1 = 51kΩ, R2 = 16kΩ.

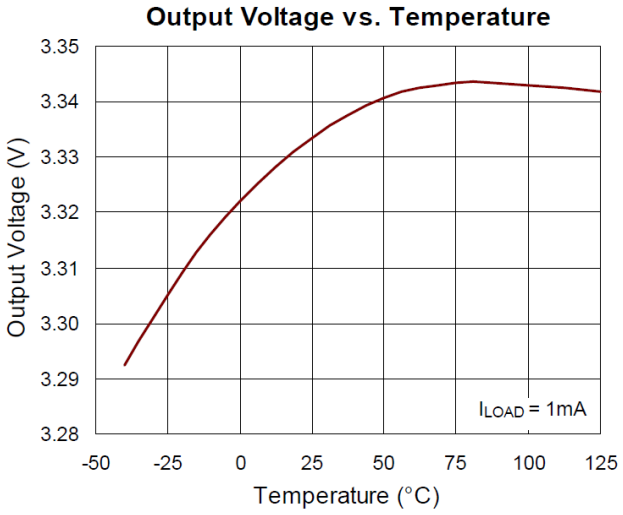


Figure 6. Temperature Coefficient of Adjustable Output Voltage

In addition, the quiescent current will also be increased when the current of the resistive voltage divider is greater than 50μA. Therefore, Figure 7 illustrates another application circuit for low power consumption conditions, and the fine-tuning range is recommended to be less than 50mV (R1 ≤ 91kΩ)

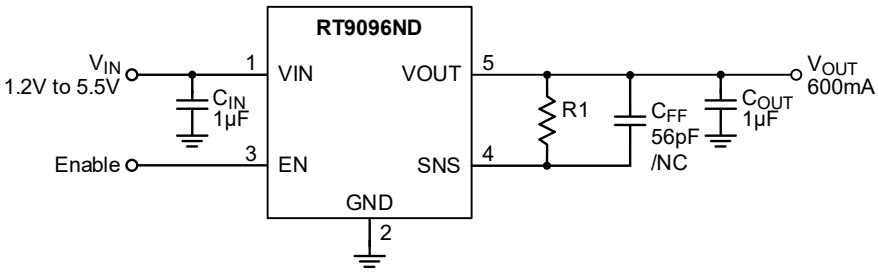


Figure 7. Fine Adjustable Output Voltage Application Circuit

17.4 Dropout Voltage

The dropout voltage, V_{DROP}, is the voltage difference between the VIN and VOUT pins while operating at a specific output current (I_{RATED}). It can also be expressed as the voltage drop across the pass-FET at a specific output current while the pass-FET is fully operating in the Ω region. In this context, the pass-FET can be characterized by its resistance, $R_{DS(ON)}$. Therefore, the dropout voltage can be defined by the equation $V_{DROP} = V_{IN} - V_{OUT} =$

$R_{DS(ON)}$ x I_{RATED}. For normal operation, it is recommended that the LDO's operating range be VIN > (V_{OUT} + V_{DROP}) to ensure better transient response and power supply rejection ratio (PSRR) performance. However, operation in the Ω region can severely degrade performance. In addition, the quiescent current will also be greatly increased when the linear regulators operate in the Ω region.

17.5 Output Active Discharge

The RT9096/RT9096N implements an output discharge function that quickly discharges the output capacitor through an internal 80Ω (typical) discharge resistor connected from the VOUT pin to GND. This function is activated when RT9096/RT9096N is disabled. It is important not to rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply collapses, as the reverse current may flow from the output to the input. If the device operates in a reverse voltage state, an external diode should be added for reverse current protection.

17.6 Overcurrent Protection (OCP)

The RT9096/RT9096N provides overcurrent protection (OCP) to prevent the IC from catastrophic damage under conditions of output overcurrent or short-circuit. This is achieved by continuously monitoring the output current. While the internal current limit circuitry is designed to inhibit the operation beyond the rated current, persistent operation above this threshold may compromise the reliability of the RT9096/RT9096N.

During current limiting, the output voltage drops as the load impedance decreases, eventually triggering thermal shutdown due to excessive power dissipation. Once the OCP condition is removed, the RT9096/RT9096N output or SNS pin voltage will return to the regulation setpoint, resuming normal operation.

17.7 Over-Temperature Protection (OTP)

The RT9096/RT9096N includes over-temperature protection (OTP) circuitry to prevent overheating. When the junction temperature exceeds the OTP threshold (T_{OTP}), the device is disabled. It will automatically resume normal operation once the junction temperature decreases by the amount of OTP hysteresis (T_{OTP_HYS}). Additionally, continuous operation at or into thermal shutdown, or maintaining a junction temperature above 125°C may diminish the reliability of the RT9096/RT9096N.

Note that the over-temperature protection is designed to protect the device during temporary overload conditions. It serves as a secondary fail-safe mechanism and is activated when operating conditions exceed the absolute maximum range. It should not be used as a substitute for proper thermal design in normal operation. Continuously operating the device above the specified absolute maximum junction temperature may compromise device reliability or result in permanent damage.

18 Application Information

(Note 11)

The RT9096/RT9096N is a low-dropout linear regulator capable of sourcing 600mA with a quiescent current of only 2μA. It supports an input voltage range from 1.2V to 5,5V and offers an adjustable output voltage from 0.8V to 3.3V. There are also options for fixed output voltage versions ranging from 0.8V to 3.3V. Additionally, it features an enable pin for sequencing control, making it well-suited for industrial applications.

18.1 Input Capacitor and Output Capacitor Selection

The RT9096/RT9096N is designed to support low equivalent-series-resistance (ESR) ceramic capacitors. X7R and C0G rated ceramic capacitors are recommended due to their stable capacitance over a range of temperatures. In contrast, the use of Y5V-rated capacitors is not recommended because of their large capacitance variations.

The input decoupling capacitor should have a capacitance greater than 1μF, and its voltage rating must exceed the maximum input voltage. The output capacitor should have a capacitance with a minimum effective capacitance of at least 0.7μF.

Note that a ceramic capacitor has a very low ESR and provides the best ripple performance. However, capacitance value can be affected by temperature and DC bias voltage, often decreasing as the DC bias voltage across the capacitor approaches its rated voltage. In many cases, the ceramic capacitors lose 50% or more of their rated capacitance under such conditions. Therefore, it is important to carefully select the value and case size of ceramic capacitors by considering the voltage coefficient.

18.2 Feed-Forward Capacitor (C_{FF})

When RT9096/RT9096N is the adjustable VOUT version, the output voltage can be set from 0.8V to 3.3V. An external feed-forward capacitor (C_{FF}) can be connected between VOUT and SNS pins to optimize the transient, noise, and PSRR performances. Note that using a higher capacitance of C_{FF} will result in a longer start-up time, and the power-good signal may incorrectly indicate that the output voltage is settled.

18.3 Input Inrush Current

During start-up, the inrush current into the VIN pin is the sum of the load current and the charging current of the output capacitor. Measuring the inrush current is challenging because it requires the removal of the input capacitor, which is not recommended. Generally, the soft-start inrush current can be estimated by the following equation:

$$I_{OUT}(t) = \frac{\left(C_{OUT} \times dV_{OUT}(t)\right)}{dt} + \left(\frac{V_{OUT}(t)}{R_{LOAD}}\right)$$

where $V_{OUT}(t)$ is the instantaneous output voltage during soft-start, $dV_{OUT}(t)/dt$ is the slope of the internal soft-start ramp and R_{LOAD} is the resistive load impedance.

18.4 Reverse Current Protection

In general applications, reverse current may occur if the output is biased above the input supply voltage level or if the input supply experiences an instantaneous drop during light load operation, resulting in V_{IN} being less than V_{OUT}. In such situations, if V_{OUT} exceeds V_{IN} by more than 0.3V, reverse current will flow through the body diode of the internal pass element, potentially causing damage over time. As illustrated in Figure 8, adding an external Schottky diode can protect the internal pass element from damage due to reverse current.

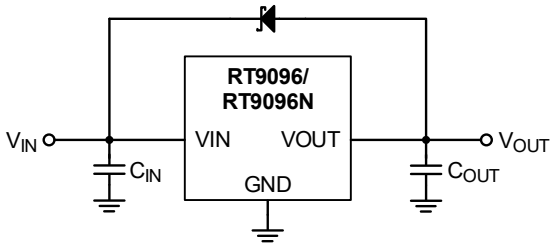


Figure 8. Application Circuit for Reverse Current Protection

18.5 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation is influenced by the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For TSOT-23-5 package, the thermal resistance, θ_{JA}, is 100.7°C/W on a standard JEDEC 51-7 four-layer thermal test board. For ZQFN-4L 1x1 package, the thermal resistance, θ_{JA}, is 236°C /W on a two-layer Richtek evaluation board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C)/(100.7°C/W) = 0.99W for TSOT-23-5 package.

$P_{D(MAX)}$ = (125°C – 25°C)/(236°C/W) = 0.42W for ZQFN-4L 1x1 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 9 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

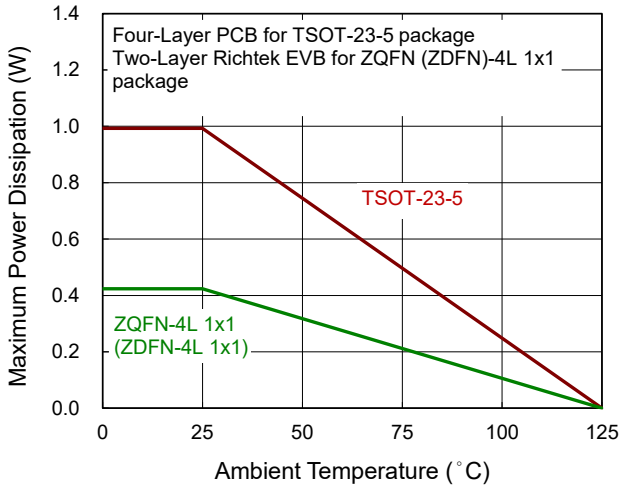


Figure 9. Derating Curve of Maximum Power Dissipation

18.6 Layout Considerations

For the best performance of the RT9096/RT9096N, the following PCB layout suggestions are highly recommended.

- Input capacitors must be placed as close as possible to the IC to minimize the power loop area.
- Minimize the power trace length and avoid using vias for the input and output capacitors connection.

Figure 10 and Figure 11 show layout reference examples, which help in minimizing inductive parasitic components, reducing load transients, and ensuring good circuit stability.

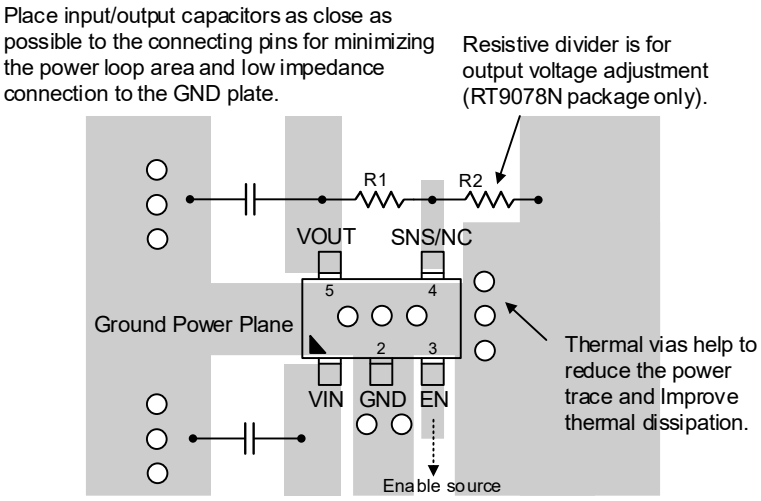


Figure 10. PCB Layout Guide for TSOT-23-5 Package

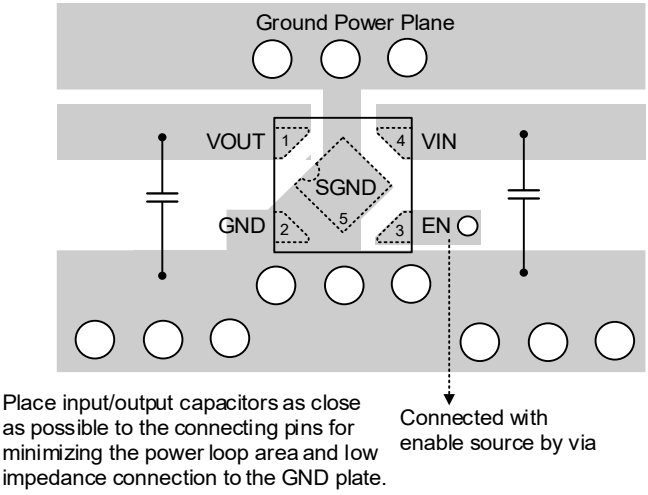
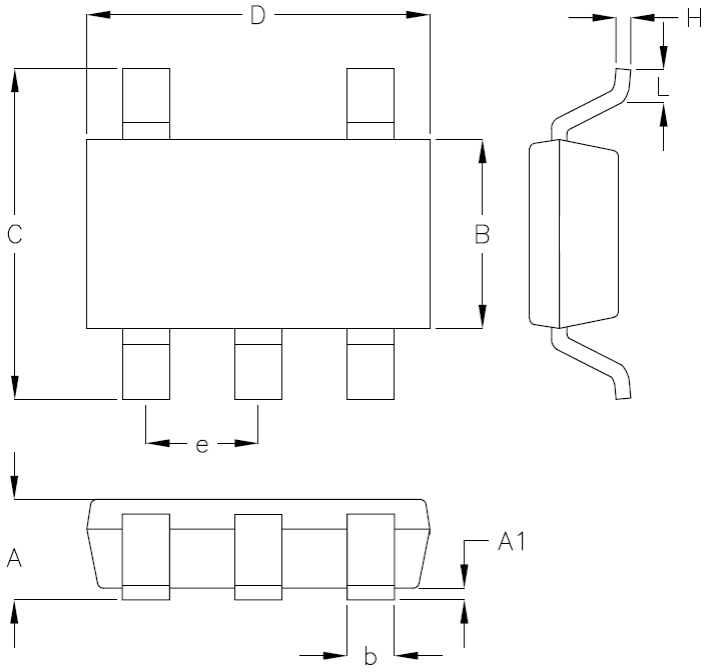


Figure 11. PCB Layout Guide for ZQFN-4L 1x1 Package

Note 11. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

19 Outline Dimension

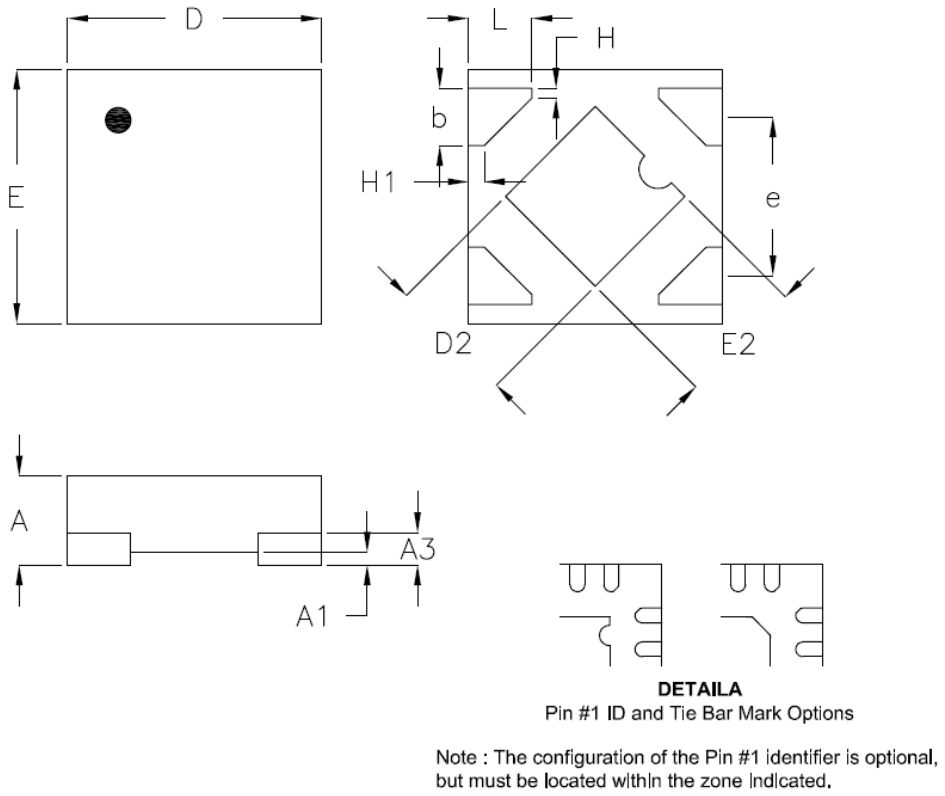
19.1 TSOT-23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.300	0.559	0.012	0.022
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-5 Surface Mount Package

19.2 ZQFN-4L 1x1 Package



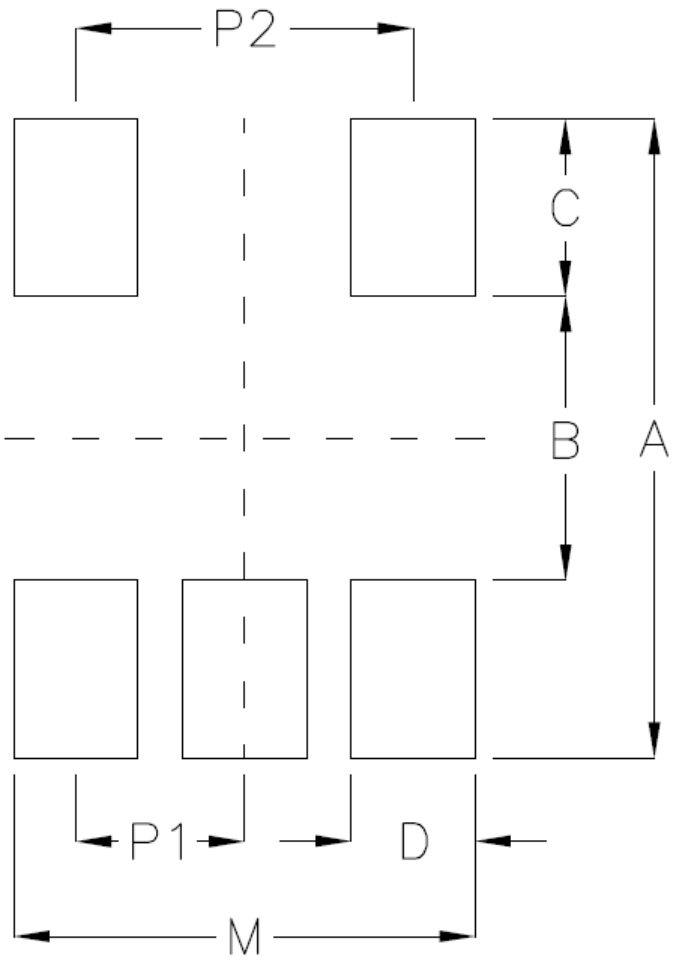
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.300	0.400	0.012	0.016
A1	0.000	0.050	0.000	0.002
A3	0.117	0.162	0.005	0.006
b	0.175	0.275	0.007	0.011
D	0.900	1.100	0.035	0.043
D2	0.450	0.550	0.018	0.022
E	0.900	1.100	0.035	0.043
E2	0.450	0.550	0.018	0.022
e	0.625		0.025	
L	0.200	0.300	0.008	0.012
H	0.039		0.002	
H1	0.064		0.003	

Z-Type 4L QFN 1x1 Package

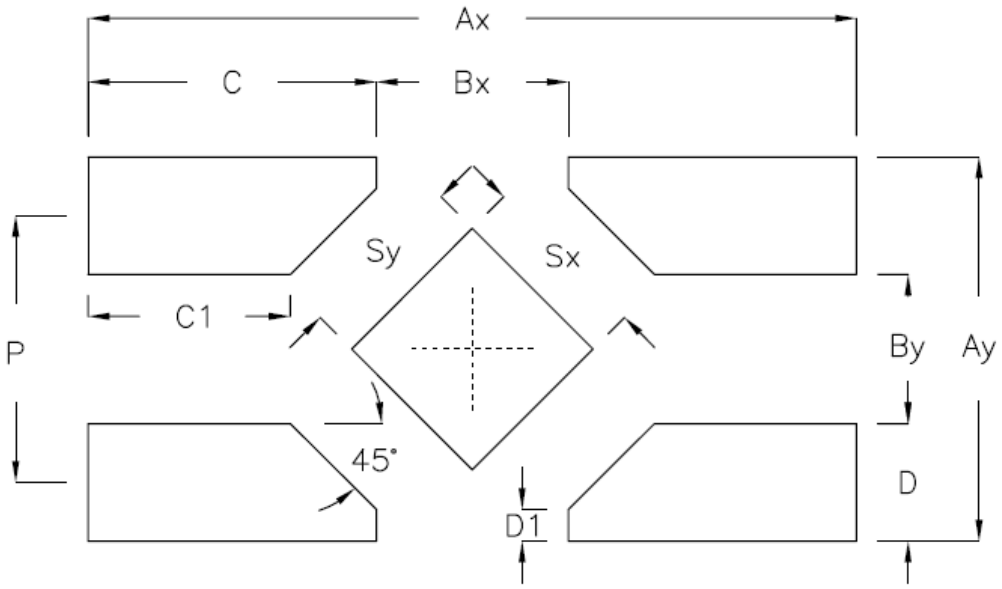
20 Footprint Information

20.1 TSOT-23-5 Package



Package	Number of Pin	Footprint Dimension (mm)							Tolerance
		P1	P2	A	B	C	D	M	
TSOT-25/TSOT-25(FC)/SOT-25	5	0.95	1.90	3.60	1.60	1.00	0.70	2.60	±0.10

20.2 ZQFN-4L 1x1 Package



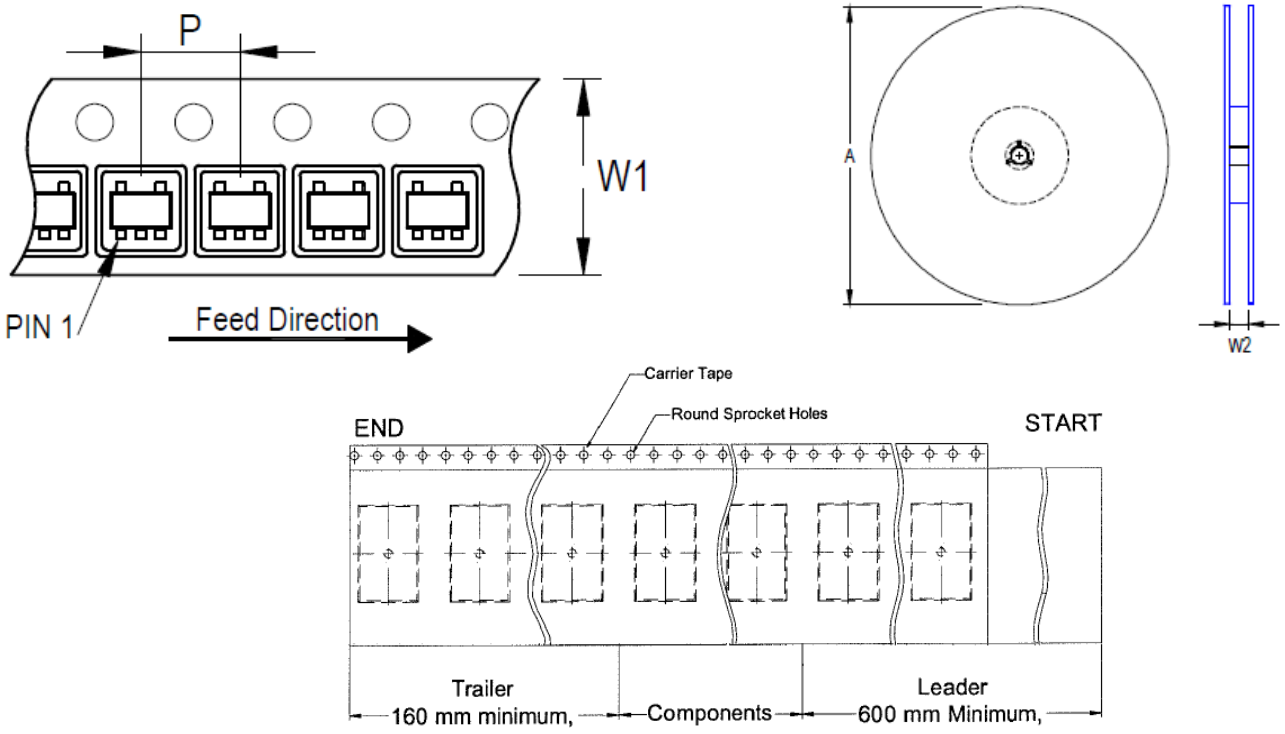
Package	Number of Pin	Footprint Dimension (mm)											Tolerance
		P	Ax	Ay	Bx	By	C	C1	D	D1	Sx	Sy	
U/X/ZQFN1x1-4	4	0.625	1.800	0.900	0.450	0.350	0.675	0.474	0.275	0.074	0.400	0.400	±0.050

21 Packing Information

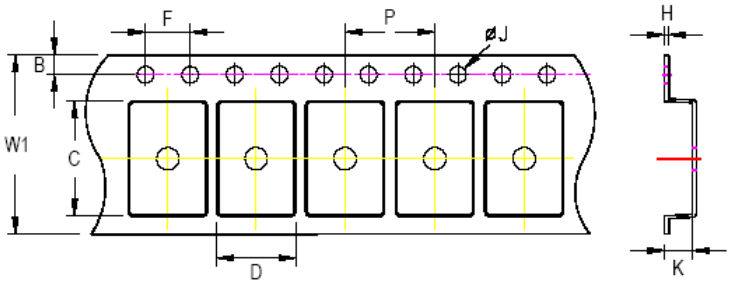
21.1 Tape and Reel Data

21.1.1 TSOT-23-5

SOT/TSOT-23-5



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader(mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
TSOT-23-5	8	4	180	7	3,000	160	600	8.4/9.9

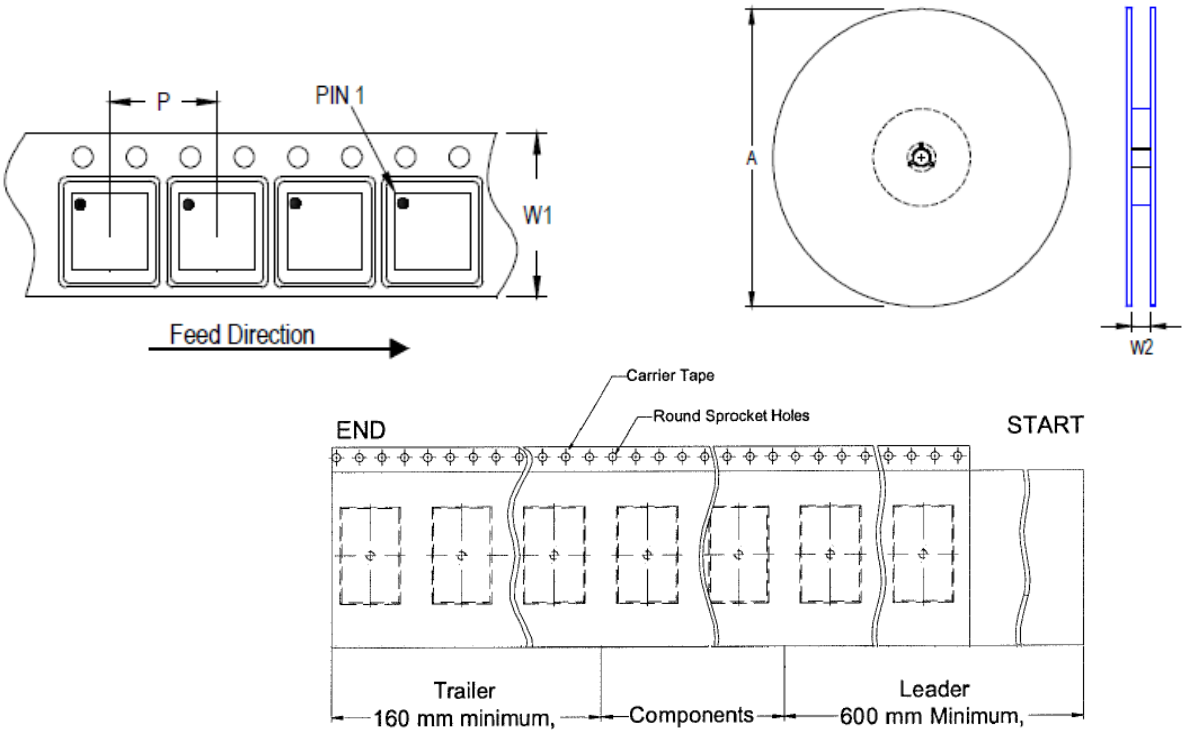


C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 8mm carrier tape: 0.5mm maximum

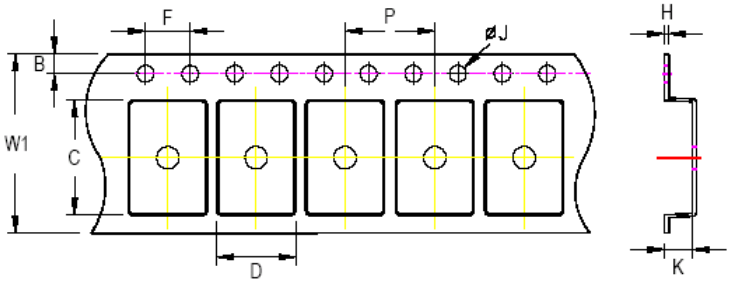
Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.2mm	0.6mm

21.1.2 ZQFN-4L 1x1

21.1.2.1 Quadrant 1



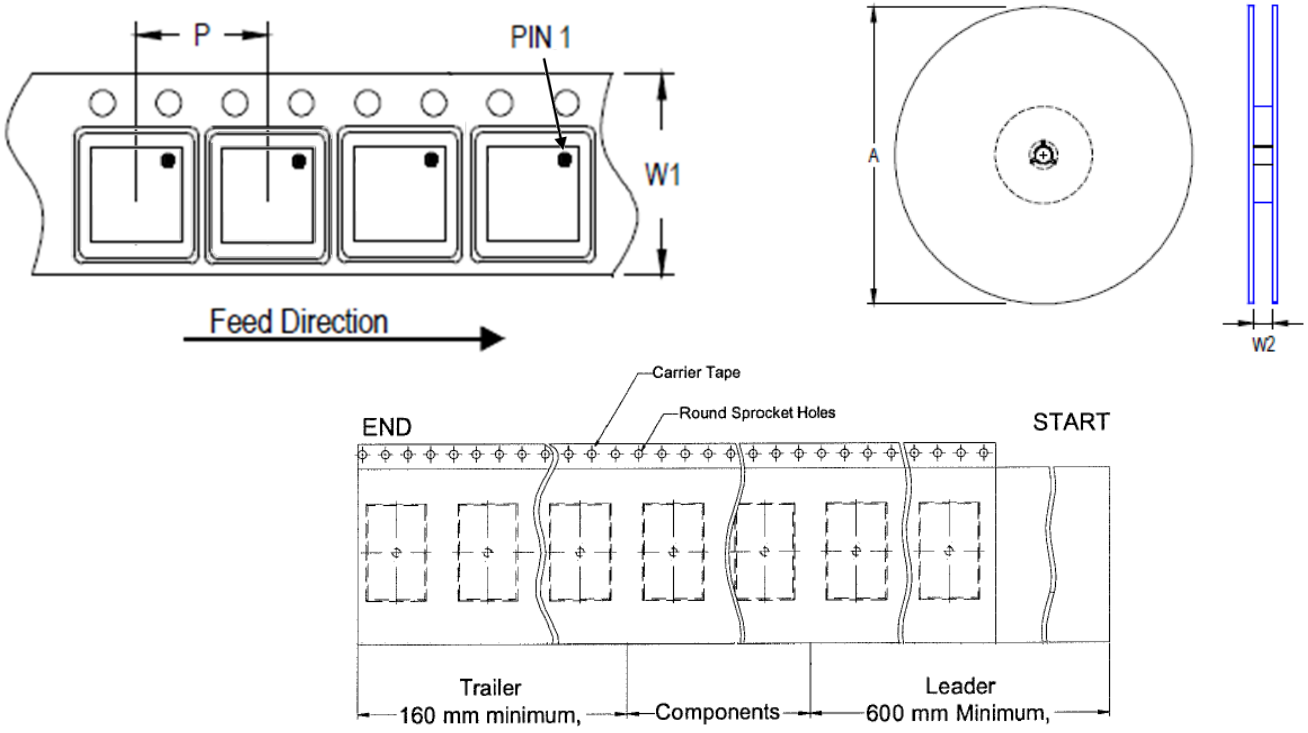
Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(Z) QFN/DFN 1x1	8	4	180	7	2,500	160	600	8.4/9.9



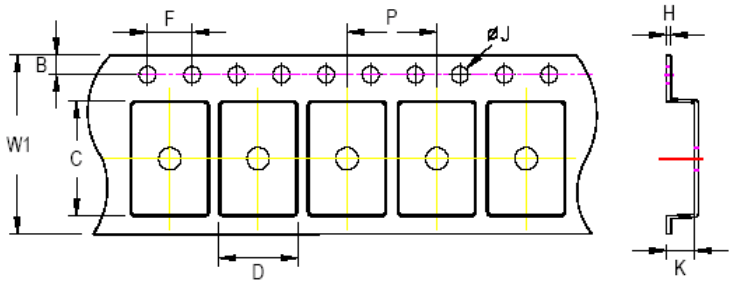
C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 8mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.5mm	0.6mm	0.6mm

21.1.2.2 Quadrant 2



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader(mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(Z) QFN/DFN 1x1	8	4	180	7	2,500	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.5mm	0.6mm	0.6 mm

21.2 Tape and Reel Packing

21.2.1 TSOT-23-5

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
TSOT-23-5	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

21.2.2 ZQFN-4L 1x1

21.2.2.1 Quadrant 1

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(Z) QFN/DFN 1x1	7”	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

21.2.2.2 Quadrant 2

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(Z) QFN/DFN 1x1	7”	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}

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22 Datasheet Revision History

Version	Date	Description
00	2026/3/18	First Edition