

2.65W PWM Class-D Power Amplifier

General Description

The RT9101 is a 2.65W, high efficiency Class-D audio amplifier featuring low-resistance internal power MOSFETs and the gain can be set by an external input resistance. The filter free topology eliminates the output filter and reduces the external component count, footprint area, and system costs.

Operating from a single 5V supply, the RT9101 is capable of driving 4Ω speaker load at a continuous average output of 2.65W/10% THD+N or 2W/0.5% THD+N. The RT9101 has a higher efficiency with speaker load compared to a typical class AB amplifier. With a 3.6V supply driving an 8Ω speaker, the efficiency for a 400mW power level is 88%.

It is very suitable for power sensitive application, such as cellular handsets and battery powered devices. In addition to these features, the RT9101 provides a fast startup time to minimize audible popping during device turn-on and turn-off. Moreover, the RT9101 also integrates thermal and over current protection circuits.

The RT9101 is available in WDFN-8L 3x3, and WL-CSP-9B 1.45x1.45 (BSC) packages.

Ordering Information

| | |
|-------------|---|
| RT9101□(□)□ | |
| □ | Package Type QW : WDFN-8L 3x3 (W-Type) WSC : WL-CSP-9B 1.45x1.45 (BSC) |
| □ | Lead Plating System G : Green (Halogen Free and Pb Free) Z : ECO (Ecological Element with Halogen Free and Pb free) |
| □ | Default : WDFN-8L 3x3 C : WL-CSP-9B 1.45x1.45 (BSC) |

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Features

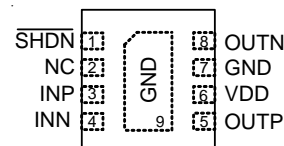
- **Wide Operating Voltage : 2.5V to 5.5V**
- **High Efficiency With an 8Ω Speaker :**
 - ▶ **88% at 400mW**
 - ▶ **80% at 100mW**
- **Low Quiescent Current and Shutdown Current**
- **Optimized PWM Output Stage Eliminates LC Filter**
- **Fully Differential Design Reduces RF Rectification and Eliminates Bypass Capacitor**
- **Internally Generated 250kHz Switching Frequency**
- **Integrated Pop and Click Suppression Circuitry**
- **RoHS Compliant and Halogen Free**

Applications

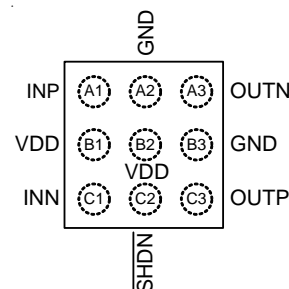
- Mobile Phones
- Handsets
- PDAs
- Portable multimedia devices

Pin Configurations

(TOP VIEW)



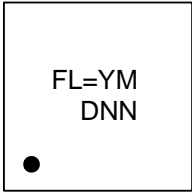
WDFN-8L 3x3



WL-CSP-9B 1.45x1.45 (BSC)

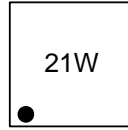
Marking Information

RT9101GQW



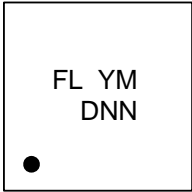
FL : Product Code
YMDNN : Date Code

RT9101CWSC



21 : Product Code
W : Date Code

RT9101ZQW



FL : Product Code
YMDNN : Date Code

Typical Application Circuit

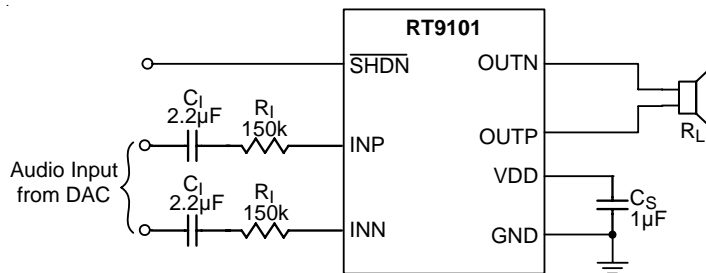


Figure 1. Application Circuit with Differential Input

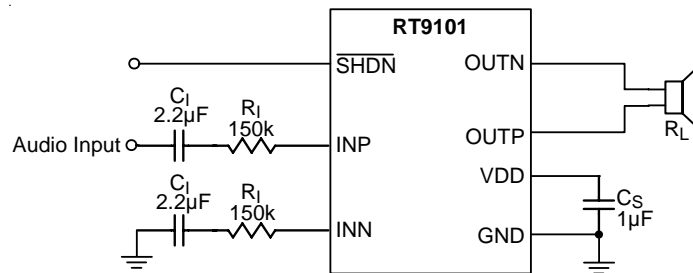
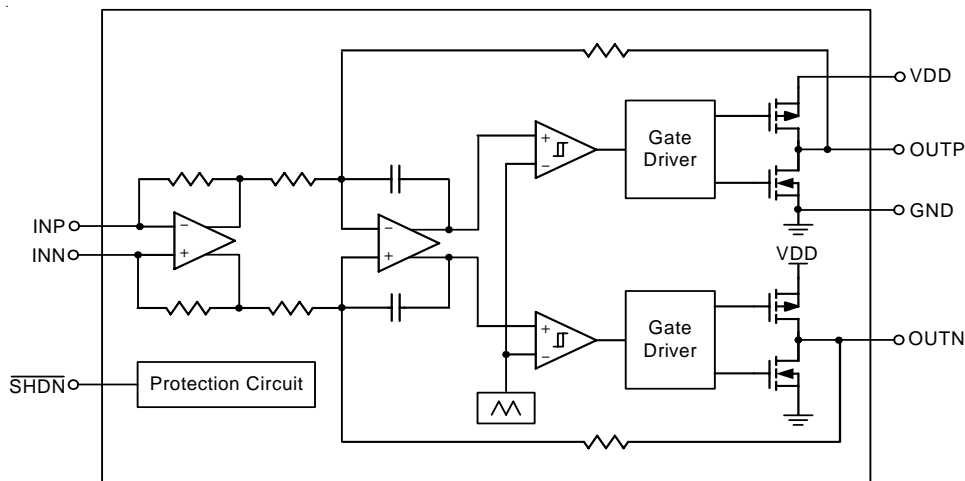


Figure 2. Application Circuit with Single-Ended Input

Functional Pin Description

| Pin No. | | Pin Name | Pin Function |
|--------------------|---------------------------|----------|---|
| WDFN-8L 3x3 | WL-CSP-9B 1.45x1.45 (BSC) | | |
| 1 | C2 | SHDN | Shutdown Control (Active Low). |
| 2 | -- | NC | No Internal Connection. |
| 3 | A1 | INP | Positive Input of Differential Audio Signal. |
| 4 | C1 | INN | Negative Input of Differential Audio Signal. |
| 5 | C3 | OUTP | Positive Output. |
| 6 | B1, B2 | VDD | Supply Voltage Input. |
| 7, 9 (Exposed Pad) | A2, B3 | GND | Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation. |
| 8 | A3 | OUTN | Negative Output. |

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{DD} ----- -0.3V to 6V
- Input Voltage, INP, INN ----- -0.3V to ($V_{DD} + 0.3V$)
- Power Dissipation, P_D @ $T_A = 25^\circ C$
 - WDFN-8L 3x3 ----- 1.429W
 - WL-CSP-9B 1.45x1.45 (BSC) ----- 1.250W
- Package Thermal Resistance (Note 2)
 - WDFN-8L 3x3, θ_{JA} ----- $70^\circ C/W$
 - WDFN-8L 3x3, θ_{JC} ----- $8.2^\circ C/W$
 - WL-CSP-9B 1.45x1.45 (BSC), θ_{JA} ----- $80^\circ C/W$
- Junction Temperature ----- $150^\circ C$
- Lead Temperature (Soldering, 10 sec.) ----- $260^\circ C$
- Storage Temperature Range ----- $-65^\circ C$ to $150^\circ C$
- ESD Susceptibility (Note 3)
 - HBM (Human Body Mode) ----- 2kV
 - MM (Machine Mode) ----- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{DD} ----- 2.7V to 5.5V
- Junction Temperature Range ----- $-40^\circ C$ to $125^\circ C$
- Ambient Temperature Range ----- $-40^\circ C$ to $85^\circ C$

Electrical Characteristics

($V_{DD} = 5V$, $T_A = 25^\circ C$, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|--|--------------|---|------------|------------|------------|------------|
| Output Offset Voltage | V_{OS} | $V_{DD} = 2.5V$ to $5.5V$ | -- | 1 | 25 | mV |
| Power Supply Rejection Ratio | PSRR | $V_{DD} = 2.5V$ to $5.5V$ (Note 5) | -- | -70 | -55 | dB |
| High Level Input Current | $ I_{IH} $ | $V_{DD} = 5.5V$, $V_I = 5.8V$ | -- | -- | 100 | μA |
| Low Level Input Current | $ I_{IL} $ | $V_{DD} = 5.5V$, $V_I = -0.3V$ | -- | -- | 5 | μA |
| SHDN Input Threshold Voltage | Logic-High | V_{IH} | 2 | -- | -- | V |
| | Logic-Low | V_{IL} | -- | -- | 0.4 | |
| Quiescent Current | I_Q | $V_{DD} = 5.5V$, No Load | -- | 3.4 | 4.9 | mA |
| | | $V_{DD} = 3.6V$, No Load | -- | 2.8 | -- | |
| | | $V_{DD} = 2.5V$, No Load | -- | 2.2 | 3.2 | |
| Shutdown Current | I_{SHDN} | $V_{SHDN} = 0V$, $V_{DD} = 2.5V$ to $5.5V$ | -- | -- | 1 | μA |
| Static Drain-Source On-State Resistance | $R_{DS(ON)}$ | $V_{DD} = 2.5V$ | -- | 600 | -- | m Ω |
| | | $V_{DD} = 3.6V$ | -- | 500 | -- | |
| | | $V_{DD} = 5V$ | -- | 400 | -- | |
| Output Impedance in \overline{SHDN} | | $V_{SHDN} = 0V$ | -- | >1 | -- | k Ω |
| Switching Frequency | | $V_{DD} = 2.5V$ to $5.5V$ | 200 | 250 | 300 | kHz |
| Gain | | $V_{DD} = 2.5V$ to $5.5V$ | $284k/R_I$ | $300k/R_I$ | $316k/R_I$ | V/V |
| Resistance from \overline{SHDN} to GND | | | -- | 200 | -- | k Ω |

To be continued

Operating Characteristics

(Gain = 2V/V, $R_L = 8\Omega$, $T_A = 25^\circ\text{C}$, unless otherwise noted)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit | |
|--------------------------------------|--------|--|-----------------|------|------|-----------|---|
| Output Power | P_O | THD+N = 10%, f = 1kHz, $R_L = 4\Omega$ | $V_{DD} = 5V$ | -- | 2.65 | -- | W |
| | | | $V_{DD} = 3.6V$ | -- | 1.5 | -- | |
| | | | $V_{DD} = 2.5V$ | -- | 0.52 | -- | |
| | | THD+N = 1%, f = 1kHz, $R_L = 4\Omega$ | $V_{DD} = 5V$ | -- | 2.08 | -- | W |
| | | | $V_{DD} = 3.6V$ | -- | 1.06 | -- | |
| | | | $V_{DD} = 2.5V$ | -- | 0.42 | -- | |
| | | THD+N = 10%, f = 1kHz, $R_L = 8\Omega$ | $V_{DD} = 5V$ | -- | 1.45 | -- | W |
| | | | $V_{DD} = 3.6V$ | -- | 0.73 | -- | |
| | | | $V_{DD} = 2.5V$ | -- | 0.33 | -- | |
| | | THD+N = 1%, f = 1kHz, $R_L = 8\Omega$ | $V_{DD} = 5V$ | -- | 1.19 | -- | W |
| | | | $V_{DD} = 3.6V$ | -- | 0.59 | -- | |
| | | | $V_{DD} = 2.5V$ | -- | 0.26 | -- | |
| Total Harmonic Distortion Plus Noise | THD+N | $V_{DD} = 5V, P_O = 1W, R_L = 8\Omega, f = 1kHz$ | -- | 0.06 | -- | % | |
| | | $V_{DD} = 3.6V, P_O = 0.5W, R_L = 8\Omega, f = 1kHz$ | -- | 0.05 | -- | | |
| | | $V_{DD} = 2.5V, P_O = 200mW, R_L = 8\Omega, f = 1kHz$ | -- | 0.04 | -- | | |
| Supply Ripple Rejection Ratio | PSRR | $V_{DD} = 5V, f = 217Hz, V_{DD-Ripple} = 200mV_{pp}$ | -- | -70 | -- | dB | |
| Signal-to-Noise Ratio | SNR | $V_{DD} = 5V, P_O = 1W, R_L = 8\Omega, A$ Weighting Filter | -- | 95 | -- | dB | |
| Input Impedance | Z_i | | 142 | 150 | 158 | $k\Omega$ | |
| Start-Up Time from Shutdown | | $V_{DD} = 3.6V$ | -- | 1 | -- | ms | |

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in natural convection at $T_A = 25^\circ\text{C}$ on a high-effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.

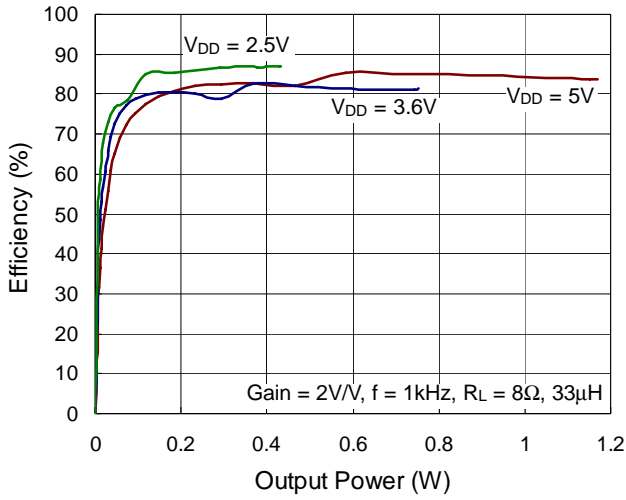
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

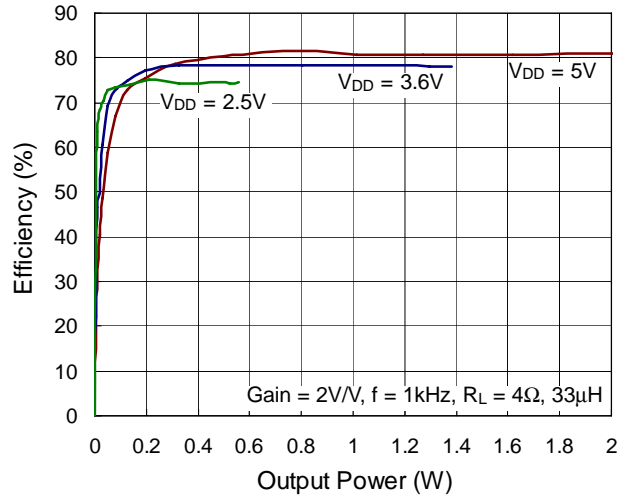
Note 5. Guarantee by design.

Typical Operating Characteristics

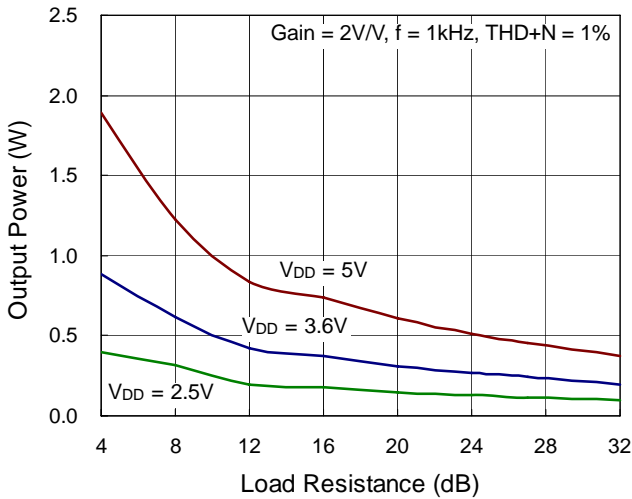
Efficiency vs. Output Power



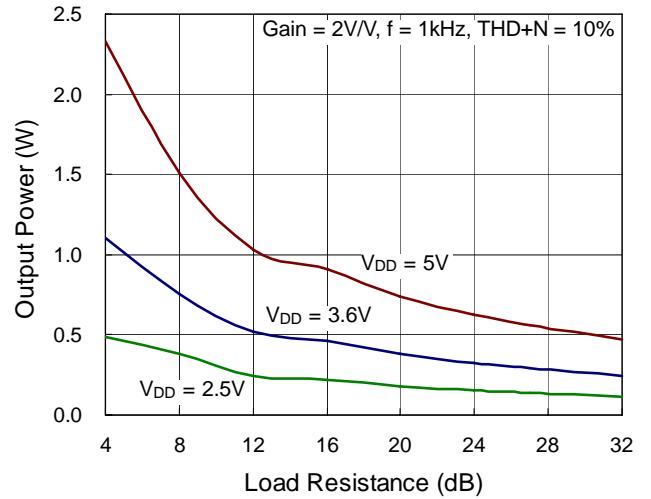
Efficiency vs. Output Power



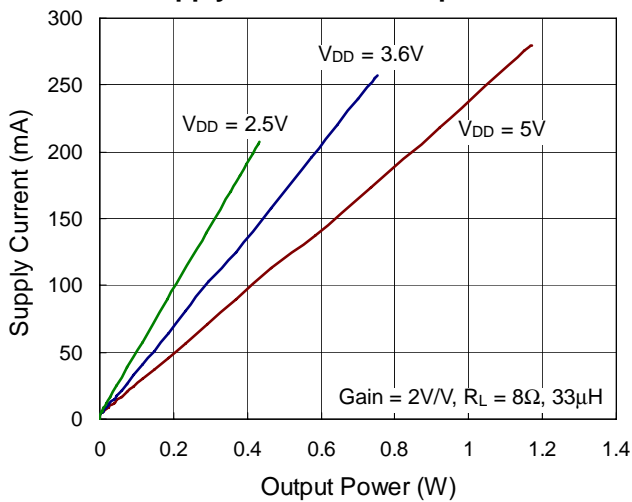
Output Power vs. Load Resistance



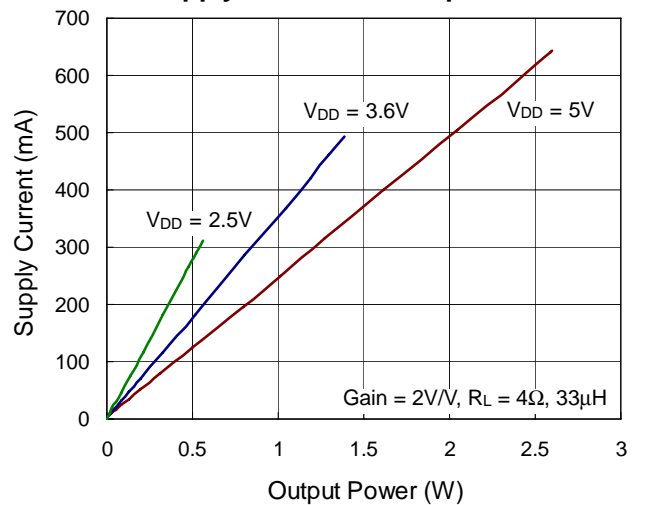
Output Power vs. Load Resistance



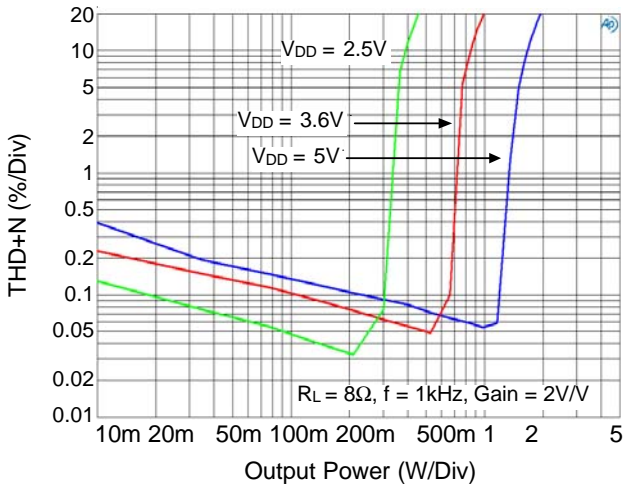
Supply Current vs. Output Power



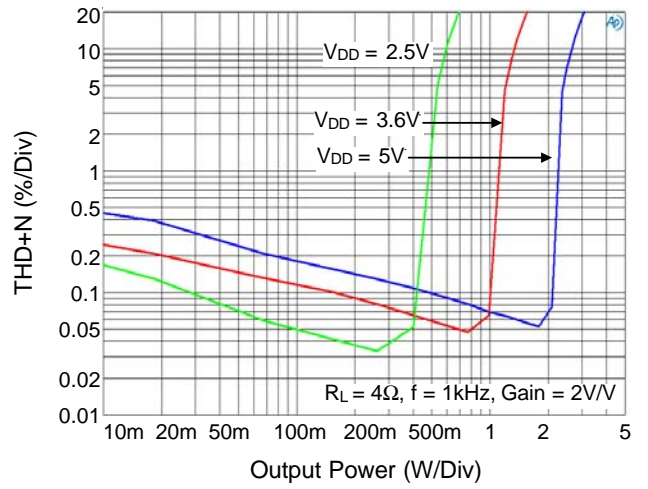
Supply Current vs. Output Power



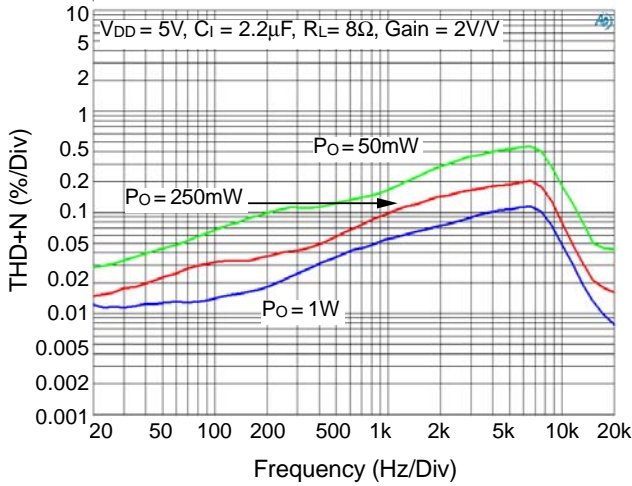
THD+N vs. Output Power



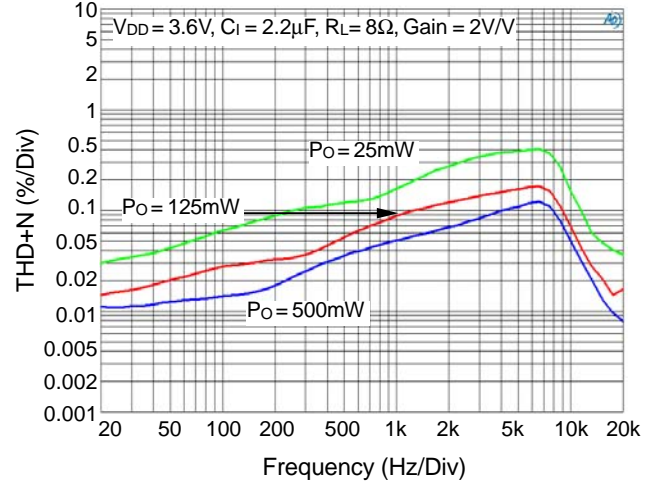
THD+N vs. Output Power



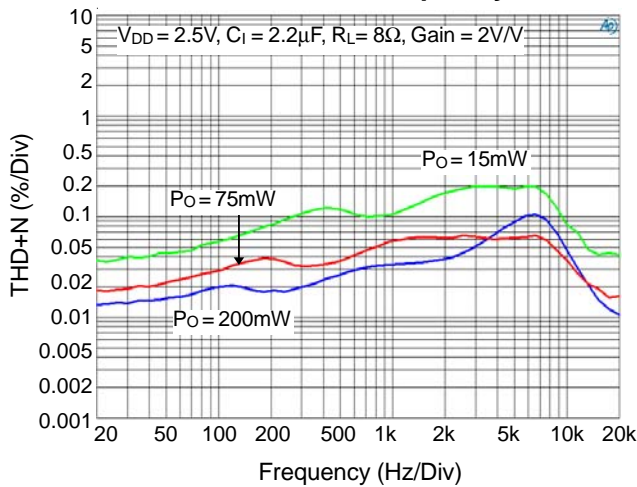
THD+N vs. Frequency



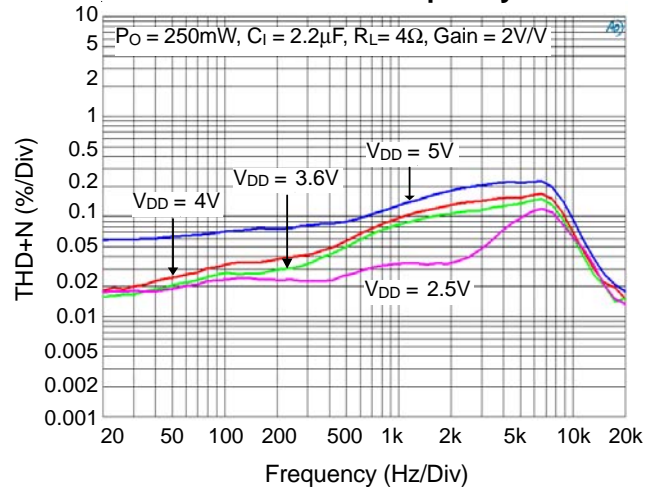
THD+N vs. Frequency



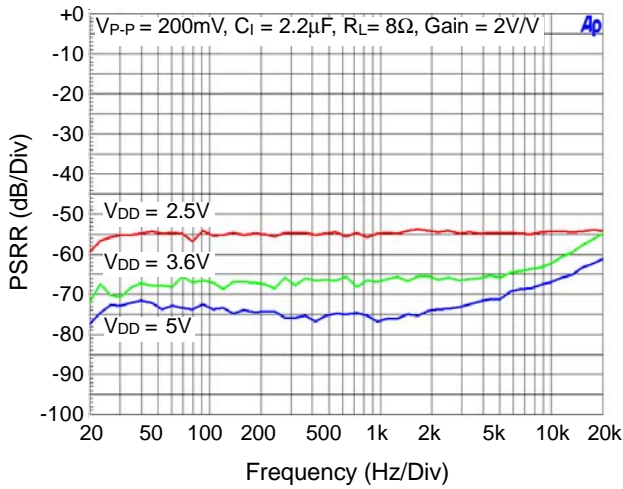
THD+N vs. Frequency



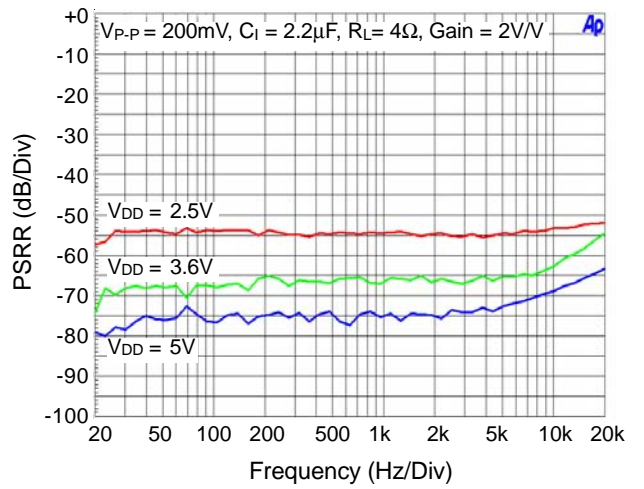
THD+N vs. Frequency



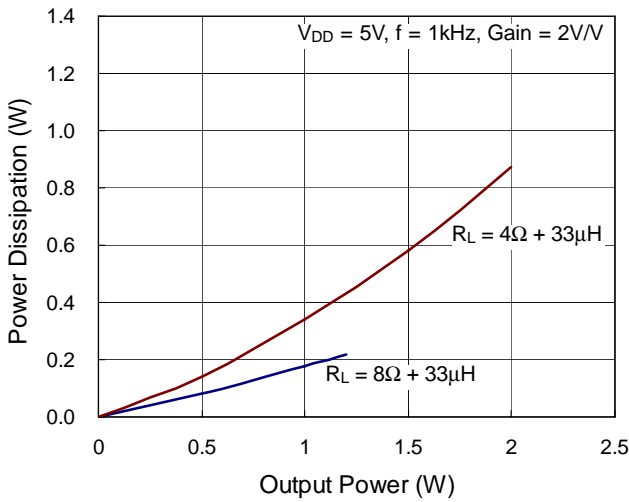
PSRR vs. Frequency



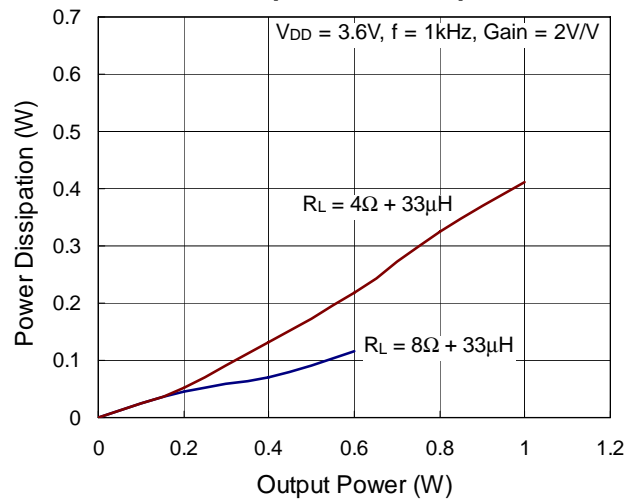
PSRR vs. Frequency



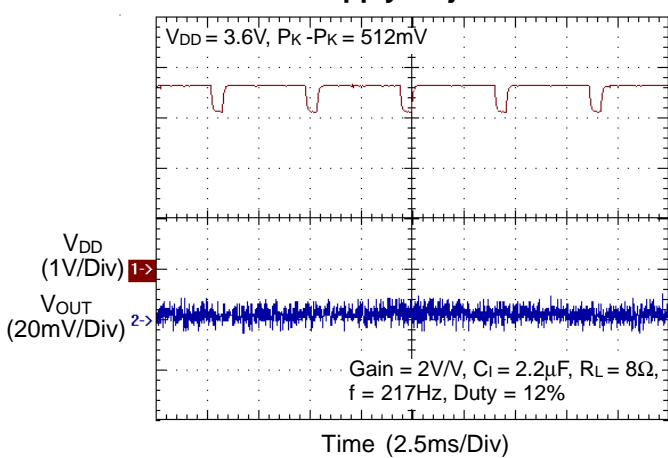
Power Dissipation vs. Output Power



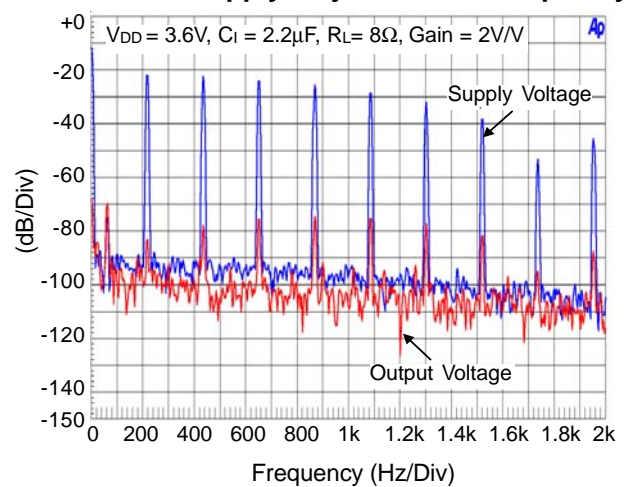
Power Dissipation vs. Output Power



GSM Power Supply Rejection vs. Time



GSM Power Supply Rejection vs. Frequency



Application information

The RT9101 is a fully differential amplifier with differential inputs and outputs. The RT9101 integrates a differential amplifier and a common mode voltage controller. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The RT9101 can support differential input and single ended input applications.

Components Selection

Input Resistors (R_I)

Amplifier can be resistors and the gain can be calculated as the following equation :

$$\text{Gain} = \frac{2 \times 150\text{k}\Omega}{R_I}$$

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the input resistors. CMRR, PSRR, and the cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance or better resistors to keep the performance optimized.

The input resistors should be placed very close to the RT9101 to limit noise injection on the high impedance nodes. It is recommended to set the gain at 2V/V or lower for better performance.

Decoupling Capacitor

The RT9101 is a high performance Class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low Equivalent-Series-Resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the VDD pin can achieve the best performance. Placing this decoupling capacitor close to the RT9101 is very important for the efficiency of the Class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower frequency noise signals, it is recommended to use a 10μF or greater capacitor placed near the audio power amplifier.

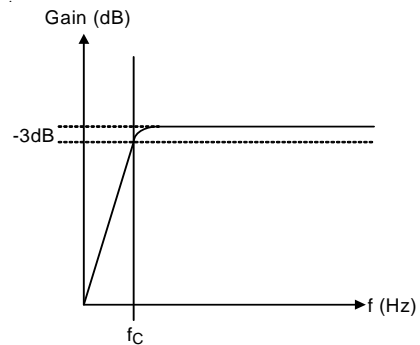
Input Capacitor

In the typical application, an input coupling capacitor (C_I) is required to allow the input signal to the proper dc level for optimum operation.

However, the RT9101 is a fully differential amplifier with good CMRR so that the RT9101 does not require input coupling capacitors if using a differential input source that is biased from 0.5 V to VDD – 0.8 V. Use 1% tolerance or better gain-setting resistors if input coupling capacitors are not used.

In the single-ended input application, an input capacitor, (C_I), is required to allow the amplifier to bias the input signal to the proper dc level. In this case, C_I and R_I form a high-pass filter with the corner frequency as shown in the following equation :

$$f_c = \frac{1}{2\pi R_I C_I}$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. For example, the flat bass response requirement is 10 Hz and R_I is 20kΩ, the value of C_I can be calculated by the following equation :

$$C_I = \frac{1}{2\pi R_I f_c}$$

In this example, C_I is 0.8μF. A capacitance 1μF or larger can be used.

Under Voltage Lockout

The under voltage lock out circuit operates as a voltage detector and always monitors the supply voltage (VDD) while $\overline{\text{SHND}} = 1$. While powered on, the chip is kept still in shutdown mode until VDD rises to greater than 2.2V (typ). While powered off, the chip does not leave operation mode until VDD falls to less than 2.1V (typ).

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT9101, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA} , is layout dependent. For WDFN-8L 3x3 packages, the thermal resistance, θ_{JA} , is 70°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WL-CSP-9B 1.45x1.45 (BSC) packages, the thermal resistance, θ_{JA} , is 80°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by the following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (70^\circ\text{C/W}) = 1.429\text{W for WDFN-8L 3x3 package}$$

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (80^\circ\text{C/W}) = 1.250\text{W for WL-CSP-9B 1.45x1.45 (BSC) package}$$

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA} . For the RT9101 packages, the derating curves in Figure 3 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

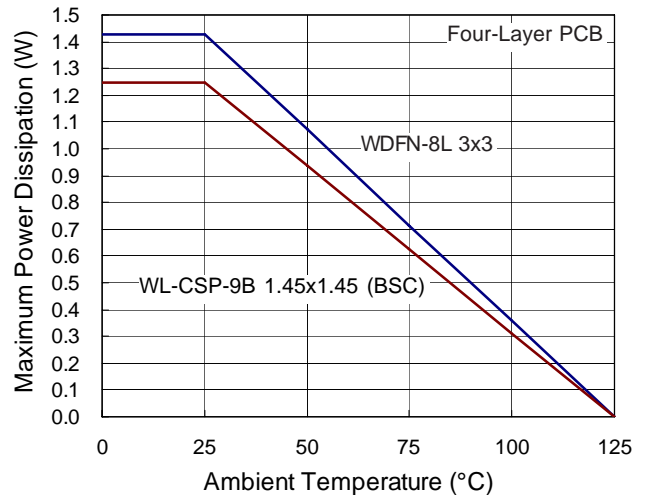


Figure 3. Derating Curves for RT9101 Packages

Layout Considerations

For best performance of the RT9101, the following PCB Layout guidelines must be strictly followed.

- ▶ Place the decoupling capacitors as close as possible to the VDD and GND pins.
- ▶ Keep the differential input and output traces as wide and short as possible. The traces of (INP & INN) and (OUTP & OUTN) should be kept equal width and length respectively.
- ▶ Connect the GND and Exposed Pad to a strong ground plane for maximum thermal dissipation and noise protection.

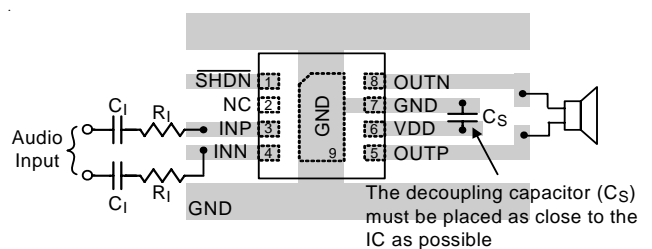
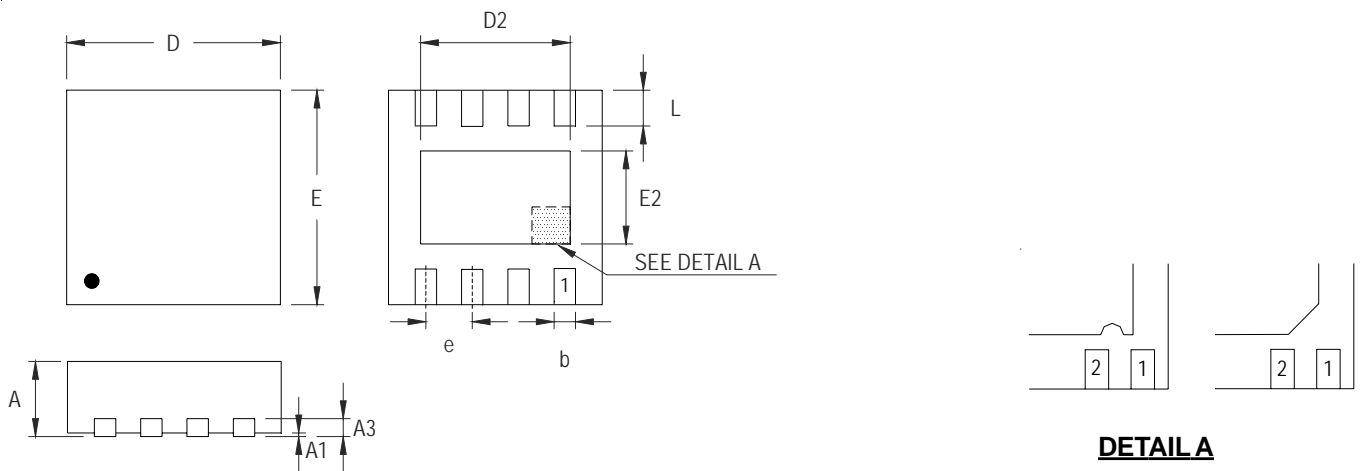


Figure 4. PCB Layout Guide

Outline Dimension



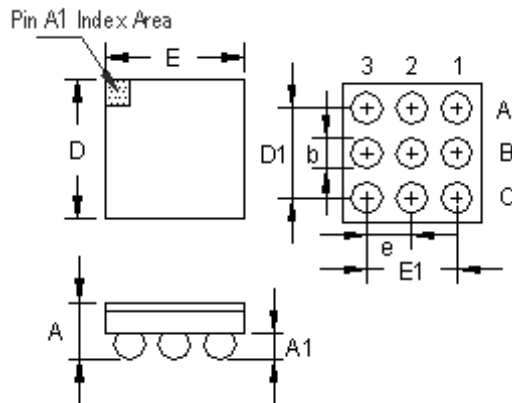
DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.200 | 0.300 | 0.008 | 0.012 |
| D | 2.950 | 3.050 | 0.116 | 0.120 |
| D2 | 2.100 | 2.350 | 0.083 | 0.093 |
| E | 2.950 | 3.050 | 0.116 | 0.120 |
| E2 | 1.350 | 1.600 | 0.053 | 0.063 |
| e | 0.650 | | 0.026 | |
| L | 0.425 | 0.525 | 0.017 | 0.021 |

W-Type 8L DFN 3x3 Package



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.525 | 0.625 | 0.021 | 0.025 |
| A1 | 0.200 | 0.260 | 0.008 | 0.010 |
| b | 0.290 | 0.350 | 0.011 | 0.014 |
| D | 1.400 | 1.500 | 0.055 | 0.059 |
| D1 | 1.000 | | 0.039 | |
| E | 1.400 | 1.500 | 0.055 | 0.059 |
| E1 | 1.000 | | 0.039 | |
| e | 0.500 | | 0.020 | |

9B WL-CSP 1.45x1.45 Package (BSC)

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