

30W, Stereo, Ultra-Low Noise, High-Efficiency, Inductor-Less, I²S General-Purpose Class-D Audio Amplifier with DRC Control

1 General Description

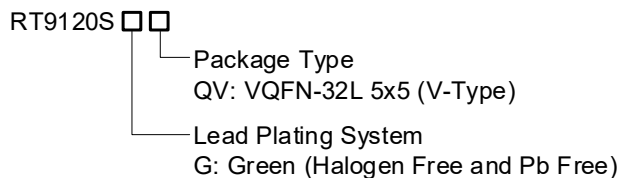
The RT9120S is a high efficiency, I²S-input, stereo channel audio power amplifier delivering maximum 2x30W into 8Ω BTL speaker loads. It can deliver over 94% power efficiency at 2x10W and eliminate the need for heatsink.

The built-in anti-pop functions can reduce the speaker's pop noise under all kind of scenarios. Built-in protection circuits can provide over-temperature, overcurrent, overvoltage, undervoltage protections and report error status.

The RT9120S is a 3-wired device receiving all clocks from external sources with standard I²S, Left-justified, Right-justified or TDM formats. It can support wide input sampling rate from 8kHz to 192kHz.

The RT9120S features one band DRC and flexible input mixer, and power clipping.

2 Ordering Information



Note 1.

Richtek products are Richtek Green Policy compliant and marked with ⁽¹⁾ indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

3 Features

- **Wide Input Supply Range: 4.5V to 26.4V**
- **Support 1.8V, 3.3V I/O**
- **Configurable 4 Different IC Slave Address**
- **1x53W, 1.0 Mode (4Ω, 22V, THD + N = 1%)**
- **2x30W, 2.0 Mode (8Ω, 24V, THD + N = 1%)**
- **SNR up to 113dB**
- **THD + N is 0.03% at 1W**
- **35μV Noise Floor**
- **Efficiency up to 94% at 2x10W for 8Ω**
- **R_{DS(ON)} Low to 90mΩ**
- **PWM Switching Frequency up to 1.536MHz**
- **Sampling Frequency from 8kHz to 192kHz**
- **Support TDM Format for Multi-Channel**
- **Built-In Anti-Pop Function**
- **Programmable Coefficients for DRC Filters**
- **Built-In DC Blocking Filters**
- **Built-in Thermal Fold Back control**
- **Protection Features: UVLO, OVP, OCP, OTP and DCP**
- **Inductor-Less Application**
- **VQFN-32L Thermally-Enhanced Package**
- **RoHS Compliant and Halogen Free**

4 Applications

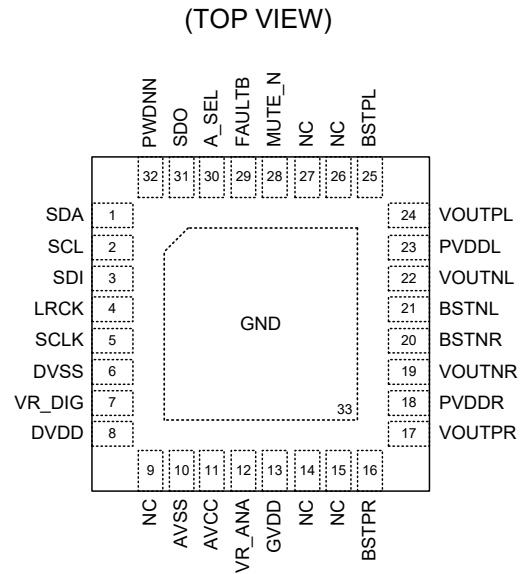
- LCD-TV
- Monitors
- Home Audio
- Amusement Equipment
- Electronic Music Equipment

5 Marking Information



RT9120SGQV: Product Code
YMDNN: Date Code

6 Pin Configuration



VQFN-32L 5x5

7 Simplified Application Circuit

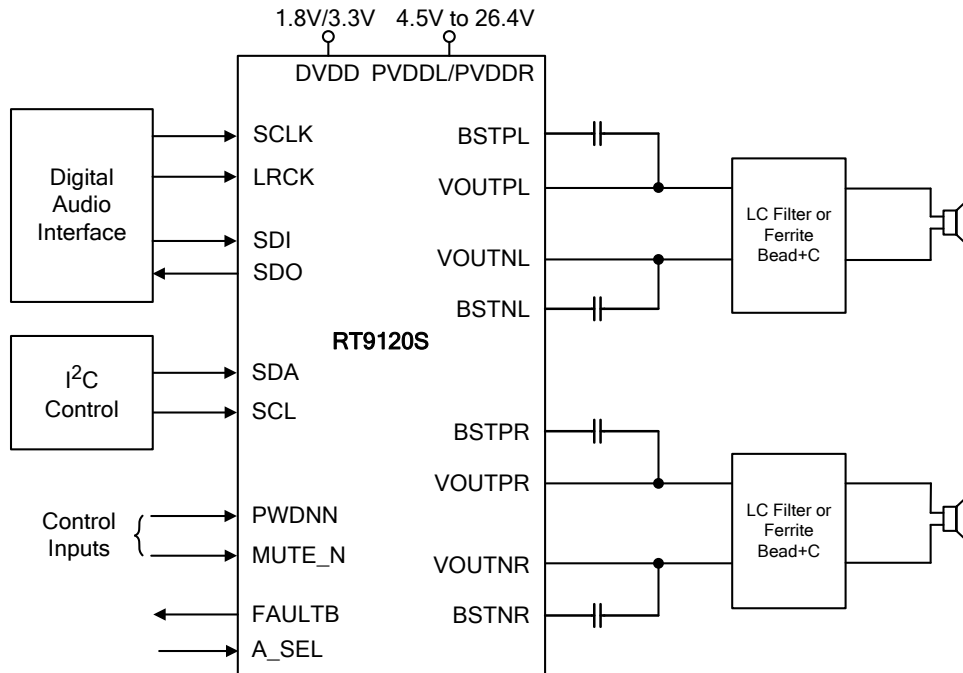


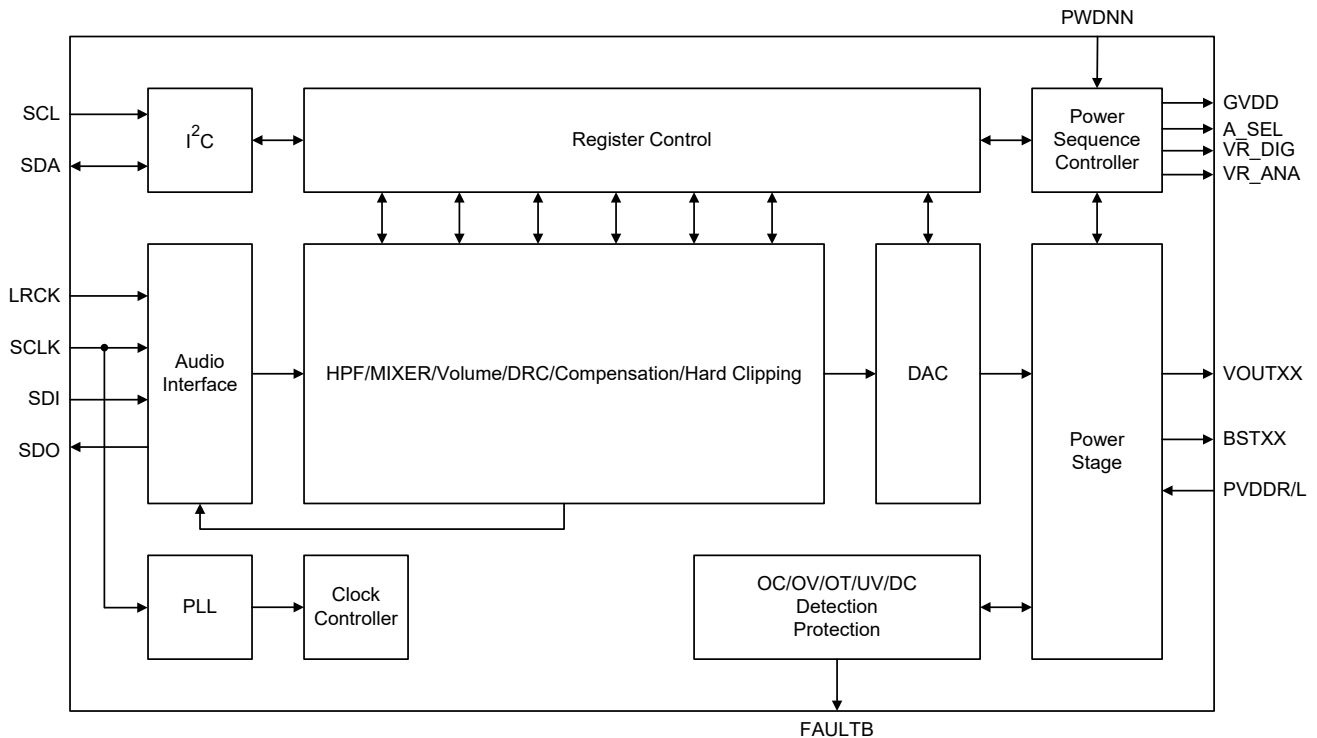
Table of Contents

1	General Description	1	18.5	DRC Control.....	26
2	Ordering Information	1	18.6	DRC Timing.....	27
3	Features	1	18.7	DRC Timing Equation.....	27
4	Applications.....	1	18.8	Peak Mode.....	29
5	Marking Information.....	2	18.9	Input Mixer	30
6	Pin Configuration	2	18.10	Input Mixer Gain Setting.....	31
7	Simplified Application Circuit	2	18.11	Mixer Inverse Phase Setting	31
8	Functional Pin Description.....	4	18.12	SDO Output Configure	32
9	Functional Block Diagram	5	19	Application Information	33
10	Operation	5	19.1	I ² C Bus Specification	33
10.1	Error Reporting	5	19.2	Communication Protocol	33
10.2	Clock Detection.....	5	19.3	Boost Capacitor Selection.....	33
10.3	Volume Control	5	19.4	Device Addressing	33
10.4	Built-In Anti-POP Function	5	19.5	I ² C Write Control	34
10.5	Overcurrent Protection.....	5	19.6	I ² C Read Control.....	34
10.6	Undervoltage Protection	6	19.7	Read Function.....	34
10.7	Overvoltage Protection	6	19.8	Write Function	34
10.8	Over-Temperature Protection.....	6	19.9	Audio Interface.....	35
10.9	Dynamic Range Enhancement	6	19.10	Amplification Gain	36
11	Absolute Maximum Ratings	7	19.11	Master Volume Gain.....	37
12	Recommended Operating Conditions	8	19.12	Volume Ramp.....	38
13	Electrical Characteristics	8	19.13	Hard Clip Function	39
14	Typical Application Circuit	12	19.14	DC Protection Function	40
14.1	3.3V I/O Application	12	19.15	Compensate Filter.....	41
14.2	1.8V I/O Application	13	19.16	TDM	42
15	Power-On Sequence	14	19.17	Example	44
16	Power-Off Sequence	15	19.18	PBTL Function.....	45
16.1	Initial Sequence (BTL Mode, PWM = 384kHz).....	16	19.19	Mono PBTL Application Circuit.....	45
16.2	Initial Sequence (BTL Mode, PWM = 768kHz, 1.5MHz).....	16	19.20	Mono Configuration	46
16.3	Initial Sequence (PBTL Mode, PWM = 384kHz).....	17	19.21	Protection Behavior.....	49
16.4	Initial Sequence (PBTL Mode, PWM = 768kHz, 1.5MHz)	17	19.22	Protection Flag	49
17	Typical Operating Characteristics	19	19.23	Protection Type	49
17.1	PWM = 384kHz.....	19	19.24	Fault Behavior Type Selection.....	50
17.2	PWM = 768kHz.....	22	19.25	Fault Mask.....	50
18	Signal Path.....	25	19.26	Thermal Considerations	51
18.1	Input High Pass Filter.....	25	20	Layout Guide.....	52
18.2	DRC	26	21	Register Map.....	55
18.3	DRC Enable.....	26	22	Outline Dimension.....	69
18.4	DRC Noise Gate Enable.....	26	23	Footprint Information	70
			24	Packing Information	71
			24.1	Tape and Reel Data	71
			24.2	Tape and Reel Packing	72
			24.3	Packing Material Anti-ESD Property.....	73

8 Functional Pin Description

Pin No.	Pin Name	IO	Pin Function
1	SDA	DIO	I ² C data input/output.
2	SCL	DI	I ² C clock input.
3	SDI	DI	I ² S data input.
4	LRCK	DI	I ² S L/R clock input.
5	SCLK	DI	I ² S bit clock input.
6	DVSS	P	Ground for digital circuits.
7	VR_DIG	P	The internal LDO output for the digital block when DVDD = 3.3V. When DVDD = 1.8V, please supply 1.8V into VR_DIG from an external power source.
8	DVDD	P	3.3V, 1.8V power supply for I/O.
9, 14, 15, 26, 27	NC	P	No internal connection. (For the layout, please tight to GND)
10	AVSS	P	Ground for analog circuits.
11	AVCC	P	26.4V power supply for analog circuits.
12	VR_ANA	P	Analog reference voltage.
13	GVDD	P	Internal power supply generated by LDO.
16	BSTPR	P	Bootstrap supply for VOUTPR.
17	VOUTPR	AO	Positive output of RCH.
18	PVDDR	P	26.4V power supply for RCH.
19	VOUTNR	AO	Negative output of RCH.
20	BSTNR	P	Bootstrap supply of VOUTNR.
21	BSTNL	P	Bootstrap supply for VOUTNL.
22	VOUTNL	AO	Negative output of LCH.
23	PVDDL	P	26.4V power supply for LCH.
24	VOUTPL	AO	Positive output of LCH.
25	BSTPL	P	Bootstrap supply for VOUTPL.
28	MUTE_N	DI	Mute pin.
29	FAULTB	DO	Fault indicator (low active).
30	A_SEL	DI	Slave address selection.
31	SDO	DO	I ² S data output.
32	PWDNN	DI	Power down pin, low active.
33 (Exposed Pad)	PVSS	P	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

9 Functional Block Diagram



10 Operation

10.1 Error Reporting

The FAULTB pin is for report error status. The FAULTB goes to low when protection happens. This pin is open-drain configuration, need pull-up resistor.

10.2 Clock Detection

The RT9120S can accept SCLK to be 32fs, 48fs, and 64fs, and support only a 1xf LRCK. The internal oscillator will check SCLK input constantly. If clock is lost, the RT9120S will shut down the power stage automatically.

10.3 Volume Control

The RT9120S has master volume MS_VOL and each channel volume CH1_VOL, CH2_VOL control. The step of each volume is 0.0625dB per step, from 24dB to mute. CH1 and CH2 also have each mute control, CH1_MUTE and CH2_MUTE.

10.4 Built-In Anti-POP Function

An internal soft-start function controls the duty ramp-up rate of the output PWM voltage to minimize the POP noise during start-up. Similarly, when power shuts down, the duty also ramps down to eliminate the POP noise. This function also acts when the PWDNN pin turns on/off.

10.5 Overcurrent Protection

The RT9120S provides OCP function to prevent the device from damage during overload or short-circuit conditions. The current function is detected by an internal sensing circuit. Once the inductor short to the each other and to GND the OCP function is designed to operate the latch mode.

10.6 Undervoltage Protection

The RT9120S monitors the voltage on PVDD voltage threshold. When the voltage on PVDDL/R pin falls below the undervoltage threshold, 4V (which can be programmable.), the UVP circuit turns off the output immediately, or the latch mode can configure to use.

10.7 Overvoltage Protection

The RT9120S monitors the voltage on PVDD voltage threshold. When the voltage on PVDDL/R pin rises behind the overvoltage threshold, 30V, the OVP circuit turns off the output immediately and operates in auto-recovery mode, or the latch mode can configure to use.

10.8 Over-Temperature Protection

The over-temperature protection function will turn off the power MOSFET when the junction temperature exceeds 150°C (minimum). Once the junction temperature cools down by approximately 30°C, the regulator will automatically resume operation, or the latch mode can configure to use.

10.9 Dynamic Range Enhancement

The dynamic range enhancement which enhances the dynamic range for the application. It will optimize the noise when the operating.

11 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, AVCC, PVDDL, PVDDR ----- -0.3V to 32V
- Supply Voltage, DVDD ----- -0.3V to 9V
- Speaker Amplifier Output Voltage, VOUTXX ----- -0.3V to 32V
- BSTXX (Note 3) ----- -0.3V to 36V
- SCL, SDA, FAULTB ----- -0.3V to 6V
- LRCK, SCLK, SDI, MUTE_N, PWDNN, A_SEL ----- -0.3V to DVDD + 0.5V
- GND to PVSS, DVSS and AVSS ----- -0.3V to 0.3V
- VOUTPR, VOUTNR, VOUTPL, VOUTNL (Note 4) ----- -10V to 37V
- SDO ----- -0.3V to 9V
- VR_DIG ----- -0.3V to 4V
- VR_ANA, GVDD ----- -0.3V to 6V
- Power Dissipation, Pd @ TA = 25°C
 - VQFN-32L 5x5 ----- 4.51W
- Package Thermal Resistance (Note 5)
 - VQFN-32L 5x5, θJA ----- 27.7°C/W
 - VQFN-32L 5x5, θJC(TOP) ----- 0.3°C/W
 - VQFN-32L 5x5, θJC(BOTTOM) ----- 0.7°C/W
- Package Thermal Resistance (4-Layer EVB)
 - VQFN-32L 5x5, θJA ----- 17.53°C/W
 - VQFN-32L 5x5, θJC(TOP) ----- 1.6°C/W
- Lead Temperature (Soldering, 10sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 6)
 - HBM (Human Body Model) ----- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. The result is defined when the cross voltage between BST and VOUT is 5V.

Note 4. The switching terminal should be used within AC peak limits. Overshoot and undershoot must be less than 100ns.

Note 5. θJA is simulated in the natural convection at TA = 25°C on a high effective four-layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θJC is simulated at the case top of the package. The result is including the bonding, GND, and real Die.

Note 6. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 7)

- Supply Input Voltage, DVDD ----- 3.0V to 3.6V
- Supply Input Voltage (For 1.8V I/O), DVDD, VR_DIG ----- 1.62V to 1.98V
- Supply Input Voltage, PVDDL, PVDDR, AVCC ----- 4.5V to 26.4V
- Ambient Temperature Range ----- -40°C to 85°C
- Junction Temperature Range ----- -40°C to 150°C

Note 7. The device is not guaranteed to function outside its operating conditions.

13 Electrical Characteristics

(PVDDL = PVDDR = AVCC = 12V, DVDD = 3.3V, R_L = 8Ω, T_A = 25°C, f_{sw} = 384kHz, L = 10μH, C = 0.47μF, unless otherwise specified.) (Note 8)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
PWDNN	VIH: High-Level-Input Voltage	VIH		DVDD x 0.7	--	--	V
	VIL: Low-Level-Input Voltage	VIL		--	--	DVDD x 0.3	
FAULTB	VOL: Low-Level-Output Voltage	VOL	IPULLUP = 3mA	--	--	0.4	V
DVDD Quiescent Current (Normal Mode)		IQ_D	PWDNN = 3.3V, for DVDD, no load, no LC filter	--	7.5	15	mA
DVDD Shut Down Current		ISD_D	PWDNN = 0.8V, for DVDD, no load, no LC filter	--	--	15	μA
PVDDL/R + AVCC Quiescent Current (Normal Mode)		IQ_P	PWDNN = 3.3V, switch 50% duty, no load, no LC filter	--	20	25	mA
PVDDL/R + AVCC Shut Down Current		ISD_P	PWDNN = 0.8V, no load, no LC filter	--	--	20	μA
Drain-Source On-State Resistance	RDS(ON)	PVDD = 12V, IO _{UT} = 500mA, T _J = 25°C	High-Side	--	90	--	mΩ
			Low-Side	--	85	--	
Speaker Gain Variation		ΔAV(SPK_AMP)	Gain different between L and R channel	-0.5	--	0.5	dB
Turn-On Time from Shutdown		t _{ON}	The timing between the AMP on command to PWM output. Note: t _{ON} time also includes the volume ramp-up time (0x0A bit 1:0 set 01)	--	80	--	ms
Shut-Down Time from PWDNN set to low		t _{OFF}	The timing between the PWDNN pin set to low to the PWM stop time. Note: t _{OFF} time also includes the volume ramp-down time (0x0A bit 1:0 set 01)	--	60	--	ms
PWM Switching Frequency	f _{sw}	384kHz mode	364.8	384	403.2	kHz	
		768kHz mode	729.6	768	806.4		
		1536kHz mode	1459.2	1536	1612.8		

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
RMS Output Power	Po	THD + N = 10%, (BTL), PVDD = 12V, RL = 8Ω	9	10	--	W
		THD + N = 1%, (BTL), PVDD = 24V, RL = 8Ω	28	30	--	
Total Harmonic Distortion + Noise	THD+N	Po = 1W (BTL)	--	0.03	0.1	%
Output Integrated Noise	Vn	20Hz to 20kHz, A-weighted	--	35	--	μV
Output Offset Voltage	Vos	PVDD = 12V, disable DC Calibration	-6.5	--	6.5	mV
		PVDD = 12V, enable DC calibration	-5	--	5	
		PVDD = 24V, disable DC Calibration	-13	--	13	
		PVDD = 24V, enable DC calibration	-5	--	5	
Cross-Talk	XTALK	Output power = 1W, none shielding choke	--	-75	--	dB
		Output power = 1W, with shielding choke	--	-100	--	
Signal-to-Noise Ratio	SNR	THD + N = 1%, PVDD = 24V	--	113	--	dB
Power Supply Rejection Ratio (On Going to Discuss)	PSRR	Frequency @1kHz	--	-75	--	dB
Dynamic Range	DR	Input level -60dBFS	--	113	--	dB
Efficiency	η	Output Power = 10W + 10W	--	94	--	%
Over-Temperature Protection	OTP	Guaranteed by design	150	160	175	°C
Thermal Hysteresis			--	30	--	°C
Overcurrent Protection	OCP	For the PWM is 384kHz	6	7	--	A
		For the PWM is 1.5MHz	5	--	--	
PVDDL/PVDDR Overvoltage	OVP		--	30	--	V
PVDDL/PVDDR Undervoltage (Programmable)	UVP		--	4	--	V
PVDD Range (Note 8)	VPVDD	BTL, R=4ohm	--	--	21	V
		BTL, R=5ohm	--	--	26	V
		BTL, R=6ohm	--	--	26.4	V
		BTL, R=8ohm	--	--	26.4	V
		PBTL, R=2ohm	--	--	21	V
		PBTL, R=3ohm	--	--	26.4	V
		PBTL, R≥4ohm	--	--	26.4	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
I²C Interface Electrical Characteristics							
High-Level Input Voltage (Belongs to the internal 1.8V domain)		V _{IH}		VR _{DIG} x 0.7	--	--	V
Low-Level Input Voltage (Belong to the internal 1.8V domain)		V _{IL}		--	--	VR _{DIG} x 0.3	V
Digital Output Low (SDA)		V _{OL}	I _{PULLUP} = 3mA	--	--	0.4	V
Clock Operating Frequency		f _{SCL}		--	--	400	kHz
Bus Free Time Between Stop and Start Condition		t _{BUF}		1.3	--	--	μs
Hold Time After (Repeated) Start Condition		t _{HD,STA}		0.6	--	--	μs
Repeated Start Condition Setup Time		t _{SU,STA}		0.6	--	--	μs
Stop Condition Time		t _{SU,STD}		0.6	--	--	μs
Input Data Hold Time		t _{HD,DAT(IN)}		0	--	900	ns
Data Setup Time		t _{SU,DAT}		100	--	--	ns
Clock Low Period		t _{LOW}		1.3	--	--	μs
Clock High Period		t _{HIGH}		0.6	--	--	μs
Clock Data Fall Time		t _F		20	--	300	ns
Clock Data Rise Time		t _R		20	--	300	ns
Spike Suppression Time		t _{SP}		--	--	20	ns
I²S Interface Electrical Characteristics							
High-Level Input Voltage		V _{IH}		2.5	--	--	V
Low-Level Input Voltage		V _{IL}		--	--	0.8	V
SDO	VOH: High-Level Output Voltage	V _{OH}		--	3.3	--	V
	VOL: Low-Level Output Voltage	V _{OL}		--	--	0.4	
High-Level Input Voltage		V _{IH}	DVDD = 1.8V	1.4	--	--	V
Low-Level Input Voltage		V _{IL}	DVDD = 1.8V	--	--	0.5	V
SDO	VOH: High-Level Output Voltage	V _{OH}	DVDD = 1.8V	--	1.8	--	V
	VOL: Low-Level Output Voltage	V _{OL}	DVDD = 1.8V	--	--	0.2	
Frequency		f _{SCLKIN}		0.256	--	24.576	MHz
Setup Time, LRCK to SCLK Rising Edge		t _{su1}		10	--	--	ns
Hold Time, LRCK from SCLK Rising Edge		t _{h1}		10	--	--	ns
Setup Time, SDIN to SCLK Rising Edge		t _{su2}		10	--	--	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Hold Time, SDIN from SCLK Rising Edge	t_{h2}		10	--	--	ns
Rise/Fall Time for SCLK/LRCK	t_r/t_f		--	--	20	ns
I ² S Duty Cycle for Rising	%		40	--	60	%

Note 8. Measurements were made using the RT9120S_EVM board and Audio Precision System 2722 with AUX-0025 low-pass filter.

Note 9. If the maximum output power does not exceed the OCP threshold, maximum PVDD range is 26.4V.

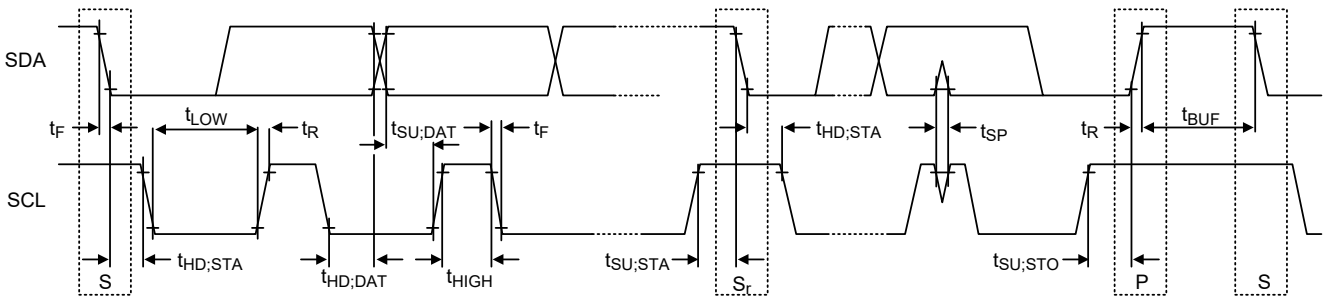


Figure 1. I²C Interface Timing Diagram

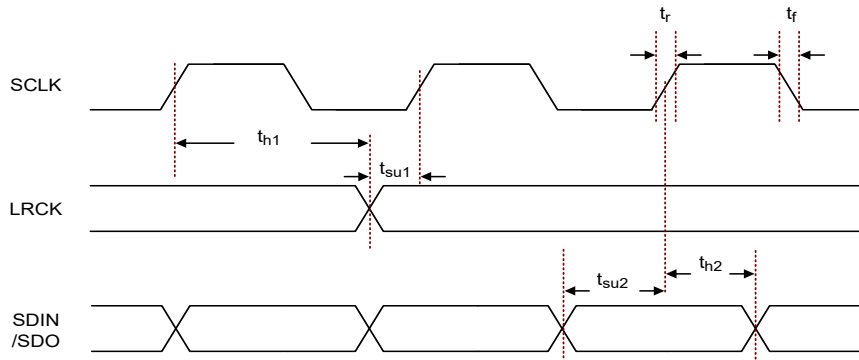
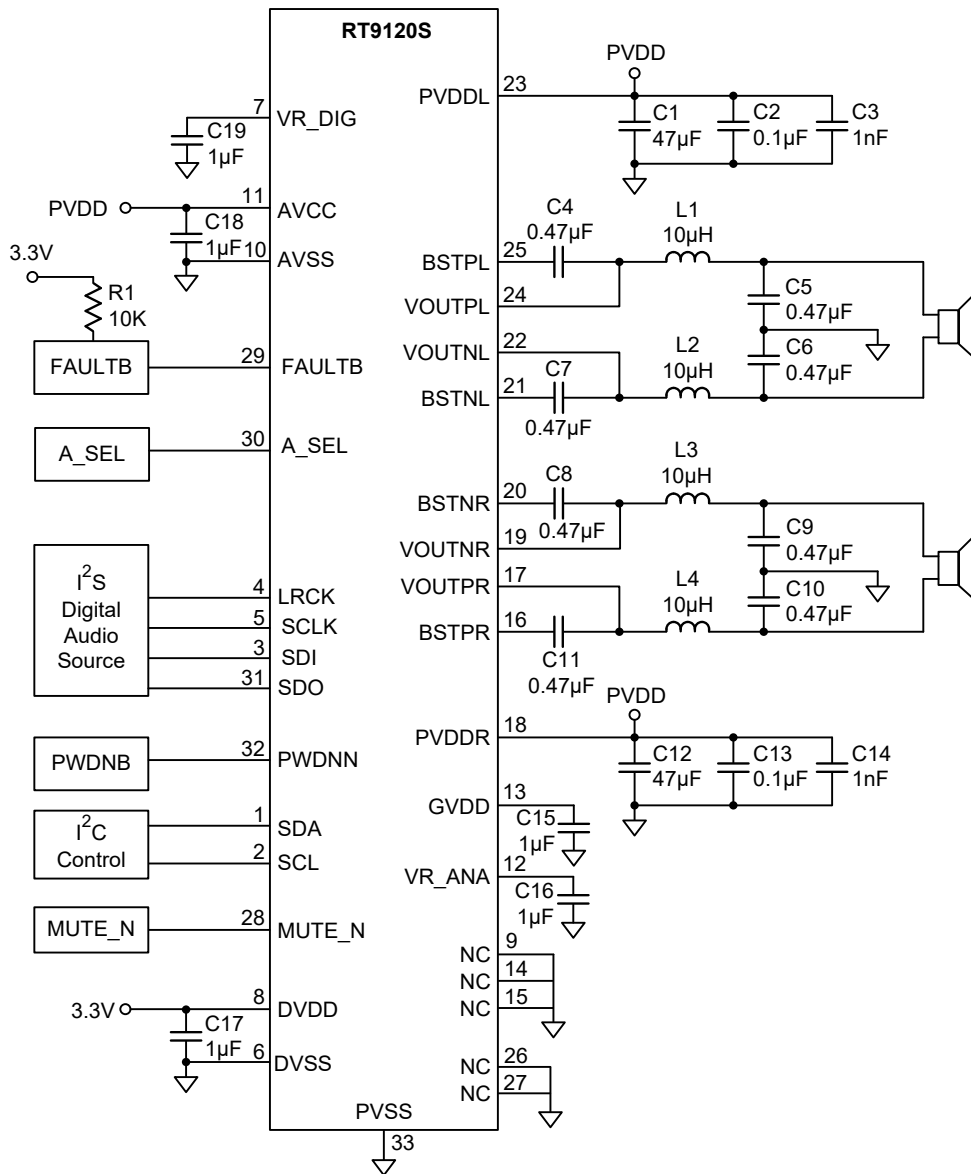


Figure 2. Timing Diagram of Slave Mode I²S Interface

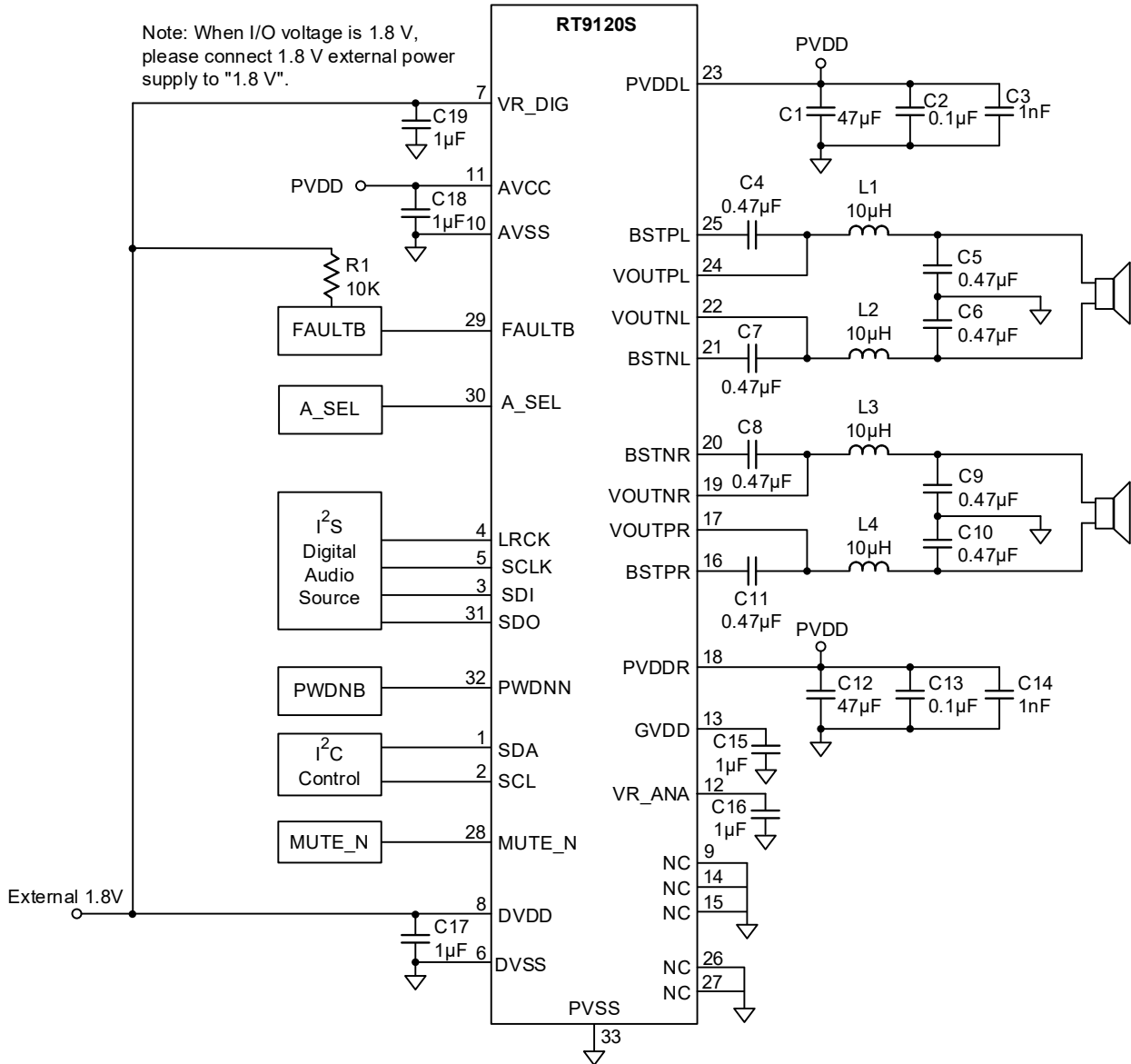
14 Typical Application Circuit

14.1 3.3V I/O Application

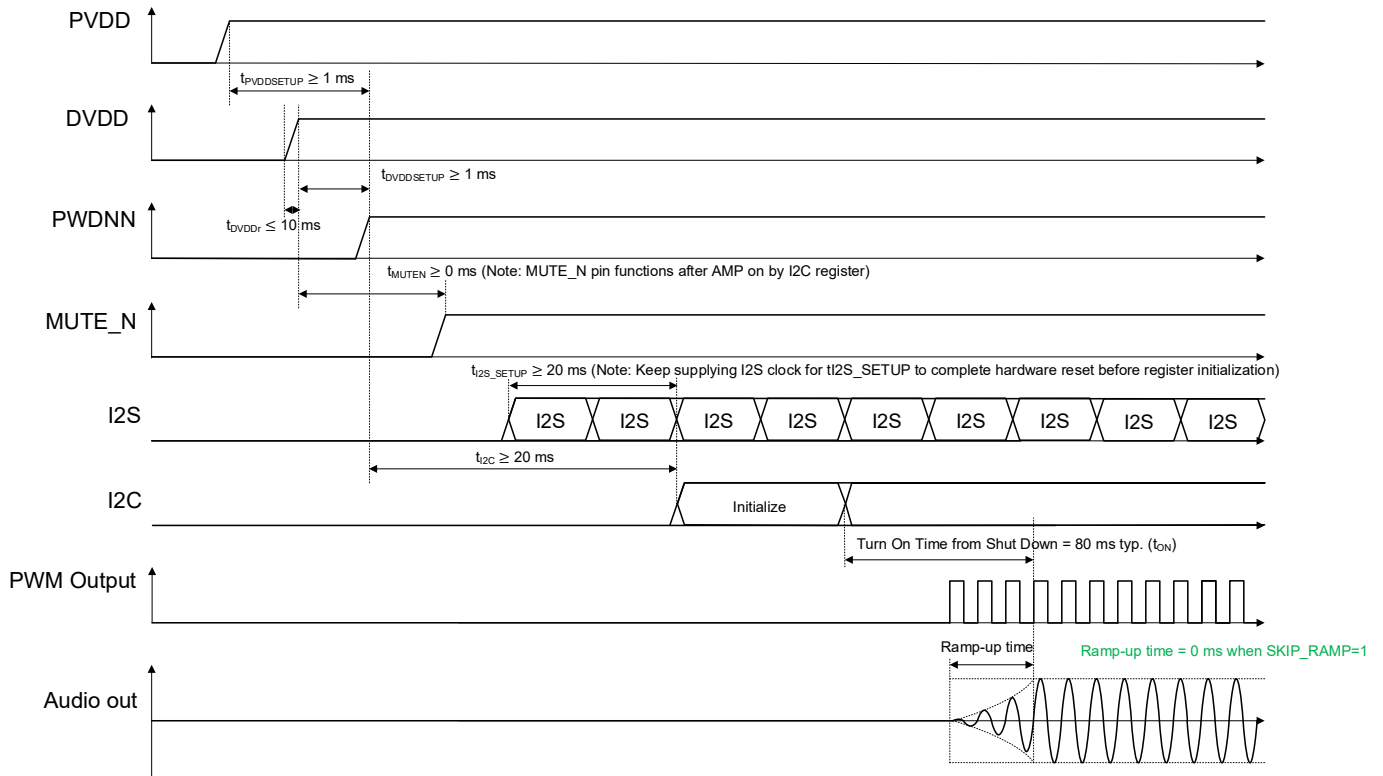


14.2 1.8V I/O Application

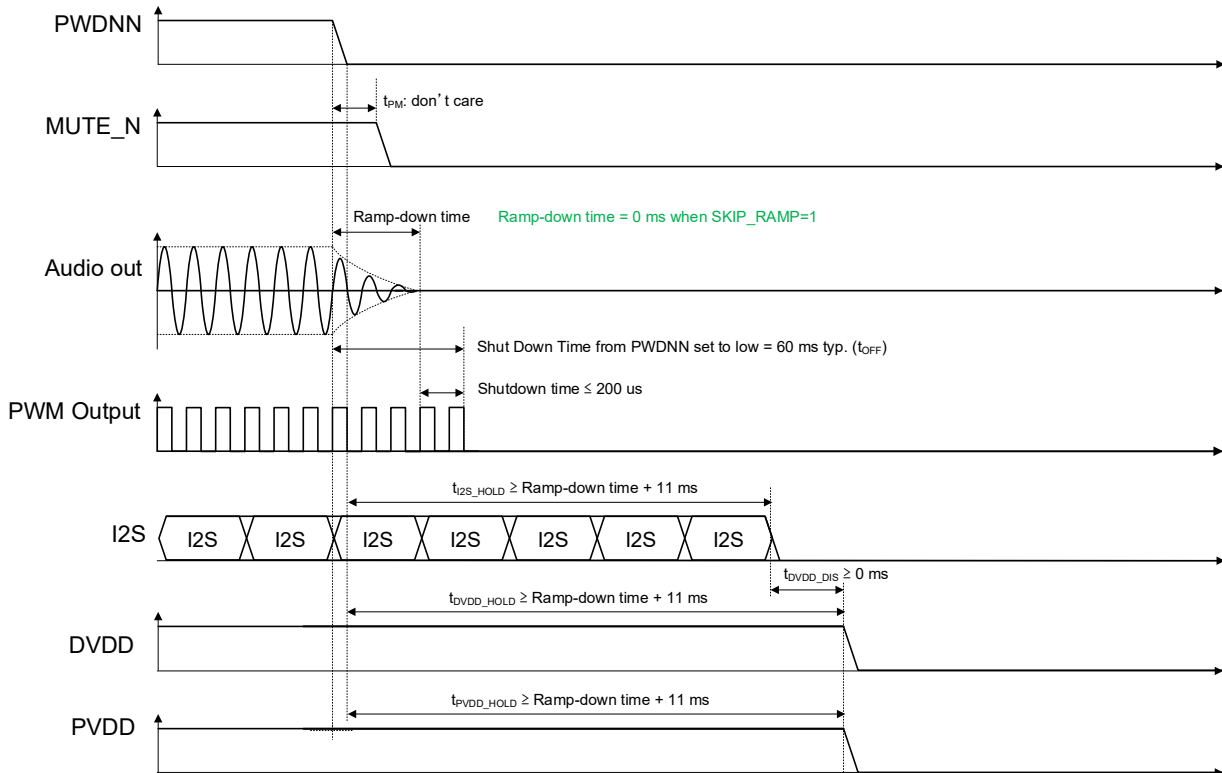
Note: When I/O voltage is 1.8 V, please connect 1.8 V external power supply to "1.8 V".



15 Power-On Sequence



16 Power-Off Sequence



16.1 Initial Sequence (BTL Mode, PWM = 384kHz)

Sequence	reg_addr	reg_size	reg_value	Description	
1	0x63	1	0xDE	Internal setting	Initial setting
2	0x07	1	0x37	Analog gain (optional)	
3	0x65	1	0x66	Internal setting	
4	0x15	1	0x20	DC offset calibration enable, set 0x20 DC offset calibration disable, skip sequence 4 to keep HW default value 0x00.	
5	0x6E	1	0x19	DC offset calibration enable, set 0x19 DC offset calibration disable, skip sequence 5 to keep HW default value 0x11.	
6	0x6C	1	0xC0	DVDD=1.8V, Set 0x6C to 0xC0. DVDD=3.3V, keep default.	
7	0x20	2	0x01, 0x80	Set the volume from mute to 0dB	
8	0x05	1	0x80	Amp turn on (PWM is 384kHz)	Amp turn on

16.2 Initial Sequence (BTL Mode, PWM = 768kHz, 1.5MHz)

Sequence	reg_addr	reg_size	reg_value	Description	
1	0x63	1	0xDE	Internal setting	Initial setting
2	0x07	1	0x37	Analog gain (optional)	
3	0x65	1	0x11	Internal setting	
4	0x15	1	0x20	DC offset calibration enable, set 0x20 DC offset calibration disable, skip sequence 4 to keep HW default value 0x00.	
5	0x6E	1	0x19	DC offset calibration enable, set 0x19 DC offset calibration disable, skip sequence 5 to keep HW default value 0x11.	
6	0x6C	1	0xC0	DVDD=1.8V, Set 0x6C to 0xC0. DVDD=3.3V, keep default.	
7	0x20	2	0x01, 0x80	Set the volume from mute to 0dB	
8	0x05	1	0x88	Amp turn on (PWM is 768kHz)	Amp turn on
		1	0x8C	Amp turn on (PWM is 1.5MHz)	

16.3 Initial Sequence (PBTL Mode, PWM = 384kHz)

Sequence	reg_addr	reg_size	reg_value	Description	
1	0x15	1	0x40	Internal setting	Initial setting
2	0x64	1	0x39	Internal setting	
3	0x63	1	0xDE	Internal setting	
4	0x07	1	0x37	Analog gain (optional)	
5	0x65	1	0x77	Internal setting	
6	0x15	1	0x60	DC offset calibration enable, set 0x60 DC offset calibration disable, skip sequence 6 to keep HW default value 0x00.	
7	0x6E	1	0x19	DC offset calibration enable, set 0x19 DC offset calibration disable, skip sequence 7 to keep HW default value 0x11.	
8	0x6C	1	0xC0	DVDD=1.8V, Set 0x6C to 0xC0. DVDD=3.3V, keep default.	
9	0x20	2	0x01, 0x80	Set the volume from mute to 0dB	
10	0x30	3	0x01, 0xC0, 0x07	Set input mixing = L/2+R/2 for mono mode	
11	0x31	3	0x01, 0xC0, 0x07		
12	0x05	1	0x90	Set to PBTL and Amp turn on (PWM is 384kHz)	Amp turn on

16.4 Initial Sequence (PBTL Mode, PWM = 768kHz, 1.5MHz)

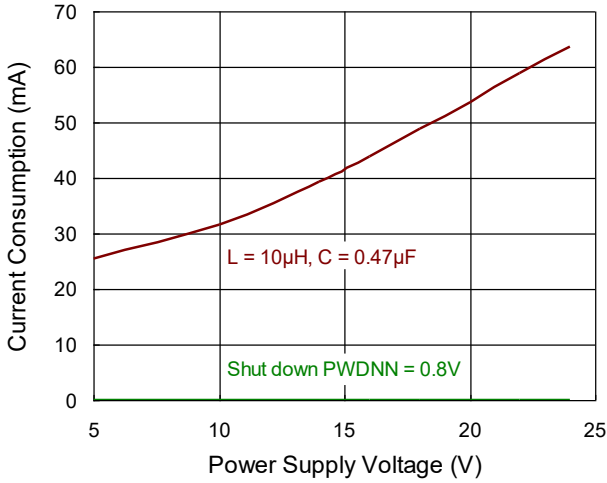
Sequence	reg_addr	reg_size	reg_value	Description	
1	0x15	1	0x40	Internal setting	Initial setting
2	0x64	1	0x39	Internal setting	
3	0x63	1	0xDE	Internal setting	
4	0x07	1	0x37	Analog gain (optional)	
5	0x65	1	0x11	Internal setting	
6	0x15	1	0x60	DC offset calibration enable, set 0x60 DC offset calibration disable, skip sequence 6 to keep HW default value 0x00.	
7	0x6E	1	0x19	DC offset calibration enable, set 0x19 DC offset calibration disable, skip sequence 7 to keep HW default value 0x11.	
8	0x6C	1	0xC0	DVDD=1.8V, Set 0x6C to 0xC0. DVDD=3.3V, keep default.	
9	0x20	2	0x01, 0x80	Set the volume from mute to 0dB	
10	0x30	3	0x01, 0xC0, 0x07	Set input mixing = L/2+R/2 for mono mode	
11	0x31	3	0x01, 0xC0, 0x07		

Sequence	reg_addr	reg_size	reg_value	Description	
12	0x05	1	0x98	Set to PBTL and Amp turn on (PWM is 768kHz)	Amp turn on
		1	0x9C	Set to PBTL and Amp turn on (PWM is 1.5MHz)	

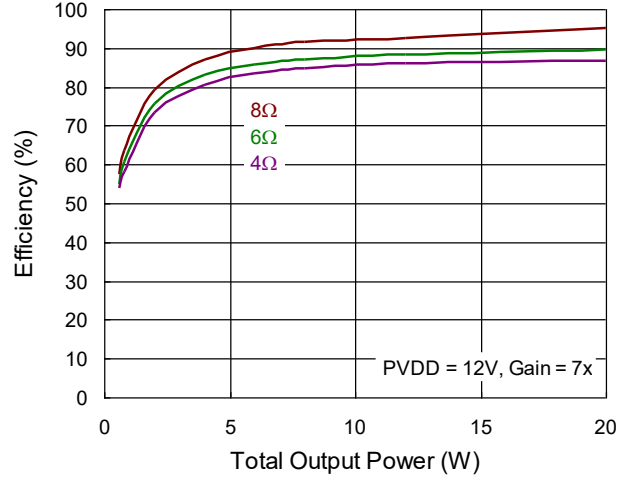
17 Typical Operating Characteristics

17.1 PWM = 384kHz

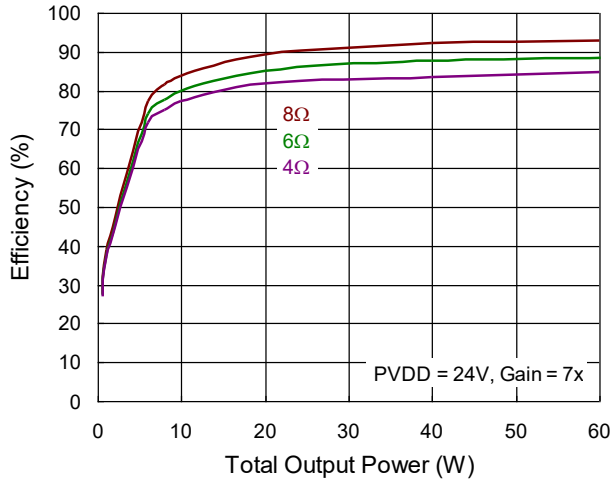
Current Consumption vs. Power Supply Voltage



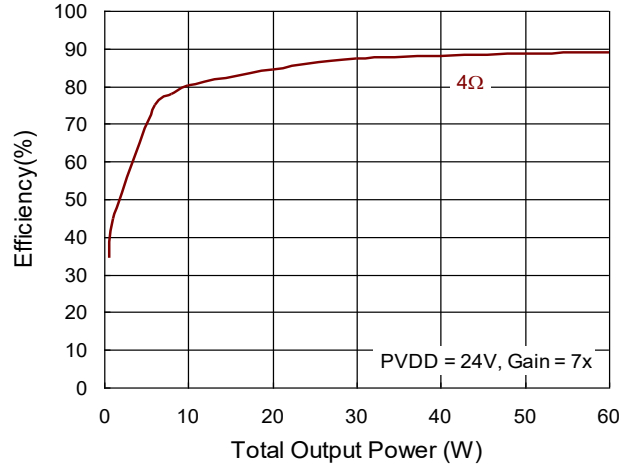
Efficiency vs. Total Output Power (BTL)



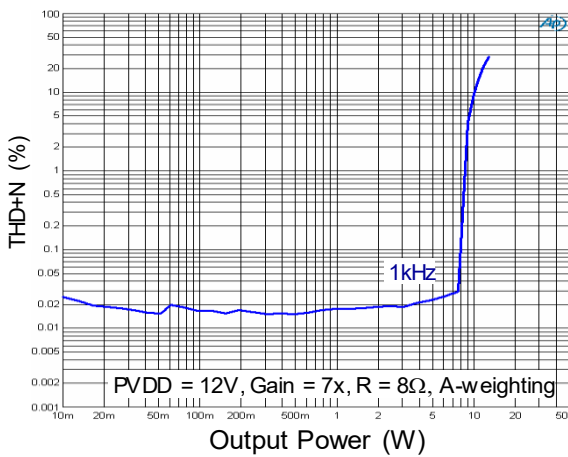
Efficiency vs. Total Output Power (BTL)



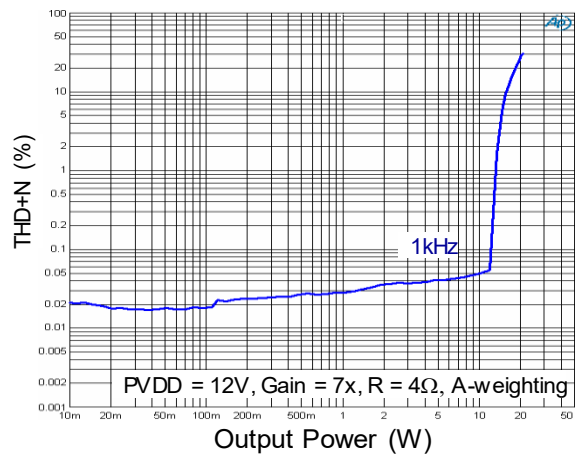
Efficiency vs. Total Output Power (PBTL)



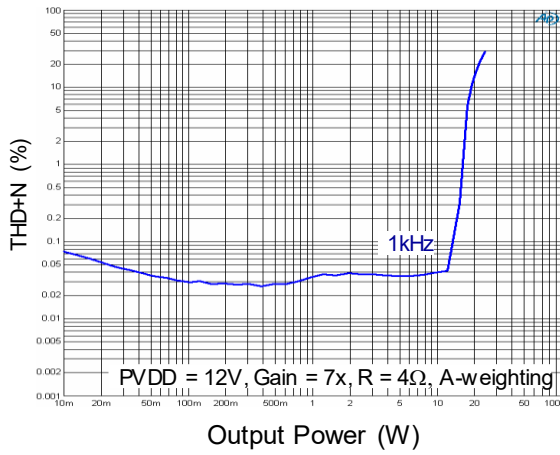
THD + N vs. Output Power (BTL)



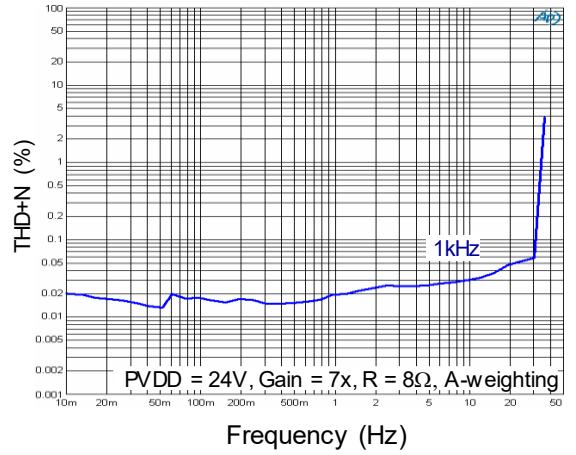
THD + N vs. Output Power (BTL)



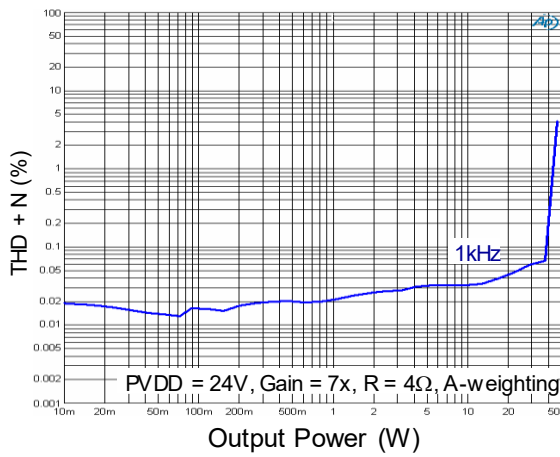
THD + N vs. Output Power (PBTL)



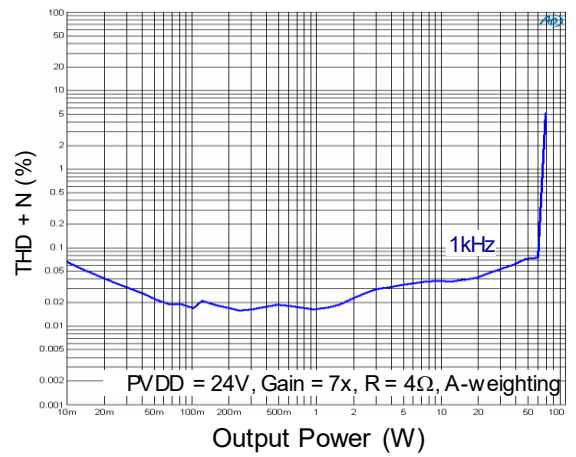
THD + N vs. Output Power (BTL)



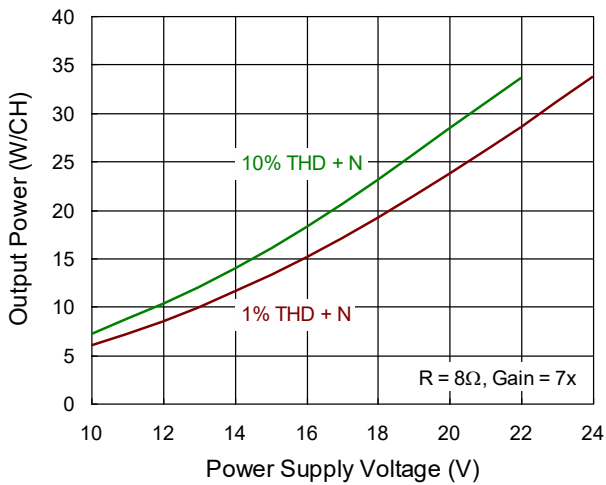
THD + N vs. Output Power (BTL)



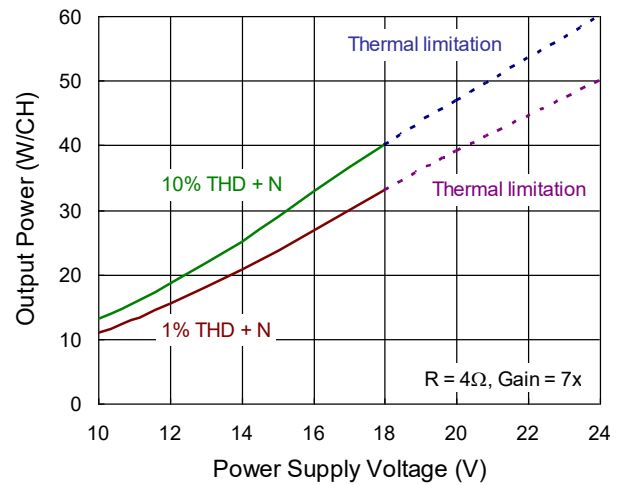
THD + N vs. Output Power (PBTL)

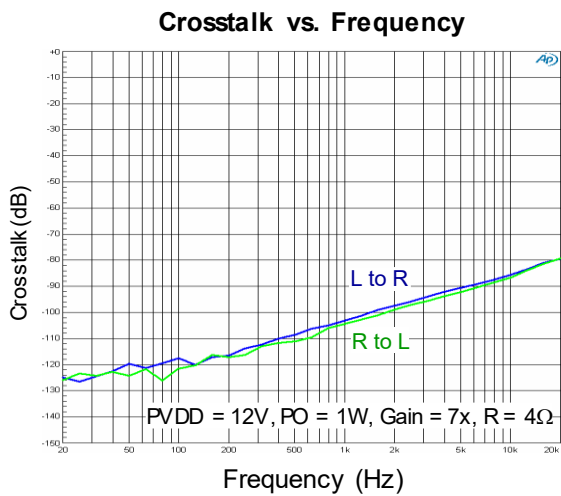
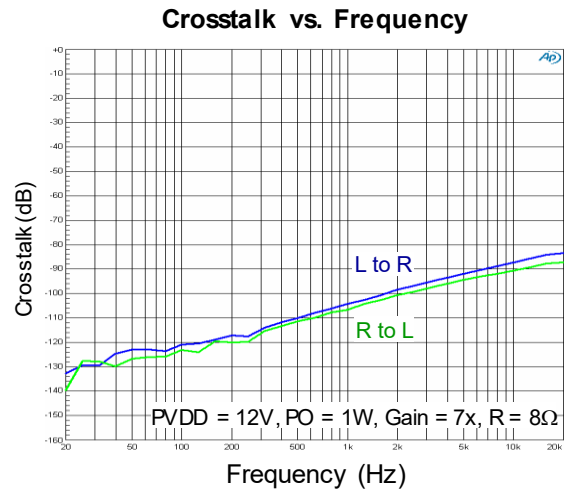
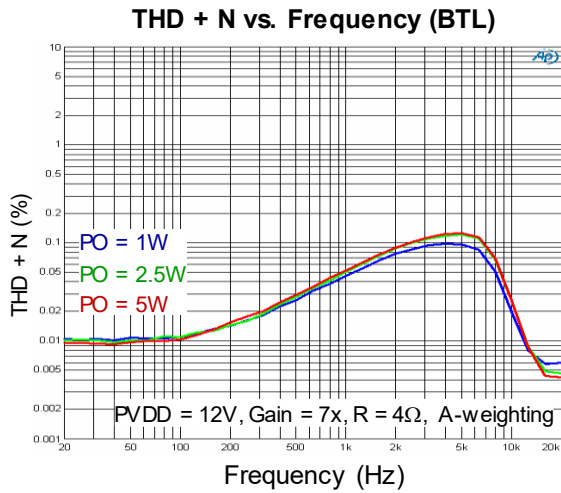
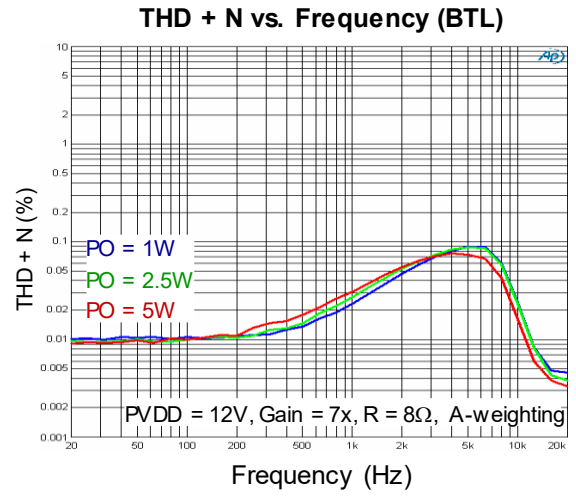
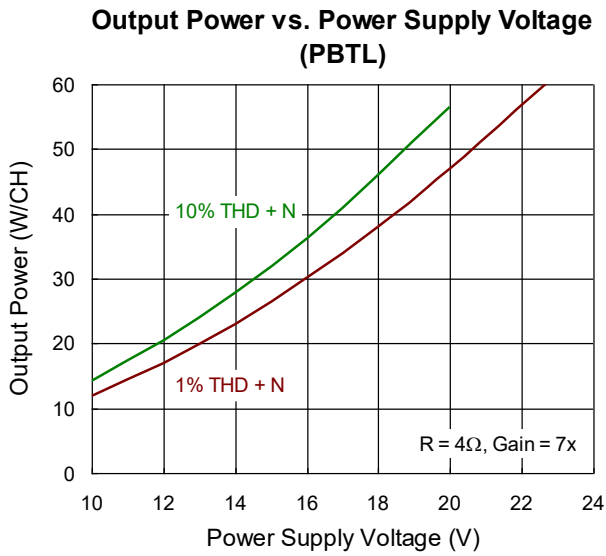


Output Power vs. Power Supply Voltage (BTL)



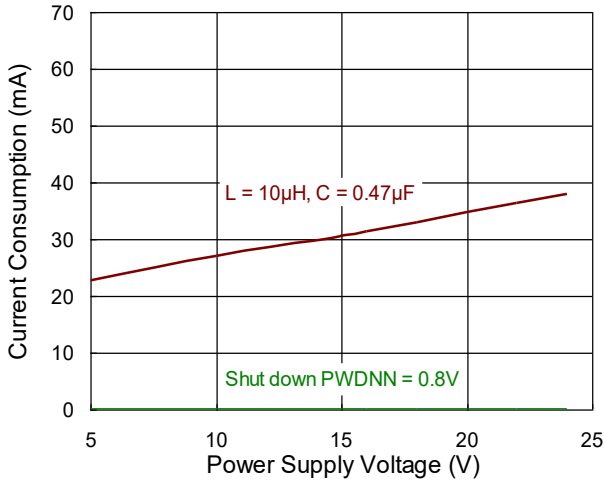
Output Power vs. Power Supply Voltage (BTL)



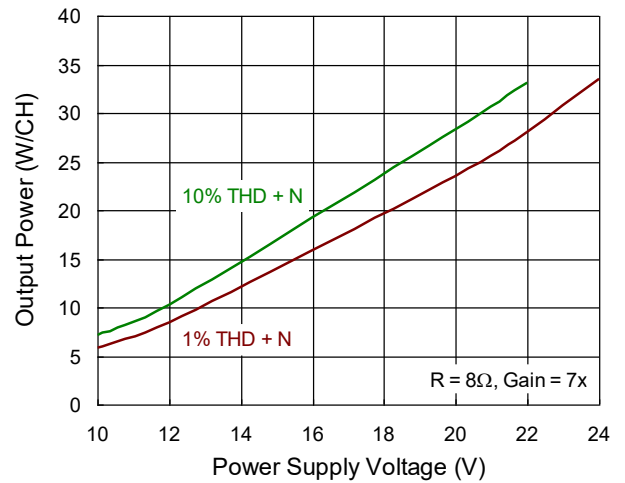


17.2 PWM = 768kHz

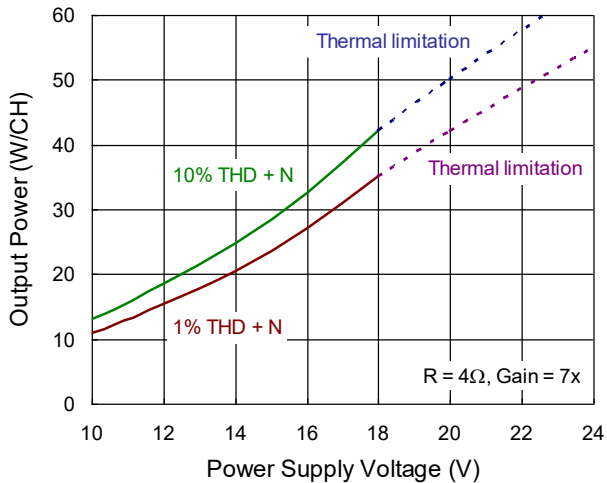
Current Consumption vs. Power Supply Voltage



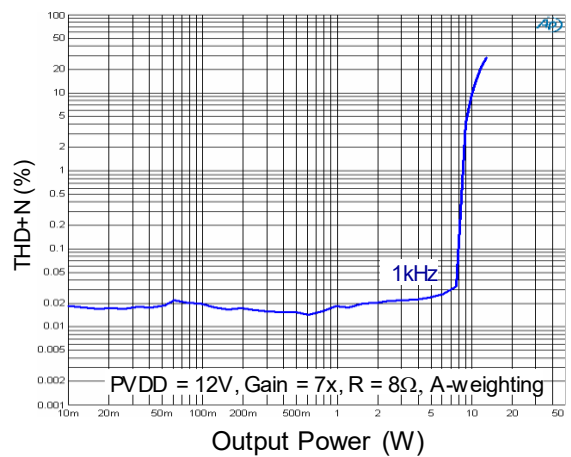
Output Power vs. Power Supply Voltage (BTL)



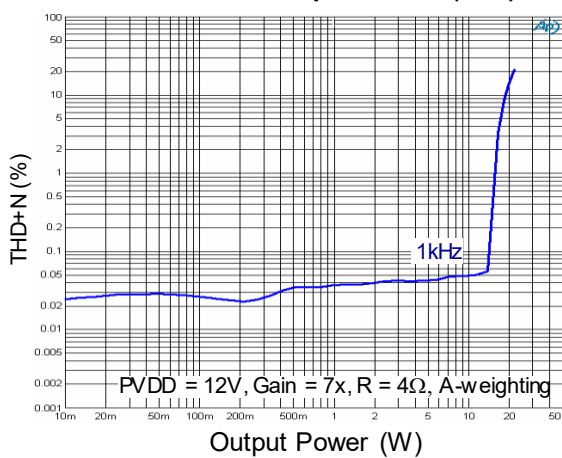
Output Power vs. Power Supply Voltage (BTL)



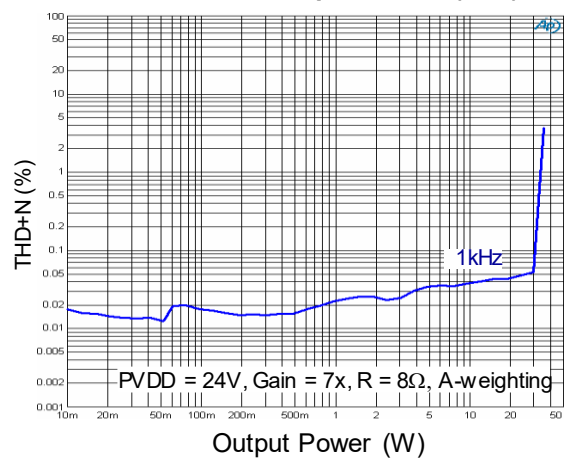
THD + N vs. Output Power (BTL)



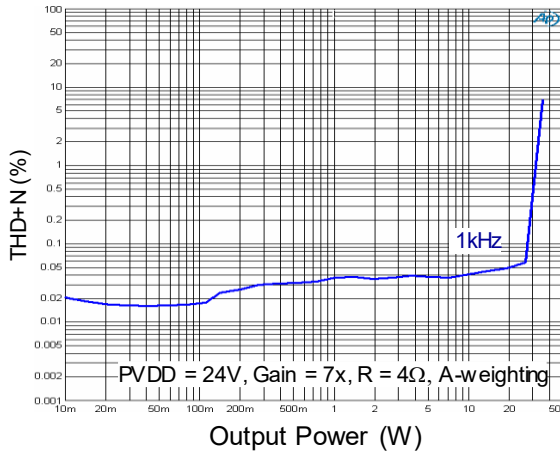
THD + N vs. Output Power (BTL)



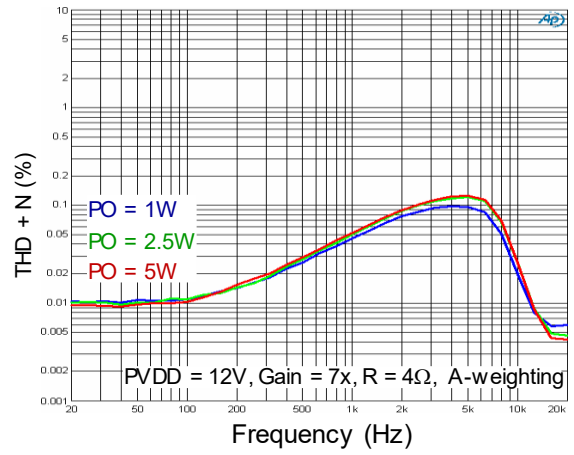
THD + N vs. Output Power (BTL)



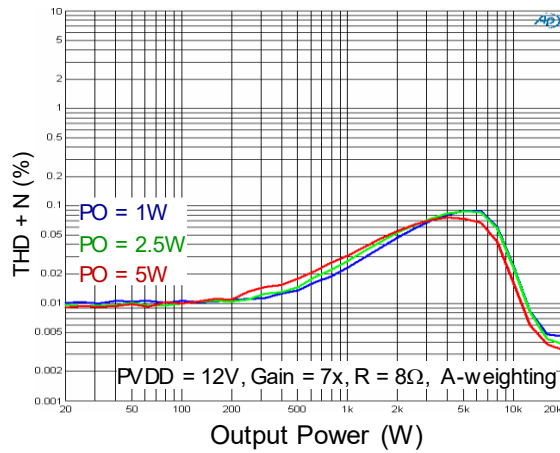
THD + N vs. Output Power (BTL)



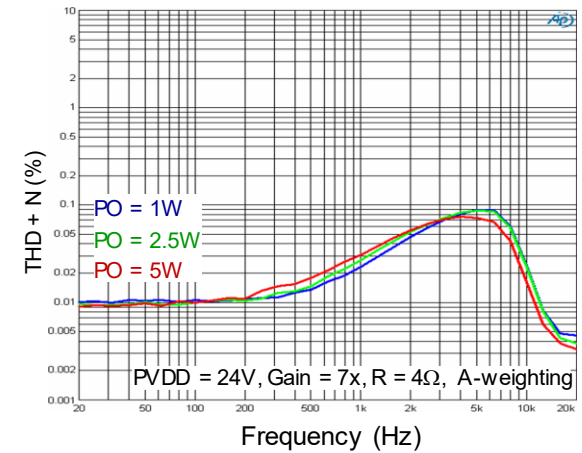
THD + N vs. Frequency (BTL)



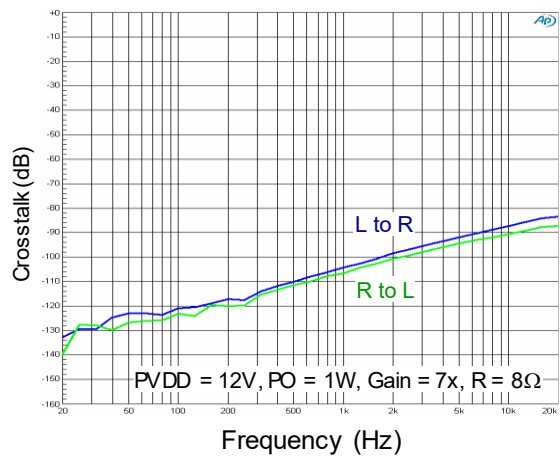
THD + N vs. Frequency (BTL)



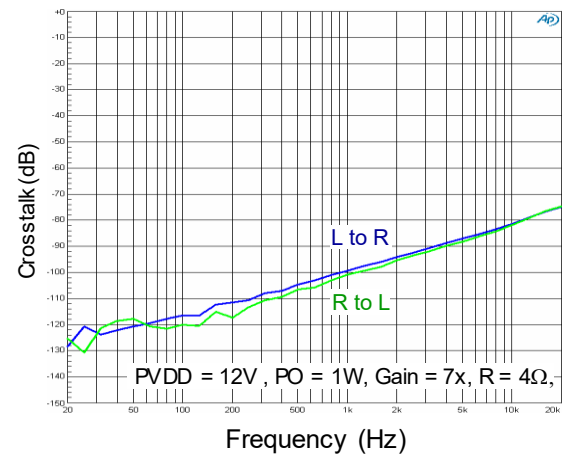
THD + N vs. Frequency (BTL)

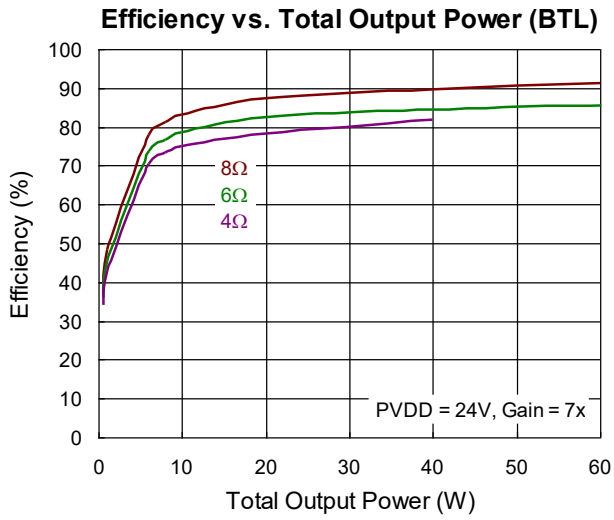


Crosstalk vs. Frequency



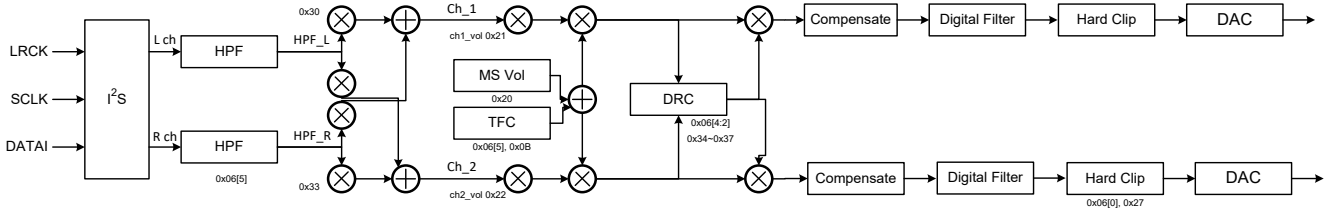
Crosstalk vs. Frequency





Note 10. Measurements were made using the RT9120S_EVM board and Audio Precision System 2722 with AUX0025 low-pass filter. All measurements taken with 1kHz.

18 Signal Path



18.1 Input High Pass Filter

Block Diagram & Description

→ There are DC-Cut filter for each output filter. The cut off frequency is 1.5Hz

Address	Bits	Name	Description
0x06	5	HPF_EN	0: Input high pass filter disable 1: Input high pass filter enable

18.2 DRC

DRC Description	Address	Description
DRC_T: Threshold	0x23	
DRC_RATIO: Compress ratio	0x24	
DRC_O: Make up gain	0x25	
DRC_N_T: Noise gate threshold	0x26	
Noise gate enable	0x06	

18.3 DRC Enable

Address	Bits	Name	Description
0x06	2	DRC_EN	0: DRC disable 1: DRC enable

18.4 DRC Noise Gate Enable

Address	Bits	Name	Description
0x06	1	DRC_N_EN	0: DRC Noise gate disable 1: DRC Noise gate enable

18.5 DRC Control

Address	Bits	Name	Description
0x23	10:0	DRC_TH[10:0]	TH[10:0], DRC Threshold
0x24	7:0	DRC_RATIO[7:0]	RATIO[7:0] DRC compression ratio
0x25	10:0	DRC_O[10:0]	O[10:0] DRC make up gain
0x26	10:0	DRC_N_T[10:0]	N_T[10:0] DRC Noise gate of the DRC

18.6 DRC Timing

Address	Bits	Name	Description
0x34	16:0	DRC_AE[16:0]	DRC_AE[16:0], DRC Energy estimator
0x35	16:0	DRC_1_AE[16:0]	DRC_1_AE[16:0], DRC Energy estimator (release) (Note 11: When set to peak mode, this value needs to be adjusted.)
0x36	16:0	DRC_AD[16:0]	DRC_AD[16:0] DRC release time
0x37	16:0	DRC_AA[16:0]	DRC_AA[16:0] DRC attack time

18.7 DRC Timing Equation

DRC Description	Equation																		
AA/AE/AD/1-AE Timing Equation	<p>Equation: $AA = (1 - e^{-2.2/(t_a * f_s)}) \times 215$ $t_a = AA/AD/AE$ timing, $f_s =$ sampling rate Ex: $t_a = 0.15ms, f_s = 48k$ $AA = (1 - e^{-2.2/(0.00015 * 48000)}) \times 215 = 8627.352$ DEC = 8627 HEX = 0x21B3</p>																		
	<table border="1"> <thead> <tr> <th>Threshold</th> <th>T_Dec</th> <th>T_Hex</th> </tr> </thead> <tbody> <tr> <td>0.15ms</td> <td>8627</td> <td>0x21B3</td> </tr> <tr> <td>⋮</td> <td>⋮</td> <td>⋮</td> </tr> <tr> <td>400ms</td> <td>3.75</td> <td>0x3</td> </tr> <tr> <td>⋮</td> <td>⋮</td> <td>⋮</td> </tr> </tbody> </table>	Threshold	T_Dec	T_Hex	0.15ms	8627	0x21B3	⋮	⋮	⋮	400ms	3.75	0x3	⋮	⋮	⋮			
	Threshold	T_Dec	T_Hex																
	0.15ms	8627	0x21B3																
⋮	⋮	⋮																	
400ms	3.75	0x3																	
⋮	⋮	⋮																	
<p>Note 12: For the different sampling rate, the maximum timing will be</p>																			
	<table border="1"> <thead> <tr> <th>fs (Sampling Rate)</th> <th>Max Time (Unit: S)</th> </tr> </thead> <tbody> <tr> <td>192kHz</td> <td>0.375</td> </tr> <tr> <td>96kHz</td> <td>0.750</td> </tr> <tr> <td>48kHz</td> <td>1.500</td> </tr> <tr> <td>32kHz</td> <td>2.250</td> </tr> <tr> <td>24kHz</td> <td>3.000</td> </tr> <tr> <td>16kHz</td> <td>4.500</td> </tr> <tr> <td>12kHz</td> <td>6.000</td> </tr> <tr> <td>8kHz</td> <td>9.000</td> </tr> </tbody> </table>	fs (Sampling Rate)	Max Time (Unit: S)	192kHz	0.375	96kHz	0.750	48kHz	1.500	32kHz	2.250	24kHz	3.000	16kHz	4.500	12kHz	6.000	8kHz	9.000
fs (Sampling Rate)	Max Time (Unit: S)																		
192kHz	0.375																		
96kHz	0.750																		
48kHz	1.500																		
32kHz	2.250																		
24kHz	3.000																		
16kHz	4.500																		
12kHz	6.000																		
8kHz	9.000																		

DRC Description	Equation																					
DRC_T: Threshold	<p>T is the threshold of the DRC Equation: $T = -(\text{Threshold})/0.0625$ (dB) Ex: $T = -10\text{dB}$, $-(-10)/0.0625 = 160$ $T_Dec = 160$ $T_Hex = \text{DEC2HEX}(160) = 0xA0$</p> <table border="1" data-bbox="536 470 1104 739"> <thead> <tr> <th>Threshold</th> <th>T_Dec</th> <th>T_Hex</th> </tr> </thead> <tbody> <tr> <td>-10dB</td> <td>160</td> <td>0xA0</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>-15dB</td> <td>240</td> <td>0xF0</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> </tbody> </table>	Threshold	T_Dec	T_Hex	-10dB	160	0xA0	-15dB	240	0xF0
Threshold	T_Dec	T_Hex																				
-10dB	160	0xA0																				
.	.	.																				
.	.	.																				
-15dB	240	0xF0																				
.	.	.																				
.	.	.																				
DRC_Ratio: Compression Ratio	<p>K is the compression ratio of the DRC Equation: $K_Hex = \text{DEC2HEX}(\text{Ratio_Value})$ EX: If compression Ratio is 50%</p> <ul style="list-style-type: none"> The Ratio_Value is $128^{0.5} = 64$ $K_Dec = 64$ $K_Hex = \text{DEC2HEX}(64) = 0x0040$ <p>Note 13: The maximum value for the full compression is 128.</p> <table border="1" data-bbox="536 1061 1442 1352"> <thead> <tr> <th>Ratio</th> <th>K_Dec</th> <th>K_Hex</th> </tr> </thead> <tbody> <tr> <td>Full Comp (100%)</td> <td>128</td> <td>0x0080</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>50%</td> <td>64</td> <td>0x0040</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> </tbody> </table>	Ratio	K_Dec	K_Hex	Full Comp (100%)	128	0x0080	50%	64	0x0040
Ratio	K_Dec	K_Hex																				
Full Comp (100%)	128	0x0080																				
.	.	.																				
.	.	.																				
50%	64	0x0040																				
.	.	.																				
.	.	.																				
DRC_O: Make Up Gain	<p>DRC_O is the offset of the DRC Equation: $\text{DRC_O} = (\text{Offset}-24)/0.0625$ EX: Offset = 0dB</p> <ul style="list-style-type: none"> $\text{Abs}[(0-24)/0.0625] = 384$ $\text{DRC_O_Dec} = 384$ $\text{DRC_O_Hex} = \text{DEC2HEX}(384) = 0x0180$ <table border="1" data-bbox="536 1626 1104 1917"> <thead> <tr> <th>Offset</th> <th>O_Dec</th> <th>O_Hex</th> </tr> </thead> <tbody> <tr> <td>0dB</td> <td>384</td> <td>0x0180</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>10dB</td> <td>224</td> <td>0x00E0</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> </tbody> </table>	Offset	O_Dec	O_Hex	0dB	384	0x0180	10dB	224	0x00E0
Offset	O_Dec	O_Hex																				
0dB	384	0x0180																				
.	.	.																				
.	.	.																				
10dB	224	0x00E0																				
.	.	.																				
.	.	.																				

18.8 Peak Mode

Block Diagram & Description

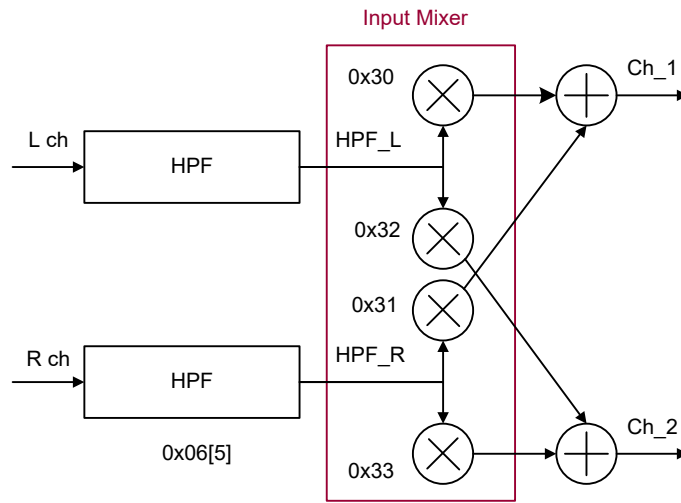
→The detecting threshold using different calculated methods.
 Peak mode: AE and 1-AE is independent.

Address	Bits	Name	Description
0x06	3	DRC_PEAK	0: RMS mode 1: Peak mode Note 14: the peak mode is recommended to use.

18.9 Input Mixer

Block Diagram & Description

→ Input mixer range is from mute to 6dB.



→Default setting is CH2_IN_MIX_1 is from HPF_R

→Default setting is CH1_IN_MIX_0 is from HPF_L

Address	Bits	Name	Description
0x30	23:0	CH1_IN_MIX_0	u[23:17], mix_0[16:0] u: Unused
0x31	23:0	CH1_IN_MIX_1	u[23:17], mix_1[16:0] u: Unused
0x32	23:0	CH2_IN_MIX_0	u[23:17], mix_0[16:0] u: Unused
0x33	23:0	CH2_IN_MIX_1	u[23:17], mix_1[16:0] u: Unused

18.10 Input Mixer Gain Setting

Address	Bits	Name	Equation																											
0x30, 0x31, 0x32, 0x33,	16:0	mix_1[16:0], mix_0[16:0]	<p>Equation: $20\text{Log}(\text{Dec}/32768)$ Range: 6dB (0xFFFF) to Mute (0x00000000) Ex: 6dB, Gain = $20\text{Log}(65535/32768) = 6\text{dB}$ Hex = 0xFFFF Dec = 65535</p> <table border="1"> <thead> <tr> <th>Gain</th> <th>Dec</th> <th>Hex</th> </tr> </thead> <tbody> <tr> <td>6dB</td> <td>65535</td> <td>0xFFFF</td> </tr> <tr> <td>2dB</td> <td>41252</td> <td>0XA124</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>0</td> <td>32768</td> <td>0X8000</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> </tbody> </table>	Gain	Dec	Hex	6dB	65535	0xFFFF	2dB	41252	0XA124	0	32768	0X8000
Gain	Dec	Hex																												
6dB	65535	0xFFFF																												
2dB	41252	0XA124																												
.	.	.																												
.	.	.																												
0	32768	0X8000																												
.	.	.																												
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.	.	.																												

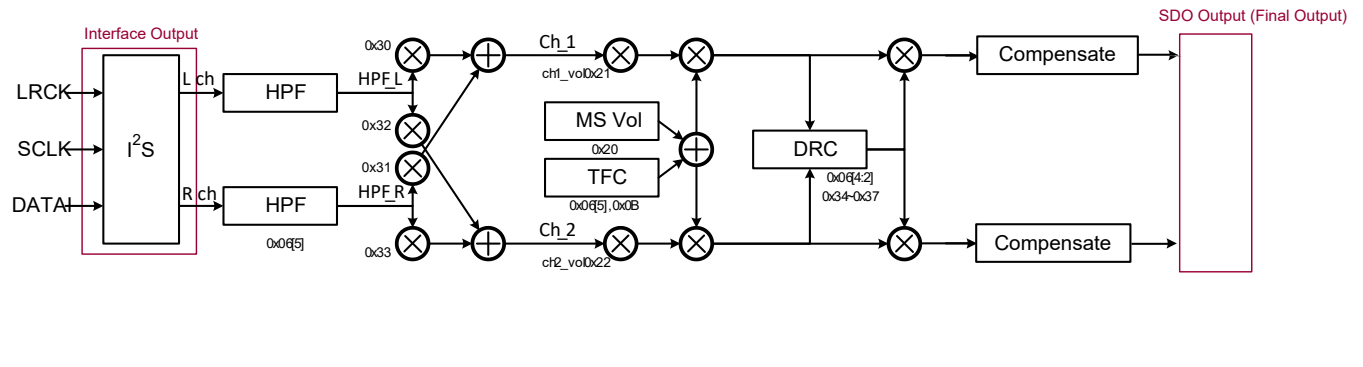
18.11 Mixer Inverse Phase Setting

Address	Bits	Name	Equation																											
0x30, 0x31, 0x32, 0x33,	16:0	mix_1[16:0], mix_0[16:0]	<p>Equation: Hex = DEC2HEX Ex: Gain = 6dB, Hex = 0x010000 Phase Inverse: Hex = DEC2HEX (-65535) = 0x010000</p> <table border="1"> <thead> <tr> <th>Gain</th> <th>Dec</th> <th>Hex</th> </tr> </thead> <tbody> <tr> <td>6dB</td> <td>-65535</td> <td>0X010000</td> </tr> <tr> <td>4dB</td> <td>-51791</td> <td>0x013523</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>0</td> <td>-32768</td> <td>0X018000</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> </tbody> </table>	Gain	Dec	Hex	6dB	-65535	0X010000	4dB	-51791	0x013523	0	-32768	0X018000
Gain	Dec	Hex																												
6dB	-65535	0X010000																												
4dB	-51791	0x013523																												
.	.	.																												
.	.	.																												
0	-32768	0X018000																												
.	.	.																												
.	.	.																												
.	.	.																												

18.12 SDO Output Configure

Block Diagram & Description

→ The final stage of whole signal path is SDO output configure. It outputs the final level of each channel before digital filter, and outputs the I²S data before the HPF.



Address	Bits	Name	Description
0x04	5:4	SDO_SEL[1:0]	00: Reserved 01: Interface output 10: Final output 11: Reserved

19 Application Information

(Note 18)

19.1 I²C Bus Specification

The RT9120S supports the I²C protocol via the input ports SCL and SDA. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The RT9120S is always a slave device in all of its communications. It can operate at up to 400kb/s. The RT9120S I²C interface is a slave only interface.

19.2 Communication Protocol

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition. START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer. STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between the RT9120S and the bus master. During the data input, the RT9120S samples the SDA signal on the rising edge of clock SCL. For correct device operation, the SDA signal must be stable during the rising edge of the clock, and the data can change only when the SCL line is low.

19.3 Boost Capacitor Selection

For the large power output, and low frequency, the boost capacitor can be chosen from 0.47μF to 1μF. Reference value can refer the table below:

Test Condition	Capacitor Value
PVDD = 24V, R = 8Ω, Output Power > 2x25W, 20Hz, BTL Mode.	1μF
PVDD = 24V, R = 4Ω, Output Power > 2x20W, 20Hz, BTL Mode.	0.47μF
PVDD = 24V, R = 4Ω, Output Power > 60W, 20Hz, PBTL Mode	1μF
PVDD = 24V, R = 8Ω, Output Power > 35W, 20Hz, PBTL Mode	1μF

19.4 Device Addressing

The RT9120S supports 4 different address setting. The default device address is 0011001 when A_SEL = DVDD, 0011000 when A_SEL = GND, 0011011 when A_SEL with 600kΩ resistor to DVDD and 0011010 when A_SEL with 600kΩ resistor to GND.

A_SEL	Device Address
DVDD	0011001
GND	0011000
With 600kΩ to DVDD	0011011
With 600kΩ to GND	0011010

19.5 I²C Write Control

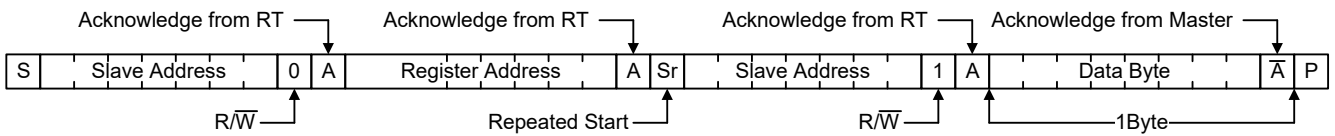
Following the START condition, the master sends a device select code with the RW bit set to 0. The RT9120S acknowledges this and the writes for the byte of internal address. After receiving the internal byte address, the RT9120S again responds with an acknowledgement.

19.6 I²C Read Control

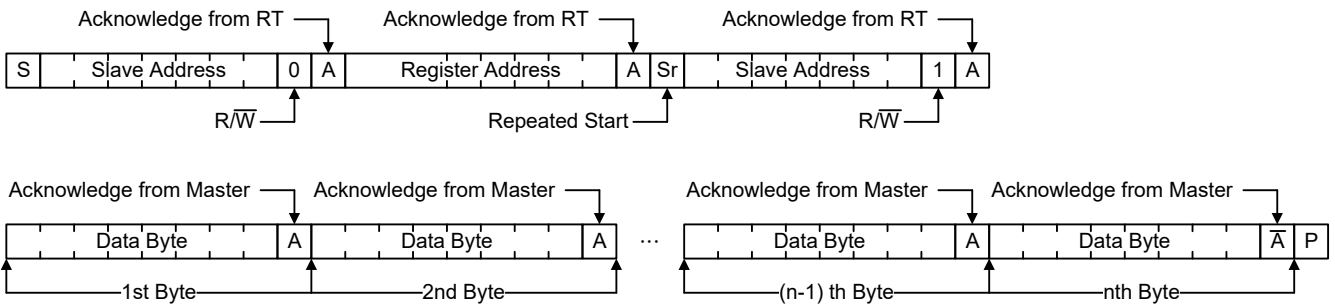
Following the START condition the master sends a device select code with the RW bit set to 1. The RT9120S acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

19.7 Read Function

- Reading One Indexed Byte of Data from RT (With 1-Byte)

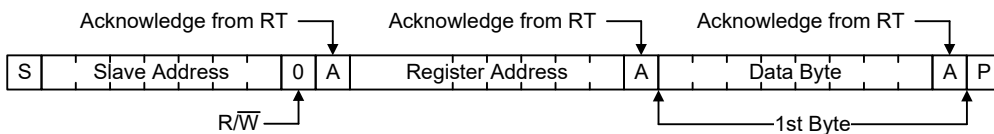


- Reading n Indexed Words of Data from RT (With N-Byte)

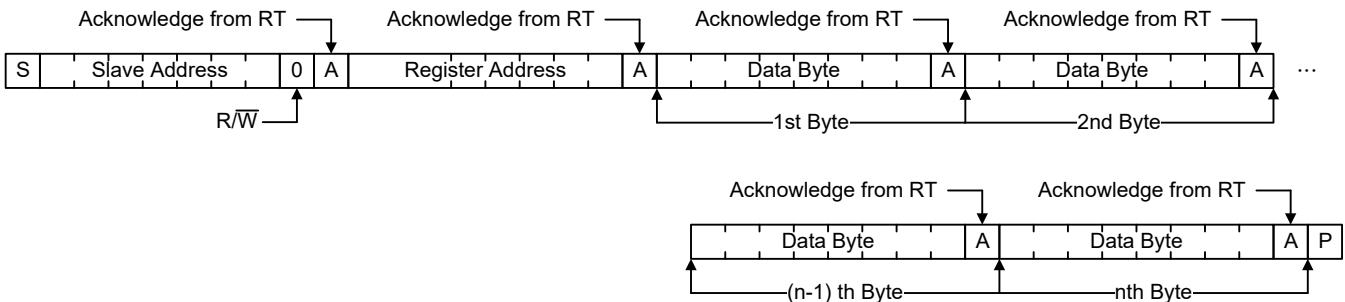


19.8 Write Function

- Writing One Byte of Data to RT (With 1-Byte)

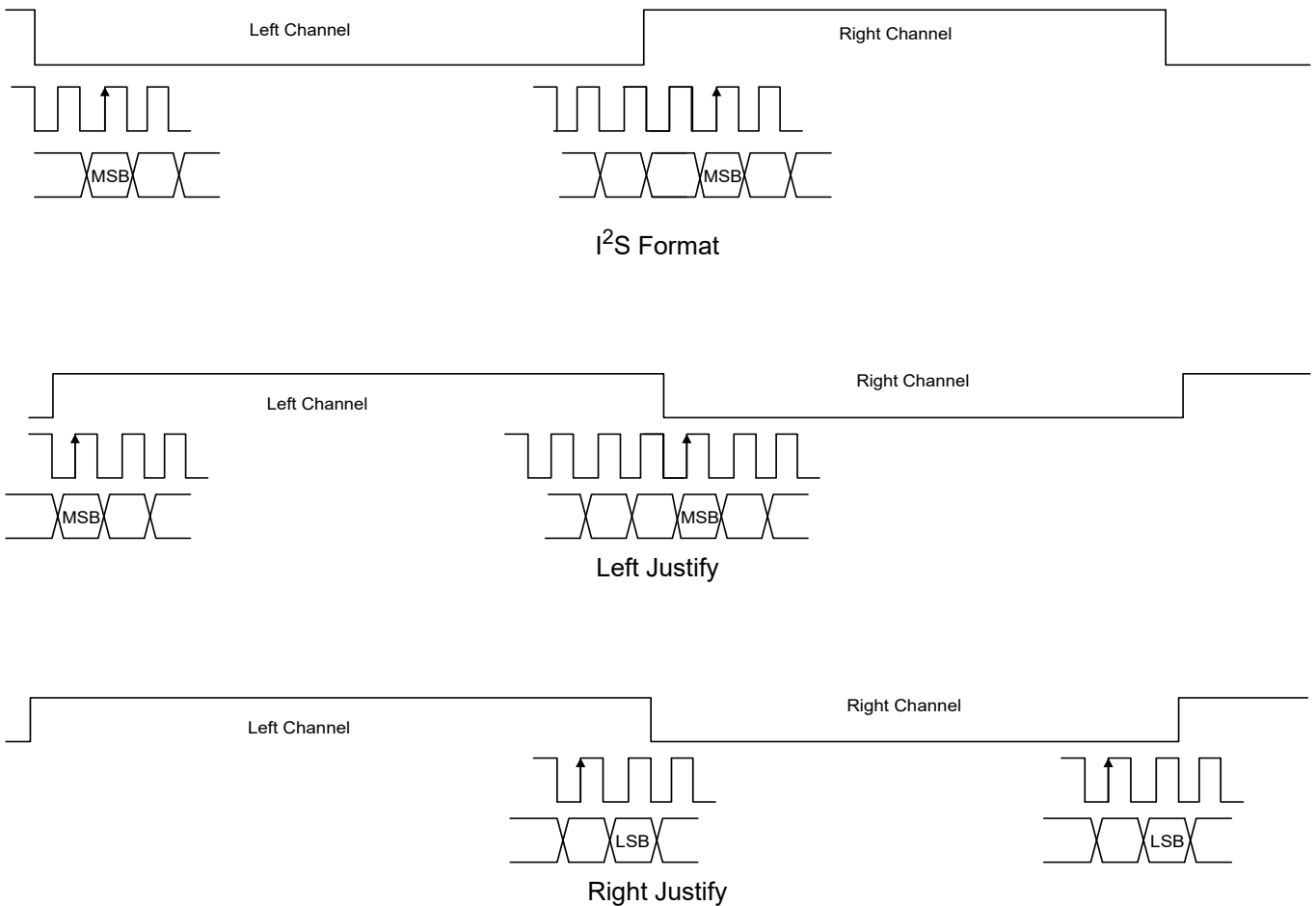


- Writing n Bytes of Data to RT (With N-Byte)



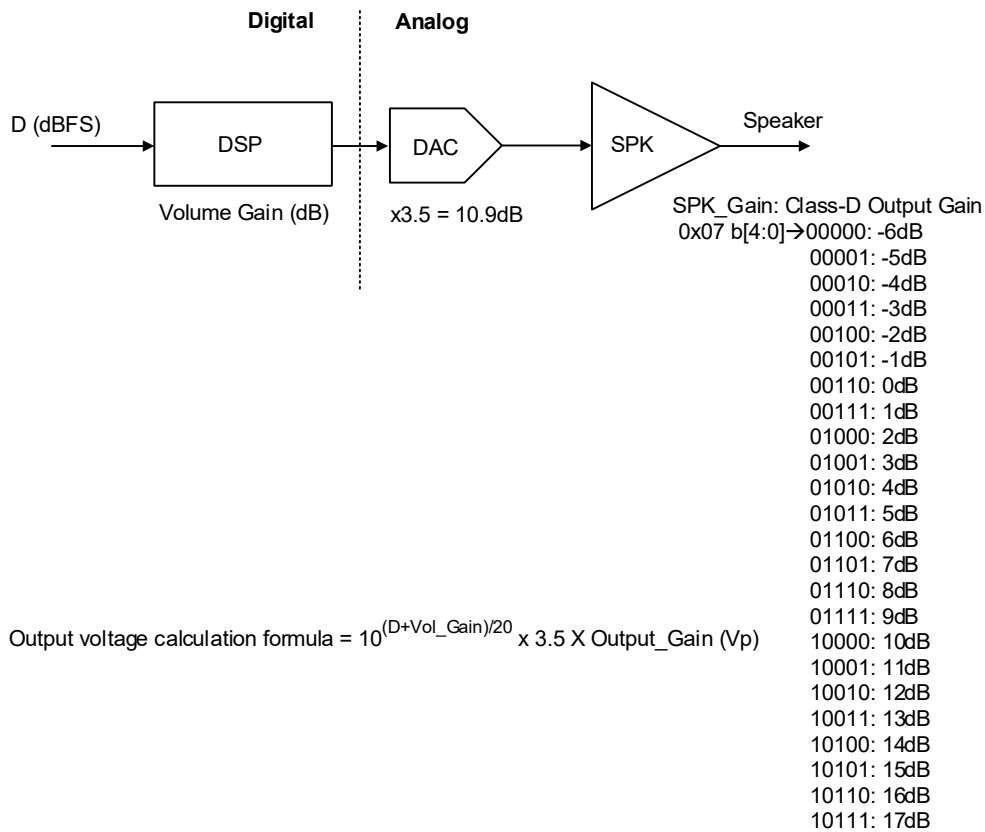
19.9 Audio Interface

The RT9120S supports four kinds of audio interface, I²S, Left-justify, Right-justify, and TDM. Each kind of interface support 32bits, 24bits, 20bits, and 16 bits format. The timing diagram is shown below.



Address	Bits	Name	Description
0x02	3:2	AUD_FMT	00: I ² S (default) 01: Left Justify 10: Right Justify 11: DSP
	1:0	AUD_BITS	00: 16bits I ² S 01: 20bits I ² S 10: 24bits I ² S 11: 32bits I ² S (default)

19.10 Amplification Gain



Output voltage calculation formula = $10^{(D+Vol_Gain)/20} \times 3.5 \times Output_Gain (Vp)$

Address	Bits	Name	Description
0x07	4:0	D_SPK_GAIN[4:0]	Class-D output gain 00000: -6dB 00001: -5dB 00010: -4dB 00011: -3dB 00100: -2dB 00101: -1dB 00110: 0dB 00111: 1dB 01000: 2dB 01001: 3dB 01010: 4dB 01011: 5dB 01100: 6dB 01101: 7dB 01110: 8dB 01111: 9dB 10000: 10dB 10001: 11dB 10010: 12dB 10011: 13dB (default) 10100: 14dB 10101: 15dB 10110: 16dB 10111: 17dB

19.11 Master Volume Gain

Address	Bits	Name	Equation																											
0x20	10:0	MS_VOL[10:0]	<p>Equation: $24\text{dB} - (\text{Dec} \times 0.0625)$ Range: 24dB (0X000) to mute (0x7ff) Ex: 10dB, Hex = 0xE0 Dec = 224 Gain = $24\text{dB} - (224 \times 0.0625) = 10\text{dB}$</p> <table border="1"> <thead> <tr> <th>Gain</th> <th>Dec</th> <th>Hex</th> </tr> </thead> <tbody> <tr> <td>24dB</td> <td>0</td> <td>0x00</td> </tr> <tr> <td>10dB</td> <td>224</td> <td>0XE0</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>0dB</td> <td>384</td> <td>0x180</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>.</td> <td>.</td> </tr> </tbody> </table>	Gain	Dec	Hex	24dB	0	0x00	10dB	224	0XE0	0dB	384	0x180
Gain	Dec	Hex																												
24dB	0	0x00																												
10dB	224	0XE0																												
.	.	.																												
.	.	.																												
0dB	384	0x180																												
.	.	.																												
.	.	.																												
.	.	.																												

19.12 Volume Ramp

00: 1 step in every sample

01: mute → -40dB, every sample with 1 step. -40dB → 24dB, 2 samples with 1 step.

10: mute → -40dB, 2 samples with 1 step. -40dB → 24dB, 4 samples with 1 step.

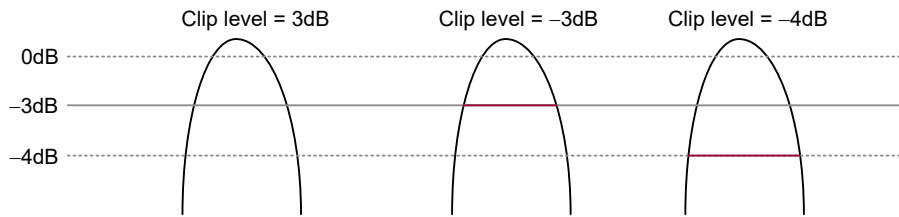
Others: mute → -40dB, 4 samples with 1 step. -40dB → 24dB, 8 samples with 1 step.

Sampling Rate	Set to 00	Set to 01	Set to 10	Set to 11
8kHz	207.875ms	287.875ms	575.75ms	1151.5ms
11.025kHz	150.839ms	208.888ms	417.777ms	835.555ms
12kHz	138.583ms	191.916ms	383.833ms	767.666ms
16kHz	103.9375ms	143.9375ms	287.875ms	575.75ms
22.05kHz	75.4195ms	104.5629ms	209.125ms	417.777ms
24kHz	69.291ms	95.9583ms	191.916ms	383.833ms
32kHz	51.968ms	71.96875ms	143.9375ms	287.875ms
44.1kHz	37.709ms	52.222ms	104.444ms	208.888ms
48kHz	34.645ms	47.979ms	95.95833ms	191.916ms
88.2kHz	18.854ms	26.111ms	52.222ms	104.444ms
96kHz	17.3229ms	23.9895ms	47.979ms	95.95833ms
192kHz	8.6614ms	11.994ms	23.989ms	47.979ms

Address	Bits	Name	Description
0x0A	1:0	VOL_RAMP_MODE[1:0]	00: 1 step in every sample 01: mute → -40dB, every sample with 1 step. -40dB → 24dB, 2 samples with 1 step. 10: mute → -40dB, 2 samples with 1 step. -40dB → 24dB, 4 samples with 1 step. Others: mute → -40dB, 4 samples with 1 step. -40dB → 24dB, 8 samples with 1 step.

19.13 Hard Clip Function

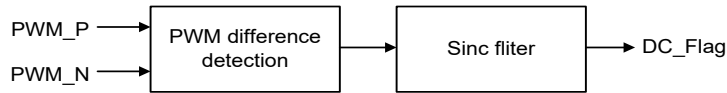
To clip the signal with different threshold, operate in time domain.



Address	Bits	Name	Description
0x06	0	HARD_CLIP_EN	0: Disable hard clip (default) 1: Enable hard clip
0x27	10:0	HARD_CLIP_TH[10:0]	Hard clip threshold for hard clip, when threshold > 0, there is no any clipping effect happened. 11'h180: 0dB 0.0625db per step Note 15: Due to there is -2dB at digital filter, so hard clipping only works when threshold < -2dB.

19.14 DC Protection Function

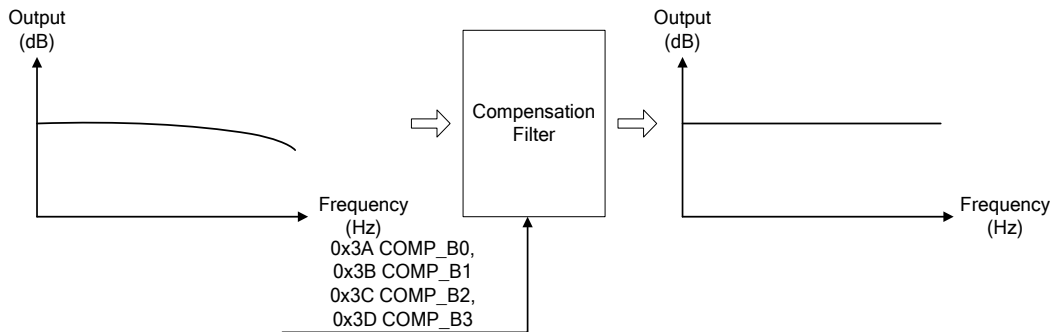
It is to use to protect the loudspeaker, when there are some DC exists at the output. The method is to detect DC at final stage (PWM), calculate the difference of the PWM and a Sinc filter to decide the DC level. The IC will shut down when detect the DC.



Address	Bits	Name	Description
0x14	7:4	Reserved	
	3:2	DC_TH[1:0]	DC threshold for DC detection 00: No available 01: 12.5% 10: 18.75% (default) 11: 25%
	1	DC_TIME_SEL	Detection time 0: 342ms (default) 1: 684ms
	0	DC_EN	0: DC Protection disable 1: DC protection enable (default)

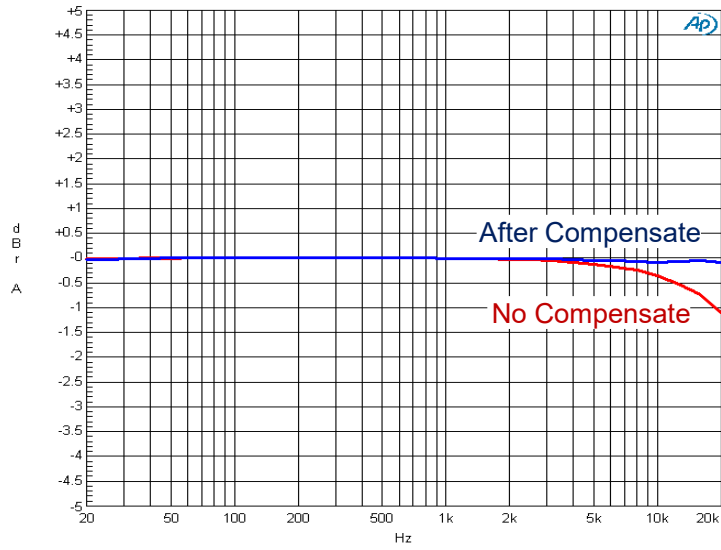
19.15 Compensate Filter

Compensation filter is purpose to compensate internal gain from DAC; this filter can also compensate for the frequency response affected by LC filter. The recommended setting is based on different application circuits to fit the curve.



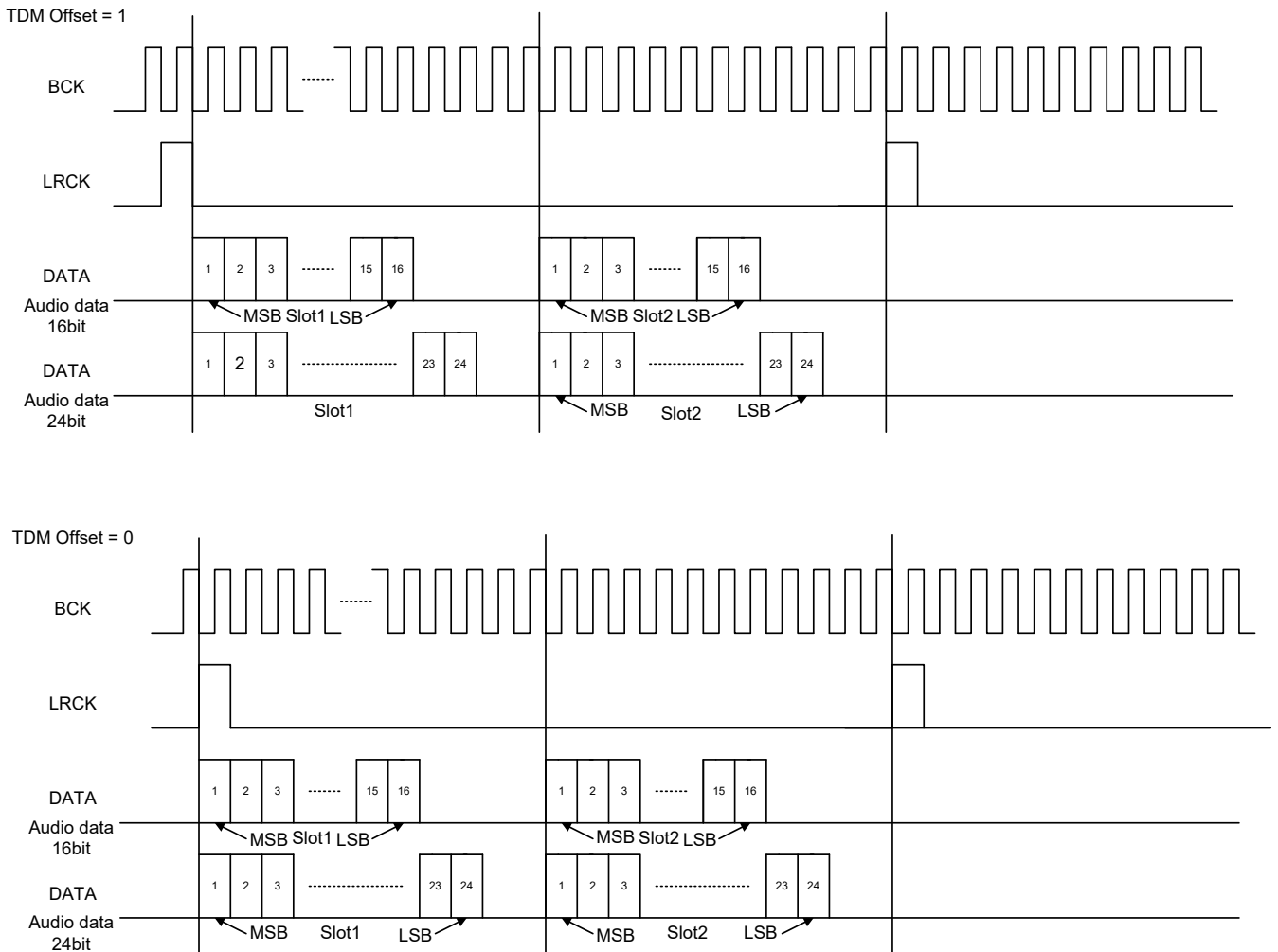
Compensate	Description									
Compensate	B0, B1, B2, B3: Compensate coefficient									
Gain										
Gain	0.1dB	0.2dB	0.3dB	0.4dB	0.5dB	0.6dB	0.7dB	0.8dB	0.9dB	1dB
Coefficient										
B3	00000	1FFFF	00003	00006	00005	00005	00004	00002	00002	00008
B2	0000E	0001E	00022	00026	0003A	00048	0005C	00073	00081	0007F
B1	1FFA1	1FF43	1FEDE	1FE79	1FE19	1FDB1	1FD51	1FCE9	1FC81	1FC14
B0	080A0	0813E	081FF	082C0	0835A	0840F	084A8	0854D	08602	086E0

Address	BITS	Name	Description
0x06	6	COMP_EN	0: Compensation filter disable (default) 1: Compensation filter enable (Not available for 96kHz and 192kHz sampling rate)
0x3A	23:17	Reserved	Compensate B0 coefficient
	16:0	COMP_B0	
0x3B	23:17	Reserved	Compensate B1 coefficient
	16:0	COMP_B1	
0x3C	23:17	Reserved	Compensate B2 coefficient
	16:0	COMP_B2	
0x3D	23:17	Reserved	Compensate B3 coefficient
	16:0	COMP_B3	



19.16 TDM

The RT9120S supports TDM format, which maximum output can reach 16Ch.



Address	Bits	Name	Description
0xA0	7:3	Reserved	
	2	DATAO_PD	Prohibited
	1	TDM_OFFSET	TDM offset selection 0: Without offset 1: 1 bit clock offset (default)
	0	TDM_EN	0: TDM disable TDM application (default) 1: TDM enable
0xA1	7:6	Reserved	
	5:0	TDM_RX_LOC_L	TDM start receiving location select for left channel (reg*8 + offset) 000000: Start from 0+offset (default) 000001: Start from 8+offset ... 111100: Start from 480+offset 111101: Start from 488+offset 111110: Not available 111111: Not available
0xA2	7:6	Reserved	
	5:0	TDM_RX_LOC_R	TDM start receiving location select for left channel (reg*8 + offset) 000000: Start from 0+offset 000001: Start from 8+offset ... 000100: Start from 32+offset (default) ... 111100: Start from 480+offset 111101: Start from 488+offset 111110: Not available 111111: Not available
0xA3	7:6	Reserved	
	5:0	TDM_TX_LOC_L	TDM start transmitting location select for left channel (reg*8 + offset) 000000: Start from 0+offset (default) 000001: Start from 8+offset ... 111100: Start from 480+offset 111101: Start from 488+offset 111110: Not available 111111: Not available
0xA4	7:6	Reserved	
	5:0	TDM_TX_LOC_R	TDM start transmitting location select for right channel (reg*8 + offset) 000000: Start from 0+offset 000001: Start from 8+offset ... 000100: Start from 32+offset (default) ... 111100: Start from 480+offset 111101: Start from 488+offset 111110: Not available 111111: Not available

19.17 Example

1. Set the 0xA0, Bit[0] to 1
2. Set the 0x02, Bit[7:6] to 00
3. Use the below setting

Note 16. The RT9120S has SDO output, which can output the I²S data and TDM data to SOC side for receiving use, so if the receiving not use, the 0xA3, and 0xA4 can keep the default setting.

Note 17. If SCLK (BCK) frequency is larger than the 10MHz, set the 0x10 to 0x00 once the initial setting is done.

If output is 16Ch, the sampling rate is 48kHz								
Output Ch	Ch1, Ch2	Ch3, Ch4	Ch5, Ch6	Ch7, Ch8	Ch9, Ch10	Ch11, Ch12	Ch13, Ch14	Ch15, Ch16
0xA1	Set to 0x00	Set to 0x08	Set to 0x10	Set to 0x18	Set to 0x20	Set to 0x28	Set to 0x30	Set to 0x38
0xA2	Set to 0x04	Set to 0x0C	Set to 0x14	Set to 0x1C	Set to 0x24	Set to 0x2C	Set to 0x34	Set to 0x3C
0xA3	Set to 0x00	Set to 0x08	Set to 0x10	Set to 0x18	Set to 0x20	Set to 0x28	Set to 0x30	Set to 0x38
0xA4	Set to 0x04	Set to 0x0C	Set to 0x14	Set to 0x1C	Set to 0x24	Set to 0x2C	Set to 0x34	Set to 0x3C

If output is 8Ch, the sampling rate is 96kHz				
Output Ch	Ch1, Ch2	Ch3, Ch4	Ch5, Ch6	Ch7, Ch8
0xA1	Set to 0x00	Set to 0x08	Set to 0x10	Set to 0x18
0xA2	Set to 0x04	Set to 0x0C	Set to 0x14	Set to 0x1C
0xA3	Set to 0x00	Set to 0x08	Set to 0x10	Set to 0x18
0xA4	Set to 0x04	Set to 0x0C	Set to 0x14	Set to 0x1C

If output is 4Ch, the sampling rate is 192kHz		
Output Ch	Ch1, Ch2	Ch3, Ch4
0xA1	Set to 0x00	Set to 0x08
0xA2	Set to 0x04	Set to 0x0C
0xA3	Set to 0x00	Set to 0x08
0xA4	Set to 0x04	Set to 0x0C

19.18 PBTL Function

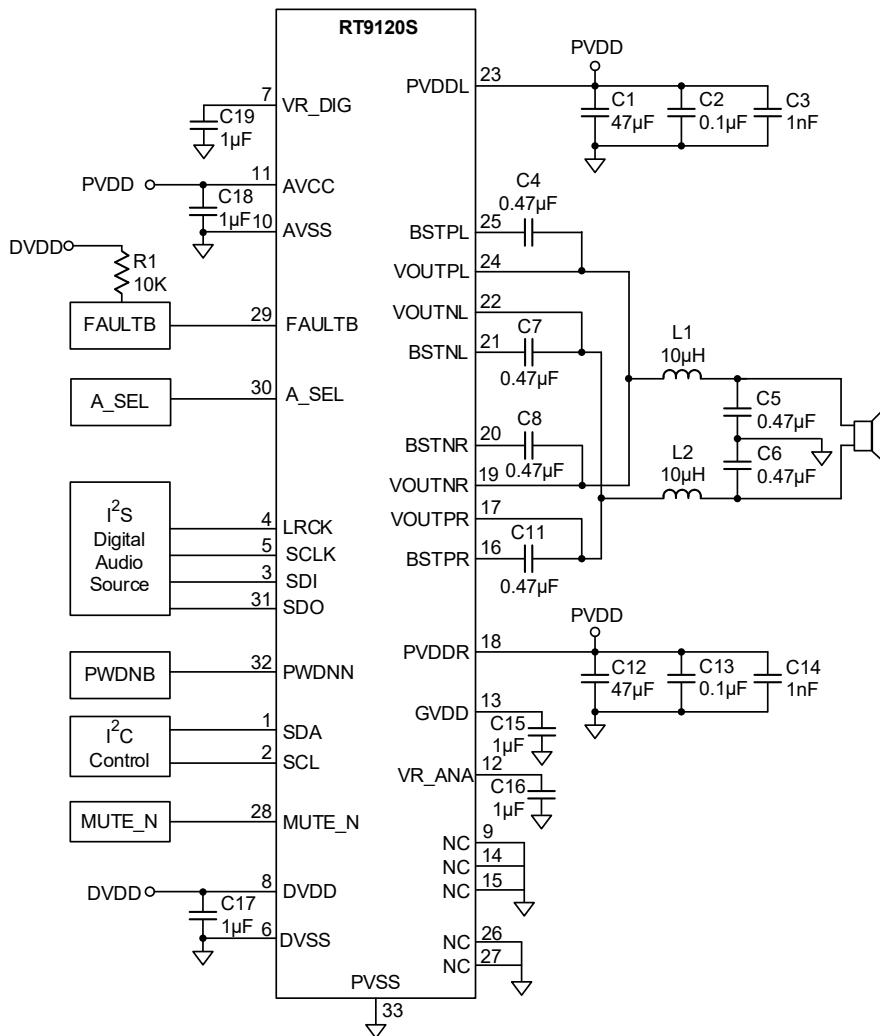
It can be configured with the hardware, and also need to change the software setting

The input signal can be configured by the input mixer, from register 0x30 to configure the input signal. The default signal for the PBTL is from 0x30 L channel signal.

Address	Bits	Name	Description
0x05	4	D_PBTL	0: BTL, 1: PBTL

Address	Bits	Name	Description
0x30	16:0	CH1_IN_MIX_0	u[23:17], mix_0[16:0] u: Unused
0x31	16:0	CH1_IN_MIX_1	u[23:17], mix_1[16:0] u: Unused

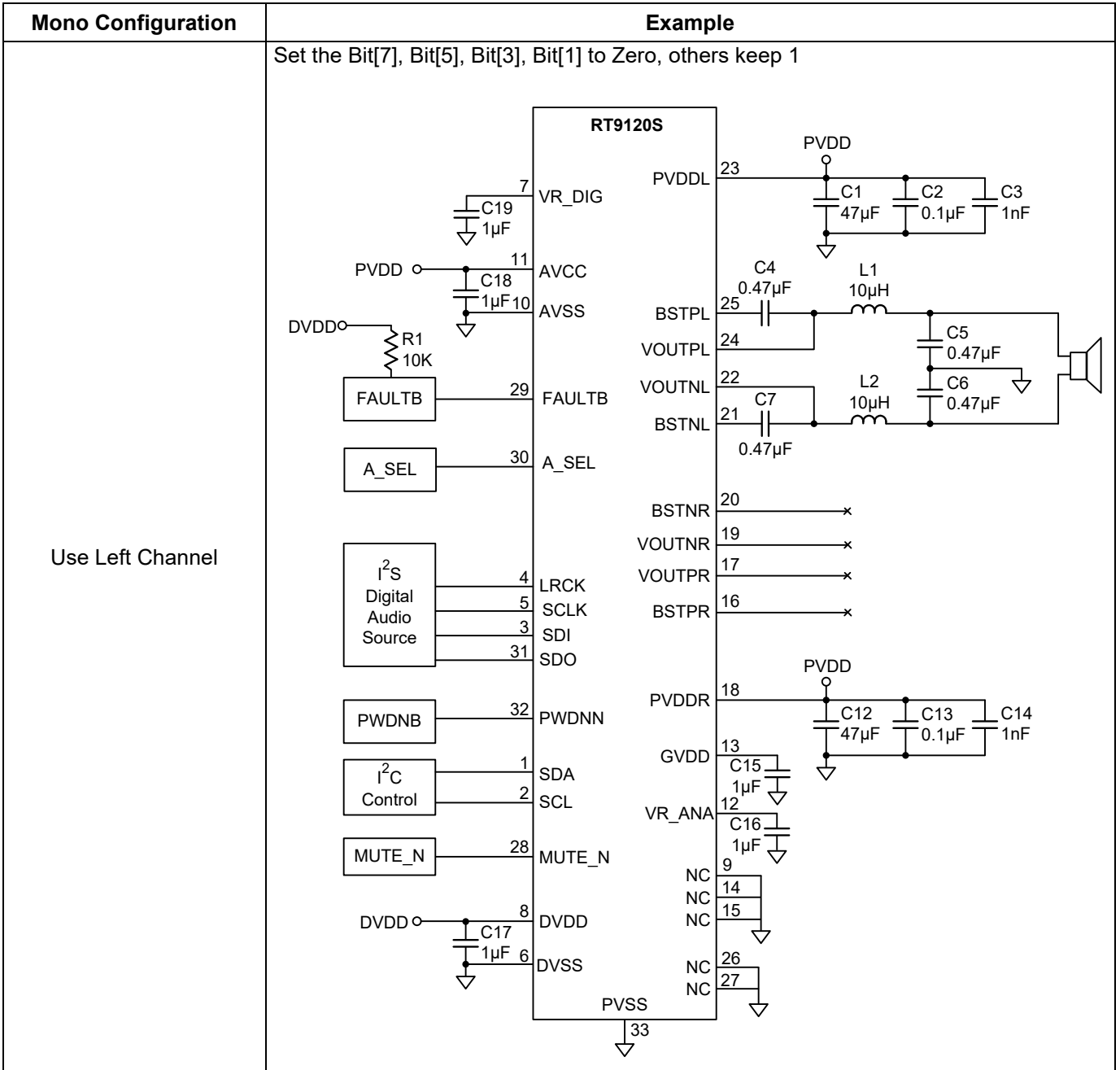
19.19 Mono PBTL Application Circuit

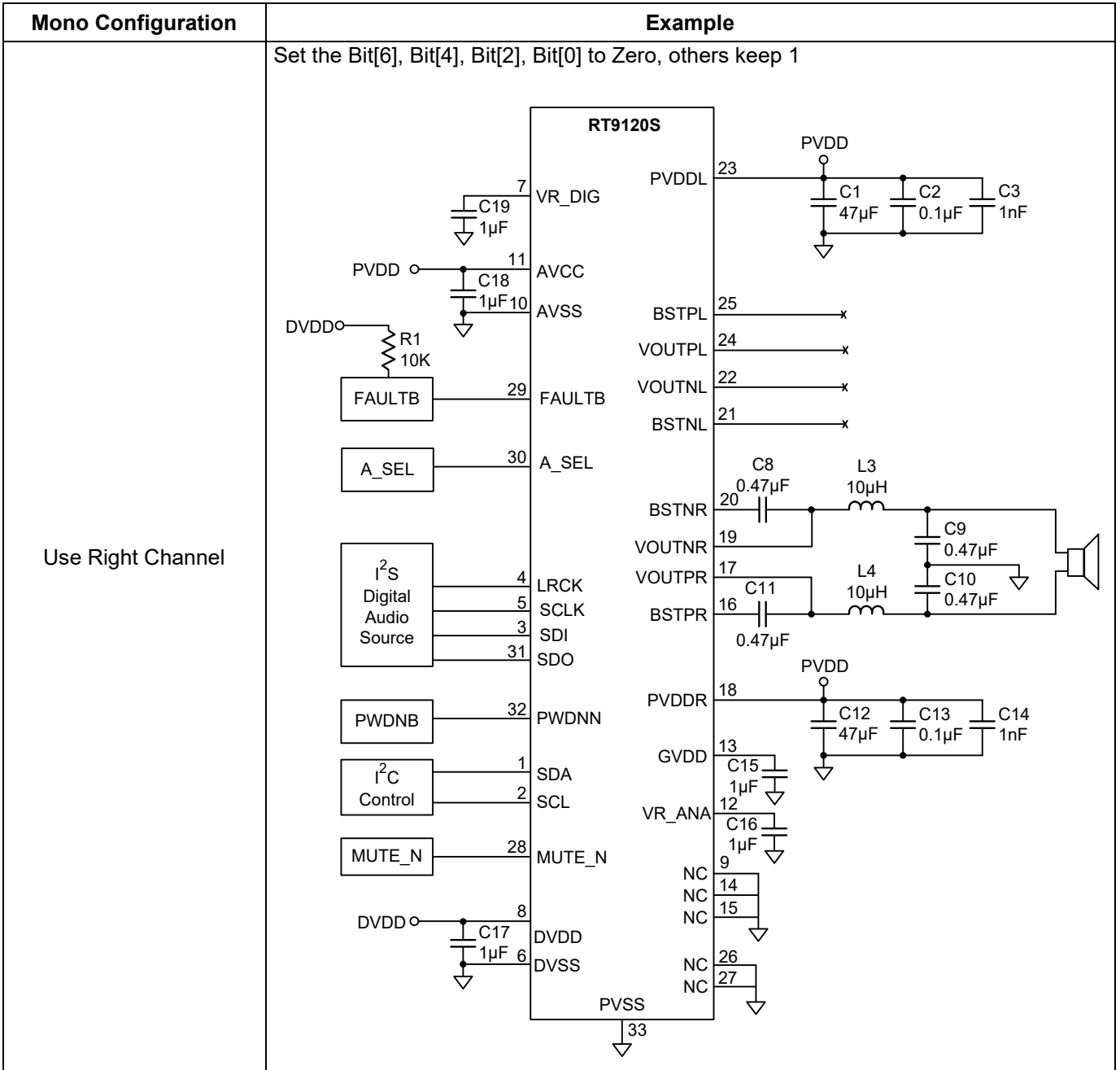


19.20 Mono Configuration

To use the mono configuration, it can be configured by register setting.

Address	Bits	Name	Description
0x08	7	D_LPFR_EN	Enable DAC RCH LPF 0: Disable 1: Enable (default)
	6	D_LPFL_EN	Enable DAC LCH LPF 0: Disable 1: enable (default)
	5	D_EN_RCH_PWR	RCH PWR stage enable 0: Disable 1: Enable (default)
	4	D_EN_LCH_PWR	LCH PWR stage enable 0: Disable 1: Enable (default)
	3	D_DAC_RCH_EN	Enable DAC_RCH 0: Disable 1: Enable (default)
	2	D_DAC_LCH_EN	Enable DAC LCH 0: Disable 1: enable (default)
	1	D_SPK_RCH_EN	Enable Class-D RCH SPK 0: Disable 1: Enable (default)
	0	D_SPK_LCH_EN	Enable Class-D LCH SPK 0: Disable 1: Enable (default)





19.21 Protection Behavior

If a protection event occurs, the IC will automatically detect it, and the error condition can be checked via the register or the FAULTB pin.

19.22 Protection Flag

Address	Bits	Name	Description
0x10	7	Reserved	
	6	DC_ERR	DC flag report 0: No DC error (default) 1: DC error
	5	SCLK_ERR	0: No SCLK error (default) 1: SCLK error, write 0 to clear flag
	4	LRCK_ERR	0: No LRCK clock error (default) 1: LRCK clock error, write 0 to clear flag
	3	OC_ERR	0: No OC error (default) 1: OC, write 0 to clear flag
	2	OV_ERR	0: No OV error (default) 1: OV, write 0 to clear flag
	1	OT_ERR	0: No OT error (default) 1: OT, write 0 to clear flag
	0	UV_ERR	0: No UV error (default) 1: UV, write 0 to clear flag

19.23 Protection Type

Protection	Auto Recovery	Shutdown Amp (Latch Type)	Fault Pin Pull Low
DC Protection	No	Yes	Yes
SCLK ERROR	Yes. The default setting is Auto recovery.	Yes, it can be configured by the 0x12 bit[5]	Yes, but the MASK can be configured by the 0x11 bit[5]
LRCK ERROR	Yes. The default setting is Auto recovery.	Yes, it can be configured by the 0x12 bit[4]	Yes, but the MASK can be configured by the 0x11 bit[4]
OC ERROR	Yes. The default setting is Auto recovery.	Yes, it can be configured by the 0x12 bit[3]	Yes, but the MASK can be configured by the 0x11 bit[3]
OV ERROR	Yes. The default setting is Auto recovery.	Yes, it can be configured by the 0x12 bit[2]	Yes, but the MASK can be configured by the 0x11 bit[2]
OT ERROR	Yes. The default setting is Auto recovery.	Yes, it can be configured by the 0x12 bit[1]	Yes, but the MASK can be configured by the 0x11 bit[1]
UV ERROR	Yes. The default setting is Auto recovery.	Yes, it can be configured by the 0x12 bit[0]	Yes, but the MASK can be configured by the 0x11 bit[0]

When protection happens, there are 2 types of the protection behavior that can be used.

1. Latch type: Will shut down the AMP directly.
2. Auto recovery type: The AMP will enter the auto recovery mode. Until the protection behavior stops, the AMP will continue to work.
3. The DC protection only has the latch type.

19.24 Fault Behavior Type Selection

If a protection event occurs, the IC will automatically detect it. Specific error types can be configured according to the list below.

Address	Bits	Name	Description
0x12	5	SCLK_ERROR_FAULT_TYPE	Fault behavior type selection. 0: Auto recovery (default) 1: Latch
	4	LRCK_ERROR_FAULT_TYPE	Fault behavior type selection. 0: Auto recovery (default) 1: Latch
	3	OC_ERROR_FAULT_TYPE	Fault behavior type selection. 0: Auto recovery 1: Latch (default)
	2	OV_ERROR_FAULT_TYPE	Fault behavior type selection. 0: Auto recovery (default) 1: Latch
	1	OT_ERROR_FAULT_TYPE	Fault behavior type selection. 0: Auto recovery (default) 1: Latch
	0	UV_ERROR_FAULT_TYPE	Fault behavior type selection. 0: Auto recovery (default) 1: Latch

19.25 Fault Mask

Address	Bits	Name	Description
0x11	5	SCLK_ERROR_mask	Fault mask for 0x10 SCLK error
	4	LRCK_ERROR_mask	Fault mask for 0x10 LRCK error
	3	OC_ERROR_mask	Fault mask for 0x10 OC error
	2	OV_ERROR_mask	Fault mask for 0x10 OV error
	1	OT_ERROR_mask	Fault mask for 0x10 OT error
	0	UV_ERROR_mask	Fault mask for 0x10 UV error

19.26 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a VQFN-32L 5x5 package, the thermal resistance, θ_{JA} , is 27.7°C/W on a standard JEDEC 51-7 high effective- thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as below:

$$P_{D(MAX)} = (150^\circ\text{C} - 25^\circ\text{C}) / (27.7^\circ\text{C/W}) = 4.51\text{W for a VQFN-32L 5x5 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curve in Figure 3 allows users to see the effect of rising ambient temperature on the maximum power dissipation.

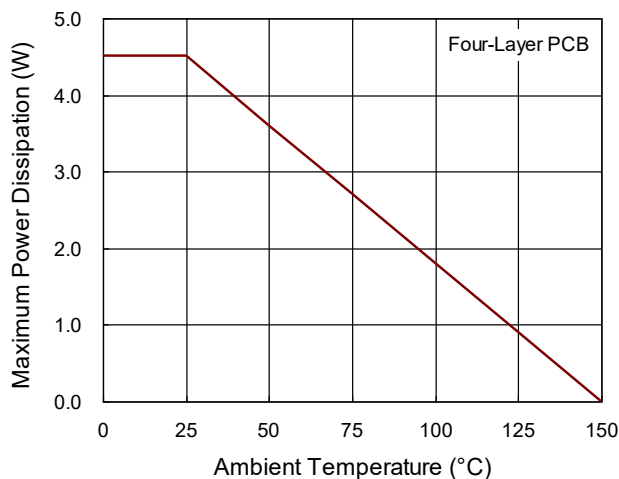
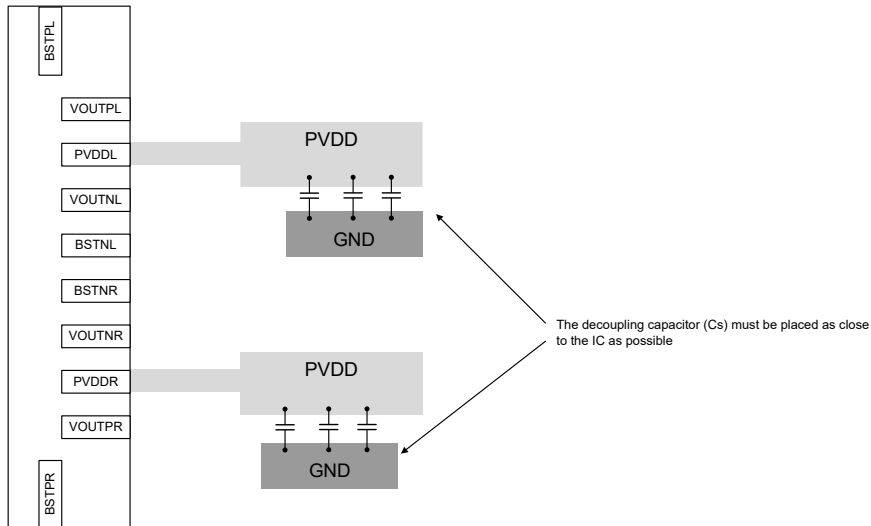


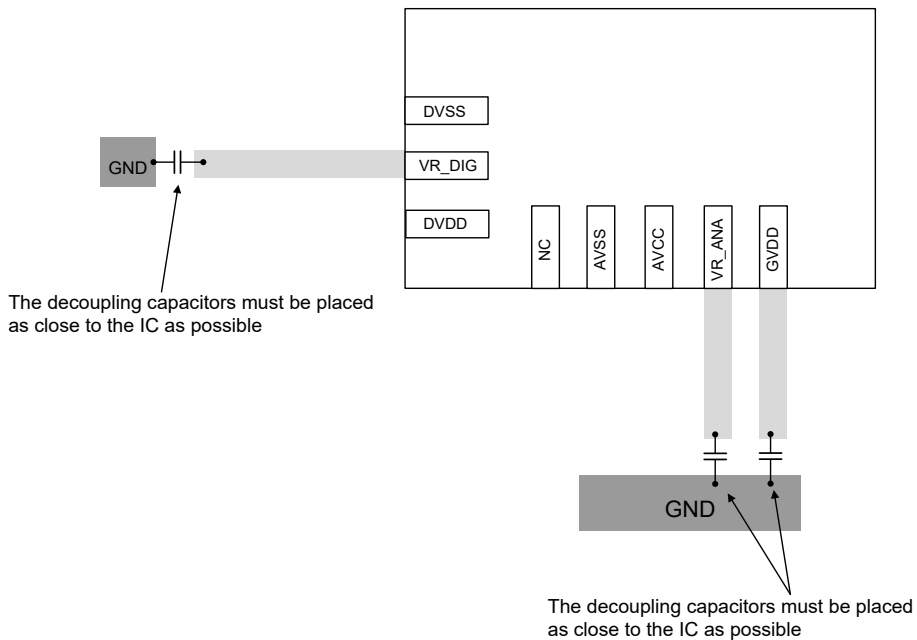
Figure 3. Derating Curve of Maximum Power Dissipation

20 Layout Guide

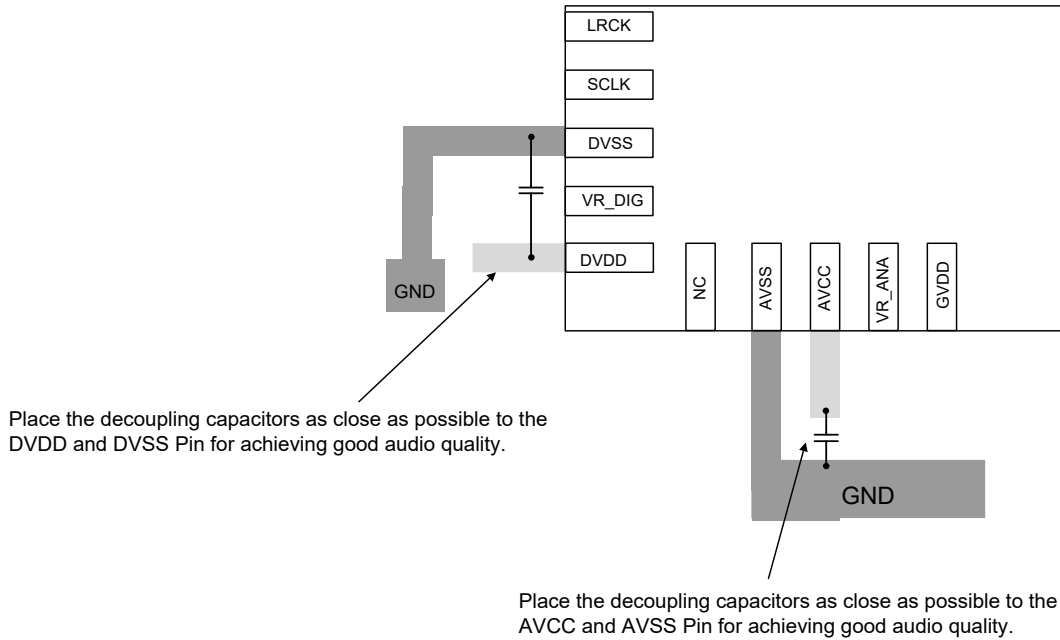
Place the decoupling capacitors as close as possible to the PVCC and GND, then use shortest trace to link these capacitors, and use more vias for GND link to GND layer to reduce parasitic inductance and resistance. The trace is at least 30mil.



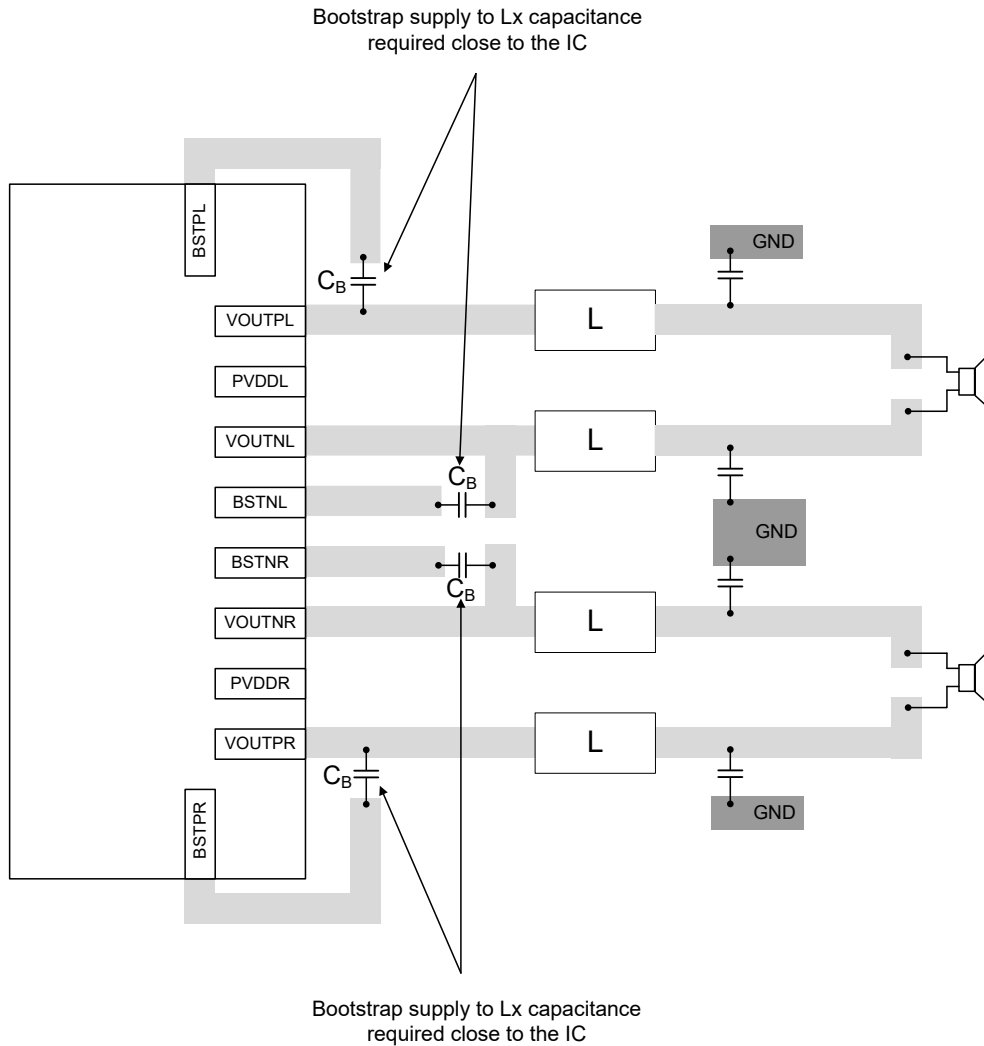
The VR_DIG, VR_ANA and GVDD decoupling capacitors must be placed as close to the IC as possible.



Place the decoupling capacitors as close as possible to the DVDD and DVSS pins, and the AVCC and AVSS pins, to achieve good audio quality. The trace width of DVDD should be at least 6mil, and the trace width of AVCC should be at least 30mil.



The traces for VOUTPL, VOUTNL, VOUTPR, and VOUTNR should be routed with equal widths and lengths, and the bootstrap capacitors connected between the bootstrap supply and the LX pins must be placed as close to the IC as possible.



If possible, use a coplanar ground fill on both sides of the differential speaker output pairs for shielding.

Note 18. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

21 Register Map

Note 19. The register description which is described as prohibit is not allowed to be set.

ADDR	Byte	RegName	Bits	R/W	Name	Description	Default
0x00	2	DEV_ID	15:0	R	DEVICE_ID[15:0]		16'h4303
0x01	1	I2S_CLK_FMT	7:4	R/W	SR_MODE[2:0]	Sampling rate report 0000: 8kHz 0001: 11.025/12kHz 0010: 16kHz 0011: 22.05/24kHz 0100: 32kHz 0101: 44.1/48kHz (default) 0110: 88.2/96kHz 0111: 192kHz Others: Not supported/ SCLK loss/LRCK loss	4'b0101
			3:0	R/W	BCK_MODE[2:0]	BCK mode report 0000: BCK = 32fs 0001: BCK = 48fs 0010: BCK = 64fs (default) 0011: BCK = 96fs 0100: BCK = 128fs 0101: BCK = 192fs 0110: BCK = 256fs 0111: BCK = 384fs 1000: BCK = 512fs others: Reserved Note 20. For the 48fs, 96fs, 192fs, 384fs, 512fs, please set 0xF8 bit[6] to 0.	4'b0010

ADDR	Byte	RegName	Bits	R/W	Name	Description	Default
0x02	1	I2S_DATA_FMT	7:6	R/W	SCLK_DEG_SEL[1:0]	SCLK deglitch time selection 00: No deglitch 01: 1T sync 10: 2T deglitch 11: 3T deglitch (default)	2'b11
			5	R/W	SCLK_EDGE_SEL	0: RX @BCK rising edge & TX @BCK falling edge (default) 1: RX @BCK falling edge & TX @BCK rising edge	1'b0
			4	R/W	DSP_M_A_S	DSP mode A select, active with AUD_FMT = 2'b11 (DSP mode) 0: DSP mode A (default) 1: DSP mode B	1'b0
			3:2	R/W	AUD_FMT	00: I ² S (default) 01: Left Justify 10: Right Justify 11: DSP mode	2'b00
			1:0	R/W	AUD_BITS	00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits (default)	2'b11
0x04	1	SDIO_SEL	7	R	Reserved		1'b0
			6	R/W	Prohibit	Prohibited	1'b1
			5:4	R/W	SDO_SEL[1:0]	00: No output (default) 01: Interface output 10: Final output 11: Peak level detect result	2'b00
			3:2	R/W	CH1_SI[1:0]	00: SDIN-L to CH1 (default) 01: SDIN-R to CH1 1X: 0 to CH1	2'b00
			1:0	R/W	CH2_SI[1:0]	00: SDIN-L to CH2 (default) 01: SDIN-R to CH2 (default) 1X: 0 to CH2	2'b01

ADDR	Byte	RegName	Bits	R/W	Name	Description	Default
0x05	1	SYS_CTL	7	R/W	SR_AUTO_DET	Prohibited	1'b1
			6	R/W	SHUTDOWN	0: Turn on 1: Shut down (default)	1'b1
			5	R	Reserved		1'b0
			4	R/W	D_PBTL	0: BTL (default) 1: PBTL	1'b0
			3:2	R/W	D_SPK_VT_FREQ	PWM frequency 00: 384kHz 01: Reserved 10: 768kHz (default) 11: 1536kHz	2'b10
			1	R/W	DIS_A_SEL_PU	Prohibited	1'b0
			0	R/W	dSR_DIV_SEL	Prohibited	1'b0
0x06	1	DIG_BLK_EN	7	R/W	Reserved		1'b0
			6	R/W	COMP_EN	0: Compensation filter disable (default) 1: Compensation filter enable (not available in 96k & 192kHz Sampling Rate)	1'b0
			5	R/W	HPF_EN	0: High-Pass filter disable 1: High-Pass filter enable (default)	1'b1
			4	R/W	TFC_EN	Thermal fold back control enable 0: Disable (default) 1: Enable	1'b0
			3	R/W	DRC_PEAK	DRC mode selection 0: RMS mode 1: Peak mode (default)	1'b1
			2	R/W	DRC_EN	DRC enable 0: Disable (default) 1: Enable	1'b0
			1	R/W	DRC_N_EN	DRC noise gate enable 0: Disable (default) 1: Enable	1'b0
			0	R/W	HARD_CLIP_EN	Hard clip enable 0: Disable (default) 1: Enable	1'b0

ADDR	Byte	RegName	Bits	R/W	Name	Description	Default
0x07	1	SPK_GAIN	7:6	R	Reserved		2'b00
			5	R/W	SPK_GAIN_SW_TO_EN	SPK gain switch @ zero crossing point, if the SPK gain change and no zero crossing point after 100ms, the gain will switch to the target gain when time out function is enable. 0: Disable 1: Enable (default)	1'b1
			4:0	R/W	D_SPK_GAIN[4:0]	Class-D output gain 00000: -6dB 00001: -5dB 00010: -4dB 00011: -3dB 00100: -2dB 00101: -1dB 00110: 0dB 00111: 1dB 01000: 2dB 01001: 3dB 01010: 4dB 01011: 5dB 01100: 6dB 01101: 7dB 01110: 8dB 01111: 9dB 10000: 10dB 10001: 11dB 10010: 12dB 10011: 13dB (default) 10100: 14dB 10101: 15dB 10110: 16dB 10111: 17dB	5'h13

ADDR	Byte	RegName	Bits	R/W	Name	Description	Default
0x08	1	INTER_PWR_CTRL	7	R/W	D_LPFR_EN	Enable DAC RCH LPF 0: Disable 1: Enable (default)	1'b1
			6	R/W	D_LPFL_EN	Enable DAC LCH LPF 0: Disable 1: Enable (default)	1'b1
			5	R/W	D_EN_RCH_PWR	RCH PWR stage enable 0: Disable 1: Enable (default)	1'b1
			4	R/W	D_EN_LCH_PWR	LCH PWR stage enable 0: Disable 1: Enable (default)	1'b1
			3	R/W	D_DAC_RCH_EN	Enable DAC_RCH 0: Disable 1: Enable (default)	1'b1
			2	R/W	D_DAC_LCH_EN	Enable DAC LCH 0: Disable 1: Enable (default)	1'b1
			1	R/W	D_SPK_RCH_EN	Enable Class-D RCH SPK 0: Disable 1: Enable (default)	1'b1
			0	R/W	D_SPK_LCH_EN	Enable Class-D LCH SPK 0: Disable 1: Enable (default)	1'b1
0x09	1	PWM_SS_OPT	7	R/W	D_FSS_EN	Spread spectrum enable 0: Disable (default) 1: Enable	1'b0
			6	R/W	PWM_MODEWHITE	Noise selection 0: Pink noise (default) 1: White noise	1'b0
			5	R/W	PWM_SELCOEF	Pink noise coefficient This will affect the noise amplitude for spread spectrum signal, not recommended to modify it. 0: 1/2 (default) 1: 1/4	1'b0
			4	R/W	PWM_NOISE_EN	Add noise to TRI_GEN 0: Disable (default) 1: Enable	1'b0
			3:2	R/W	D_NOISE_AMP[1:0]	Nosie amplitude for SSC	2'b00
			1:0	R/W	D_FSS_AMP[1:0]	Spread spectrum frequency variation amplitude 00: 20kHz 01: 40kHz (default) 10: 40kHz 11: 60kHz	2'b01

ADDR	Byte	RegName	Bits	R/W	Name	Description	Default
0x0A	1	VOL_RAMP	7:6	R	Reserved		2'b00
			5	R/W	CH2_MUTE	0: Unmute (default) 1: CH2 soft mute	1'b0
			4	R/W	CH1_MUTE	0: Unmute (default) 1: CH1 soft mute	1'b0
			3	R/W	SKIP_RAMP	0: Enable volume ramp (default) 1: Skip Volume ramp	1'b0
			2	R	Reserved		1'b0
			1:0	R/W	VOL_RAMP_MODE [1:0]	Volume Slew step control 00: 1 step in every sample 01: mute → -40dB, every sample with 1 step. -40dB → 24dB, 2 samples with 1 step. (default) 10: mute → -40dB, 2 samples with 1 step. -40dB → 24dB, 4 samples with 1 step. (default) Others: Mute → -40dB, 4 samples with 1 step. -40dB → 24dB, 8 samples with 1 step.	2'b01
0x0B	1	TFC_CTRL	7:6	R	Reserved	Prohibited	2'b00
			5	R	D_TFC_UPBOUN_FLAG	Prohibited	1'b0
			4	R	D_TFC_LOWBOUN_FLAG	Prohibited	1'b0
			3:2	R/W	TFC_TH	Thermal fold back active threshold 00: Temp 110°C (default) 01: Temp 120°C 10: Temp 130°C 11: Temp 140°C	2'b00
			1:0	R/W	TFC_RATE	Thermal fold back attack/release rate 00: 0.0625dB/50ms (default) 01: 0.0625dB/100ms 10: 0.0625dB/200ms 11: 0.0625dB/400ms	2'b00
0x0C	1	Reserved	7:0	R/W	Reserved	Prohibited	8'h30

ADDR	Byte	RegName	Bits	R/W	Name	Description	Default
0x10	1	ERR_RPT	7	R/W	ADS_ERR	Address R detection error 0: No R detect error (default) 1: R detect error, write 0 to clear flag	1'b0
			6	R	DC_ERR	DC flag report 0: No DC error (default) 1: DC error	1'b0
			5	R/W	SCLK_ERR	0: No SCLK error (default) 1: SCLK error, write 0 to clear flag	1'b0
			4	R/W	LRCK_ERR	0: No LRCK clock error (default) 1: LRCK clock error, write 0 to clear flag	1'b0
			3	R/W	OC_ERROR	0: No OC error (default) 1: OC, write 0 to clear flag	1'b0
			2	R/W	OV_ERROR	0: No OV error (default) 1: OV, write 0 to clear flag	1'b0
			1	R/W	OT_ERROR	0: No OT error (default) 1: OT, write 0 to clear flag	1'b0
			0	R/W	UV_ERROR	0: No UV error (default) 1: UV, write 0 to clear flag	1'b0

ADDR	Byte	RegName	Bits	R/W	Name	Description	Default
0x11	1	ERR_MASK	7:6	R	Reserved	Prohibited	2'b00
			5	R/W	SCLK_ERROR_MASK	Fault mask for 0x10 SCLK error 0: Not mask 1: Mask (default)	1'b1
			4	R/W	LRCK_ERROR_MASK	Fault mask for 0x10 LRCK error 0: Not mask 1: Mask (default)	1'b1
			3	R/W	OC_ERROR_MASK	Fault mask for 0x10 OC error 0: Not mask (default) 1: Mask	1'b0
			2	R/W	OV_ERROR_MASK	Fault mask for 0x10 OV error 0: Not mask (default) 1: Mask	1'b0
			1	R/W	OT_ERROR_MASK	Fault mask for 0x10 OT error 0: Not mask (default) 1: Mask	1'b0
			0	R/W	UV_ERROR_MASK	Fault mask for 0x10 UV error 0: Not mask (default) 1: Mask	1'b0

ADDR	Byte	RegName	Bits	R/W	Name	Description	Default
0x12	1	ERR_TYPE	7:6	R	Reserved		2'b00
			5	R/W	SCLK_ERROR_FAULT_TYPE	Fault behavior type selection. 0: Auto recovery (default) 1: Latch	1'b0
			4	R/W	LRCK_ERROR_FAULT_TYPE	Fault behavior type selection. 0: Auto recovery (default) 1: Latch	1'b0
			3	R/W	OC_ERROR_FAULT_TYPE	Fault behavior type selection. 0: Auto recovery 1: Latch (default)	1'b1
			2	R/W	OV_ERROR_FAULT_TYPE	Fault behavior type selection. 0: Auto recovery (default) 1: Latch	1'b0
			1	R/W	OT_ERROR_FAULT_TYPE	Fault behavior type selection. 0: Auto recovery (default) 1: Latch	1'b0
			0	R/W	UV_ERROR_FAULT_TYPE	Fault behavior type selection. 0: Auto recovery (default) 1: Latch	1'b0
0x13	1	AUTO_RCVRY	7:6	R	Reserved		2'b00
			5	R/W	FAULT_B_TYPE	0: Recovery type (default) 1: Latch type	1'b0
			4	R/W	PROT_PWR_PL_EN	Prohibited	1'b1
			3:0	R/W	RCVRY_TIME[3:0]	Power Stage auto recovery time 0010: 299ms (default) 0011: 449ms 0100: 598ms 0101: 748ms 0110: 898ms 0111: 1047ms 1000: 1197ms 1001: 1346ms 101X: 1496ms 11XX: 1496ms	4'b0010

ADDR	Byte	RegName	Bits	R/W	Name	Description	Default
0x14	1	DC_PROT	7:4	R	Reserved	Prohibited	4'b0000
			3:2	R/W	DC_TH[1:0]	DC threshold for DC detection 00: No available 01: 12.5% 10: 18.75% (default) 11: 25%	2'b10
			1	R/W	DC_TIME_SEL	Detection time 0: 342ms (default) 1: 684ms	1'b0
			0	R/W	DC_EN	DC protection enable 0: Disable 1: Enable (default)	1'b1
0x20	2	MS_VOL	15:11	R	Reserved	Prohibited	5'b00000
			10:0	R/W	MS_VOL[10:0]	Master volume control 11'h000: 24dB 11'h180: 0dB 11'h7FF: mute (default) 0.0625dB per step	11'h7FF
0x21	2	CH1_VOL	15:11	R	Reserved	Prohibited	5'b00000
			10:0	R/W	CH1_VOL[10:0]	CH1 volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: mute 0.0625dB per step	11'h180
0x22	2	CH2_VOL	15:11	R	Reserved	Prohibited	5'b00000
			10:0	R/W	CH2_VOL[10:0]	CH2 volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: mute 0.0625dB per step	11'h180
0x23	2	DRC_TH	15:11	R	Reserved	Prohibited	5'b00000
			10:0	R/W	DRC_TH	DRC threshold 11'h000: 0dB (default) 11'h180: -24dB 11'h67E: -103.875dB 11'h67F~11'h7FF: Not available 0.0625dB per step	11'h000
0x24	2	DRC_RATIO	15:8	R	Reserved	Prohibited	8'h00
			7:0	R/W	DRC_RATIO	DRC compress ratio 8'h00: No compression 8'h80~8'hFF: Full compression 1/128 per step	8'h80

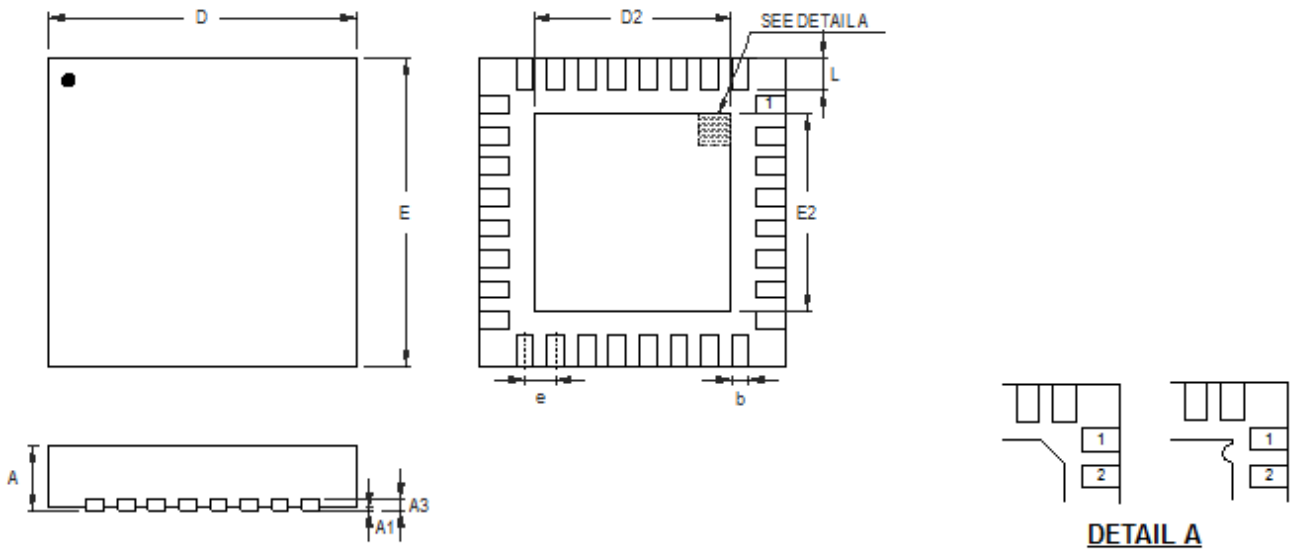
ADDR	Byte	RegName	Bits	R/W	Name	Description	Default
0x25	2	DRC_OFFSET	15:11	R	Reserved	Prohibited	5'b00000
			10:0	R/W	DRC_OFFSET	DRC make up gain (Offset) 11'h000: 24dB 11'h180: 0dB (default) 11'h7FE: -103.875dB 11'h7FF: Not available 0.0625dB per step	11'h180
0x26	2	DRC_NG_TH	15:11	R	Reserved	Prohibited	5'b00000
			10:0	R/W	DRC_NG_TH	Noise gate threshold 11'h000: 0dB 11'h180: -24dB 11'h640: -100dB (default) 11'h67E: -103.875dB 11'h67F~11'h7FF: Not available 0.0625dB per step	11'h640
0x27	2	HARD_CLIP_TH	15:11	R	Reserved	Prohibited	5'b00000
			10:0	R/W	HARD_CLIP_TH [10:0]	Hard Clip Threshold when HARD_CLIP_EN = 1 > 0dB is not allowable for hard clip threshold setting 11'h180: 0dB (default) 0.0625db per step	11'h180
0x30	3	CH1_IN_MIX_0	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	CH1_IN_MIX_0	CH1_IN_MIX_0	17'h08000
0x31	3	CH1_IN_MIX_1	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	CH1_IN_MIX_1	CH1_IN_MIX_1	17'h00000
0x32	3	CH2_IN_MIX_0	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	CH2_IN_MIX_0	CH2_IN_MIX_0	17'h00000
0x33	3	CH2_IN_MIX_1	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	CH2_IN_MIX_1	CH2_IN_MIX_1	17'h08000
0x34	3	DRC_AE	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	DRC_AE	DRC energy estimator	17'h08000
0x35	3	DRC_1-AE	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	DRC_1-AE	DRC energy estimator when releasing	17'h00000
0x36	3	DRC_AD	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	DRC_AD	DRC release time	17'h08000
0x37	3	DRC_AA	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	DRC_AA	DRC attack time	17'h08000

ADDR	Byte	RegName	Bits	R/W	Name	Description	Default
0x38	3	RMS_RPT_AE	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	RMS_RPT_AE	Prohibited	17'h00000
0x3A	3	COMP_B0	23:17	R	Reserved		7'h00
			16:0	R/W	COMP_B0	Compensation filter coefficient B0	17'h08000
0x3B	3	COMP_B1	23:17	R	Reserved		7'h00
			16:0	R/W	COMP_B1	Compensation filter coefficient B1	17'h08000
0x3C	3	COMP_B2	23:17	R	Reserved		7'h00
			16:0	R/W	COMP_B2	Compensation filter coefficient B2	17'h00000
0x3D	3	COMP_B3	23:17	R	Reserved		7'h00
			16:0	R/W	COMP_B3	Compensation filter coefficient B3	17'h00000
0x3E	4	CH1_RMS_RPT	31:0	R	CH1_RMS_RPT[31:0]	Prohibited	32'h00000000
0x3F	4	CH2_RMS_RPT	31:0	R	CH2_RMS_RPT[31:0]	Prohibited	32'h00000000
0x6C	1	UVP_OPT	7	R/W	D_VCORE_OK	For initial sequence 1: DVDD and VR_ANA are ready 0: not ready	1'b1
			6	R/W	D_EN_DVDD_UV	0: disable (default) 1: enable	1'b1
			5:4	R/W	D_UVP_DVDD_VTH	Adjust UVP threshold for detecting DVDD=3.3V Rising: 00=2.475V; 01=2.33V; 10=2.084V; 11=DVDD Falling: 00=2.333V; 01=2.21V; 10=2.0V; 11=DVDD	2'b10
			3	R/W	D_UV_RAMP_DOWN	SPK UV protection behavior 0: HZ_PROT directly (default) 1: Power-off sequence	1'b0
			2:0	R/W	D_UVP_PVDD_SEL [2:0]	Select UVP level for PVDD power domain 000: 4V (default) 001: 6.1V 010: 8.7V 011: 11V 100: 12.8V 101: 15.2V 110: 20.3V 111: 21.2V	3'b000

ADDR	Byte	RegName	Bits	R/W	Name	Description	Default
0xA0	1	AUD_TDM2	7:3	R	Reserved		5'b00000
			2	R/W	DATAO_PD	Prohibited	1'b0
			1	R/W	TDM_OFFSET	TDM offset selection 0: Without offset 1: 1 bit clock offset (default)	1'b1
			0	R/W	TDM_EN	0: TDM disable TDM application (default) 1: TDM enable	1'b0
0xA1	1	TDM_RX_L	7:6	R	Reserved		2'b00
			5:0	R/W	TDM2_RX_LOC_L	TDM start receiving location select for left channel 00000: Start from 0 + offset (default) 00001: Start from 8 + offset ... 11100: Start from 488 + offset 11101: Start from 496 + offset 11110: Not available 11111: Not available	6'b000000
0xA2	1	TDM_RX_R	7:6	R	Reserved		2'b00
			5:0	R/W	TDM2_RX_LOC_R	TDM start receiving location select for left channel 00000: Start from 0 + offset 00001: Start from 8 + offset ... 000100: Start from 32+offset (default) ... 11100: Start from 488 + offset 11101: Start from 496 + offset 11110: Not available 11111: Not available	6'b000100

ADDR	Byte	RegName	Bits	R/W	Name	Description	Default
0xA3	1	TDM_TX_L	7:6	R	Reserved		2'b00
			5:0	R/W	TDM2_TX_LOC_L	TDM start transmitting location select for left channel 00000: Start from 0 + offset (default) 00001: Start from 8 + offset ... 11100: Start from 488 + offset 11101: Start from 496 + offset 11110: Not available 11111: Not available	6'b000000
0xA4	1	TDM_TX_R	7:6	R	Reserved		2'b00
			5:0	R/W	TDM2_TX_LOC_R	TDM start transmitting location select for right channel 00000: Start from 0+offset 00001: Start from 8+offset ... 000100: Start from 32+offset (default) ... 11100: Start from 488 + offset 11101: Start from 496 + offset 11110: Not available 11111: Not available	6'b000100

22 Outline Dimension



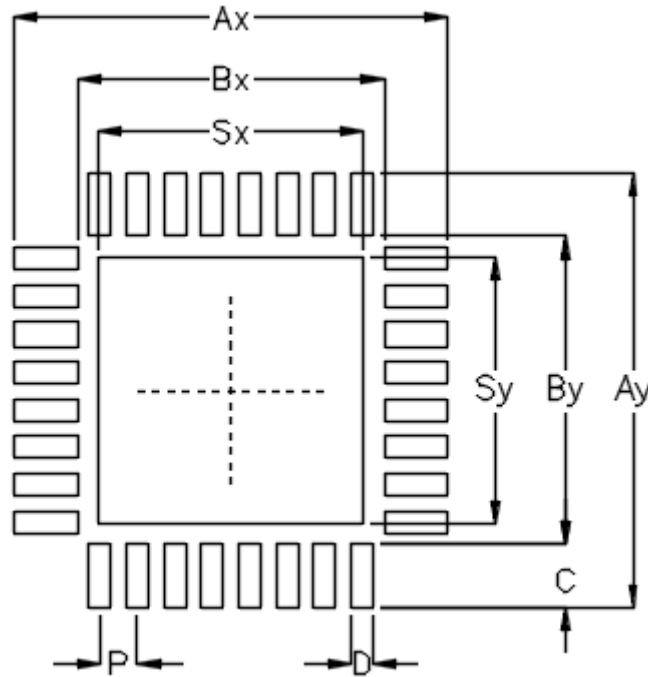
DETAIL A
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	4.950	5.050	0.195	0.199
D2	3.400	3.750	0.134	0.148
E	4.950	5.050	0.195	0.199
E2	3.400	3.750	0.134	0.148
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 32L QFN 5x5 Package

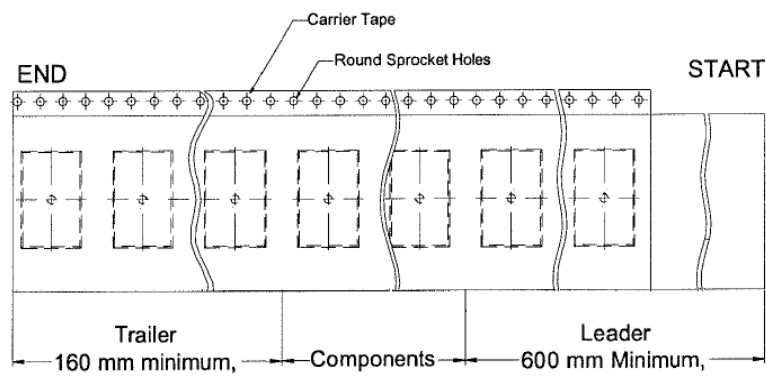
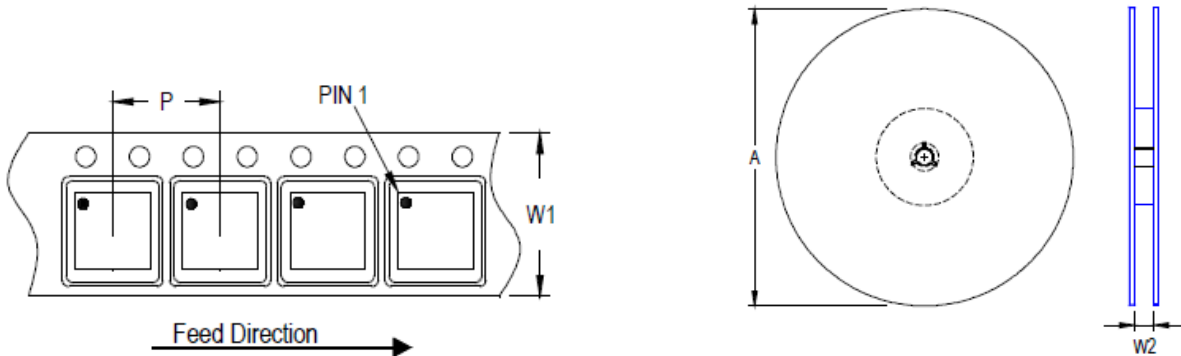
23 Footprint Information



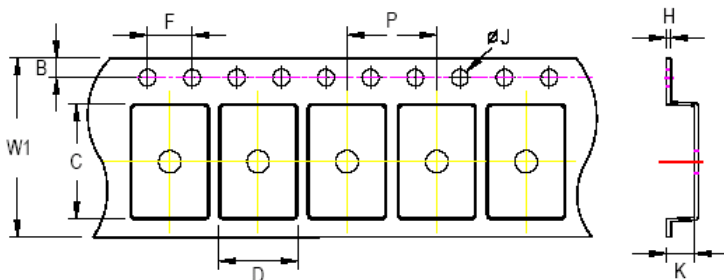
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN5*5-32	32	0.50	5.80	5.80	4.10	4.10	0.85	0.30	3.55	3.55	±0.05

24 Packing Information

24.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 5x5	12	8	180	7	1,500	160	600	12.4/14.4









C, D and K are determined by component size.

The clearance between the components and

Tape Size	W1		P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max	
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm	

24.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 <p>Reel 7"</p>	4	 <p>3 reels per inner box Box A</p>
2	 <p>HIC & Desiccant (1 Unit) inside</p>	5	 <p>12 inner boxes per outer box</p>
3	 <p>Caution label is on backside of Al bag</p>	6	 <p>Outer box Carton A</p>

Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN/DFN 5x5	7"	1,500	Box A	18.3*18.3*8.0	3	4,500	Carton A	38.3*27.2*38.3	12	54,000
			Box E	18.6*18.6*3.5	1	1,500	For Combined or Partial Reel.			

24.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}

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Datasheet Revision History

Version	Date	Description
00	2022/12/28	First Edition
01	2026/04/29	Content descriptions have been enhanced; no changes were made to the specifications. Electrical Characteristics Power-Off Sequence Volume Ramp Register Map