Programmable Frequency Synchronous Buck PWM Controller

General Description

The RT9232A is a single-phase synchronous buck PWM DC-DC converter controller designed to drive two N-Channel MOSFET. It provides a highly accurate, programmable output voltage precisely regulated to low voltage requirement with an internal 0.8V ± 1% reference.

The RT9232A uses an external compensated, single feedback loop voltage mode PWM control for fast transient response. An oscillator with Programmable frequency (50kHz to 800kHz) reduces the external inductor and capacitor component size for saving PCB board area.

The RT9232A provides fast transient response to satisfy high current output applications (up to 25A) while minimizing external components. It is suitable for high-performance graphic processors, DDR and VTT power.

The RT9232A integrates complete protect functions such as Soft Start, Output Enable, UVLO(under-voltage lockout) into a small 14-pin package.

Ordering Information

RT9232A □ □

- Package Type
  S : SOP-14
- Lead Plating System
  P : Pb Free
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

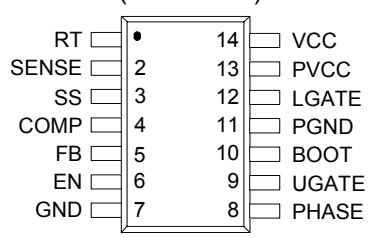
- **Single IC Supply Voltage : 12V**
- **Single phase DC/DC Buck Converter with**
  - **High Output Current (up to 25A)**
  - **Low Output Voltage (down to 0.8V)**
  - **High Input Voltage (up to 12V)**
- **Operate from 12V, 5V or 3.3V Input**
- **0.8V ± 1% Internal Reference**
- **Adaptive Non-Overlapping Gate Drivers**
- **Integrated High-Current, HV Gate Drivers**
- **External Programmable Soft Start**
- **External Programmable Frequency (Range : 50kHz to 800kHz, 200kHz Free Run)**
- **Integrated Output Short Circuit Protection**
- **On/Off Control by Enable Pin**
- **Drives Two N-MOSFET**
- **Full 0 to 100% Duty Cycle**
- **Fast Transient Response**
- **Voltage Mode PWM Control with External Feedback Loop Compensation**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- System (Graphic, MB) with 12V Power.
- Graphic Cards (AGP 8X, 4X, PCI Express*16):
  - High-Current for High-Performance Graphic Processors (GPU, VPU)
  - Middle Current for High-Performance Graphic Memory Power (DDR, DDR II)
  - Low Current with Sink Capacity for High-Performance Graphic Memory Power (DDR/VTT)
- 3.3V to 12V Input DC-DC Regulators
- Low Voltage Distributed Power Supplies

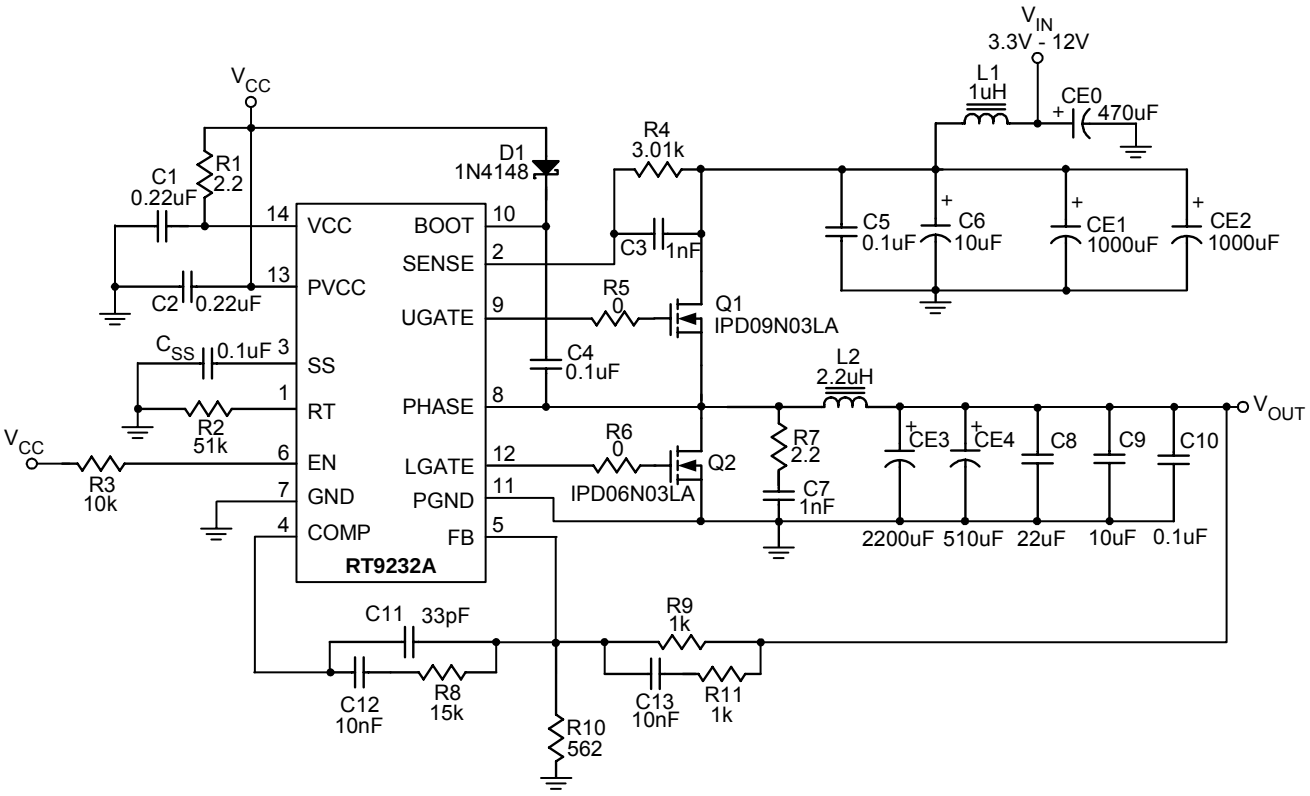
Pin Configurations

(TOP VIEW)



SOP-14

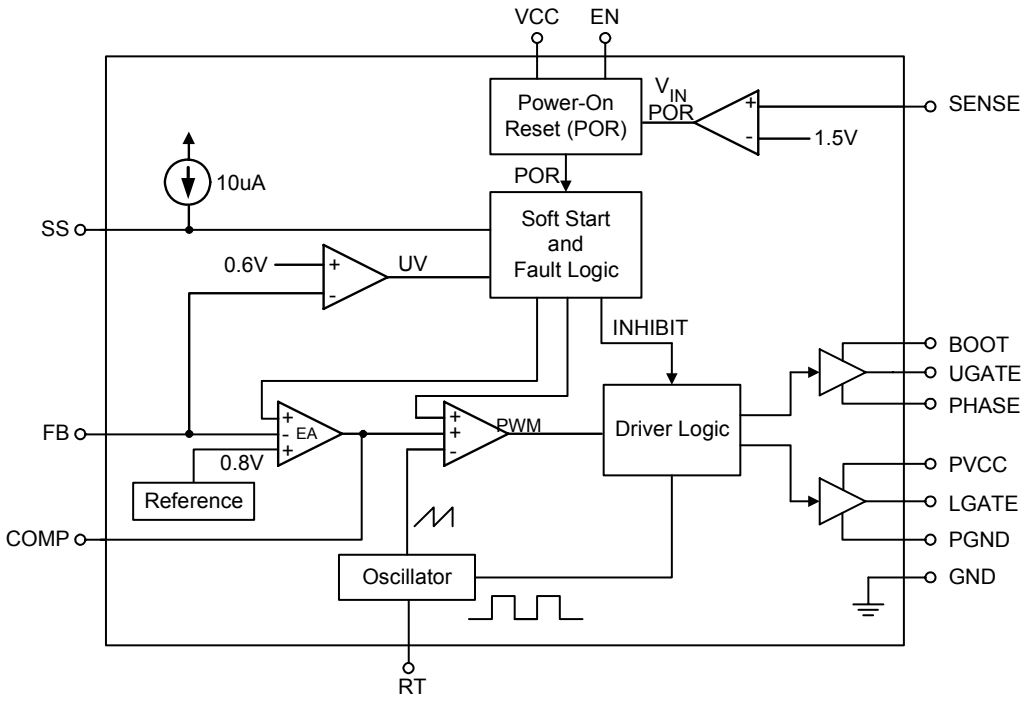
Typical Application Circuit



Functional Pin Description

No	Pin Name	Pin Function
1	RT	Oscillator Frequency Setting
2	SENSE	Sense V_{IN} Power Condition
3	SS	Soft Start Time Interval Setting
4	COMP	Feedback Compensation
5	FB	Voltage Feedback
6	EN	Chip Enable (Active High)
7	GND	IC Signal Reference Ground
8	PHASE	Return Path for Upper MOSFET
9	UGATE	Upper MOSFET Gate Drive
10	BOOT	Input Supply for Upper Gate Drive
11	PGND	Power Ground
12	LGATE	Lower MOSFET Gate Drive
13	PVCC	Input Supply for Lower Gate Drive
14	VCC	Internal IC Supply (12V Bias)

Function Block Diagram



Operation

Startup

RT9232A initializes automatically after receiving both V_{CC} and V_{IN} power. Special power-on sequence is not necessary. The Power-On Reset (POR) function continually monitors input supply voltages and enable voltage. POR function monitors IC power via VCC pin and external MOSFET power via SENSE pin. Voltage on SENSE pin is a fixed voltage drop less than V_{IN}. When voltages on VCC, SENSE, and EN pins exceed their thresholds, POR function initializes soft-start operation. POR inhibits driver operation while EN pin pulls low. Transitioning EN pin high after input supply voltages ready initializes soft-start operation.

Soft-Start

After POR function releases soft-start operation, an internal 10uA current source charges an external capacitor on SS pin (Css) to 5V. Soft-start function clamps both COMP & FB pins to SS pin voltage & a fixed voltage drop less than SS pin voltage respectively. Thus upper MOSFET turns on at a limited duty and output current overshoot can be reduced. This method provides a rapid and controlled output voltage rise.

Under Voltage Protection

The under voltage protection function protects the converter from an shorted output by detecting the voltage on FB pin to monitor the output voltage. The UVP function cycles soft-start function in a hiccup mode. When output voltage lower than 75% of designated voltage, UVP function initializes soft-start cycles. The soft-start function discharges Css with 10uA current sink and disable PWM operation. Then soft-start function recharges Css and PWM operation resumes. The soft-start hiccup restarts after SS voltage fully charges to 4V if the output short event still remains. The converter is shutdown permanently after 3 times hiccup and only restarting supply voltages can enable the converter.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{CC}, PVCC ---------- 15V
- PHASE to GND
  DC ---------- –5V to 15V
  < 200ns ---------- –10V to 30V
- BOOT to PHASE ---------- 15V
- BOOT to GND
  DC ---------- –0.3V to V_{CC}+15V
  < 200ns ---------- –0.3V to 42V
- SS, FB, COMP, RT ---------- 6V
- Input, Output or I/O Voltage ---------- GND–0.3V to V_{CC}+ 0.3V
- Package Thermal Resistance (Note 2)
  SOP-14, θ_{JA} ---------- 100°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{CC} ---------- 12V ±10%
- Supply Voltage to Drain of Upper MOSFETs, V_{IN} ---------- 3.3V, 5V to 12V ±10%
- Ambient Temperature Range ---------- 0°C to 70°C
- Junction Temperature Range ---------- 0°C to 125°C

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C, Unless otherwise specified.)

Parameter		Symbol	Test Conditions	Min	Typ.	Max	Unit
V_{CC} Supply Current							
Nominal Supply Current		I_{CC}	EN=V_{CC}, UGATE, LGATE open	--	3	--	mA
Power-On Reset (POR)							
V_{CC} Rising Threshold		V_{CC_ON}	V_{SENSE} = 4.5V	8.4	--	10	V
Power On Reset Hysteresis			V_{SENSE} = 4.5V	0.4	0.7	--	V
SENSE Rising Threshold for start up		V_{SENSE_ON}		--	1.5	2	V
Enable Input Threshold (ON)		V_{EN_ON}	V_{SENSE} = 4.5V	--	--	2	V
Enable Input Threshold (OFF)		$V_{EN,\_OFF}$	V_{SENSE} = 4.5V	0.8	--	--	V
Oscillator							
Free Running Frequency	RT9232A	f_{OSC}		170	200	230	kHz
	Variation		6k < (RT to GND) < 200k	–20		20	%
Ramp Amplitude		ΔV_{OSC}		--	2	--	V_{P-P}
Reference							
Error Amplifier Reference Voltage		V_{REF}		0.792	0.8	0.808	V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Error Amplifier						
DC gain			--	88	--	dB
Gain-Bandwidth product	GBW		--	15	--	MHz
Slew Rate	SR	COMP=10pF	--	6	--	V/μs
Soft Start						
External SS Source Current	I_{SS}		7	10	--	μA
PWM Controller Gate Driver						
Upper Drive Source	R_{UG_SC}	$V_{BOOT-PHASE}$ = 12V $V_{BOOT-UGATE}$ = 1V	--	3.3	--	Ω
Upper Drive Sink	R_{UG_SK}	$V_{BOOT-PHASE}$ = 12V $V_{UGATE-PHASE}$ = 1V	--	3.7	--	Ω
Lower Drive Source	R_{LG_SC}	$V_{PVCC - LGATE}$ = 1V	--	2.5	--	Ω
Lower Drive Sink	R_{LG_SK}	$V_{LGATE - PGND}$ = 1V	--	2.1	--	Ω
Driving Capability						
Upper Drive Source	I_{UG_SC}	$V_{BOOT-UGATE}$ = 12V	--	1.7	--	A
Upper Drive Sink	I_{UG_SK}	$V_{UGATE-PHASE}$ = 12V	--	1.2	--	A
Lower Drive Source	I_{LG_SC}	$V_{PVCC - LGATE}$ = 12V	--	2.6	--	A
Lower Drive Sink	I_{LG_SK}	$V_{LGATE - PGND}$ = 12V	--	2.4	--	A
Protection						
Under-Voltage Protection		FB Falling	0.5	0.6	0.7	V
Under-Voltage Protection Delay			--	30	--	μs

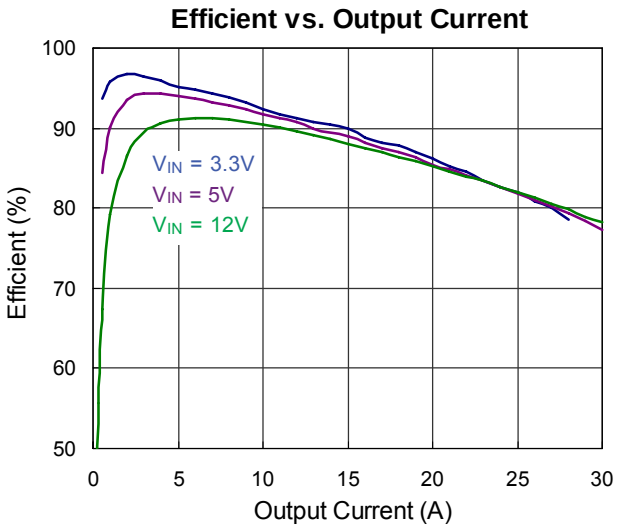
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

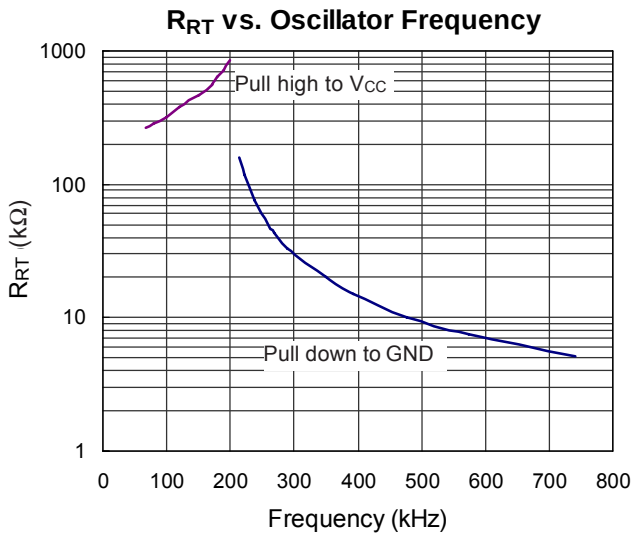
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

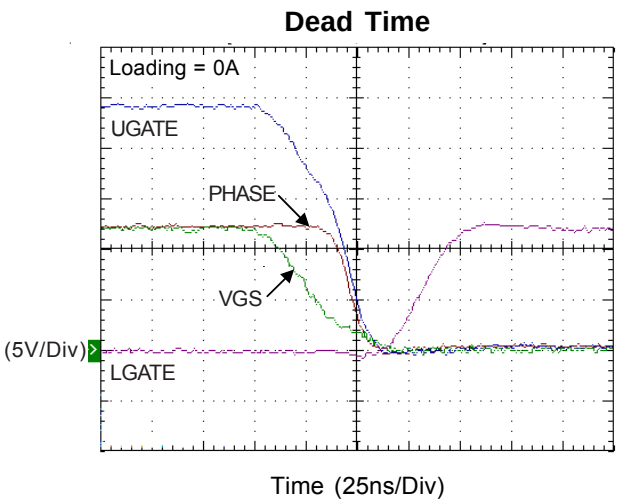
Note 3. Devices are ESD sensitive. Handling precaution recommended.

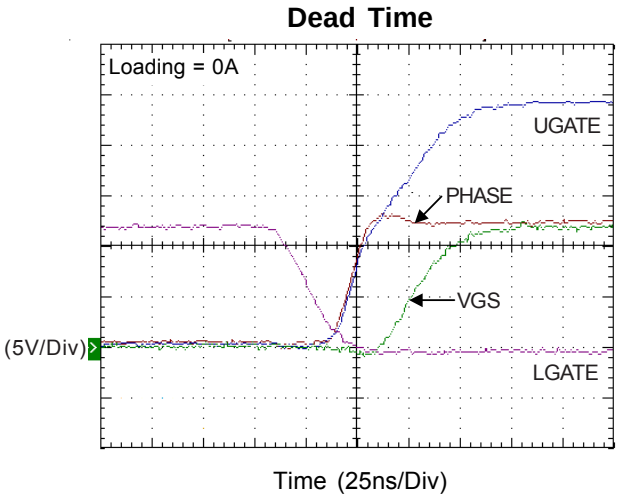
Note 4. The device is not guaranteed to function outside its operating conditions.

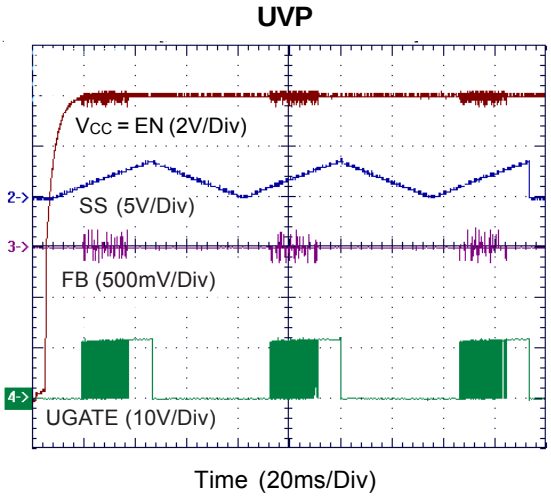
Typical Operating Characteristics

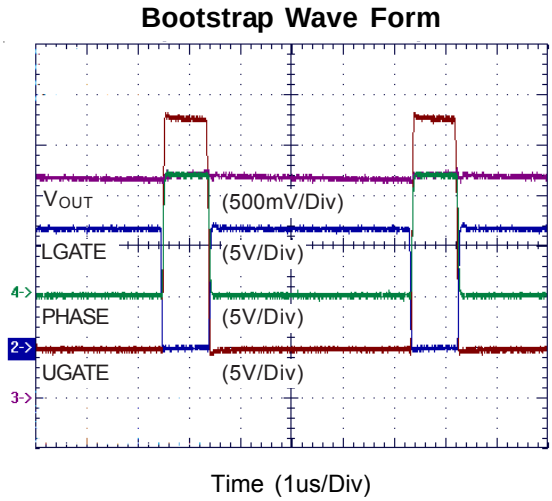




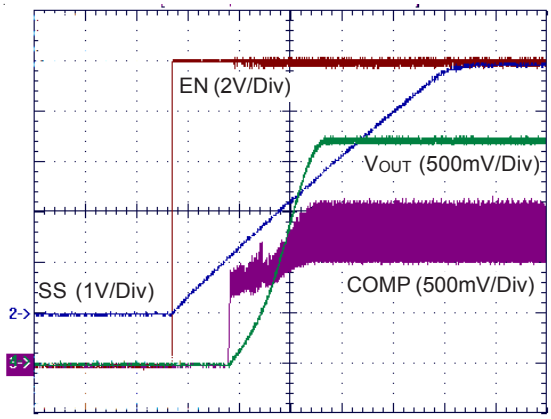






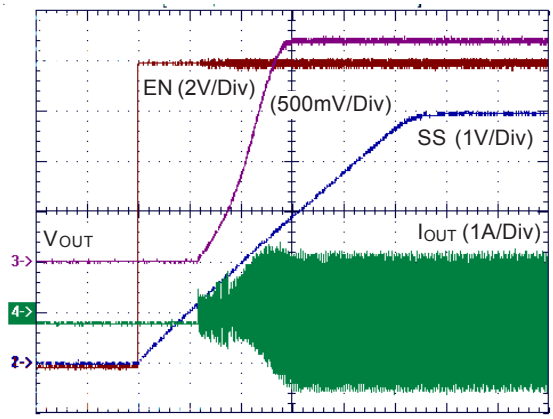


Power On



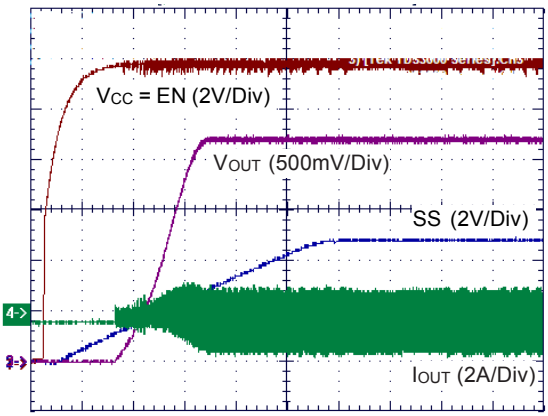
Time (10ms/Div)

Power On



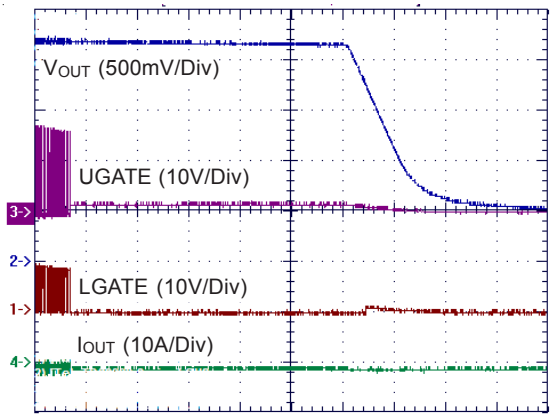
Time (10ms/Div)

Power On



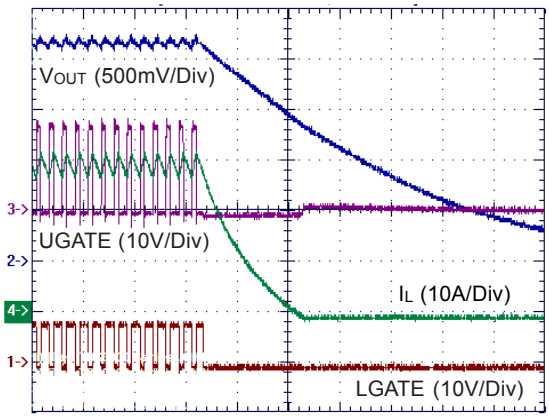
Time (10ms/Div)

Power Off



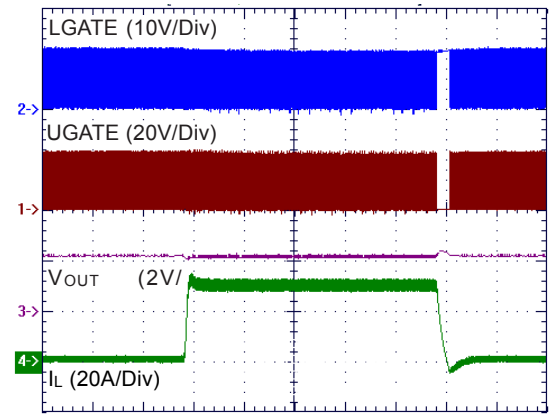
Time (10ms/Div)

Power Off



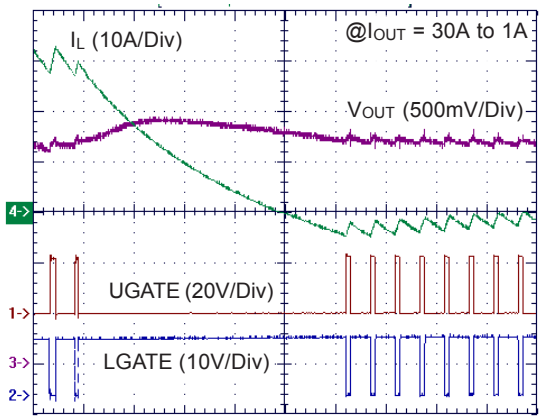
Time (20us/Div)

Load Transient Response

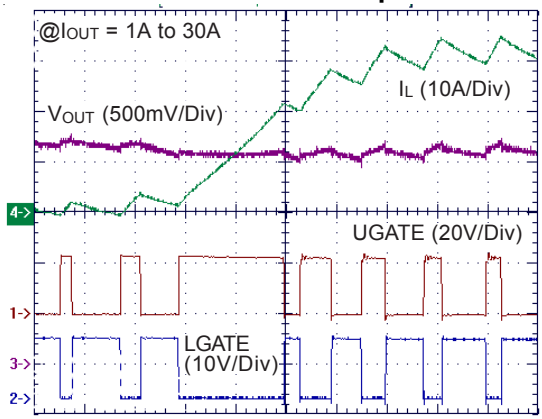


Time (200us/Div)

Load Transient Response



Load Transient Response



Application Information

The RT9232A is a single-phase synchronous buck PWM DC-DC converter controller designed to drive two N-Channel MOSFETs. It provides a highly accurate, programmable output voltage precisely regulated to low voltage requirement with an internal 0.8V ±1% reference.

Initialization

The RT9232A automatically initiates its softstart cycle only after VCC and V_{IN} power and chip enabling signals are ready. There is no special power-on sequence should be took care especially while implement the chip in. The internal Power-On Reset (POR) logic continually monitors the voltage level of input power and enabling pin; in which the IC supply power is monitored via VCC pin and input power V_{IN} is via SENSE pin. An internal current source with driving capability of 200uA causes a fixed voltage drop across the resistor connecting V_{IN} to SENSE pin. The RT9232A internal logic will deem the input voltage ready once the voltage of SENSE pin is high than 1.5V. The preferred V_{IN} ready level could be set by selecting an appropriate resistor R_{SENSE} as:

$$R_{SENSE} < \frac{V_{IN\_READY} - 1.5V}{200\mu A}\ \Omega$$

Once all voltages of VCC, SENSE, and EN pins ramp higher than the internal specific thresholds. The internal POR logic will initialize the softstart operation then. Moreover, the POR inhibits driver operation while pulling the EN pin low. Transitioning EN pin high after input supply voltages ready to initialize soft-start operation.

Soft-Start

The behavior of RT9232A Soft-Start can be simply described as shown as Figure.1 below; and the Soft-Start can be sliced to several time-frames with specific operation respectively.

T0~T1

The RT9232A initiates the softstart cycle as shown in Figure 1 when POR function is OK. An internal 10uA current source charges an external capacitor on SS pin (Css) to 5V. The softstart function produces an SSE signal that is equal to (SS-1.2V)/2. Error Amplifier (EA) and PWM comparator are triple-input devices. The non-inverting input whichever is smaller dominates the behavior of the devices. During T0~T1, since SS is smaller than the sawtooth valley, the PWM comparator outputs low no matter what the COMP voltage is.

T1~T2

During T1~T2, EA keeps COMP voltage low that makes the PWM output low.

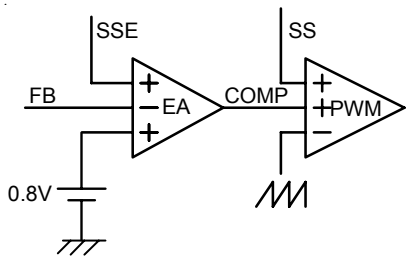
T2~T3

SSE ramps up and dominates the behavior of EA during T2~T3. EA regulates COMP appropriately so that FB ramps up along the SSE curve. The output voltage ramps up accordingly. Thus upper MOSFET turns on at a limited duty and output current overshoot can be reduced.

It is noted that lower MOSFET keeps off before the upper MOSFET starts switching. This method provides smooth start up when there is residual voltage on output capacitors. The output voltage delay time and ramp up time are calculated as Equation (1) and (2) respectively.

$$T2 - T0 = \frac{1.2V \times C_{SS}}{10uA}\ (s) \qquad (1)$$

$$T3 - T2 = \frac{1.6V \times C_{SS}}{10uA}\ (s) \qquad (2)$$



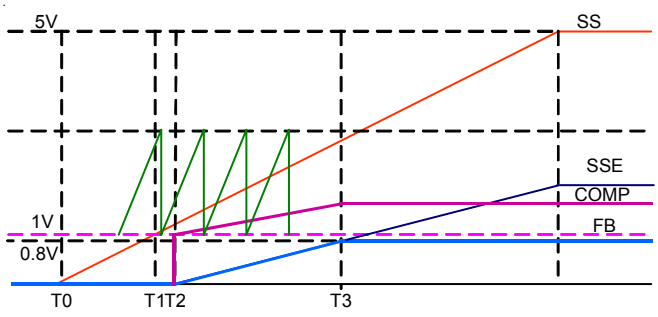


Figure 1. Timing diagram of softstart

Switching Frequency Setting

The default switching frequency is 200kHz when RT pin left open. A resistor connected (R_{RT}) from RT pin to ground increases the switching frequency as Equation (3).

$$f_{OSC} = 200kHz + \frac{2.9 \times 10^6}{R_{RT}(\Omega)} kHz \quad (3) \quad (R_{RT} \text{ to GND})$$

Conversely, connecting a pull-up resistor (R_{RT}) from RT pin reduces the switching frequency according to Equation (4)

$$f_{OSC} = 200kHz - \frac{33 \times 10^6}{R_{RT}(\Omega)} kHz \quad (4) \quad (R_{RT} \text{ to } V_{CC} = 12V)$$

Under Voltage Protection

The under voltage protection is enabled when the RT9232A is activated and SS voltage is higher than 4V. The UVP function is specified for protecting the converter from an instant output short circuit during normal operation. The RT9232A continuously monitors the output voltage by detecting the voltage on FB pin. The UVP function is triggered and initiates the hiccup cycles when output voltage lower than 75% of designated voltage with a 30us delay.

Hiccup cycle turns off both upper and lower MOSFET first. An internal 10uA current sink discharges the softstart capacitor C_{SS}. SS pin voltage ramps down linearly. When SS pin voltage touches 0V, hiccup cycle releases and normal softstart cycle takes over. When SS voltage is higher than 4V, the UVP function is enabled again. The hiccup cycle restarts if the output short event still remains. The converter is shutdown permanently after 3 times hiccup and only restarting supply voltages can enable the converter.

Note that triggering the POR function or EN will reset the hiccup counter. Make sure that VCC, EN and SENSE pin voltages are higher than their respective trip level when output short circuit occurs or the UVP function may not latch up the converter causing permanent damage to the converter.

Short Circuit Protection

There is a protection implemented in RT9232A for short circuit protection, the protection can significantly protect the power stage from burn-out while the congenital output circuit short as shown in Figure 2. The SCP will be triggered while the POR is triggered 3 times including the 1st POR of system power on. While the SCP been triggered, the fault is latched until the V_{CC} power is removed.

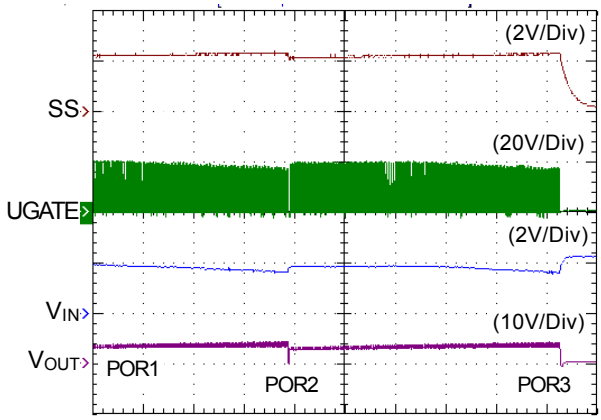


Figure 2

As shown as Figure 3. The POR of the chip could be triggered by three major signal including $5V_{BUS}$ which is applied for internal logic use only, 12V, and EN. The POR will be issued if all of the 3 events are true.

Per RT9232A implementation, the EN is one of signals will trigger SCP, and it's possible to mal-trigger SCP while a unclear EN signals being applied. The enabling circuitry should be took care specially while implementing the EN circuit.

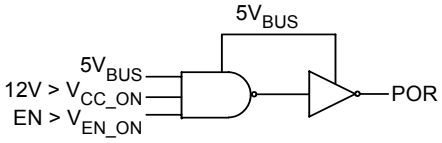


Figure 3

Component Selection

Components should be appropriately selected to ensure stable operation, fast transient response, high efficiency, minimum BOM cost and maximum reliability.

Output Inductor Selection

The selection of output inductor is based on the considerations of efficiency, output power and operating frequency. For a synchronous buck converter, the ripple current of inductor (ΔI_L) can be calculated as follows:

$$\Delta I_L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times f_{OSC} \times L} \quad (5)$$

Generally, an inductor that limits the ripple current between 20% and 50% of output current is appropriate. Make sure that the output inductor could handle the maximum output current and would not saturate over the operation temperature range.

Output Capacitor Selection

The output capacitors determine the output ripple voltage (ΔV_{OUT}) and the initial voltage drop after a high slew-rate load transient. The selection of output capacitor depends on the output ripple requirement. The output ripple voltage is described as Equation (6).

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{1}{8} \times \frac{V_{OUT}}{f_{OSC}^2 \times L \times C_{OUT}} (1 - D) \quad (6)$$

For electrolytic capacitor application, typically 90~95% of the output voltage ripple is contributed by the ESR of output capacitors. Paralleling lower ESR ceramic capacitor with the bulk capacitors could dramatically reduce the equivalent ESR and consequently the ripple voltage.

Input Capacitor Selection

Use mixed types of input bypass capacitors to control the input voltage ripple and switching voltage spike across the MOSFETs. The buck converter draws pulsewise current from the input capacitor during the on time of upper MOSFET. The RMS value of ripple current flowing through the input capacitor is described as:

$$I_{IN(RMS)} = I_{OUT} \times \sqrt{D \times (1 - D)} \quad (7)$$

The input bulk capacitor must be cable of handling this ripple current. Sometime, for higher efficiency the low ESR capacitor is necessarily. Appropriate high frequency ceramic capacitors physically near the MOSFETs effectively reduce the switching voltage spikes.

MOSFET Selection

The selection of MOSFETs is based upon the considerations of $R_{DS(ON)}$, gate driving requirements, and thermal management requirements. The power loss of upper MOSFET consists of conduction loss and switching loss and is expressed as:

$$P_{UPPER} = P_{COND\_UPPER} + P_{SW\_UPPER} \quad (8)$$

$$= I_{OUT} \times R_{DS(ON)} \times D + \frac{1}{2} I_{OUT} \times V_{IN} \times (T_{RISE} + T_{FALL}) \times f_{OSC}$$

where T_{RISE} and T_{FALL} are rising and falling time of V_{DS} of upper MOSFET respectively. $R_{DS(ON)}$ and Q_G should be simultaneously considered to minimize power loss of upper MOSFET.

The power loss of lower MOSFET consists of conduction loss, reverse recovery loss of body diode, and conduction loss of body diode and is express as:

$$P_{LOWER} = P_{COND\_LOWER} + P_{RR} + P_{DIODE} \quad (9)$$

$$= I_{OUT} \times R_{DS(ON)} \times (1 - D) + Q_{RR} \times V_{IN} \times f_{OSC}$$

$$+ \frac{1}{2} \times I_{OUT} \times V_F \times T_{DIODE} \times f_{OSC}$$

where T_{DIODE} is the conducting time of lower body diode.

Special control scheme is adopted to minimize body diode conducting time. As a result, the $R_{DS(ON)}$ loss dominates the power loss of lower MOSFET. Use MOSFET with adequate $R_{DS(ON)}$ to minimize power loss and satisfy thermal requirements.

Feedback Compensation

Figure 4 highlights the voltage-mode control loop for a synchronous buck converter. Figure 5 shows the corresponding Bode plot. The output voltage (V_{OUT}) is regulated to the reference voltage. The error amplifier EA output (COMP) is compared with the oscillator (OSC) sawtooth wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L and C_{OUT}).

The modulator transfer function is the small-signal transfer function of V_{OUT}/COMP. This function is dominated by a DC gain and the output filter (L and C_{OUT}), with a double pole break frequency at F_{P_LC} and a zero at F_{Z_ESR}. The DC gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

The break frequency F_{LC} and F_{ESR} are expressed as Equation (10) and (11) respectively.

$$F_{P\_LC} = \frac{1}{2\pi\sqrt{LC_{OUT}}} \quad (10)$$

$$F_{Z\_ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}} \quad (11)$$

The compensation network consists of the error amplifier EA and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest DC gain, the highest 0dB crossing frequency (F_C) and adequate phase margin. Typically, F_C in range 1/5~1/10 of switching frequency is adequate. The higher F_C is, the faster dynamic response is. A phase margin in the range of 45°C~ 60°C is desirable.

The equations below relate the compensation network poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 4.

$$F_{Z1} = \frac{1}{2\pi \times R2 \times C1} \quad (12)$$

$$F_{Z2} = \frac{1}{2\pi \times (R1+R3) \times C3} \quad (13)$$

$$F_{P1} = \frac{1}{2\pi \times R2 \times \frac{C1 \times C2}{C1+C2}} \quad (14)$$

$$F_{P2} = \frac{1}{2\pi \times R3 \times C3} \quad (15)$$

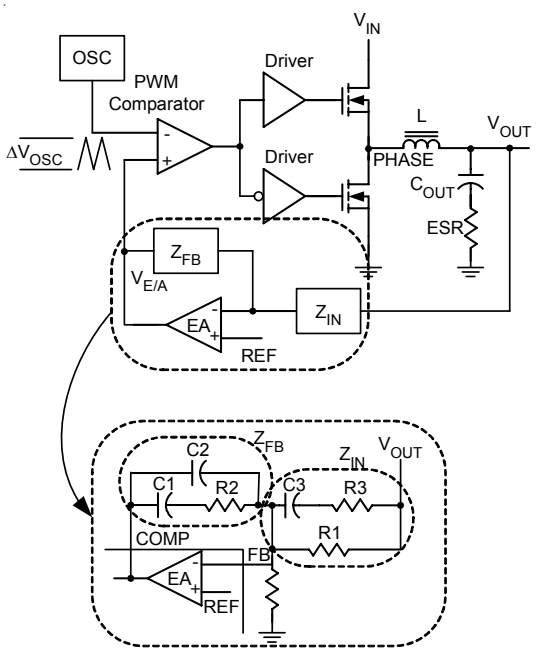


Figure 4

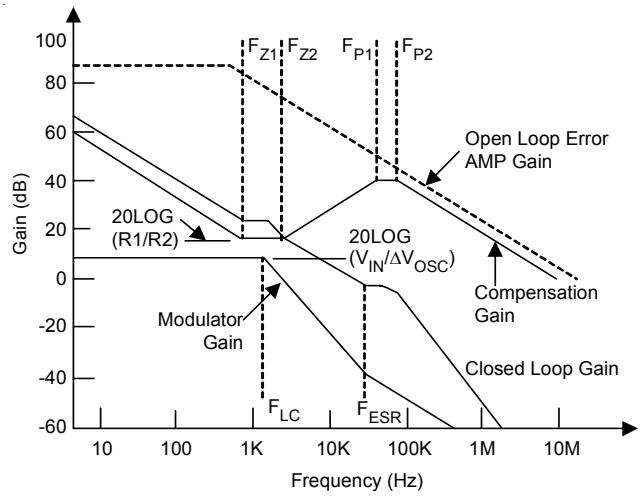


Figure 5

Feedback Loop Design Procedure

Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R2/R1) for desired 0dB crossing frequency (F_C).
2. Place 1ST zero F_{Z1} below modulator double pole F_{LC} (~75% F_{LC}).
3. Place 2ND zero F_{Z2} at modulator double pole F_{LC}.
4. Place 1ST pole F_{Z1} at the ESR zero F_{Z_ESR}
5. Place 2ND pole F_{Z2} at half the switching frequency.
6. Check gain against error amplifier's open-loop gain.
7. Pick R_{FB} for desired output voltage.
8. Estimate phase margin and repeat if necessary.

Layout Consideration

Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. First, place the PWM power stage components. Mount all the power components and connections in the top layer with wide copper areas. The MOSFETs of Buck, inductor, and output capacitor should be as close to each other as possible. This can reduce the radiation of EMI due to the high frequency current loop. If the output capacitors are placed in parallel to reduce the ESR of capacitor, equal sharing ripple current should be considered. Place the input capacitor directly to the drain

of high-side MOSFET. The MOSFETs of linear regulator should have wide pad to dissipate the heat. In multilayer PCB, use one layer as power ground and have a separate control signal ground as the reference of the all signal. To avoid the signal ground is effect by noise and have best load regulation, it should be connected to the ground terminal of output. Furthermore, follows below guidelines can get better performance of IC:

(1). The IC needs a bypassing ceramic capacitor as a R-C filter to isolate the pulse current from power stage and supply to IC, so the ceramic capacitor should be placed adjacent to the IC.

(2). Place the high frequency ceramic decoupling close to the power MOSFETs.

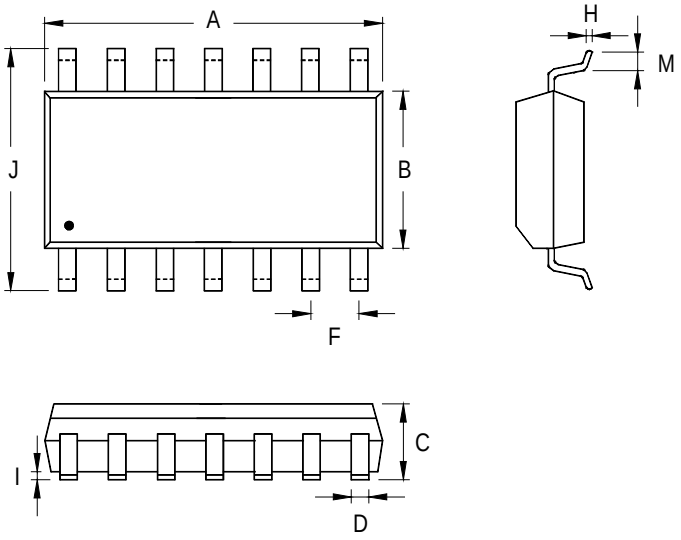
(3). The feedback part should be placed as close to IC as possible and keep away from the inductor and all noise sources.

(4). The components of bootstraps should be closed to each other and close to MOSFETs.

(5).The PCB trace from Ug and Lg of controller to MOSFETs should be as short as possible and can carry 1A peak current.

(6). Place all of the components as close to IC as possible.

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	8.534	8.738	0.336	0.344
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050

14-Lead SOP Plastic Package

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