I²C Interface PMIC with 6-Channel WLED Driver and 4-LDO

General Description

The RT9396 is a power management IC (PMIC) for backlighting and phone camera applications. The PMIC contains a 6-Channel charge pump white LED driver and four low dropout linear regulators.

The charge pump drives up to 6 white LEDs with regulated constant current for uniform intensity. Each channel (LED1 to LED6) supports up to 25mA of current. These 6-Channels can be also programmed as 4 plus 2-Channels or 5 plus 1-Channel with different current setting for auxiliary LED application. The RT9396 maintains highest efficiency by utilizing a x1/ x1.5/ x2 fractional charge pump and low dropout current regulators. An internal 6-bit DAC is used for backlight brightness control. Users can easily configure up to 64 steps of LED current via the I²C interface control.

The RT9396 also comprises low noise, low dropout regulators, which provide up to 200mA of current for each of the four channels. The four LDOs deliver 3% output accuracy and low dropout voltage of 200mV @ 200mA. Users can easily configure LDO output voltage via the I²C interface control. The LDOs also provide current limiting and over temperature functions.

The RT9396 is available in a WQFN-24L 3x3 package.

Ordering Information

RT9396□□

- Package Type
  QW : WQFN-24L 3x3 (COL) (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

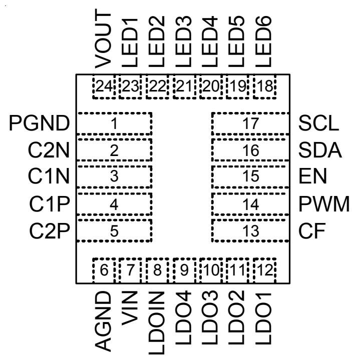
- **Tri-Mode (x1/x1.5/x2) Charge Pump**
- **Maximum 25mA x 6-Channel LED Backlighting Output Current**
- **Support Main/Sub (4+2/5+1) LED Function**
- **64 Steps Programmable LED Current**
- **Support PWM Dimming Function**
- **Fade In/Out Via I²C Control**
- **4 Low Dropout Regulators**
- **Maximum 200mA x 4-Channel LDO Output Current**
- **16-Level LDO Output Voltage Setting**
- **I²C Programmable Independent LDO Channel ON/OFF Control**
- **Over Temperature Protection**
- **Thin 24-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- Cellular Phones
- PDAs and Smart Phones

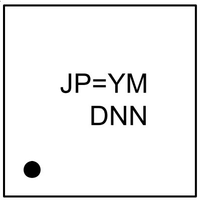
Pin Configurations

(TOP VIEW)



WQFN-24L 3x3 (COL)

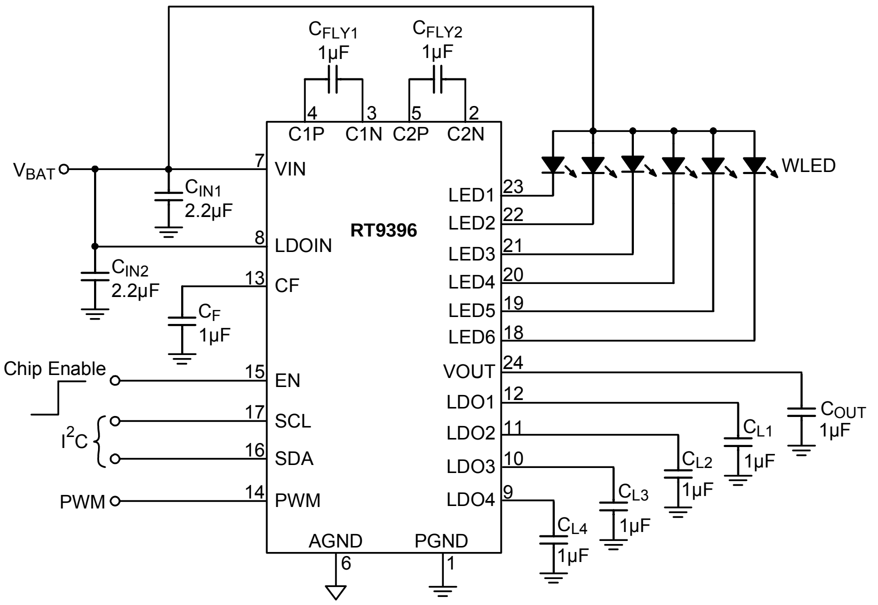
Marking Information



JP= : Product Code

YMDNN : Date Code

Typical Application Circuit



Timing Diagram

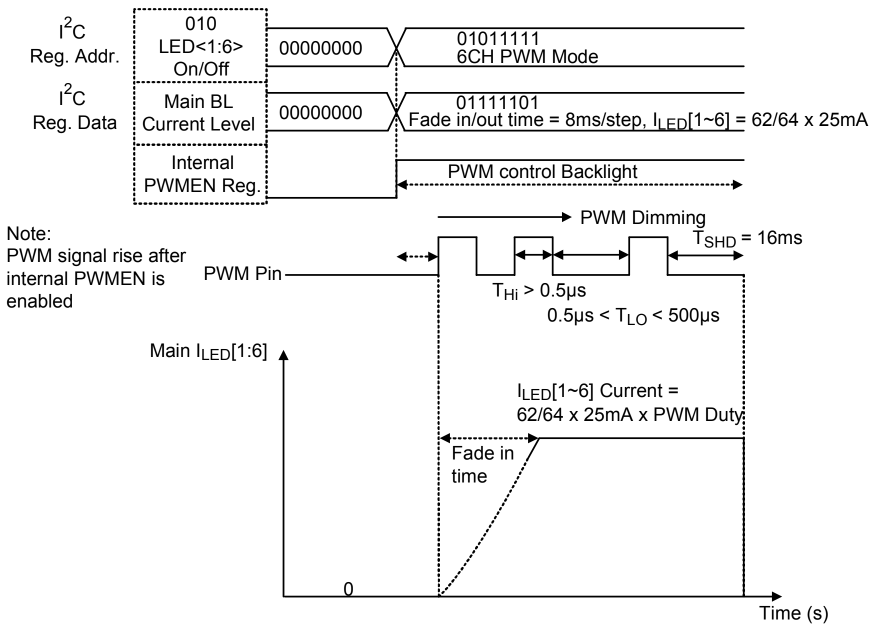


Figure 1. Timing Diagram

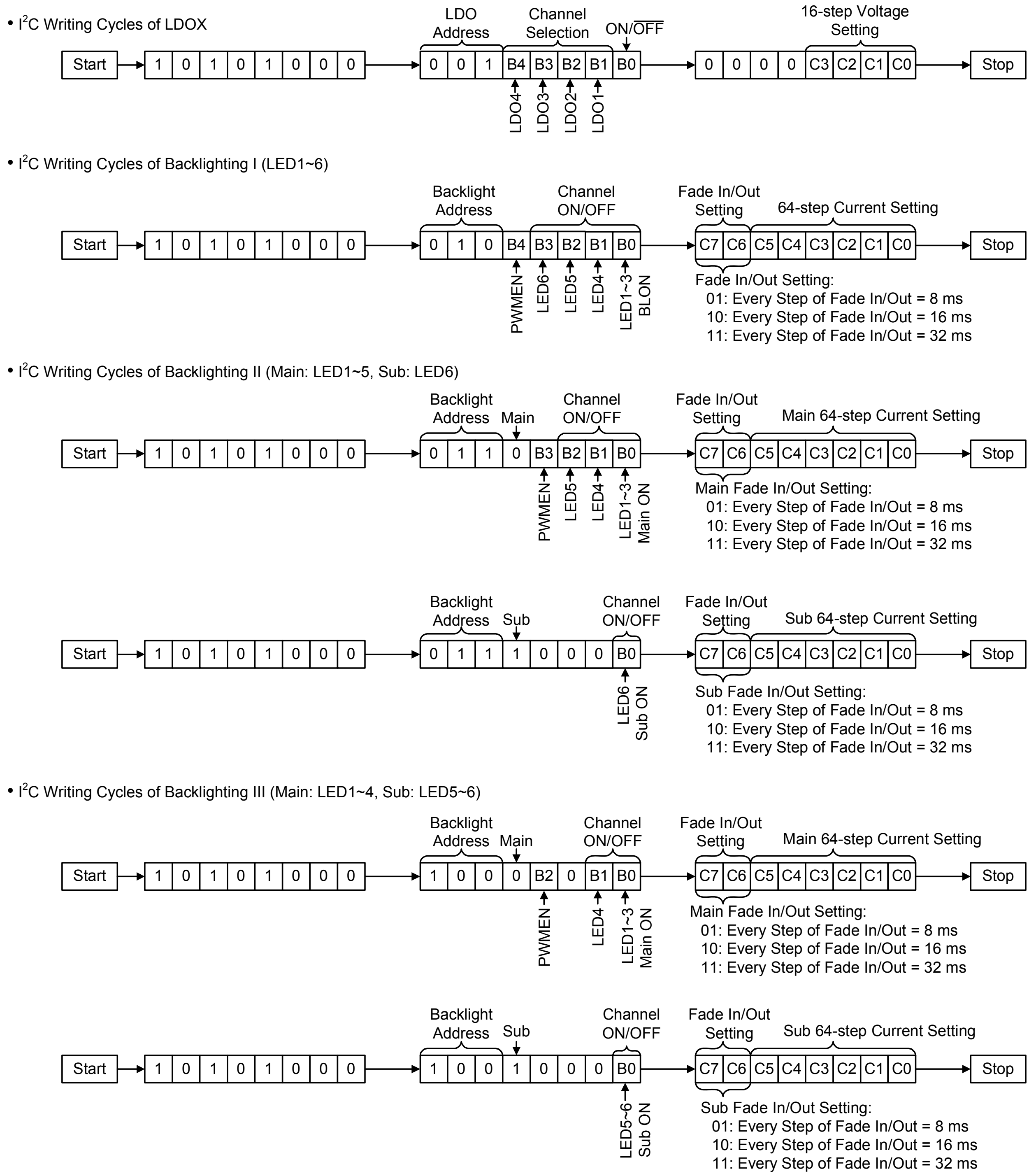


Figure 2. Control Sequences of LDO Setting and LED Dimming

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PGND	Charge Pump Ground.
2	C2N	Fly Capacitor 2 Negative Connection.
3	C1N	Fly Capacitor 1 Negative Connection.
4	C1P	Fly Capacitor 1 Positive Connection.
5	C2P	Fly Capacitor 2 Positive Connection.
6	AGND	Ground for LDO1 to LDO4.
7	VIN	Charge Pump Power Input. Connect this pin to LDOIN pin.
8	LDOIN	LDO Power Input. Connect this pin to VIN pin.
9	LDO4	LDO4 Output.
10	LDO3	LDO3 Output.
11	LDO2	LDO2 Output.
12	LDO1	LDO1 Output.
13	CF	PWM Filter Capacitor Connection.
14	PWM	PWM Dimming Control Input.
15	EN	Chip Enable (Active High).
16	SDA	I^2C Data Input.
17	SCL	I^2C Clock Input.
18	LED6	Current Sink for LED6.
19	LED5	Current Sink for LED5.
20	LED4	Current Sink for LED4.
21	LED3	Current Sink for LED3.
22	LED2	Current Sink for LED2.
23	LED1	Current Sink for LED1.
24	VOUT	Charge Pump Output. Connect a 1μF ceramic capacitor between VOUT and GND.

Function Block Diagram

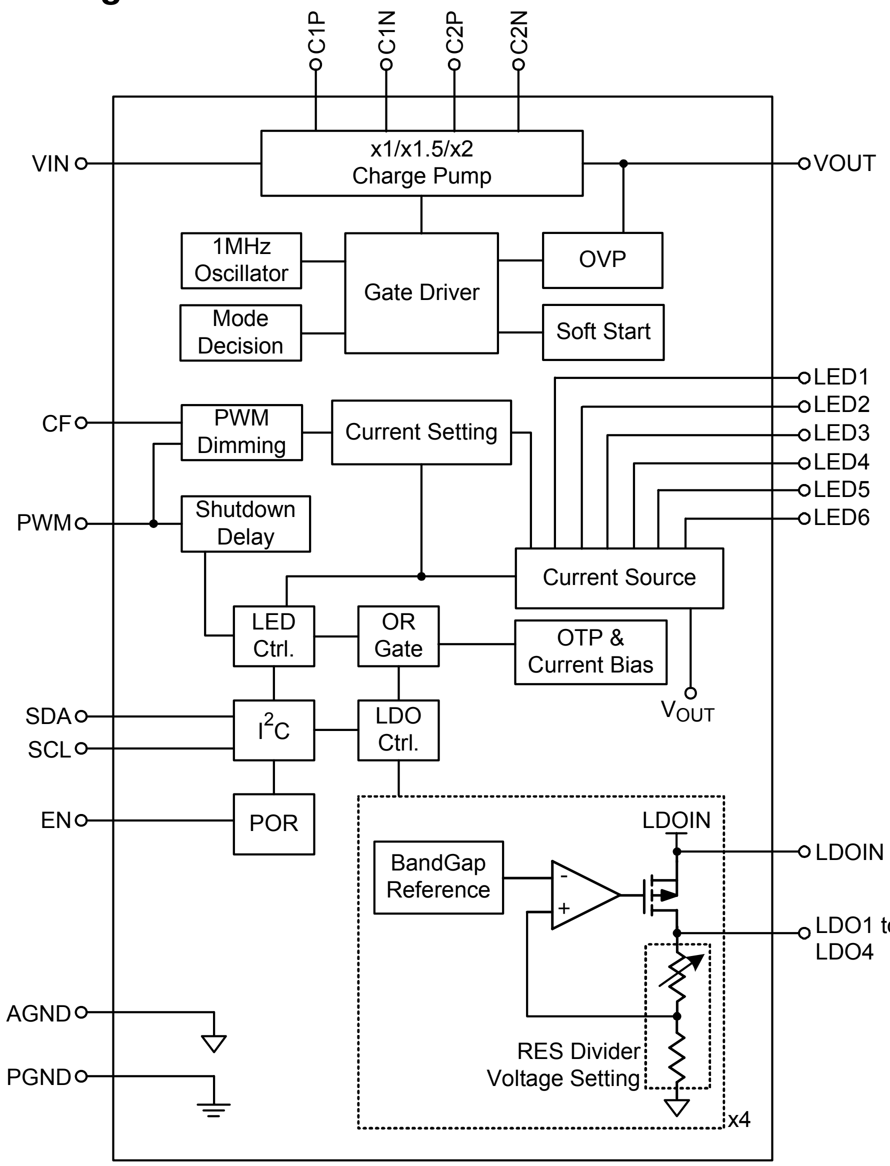


Table 1. 16-Step LDO Output Voltage Setting

C3	C2	C1	C0	LDO1 & LDO2 Output Voltage (V)	LDO3 & LDO4 Output Voltage (V)
0	0	0	0	1	1.1
0	0	0	1	1.1	1.2
0	0	1	0	1.2	1.4
0	0	1	1	1.3	1.7
0	1	0	0	1.5	1.8
0	1	0	1	1.6	1.9
0	1	1	0	1.8	2
0	1	1	1	2.1	2.1

C3	C2	C1	C0	LDO1 & LDO2 Output Voltage (V)	LDO3 & LDO4 Output Voltage (V)
1	0	0	0	2.5	2.2
1	0	0	1	2.6	2.3
1	0	1	0	2.7	2.4
1	0	1	1	2.8	2.5
1	1	0	0	2.9	2.8
1	1	0	1	3	2.85
1	1	1	0	3.1	3.2
1	1	1	1	3.3	3.3

Table 2. 64-Step WLED Current Setting

C5	C4	C3	C2	C1	C0	WLED Current (mA)
0	0	0	0	0	0	0.39
0	0	0	0	0	1	0.78
0	0	0	0	1	0	1.17
0	0	0	0	1	1	1.56
0	0	0	1	0	0	1.95
0	0	0	1	0	1	2.34
0	0	0	1	1	0	2.73
0	0	0	1	1	1	3.13
0	0	1	0	0	0	3.52
0	0	1	0	0	1	3.91
0	0	1	0	1	0	4.3
0	0	1	0	1	1	4.69
0	0	1	1	0	0	5.08
0	0	1	1	0	1	5.47
0	0	1	1	1	0	5.86
0	0	1	1	1	1	6.25
0	1	0	0	0	0	6.64
0	1	0	0	0	1	7.03
0	1	0	0	1	0	7.42
0	1	0	0	1	1	7.81
0	1	0	1	0	0	8.2
0	1	0	1	0	1	8.59
0	1	0	1	1	0	8.98
0	1	0	1	1	1	9.38
0	1	1	0	0	0	9.77
0	1	1	0	0	1	10.16
0	1	1	0	1	0	10.55
0	1	1	0	1	1	10.94
0	1	1	1	0	0	11.33
0	1	1	1	0	1	11.72
0	1	1	1	1	0	12.11
0	1	1	1	1	1	12.5

C5	C4	C3	C2	C1	C0	WLED Current (mA)
1	0	0	0	0	0	12.89
1	0	0	0	0	1	13.28
1	0	0	0	1	1	14.06
1	0	0	1	0	0	14.45
1	0	0	1	0	1	14.84
1	0	0	1	1	0	15.23
1	0	0	1	1	1	15.63
1	0	1	0	0	0	16.02
1	0	1	0	0	1	16.41
1	0	1	0	1	0	16.8
1	0	1	0	1	1	17.19
1	0	1	1	0	0	17.58
1	0	1	1	0	1	17.97
1	0	1	1	1	0	18.36
1	0	1	1	1	1	18.75
1	1	0	0	0	0	19.14
1	1	0	0	0	1	19.53
1	1	0	0	1	0	19.92
1	1	0	0	1	1	20.31
1	1	0	1	0	0	20.7
1	1	0	1	0	1	21.09
1	1	0	1	1	0	21.48
1	1	0	1	1	1	21.88
1	1	1	0	0	0	22.27
1	1	1	0	0	1	22.66
1	1	1	0	1	0	23.05
1	1	1	0	1	1	23.44
1	1	1	1	0	0	23.83
1	1	1	1	0	1	24.22
1	1	1	1	1	0	24.61
1	1	1	1	1	1	25

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- –0.3V to 6V
- Output Voltage, V_{OUT} ---------- –6V to 0.3V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-24L 3x3 ---------- 1.667W
- Package Thermal Resistance (Note 2)
  WQFN-24L 3x3, θ_{JA} ---------- 60°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN}, V_{LDOIN} ---------- 2.8V to 5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = V_{LDOIN} = 3.6V, C_{IN} = 2.2μF, C_{OUT} = 1μF, C_{FLY1} = C_{FLY2} = 1μF, V_F = 3.5V, I_{LEDx} = 25mA, T_A = 25°C, unless otherwise specification)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Supply						
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} Rising.	1.8	2.1	2.5	V
Under-Voltage Lockout Hysteresis	ΔV_{UVLO}		--	200	--	mV
Quiescent of x1 Mode	I_{Q_x1}	x1 Mode, V_{IN} = 5V, No Load, LDO[1:4] OFF	--	1	2	mA
Quiescent of x2 Mode	I_{Q_x2}	x2 Mode, V_{IN} = 3.5V, No Load, LDO[1:4] OFF	--	3.5	5	mA
Shutdown Current	I_{SHDN}	V_{IN} = 5V, V_{EN} = 0V	--	0.5	1	μA
Charge Pump WLED Driver						
Backlight I_{LEDx} Accuracy			–5	0	5	%
Backlight Current Matching			–3	0	3	%
Dropout Voltage			--	70	--	mV
Charge Pump						
Oscillator Frequency			--	1000	--	kHz
x1 Mode to x1.5 Mode Transition Voltage (V_{IN} falling)		V_f = 3.5V, I_{OUT} = 150mA	--	3.6	3.75	V
Mode Transition Hysteresis		V_f = 3.5V, I_{OUT} = 150mA	--	250	--	mV
Over Voltage Protection		V_{IN} = 4.5V	5.2	5.5	5.8	V

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
LDO1 to LDO4							
Input Voltage			V_{IN} = 2.8V to 5V	2.8	--	5	V
Dropout Voltage			$V_{IN} \geq 2.8V$, I_{OUT} = 200mA	--	--	200	mV
Output voltage Range			By I^2C Setting	1.1	--	3.3	V
VOUT Accuracy			I_{OUT} = 1mA	–3		3	%
Line Regulation			V_{IN} = (V_{OUT} + 0.3V) to 5V or V_{IN} > 2.5V, whichever is larger	--	--	0.2	%/V
Load Regulation			1mA < I_{OUT} < 200mA	--	--	0.6	%
Current Limit		I_{LIM}	R_{LOAD} = 1Ω	230	350	600	mA
Quiescent Current		I_Q	4-Channel All Turn On	--	140	200	μA
Shutdown Current		I_{SHDN}		--	--	1	μA
Thermal Shutdown		T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	20	--	°C
I^2C interface							
EN, SDA,SCL Pull Low Current		I_{EN}		--	5	10	μA
EN, SDA, SCL Threshold Voltage	Logic-High	V_{IH}		1.4	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	V
SDA Output Low Voltage		V_{CL}		--	--	0.4	V
SCL Clock Frequency		f_{SCL}		--	--	400	kHz
SCL Clock Low Period		t_{Low}		1.3	--	--	μs
SCL Clock High Period		t_{High}		0.6	--	--	μs
Hold Time START Condition		t_{HD_STR}		0.6	--	--	μs
Setup Time for Repeat START		t_{SU_STR}		0.6	--	--	μs
SDA Data Setup Time		t_{SU_DAT}		100	--	--	ns
SDA Data HOLD Time		t_{HD_DAT}		0.05	--	0.9	μs
Setup Time for STOP Condition		t_{SU_STO}		0.6	--	--	μs
Bus Free Time Between STOP and START Condition		t_{BUF}		1.3	--	--	μs
PWM Dimming Control							
PWM Dimming Frequency				1	--	200	kHz
PWM Dimming High Time				0.5	--	--	μs
PWM Dimming Low Time				0.5	--	500	μs
Shutdown Delay				16	--	--	ms

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard.

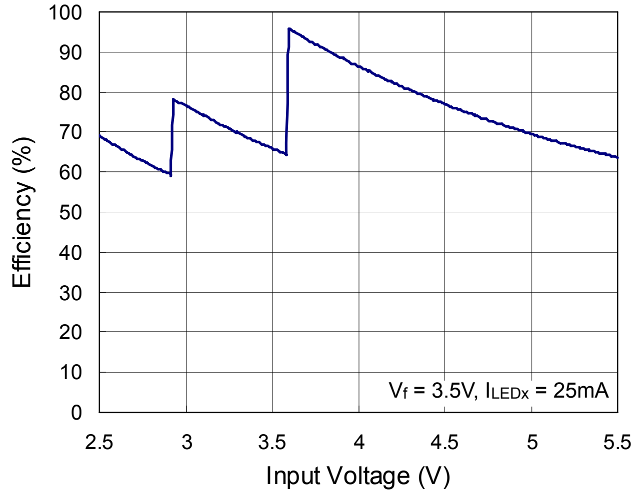
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

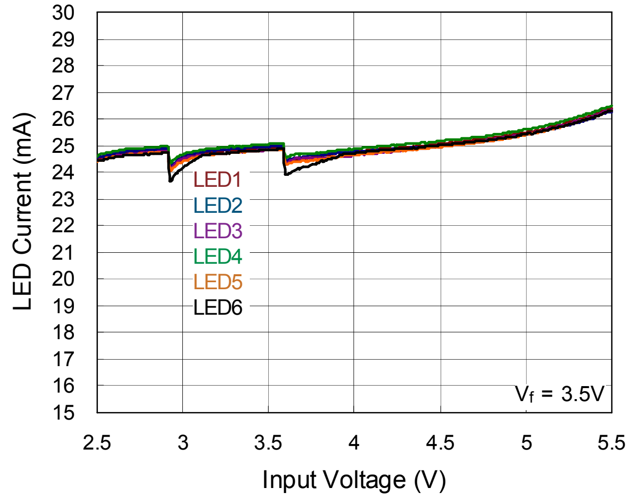
Typical Operating Characteristics

For Charge Pump

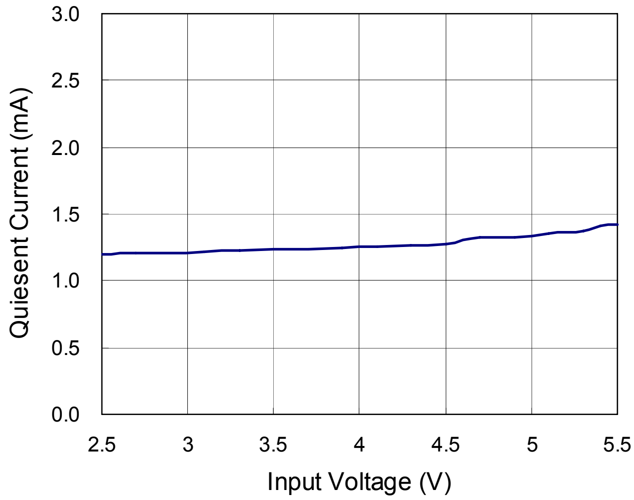
Efficiency vs. Input Voltage



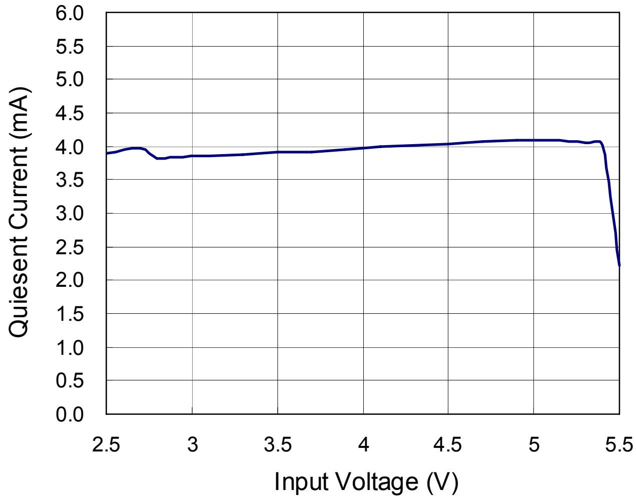
LED Current vs. Input Voltage



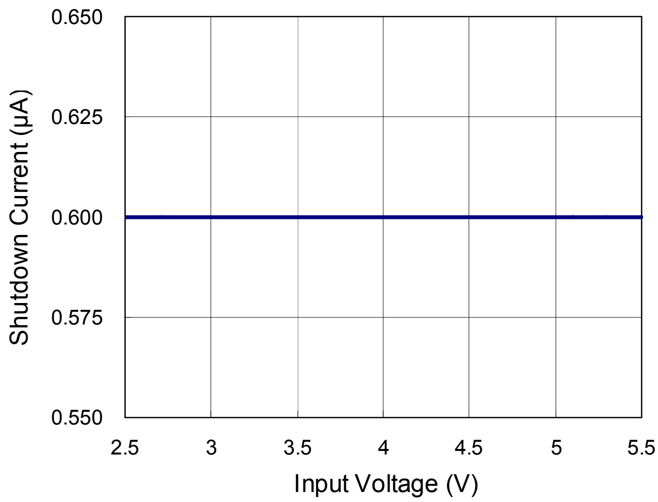
x1 Mode Quiescent Current vs. Input Voltage



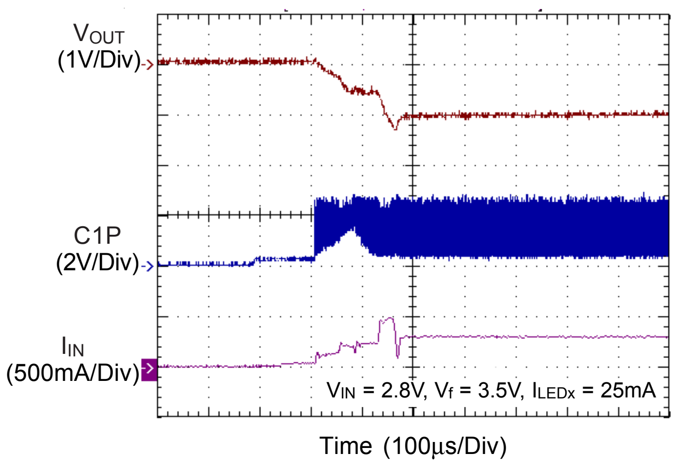
x2 Mode Quiescent Current vs. Input Voltage



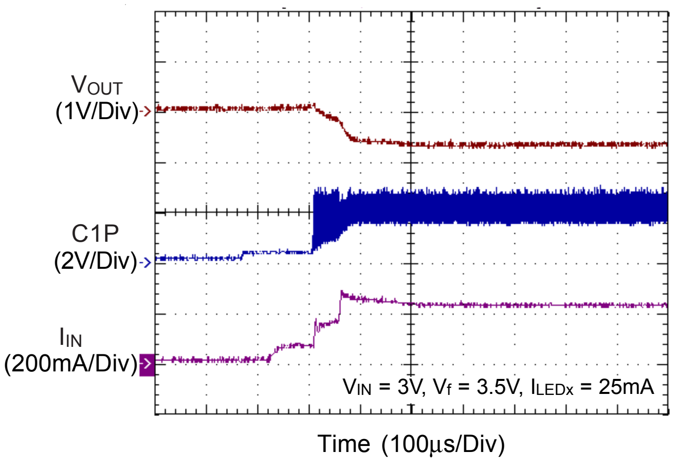
Shutdown Current vs. Input Voltage



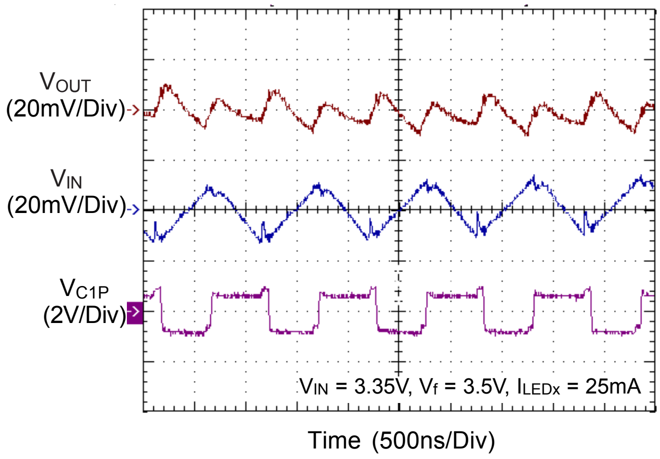
x2 Mode Inrush Current Response



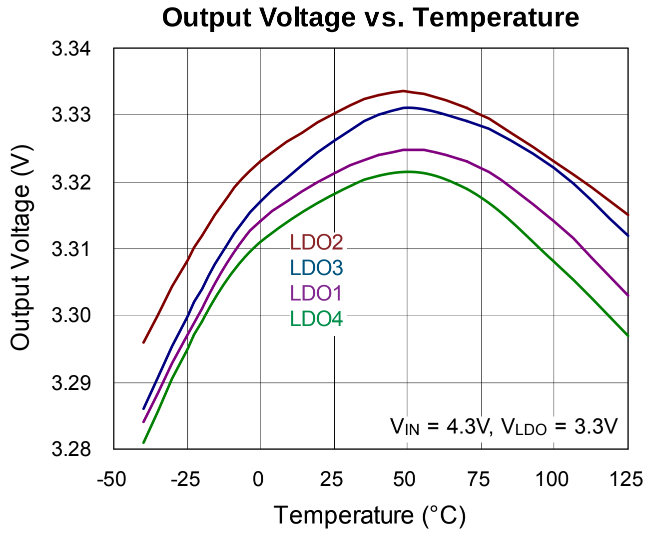
x1.5 Mode Inrush Current Response

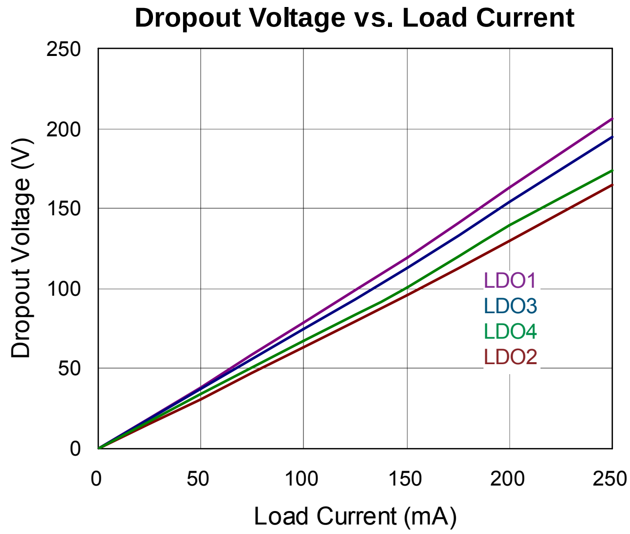


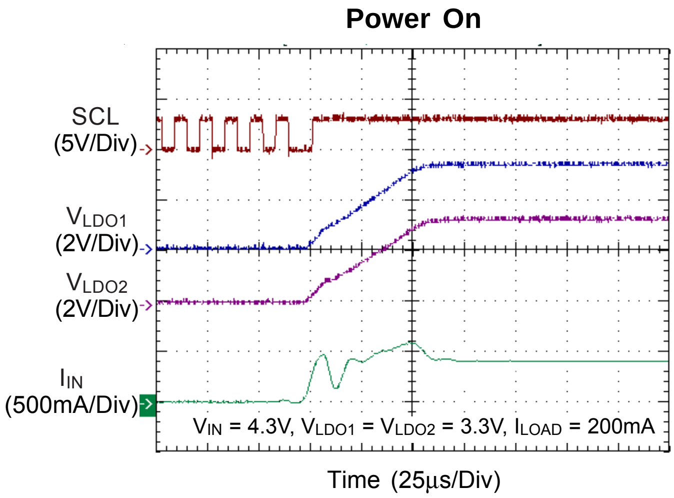
Ripple & Spike

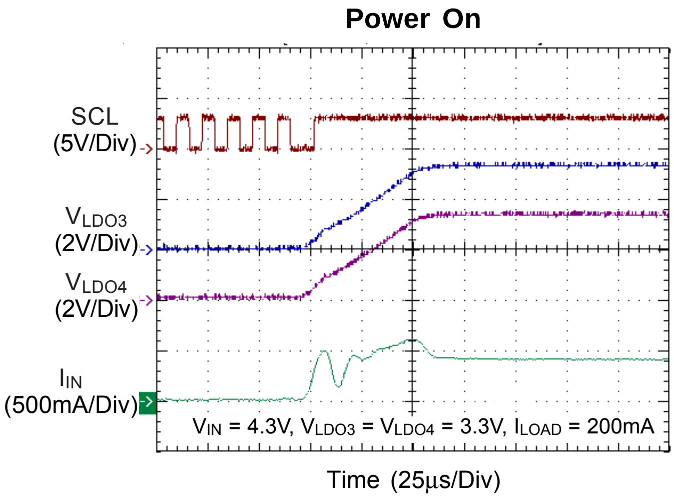


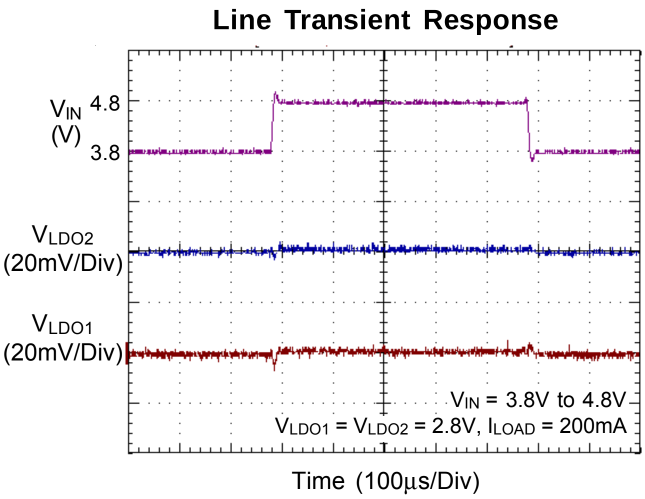
For LDO

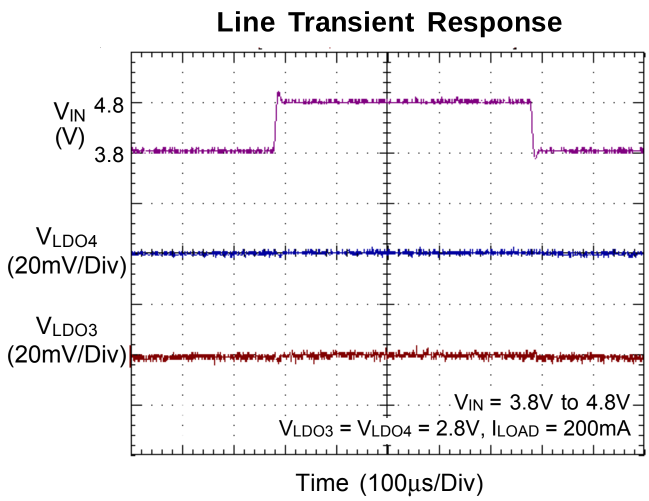

Output Voltage vs. Temperature
Output Voltage (V)
Temperature (°C)
LDO2
LDO3
LDO1
LDO4
VIN = 4.3V, VLDO = 3.3V


Dropout Voltage vs. Load Current
Dropout Voltage (V)
Load Current (mA)
LDO1
LDO3
LDO4
LDO2

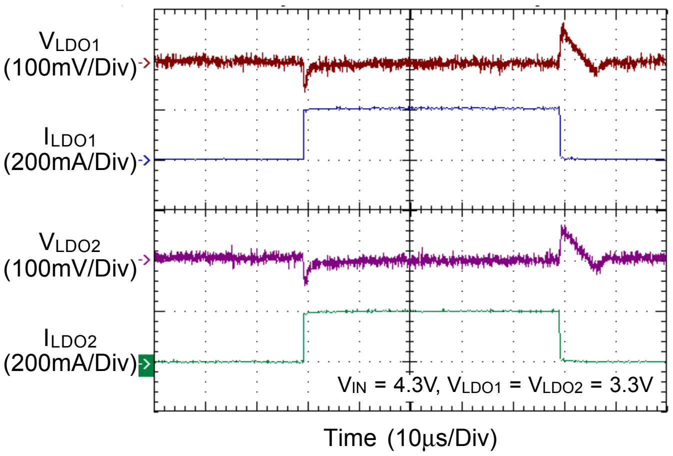

Power On
SCL (5V/Div)
VLDO1 (2V/Div)
VLDO2 (2V/Div)
IIN (500mA/Div)
VIN = 4.3V, VLDO1 = VLDO2 = 3.3V, ILOAD = 200mA
Time (25μs/Div)


Power On
SCL (5V/Div)
VLDO3 (2V/Div)
VLDO4 (2V/Div)
IIN (500mA/Div)
VIN = 4.3V, VLDO3 = VLDO4 = 3.3V, ILOAD = 200mA
Time (25μs/Div)

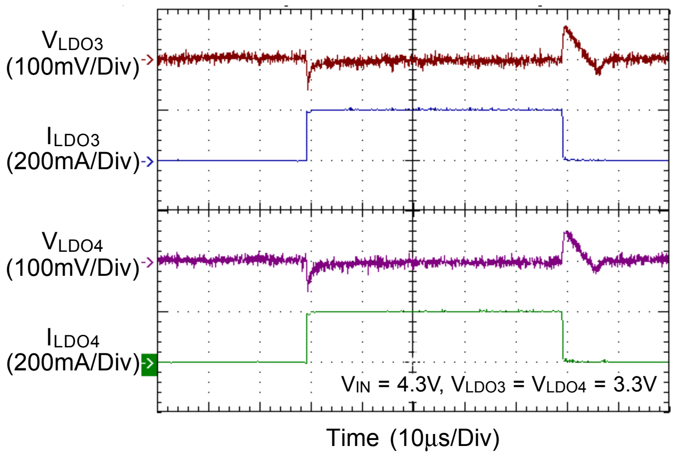

Line Transient Response
VIN (V)
4.8
3.8
VLDO2 (20mV/Div)
VLDO1 (20mV/Div)
VIN = 3.8V to 4.8V
VLDO1 = VLDO2 = 2.8V, ILOAD = 200mA
Time (100μs/Div)


Line Transient Response
VIN (V)
4.8
3.8
VLDO4 (20mV/Div)
VLDO3 (20mV/Div)
VIN = 3.8V to 4.8V
VLDO3 = VLDO4 = 2.8V, ILOAD = 200mA
Time (100μs/Div)

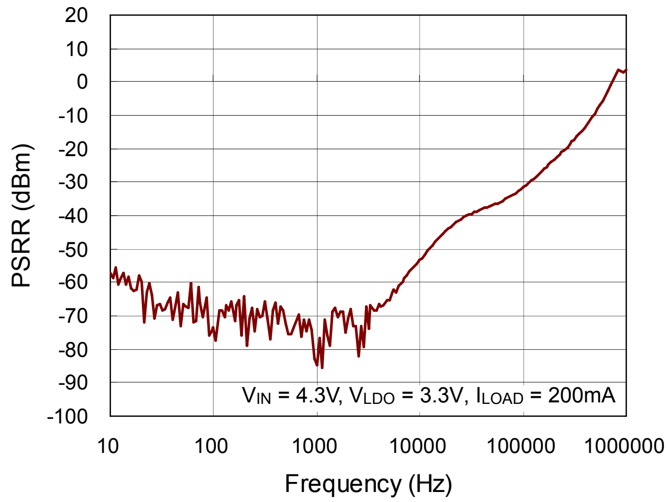
Load Transient Response



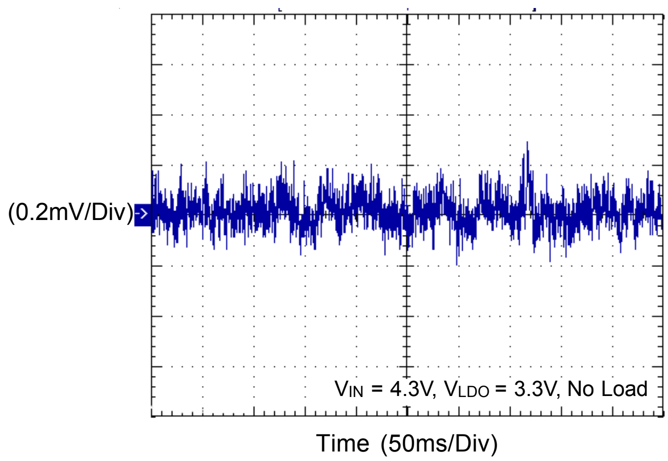
Load Transient Response



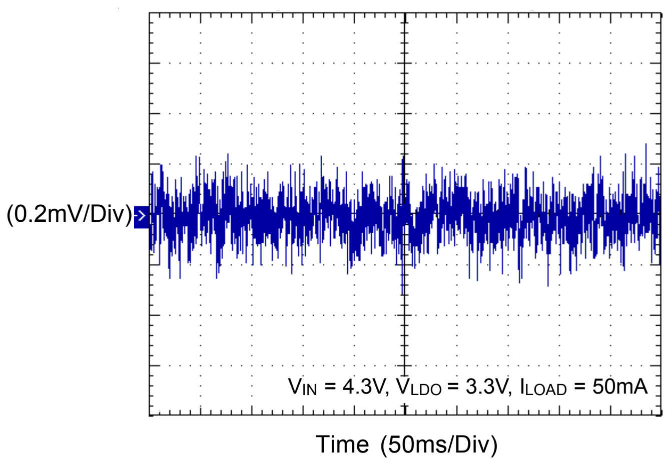
PSRR



Noise



Noise



Applications Information

The RT9396 is an I^{2}C interface PMIC with one 6-Channel charge pump white LED driver and four LDOs. The charge pump provides 6-Channel low dropout voltage current source to regulate up to 6 white LEDs. For high efficiency, the RT9396 implements a smart mode transition for charge pump operation. The four LDOs are capable of delivering low dropout voltage of 200mV @ 200mA with 3% output accuracy. The I^{2}C dimming function allows for a 64 steps LED brightness control and 16 steps LDO voltage control.

Input UVLO

An under voltage lockout (UVLO) function is provided to prevent unstable occurrences during start-up. The UVLO threshold is set at an input rising voltage of 2.1V typically with a hysteresis of 0.2V. The input operating voltage range of the RT9396 is from 2.8V to 5V. An input capacitor should be placed near the VIN pin to reduce ripple voltage. It is recommended to use a ceramic 2.2µF or larger capacitance as the input capacitor.

Soft-Start

The RT9396 includes a soft-start circuit to limit the inrush current at power on and mode switching. The soft-start circuit limits the input current before the output voltage reaches a desired voltage level.

Mode Decision

The RT9396 uses a smart mode decision method to choose the working mode for maximum efficiency. The charge pump can operate at x1, x1.5 or x2 mode. The mode decision circuit senses the output voltage and LED voltage to determine the optimum working mode.

Power Sequence

In order to assure normal operating condition, the input voltage and EN should be active before the RT9396 receives the I^{2}C signal, as shown in Figure 3. The RT9396 can be shut down by pulling EN low. When EN is reset, the I^{2}C signal also needs to be re-applied to resume normal operating condition.

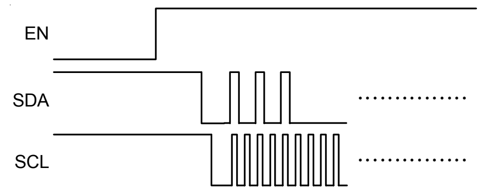


Figure 3. The Power Sequence

I^{2}C Compatible Interface

Figure 4 shows the timing diagram of the I2C interface. The RT9396 communicates with a host (master) using the standard I^{2}C 2-wire interface. The two bus lines of SCL and SDA must be pulled high when the bus is not in use. Internal pull-up resistors are installed. After the START condition, the I^{2}C master sends 8-bits data, consisting of seven address bits and a following data direction bit (R/W). The RT9396 address is 1010100 (54h) and is a receive-only (slave) device. The second word selects the register to which the data will be written. The third word contains data to write to the selected register.

Figure 2 shows the writing information for voltage of the four LDOs and current of the six LEDs. In the second word, the sub-address of the four LDOs is "001" and the sub-address of the LED Driver for different dimming modes are respectively "010", "011" and "100". For the LDO output voltage setting, bits B1 to B4 represent each LDO channel respectively where a "1" indicates selected and a "0" means not selected. The B0 bit controls on/off (1/0) mode for the selected LDO channel(s). Then, in the third word, bits C0 to C3 control a 16-step setting of LDO1 to LDO4. The voltage values are listed in Table 1.

For LED dimming, there are three operating modes (Backlight I, Backlight II and Backlight III) to select from by writing respectively "010", "011" and "100" into the first three bits of the second word. When Backlight I is selected, all six LEDs have the same behavior. Their 64-step dimming currents are set by bits C0 to C5, which are listed in Table 2. The bits C6 and C7 determine the fade in/out time of each step as shown in Figure 2. For Backlight II and Backlight III, two sets of LEDs, called main and Sub, can work separately and turn on solely. It should be noticed that no matter which mode is selected, the B0 bit must be a "1" in order for te LEDs in the main set to be turned on.

In Backlight II, the main set consists of LED1 to LED5 and LED6 is the Sub set. In Backlight III, the main set consists of LED1 to LED4, while the Sub set comprises of LED5 and LED6. The RT9396 has another dimming function called PWM dimming, which can be enabled by selecting the B4 bit in Backlight I, B3 bit in Backlight II, and B2 bit in Backlight III. Once the function is enabled, a PWM signal is applied to the PWM pin to perform PWM dimming. The LED current value is the current value set by C0 to C5 multiplied by the duty cycle. It is important to note that the PWM dimming function applies only to the main set.

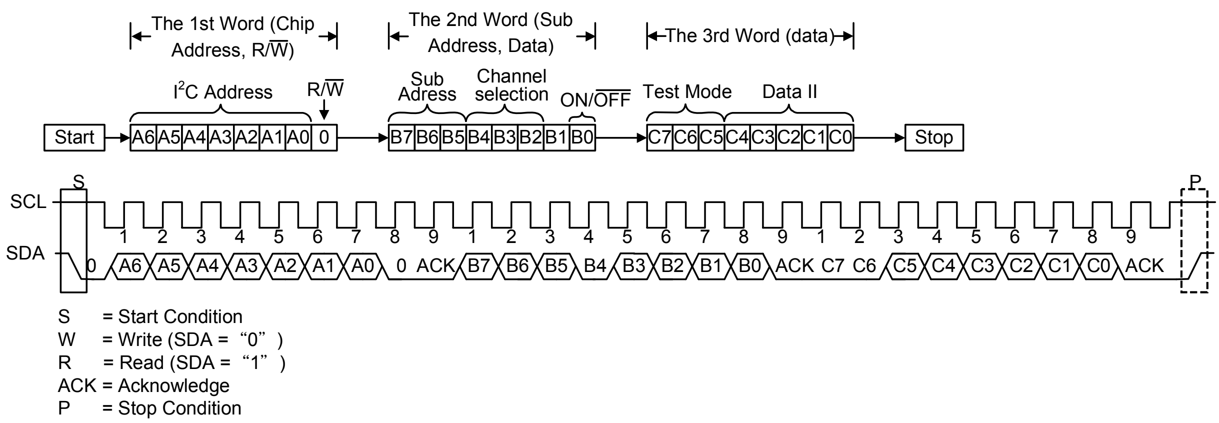


Figure 4. I²C Communication Sequence

Flying Capacitors Selection

To attain better performance of the RT9396, the selection of peripherally appropriate capacitor and value is very important. These capacitors determine some parameters such as input/output ripple voltage, power efficiency and maximum supply current by charge pump. To reduce the input and output ripple effectively, low ESR ceramic capacitors are recommended. For LED driver applications, the input voltage ripple is more important than the output voltage ripple. The input ripple is influenced by the input capacitor, C_{IN}. Increasing the input capacitance can further reduce the ripple. The flying capacitors ,C_{FLY1} and C_{FLY2} determine the supply current capability of the charge pump, which in turn influences the overall efficiency of the system. A lower capacitance will improve efficiency, but it will limit the LED's current at low input voltage. For a 6 x 25mA load over the entire input voltage range of 2.8V to 5V, it is recommended to use a 1μF ceramic capacitor for C_{FLY1}, C_{FLY2} and C_{OUT}.

LDO Capacitor Selection

Like for any low dropout regulator, the external capacitors used for the RT9396 must be carefully selected for regulator stability and performance. A capacitor with capacitance larger than 1μF is placed close to the RT9396 supply input to reduce ripple. The value of this capacitor can be increased without limit. The input capacitor must be located at a distance of not more than 0.5 inch away from the input pin of the IC and tied to a clean analog ground. Any good quality ceramic or tantalum capacitor can meet the requirement. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR power supply rejection ratio and line-transient response. The output capacitor must meet minimum requirement for both capacitance and ESR in all LDO's applications. For stability consideration, a ceramic capacitor with minimum capacitance of 1μF and minimum ESR of 20mΩ is recommended for the output capacitor. For space-saving and performance consideration, the RT9396 is designed to work with ceramic capacitor of low ESR. However, because of it's wide ESR range tolerance, the RT9396 can work stably with output capacitor of other types as well. Figure 5 shows the stable region for various load current and output capacitor conditions. Large output capacitance can reduce noise and improve load transient response, stability, and PSRR. The capacitor must be located at a distance not more than 0.5 inch away from the VOUT pin and tied to a clean analog ground.

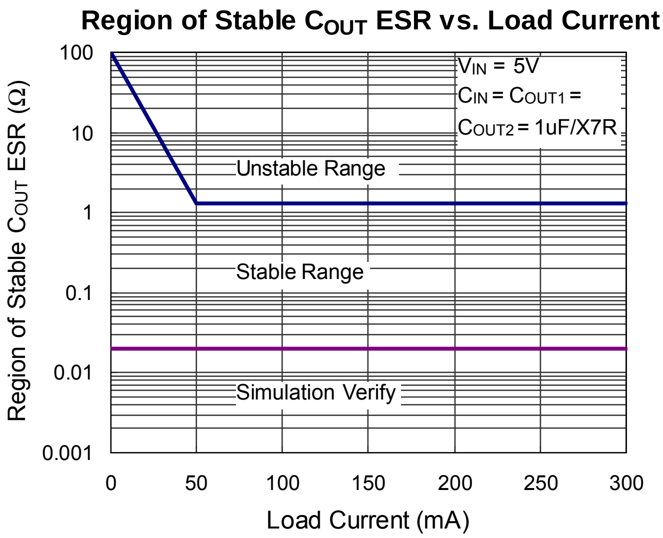


Figure 5. Stable C_{OUT} ESR Range

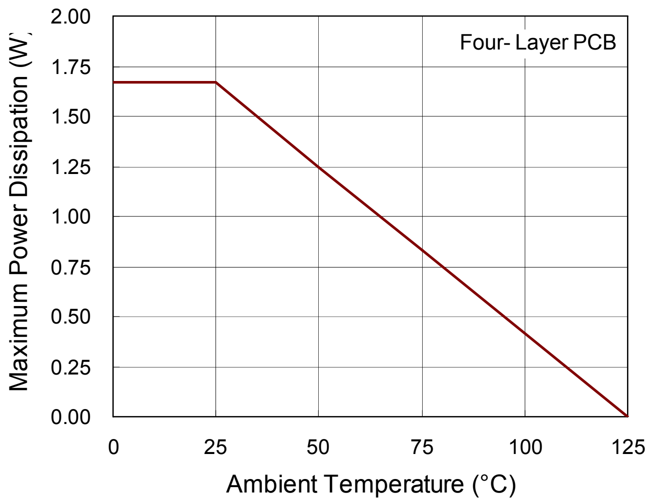


Figure 6. Derating Curve for RT9396 Package

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, rate of surrounding airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following the formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of the RT9396, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WQFN-24L 3x3 package, the thermal resistance θ_{JA} is 60°C/W on the standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (60°C/W) = 1.667W for WQFN-24L 3x3 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT9396 package, the derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

Layout Considerations

The RT9396 is a high-frequency switched-capacitor converter. For best performance, careful PCB layout is necessary. Place all peripheral components as close as possible to the IC. Place C_{IN1}, C_{IN2}, C_{OUT}, C_{L1}, C_{L2}, C_{L3}, C_{L4}, C_{FLY1}, and C_{FLY2} near to VIN, LDOIN, VOUT, LDO1, LDO2, LDO3, LDO4, C1P, C1N, C2P, C2N, and GND pin respectively. A short connection is highly recommended. The following guidelines should be strictly followed when designing a PCB layout for the RT9396.

- The exposed GND pad must be soldered to a large ground plane for heat sinking and noise prevention. The through-hole vias located at the exposed pad is connected to the ground plane of internal layer.
- VIN traces should be wide enough to minimize inductance and handle high currents. The trace running from the battery to the IC should be placed carefully and shielded strictly.
- Input and output capacitors must be placed close to the IC. The connection between pins and capacitor pads should be copper traces without any through-hole via connection.
- The flying capacitors must be placed close to the IC. The traces running from the pins to the capacitor pads should be as wide as possible. Long traces will also produce large noise radiation caused by the large dv/dt on these pins. Short trace is recommended.

- All the traces of LEDs and VIN running from pins to LCM module should be shielded and isolated by the ground plane. The shielding prevents the interference of high frequency noise coupled from the charge pump.

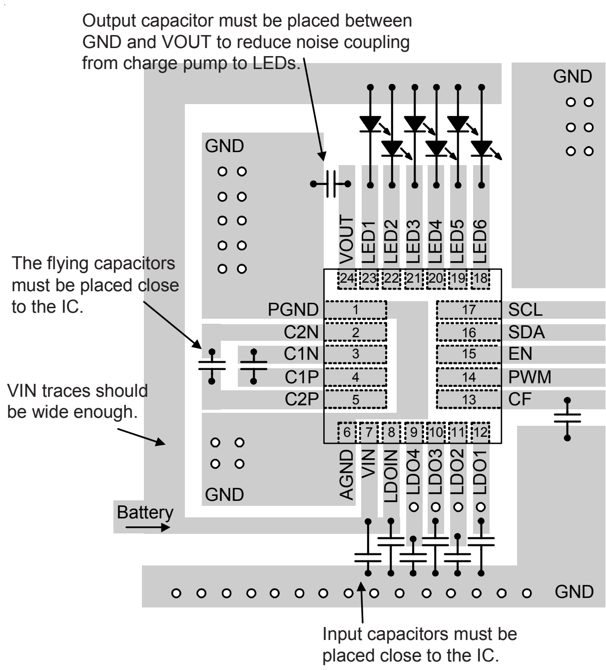
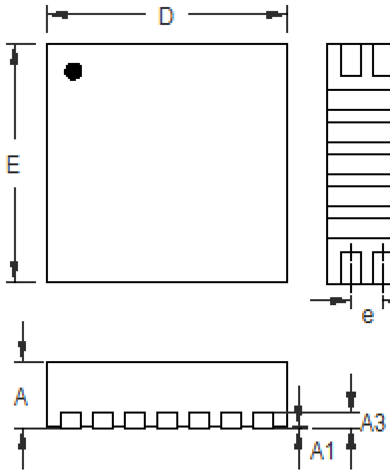


Figure 7. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
e	0.400		0.016	
L	0.350	0.450	0.014	0.018
L1	0.950	1.050	0.037	0.041

W-Type 24L QFN 3x3 (COL) Package

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