2 to 5 Series Cell Fuel Gauge with Integrated Protection Solution for Li-Ion Battery Packs

1 General Description

The RT9440 device is a highly accurate and integrated solution for 2 to 5 series cell fuel gauge and protection It features autonomous cell balancing, protection, and charger control.

The RT9440 integrates highly accurate analog peripherals, measures and maintains an accurate record of available capacity, voltage, current, and temperature. It reports the battery pack parameters to the system host controller via the SMBus interface.

The recommended junction temperature range spans from –40°C to 125°C, while the ambient temperature range extends from –40°C to 85°C.

2 Ordering Information

RT9440 ☐-☐☐

Packing
A: Standard

Programmed Firmware Code AABBX
AA: Application Code
BB: Model Code
X: Customer Approved Version Code

Package Type(1)
N: VQFN-32L 4x4 (V-Type)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

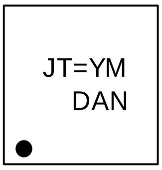
3 Applications

- Notebooks
- Power Tools
- Drones
- Tablets
- UPS/Battery Backup Systems
- Medical Equipment
- Handheld Vacuum Cleaners and Vacuum Robots

4 Features

- **State of Charge (SOC) Calculated by VoltaicGauge$^{\text{TM}}$ with Current Sensing (VGCS)**
- **Voltage Measurement: ±3mV**
- **Current Measurement: ±0.5%**
- **Battery Temperature Measurement: ±1°C (T_A = 0°C to 45°C)**
- **Hardware Current Protection: ±1mV**
- **Autonomous Cell Balance**
- **Configurable Protection Levels and Delay Times for Voltage, Temperature, and Current Protection**
- **Support Both Voltage-Base and SOC-Base Cell Balance**
- **1.5V to 3.3V Configurable VOUT Power Supply**
- **High-Side N-Channel MOSFET Drivers**
- **Auxiliary Overcurrent Protection by High-Side N-Channel MOSFET Drop Voltage**
- **Low Power Consumption**
  - **Normal Mode: 240μA**
  - **Sleep Mode Options: 70μA to 125μA**
  - **Deep Sleep Mode: 30μA**
  - **Shutdown Mode: 1.6μA**
- **Low Value Sense Resistor: 0.5mΩ to 10mΩ**
- **SHA-1/SHA-256/ECC Authentication**
- **Hardware Load and Charger Detection**
- **Support Intel® Dynamic Battery Power Technology (DBPT V2.0)**
- **Support Battery Trip Point (BTP)**
- **Lifetime Data Log and Black Box Recorder**
- **LED Display Driver Pins with Scan Function**
- **FUSE Driver**
- **Support up to 1MHz SMBus Interface**
- **IATA Support**
- **32 Pin VQFN Package with 0.4mm Pitch**

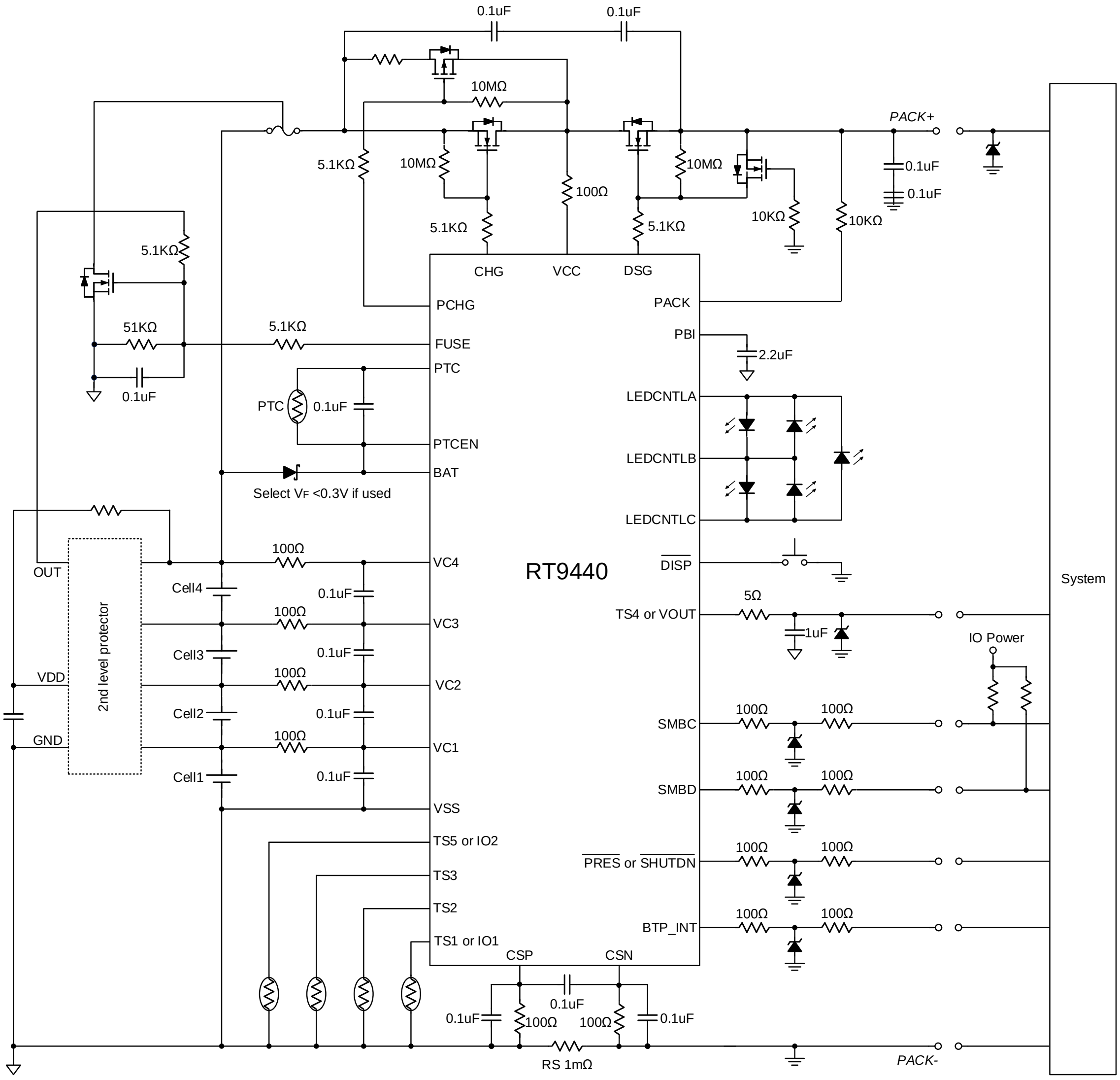
5 Marking Information



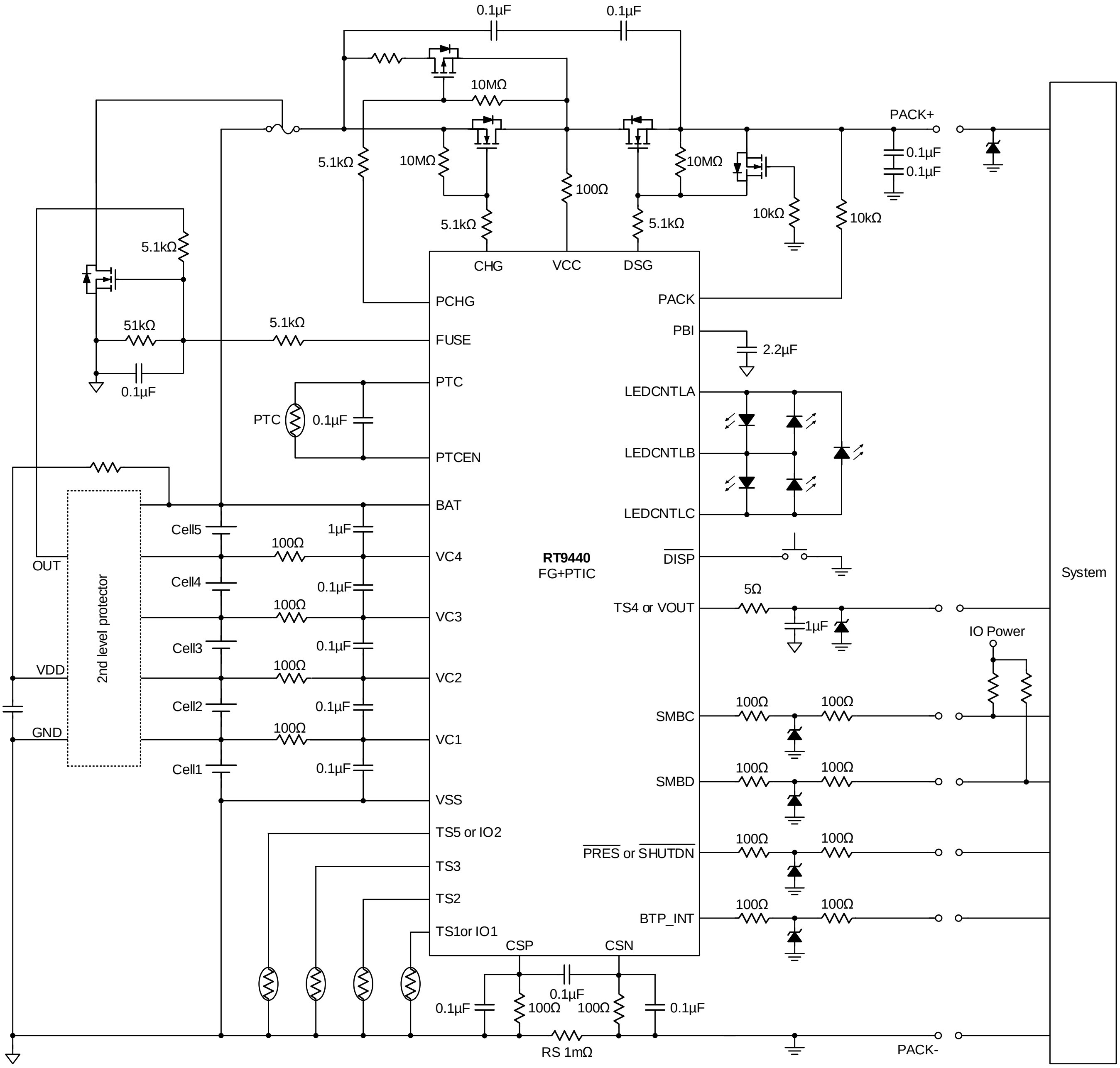
JT=: Product Code
YMDAN: Date Code

6 Simplified Application Circuit

6.1 4-cell Application Circuit



6.2 5-cell Application Circuit



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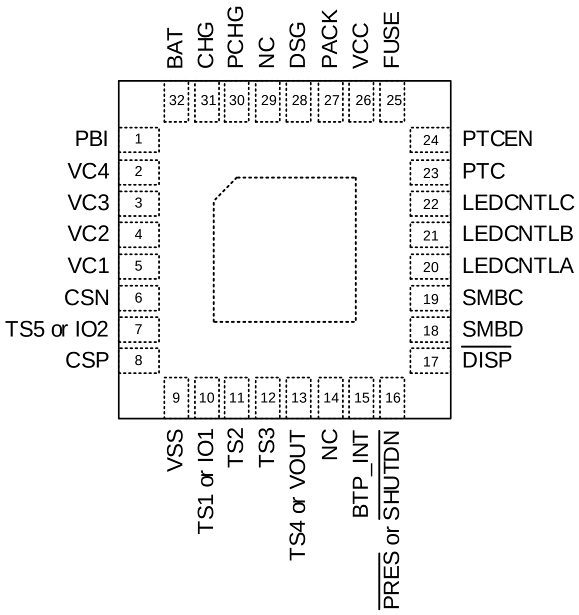
7 Pin Configuration

(TOP VIEW)



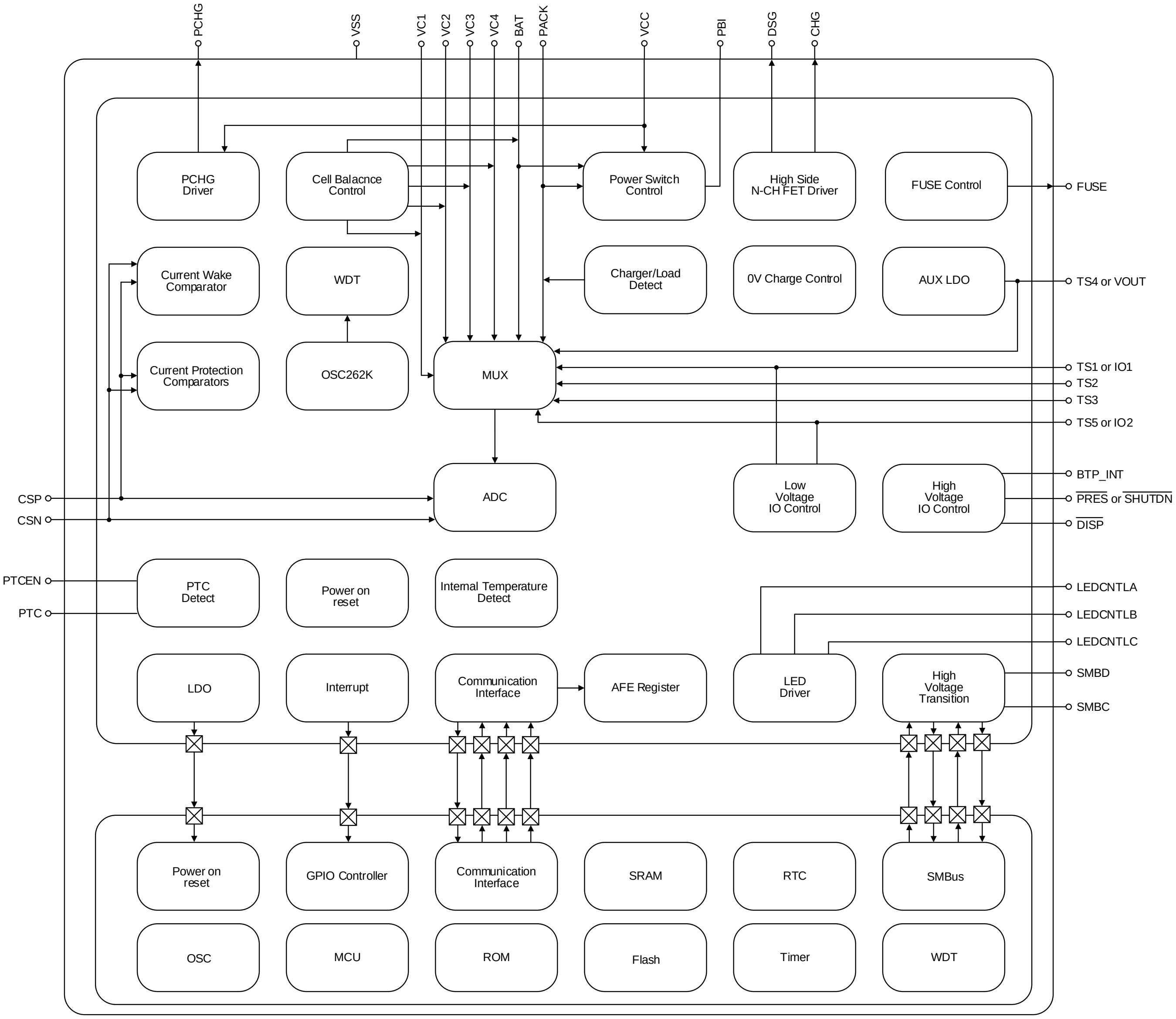
VQFN-32L 4x4

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PBI	Power backup pin.
2	VC4	The voltage input pin is for the 4th cell. The balance current input is for the 4th cell.
3	VC3	The voltage input pin is for the 3rd cell. The balance current input is for the 3rd cell and return the balance current for the 4th cell.
4	VC2	The voltage input pin is for the 2nd cell. The balance current input is for the 2nd cell and return the balance current for the 3rd cell.
5	VC1	The voltage input pin is for the 1st cell. The balance current input is for the 1st cell and return the balance current for the 2nd cell.
6	CSN	Battery current sensing negative input.
7	TS5 or IO2	Temperature sensor 5 measurement input pin, or multi-function GPIO.
8	CSP	Battery current sensing positive input.
9	VSS	Ground.
10	TS1 or IO1	Temperature sensor 1 measurement input pin, or multi-function GPIO.
11	TS2	Temperature sensor 2 measurement input pin.
12	TS3	Temperature sensor 3 measurement input pin.

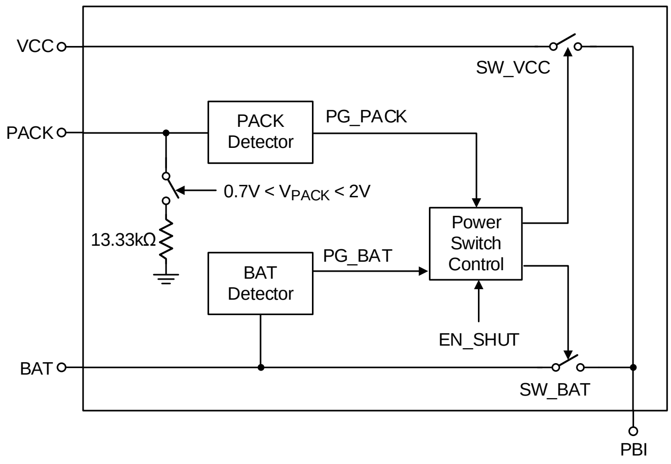
Pin No.	Pin Name	Pin Function
13	TS4 or VOUT	Temperature sensor 4 measurement input pin or it can be used as the power supply for VOUT.
14, 29	NC	There is no internal connection.
15	BTP_INT	Battery Trip Point (BTP) interrupt output pin. It should be connected to VSS if it is not being used.
16	$\overline{\text{PRES}}$ or $\overline{\text{SHUTDN}}$	Host system present input for removable battery pack or emergency shutdown for non-removable battery pack input pin. No need external pull up resistor. It should be connected to VSS if it is not being used.
17	$\overline{\text{DISP}}$	This pin is used to control the LED display It should be connected to VSS if it is not being used.
18	SMBD	SMBus data pin.
19	SMBC	SMBus clock pin.
20	LEDCTLA	LED display segment that drives the external LEDs. It should be left unconnected if not being used.
21	LEDCTLB	LED display segment that drives the external LEDs. It should be left unconnected if not being used.
22	LEDCTLC	LED display segment that drives the external LEDs. It should be left unconnected if not being used.
23	PTC	Safety PTC thermistor input pin. To disable, connect both PTC and PTCEN to VSS.
24	PTCEN	Safety PTC thermistor enable input pin. Connect to BAT. To disable, connect both PTC and PTCEN to VSS.
25	FUSE	Fuse drive output pin. It should be connected to VSS if it is not being used.
26	VCC	Secondary power supply input pin.
27	PACK	Pack sense input pin.
28	DSG	N-Channel MOSFET drive output pin for discharge MOSFET control.
30	PCHG	PMOS pre-charge MOSFET drive output pin.
31	CHG	N-Channel MOSFET drive output pin for charge MOSFET control.
32	BAT	Primary power supply input pin. The voltage input pin is for the 5th cell. The balance current input is for the 5th cell.

9 Functional Block Diagram

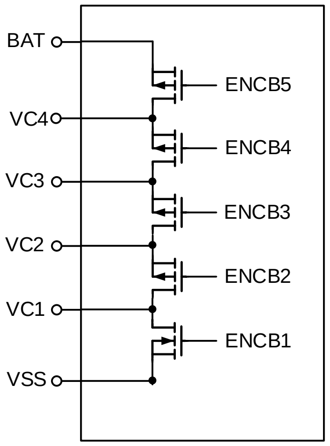


10 Pin Block Diagram

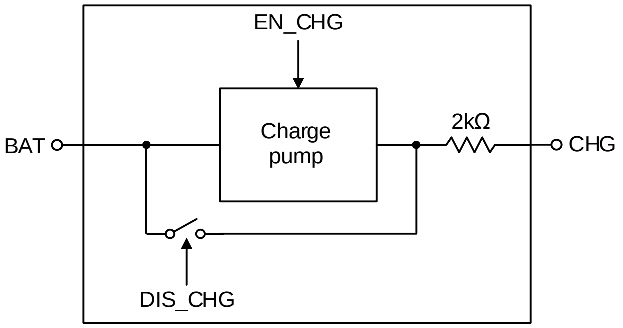
Power Switch Control



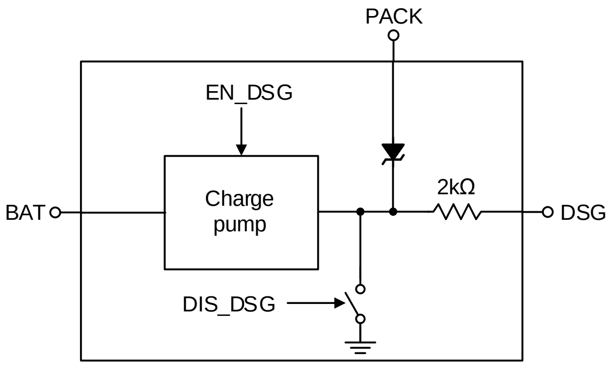
Cell Balance



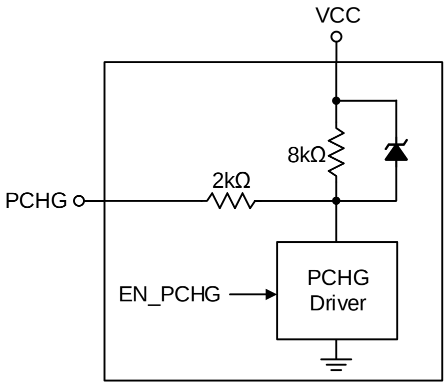
CHG Driver



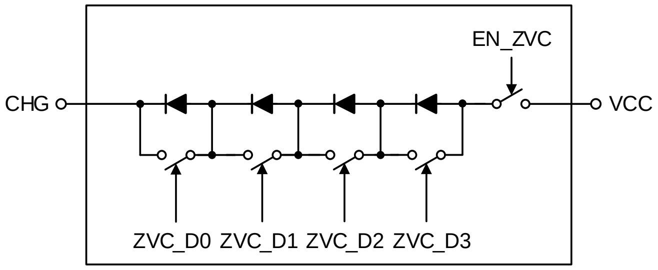
DSG Driver



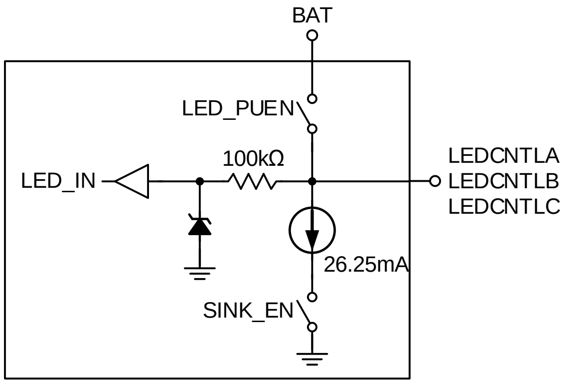
PCHG Driver



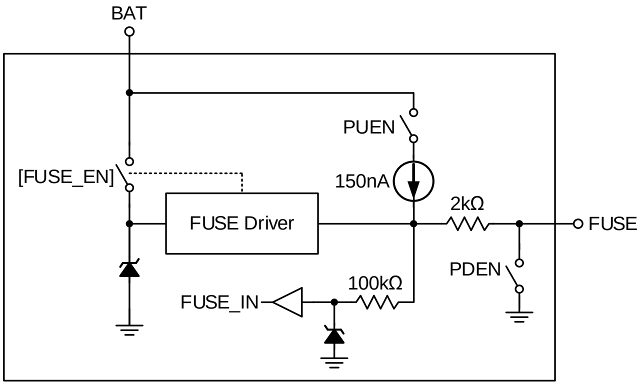
Zero Voltage Control



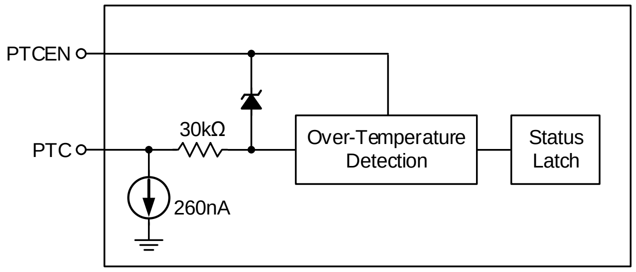
LED Control



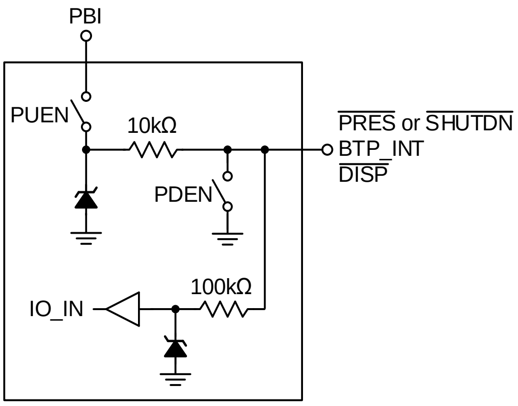
FUSE Control



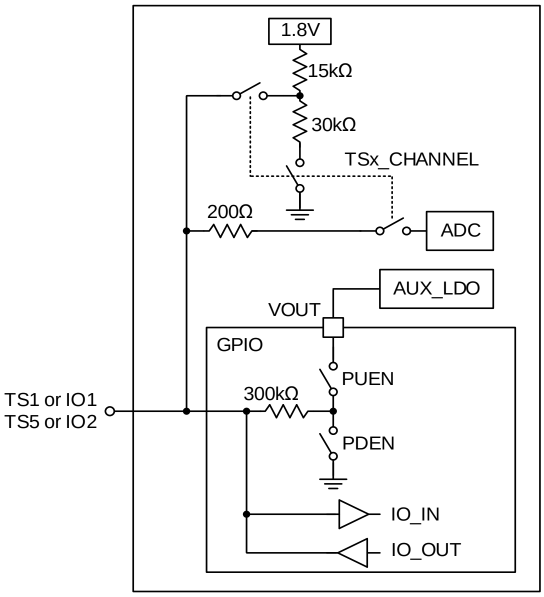
PTC Detection



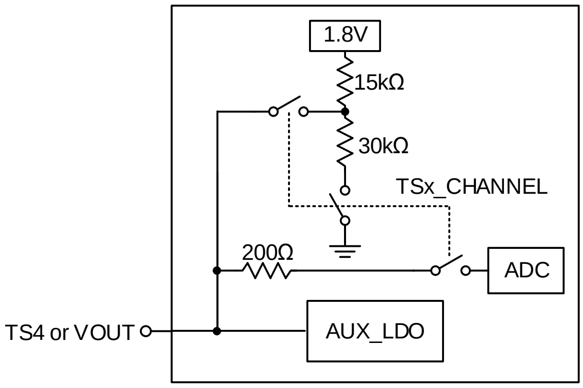
High Voltage GPIO

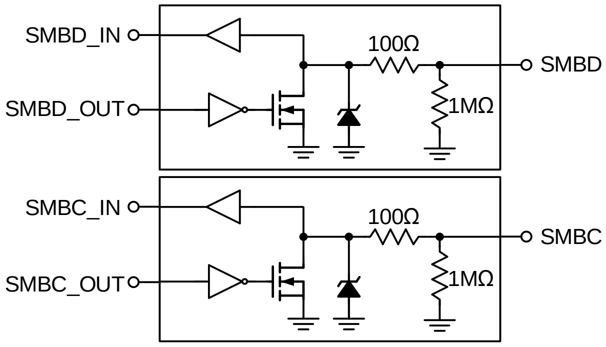
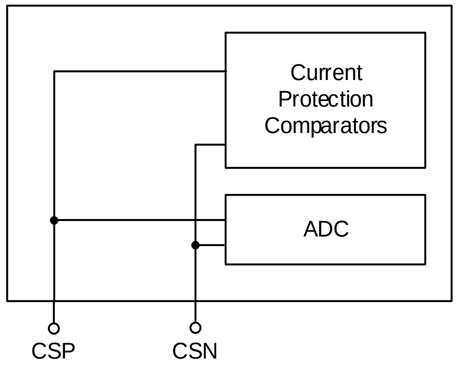
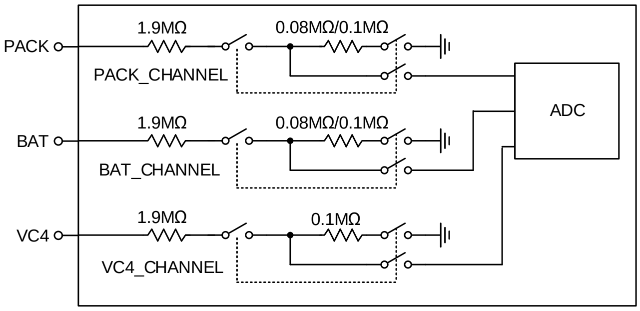


TS1 or IO1 and TS5 or IO2



TS4 or VOUT



SMBD and SMBC	OCD, SCC, SCD1, SCD2 Comparators, and CADC
	
VC4, BAT, and PACK Dividers	
	

11 Absolute Maximum Ratings

(Note 2)

- Supply Voltage on VCC, PBI Pin to VSS -- –0.3V to 30V
- Input Voltage on PACK, $\overline{\text{PRES}}$, BTP_INT, $\overline{\text{DISP}}$ to VSS --------------------- –0.3V to 30V
- Input Voltage on SMB, SMBD to VSS--- –0.3V to 30V
- Input Voltage on PTC, PTCEN, LEDCNTLA,
  LEDCNTLB, LEDCNTLC to VSS --- –0.3V to 30V
- Input Voltage on CSP, CSN to VSS -- –0.3V to 0.3V
- Input Voltage on BAT-- VC4 - 0.3V to VC4 + 8.5V or VSS + 30V
- Input Voltage on VC4-- VC3 - 0.3V to VC3 + 8.5V or VSS + 30V
- Input Voltage on VC3-- VC2 - 0.3V to VC2 + 8.5V or VSS + 30V
- Input Voltage on VC2-- VC1 - 0.3V to VC1 + 8.5V or VSS + 30V
- Input Voltage on VC1-- VSS - 0.3V to VSS + 8.5V or VSS + 30V
- Input Voltage on BAT to PACK (5 Cells Connection)-------------------------- V_{PACK} - 0.3V to V_{PACK} + 8.5V
- Input Voltage on VC4 to PACK (4 Cells Connection)-------------------------- V_{PACK} - 0.3V to V_{PACK} + 8.5V
- Output on CHG, DSG to VSS -- –0.3V to 36V
- Output on PCHG, FUSE to VSS--- –0.3V to 30V
- Input Voltage on TS1, TS2, TS3, TS4, TS5 to VSS --------------------------- –0.3V to 5.5V
- Functional Temperature --- –40°C to 85°C
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-32L 4x4 --- 3.59W
- Package Thermal Resistance (Note 3)
  VQFN-32L 4x4, θ_{JA} -- 27.8°C/W
  VQFN-32L 4x4, θ_{JC} -- 4.6°C/W
- Lead Temperature (Soldering, 10 sec.)-- 260°C
- Junction Temperature --- 150°C
- Storage Temperature Range --- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model) -- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 5)

- Voltage on BAT, VCC, PBI Pin to VSS ---------- 2.8V to 26V
- Input Voltage Range, PACK, SMBC, SMBD, $\overline{\text{PRES}}$, BTP_INT, $\overline{\text{DISP}}$ to VSS ---------- 0V to 26V
- Input Voltage Range, PTC, PTCEN, LEDCNTLA, LEDCNTLB, LEDCNTLC to VSS ---------- 0V to V_{BAT}
- Input Voltage Range, CSP, CSN to VSS ---------- –0.2V to 0.2V
- Input Voltage Range, VC4 ---------- V_{VC3} to V_{VC3} + 5V
- Input Voltage Range, VC3 ---------- V_{VC2} to V_{VC2} + 5V
- Input Voltage Range, VC2 ---------- V_{VC1} to V_{VC1} + 5V
- Input Voltage Range, VC1 ---------- 0V to 5V
- Input Voltage Range, BAT to PACK (5 cells connection) ---------- V_{PACK} - 0.2V to V_{PACK} + 5V
- Input Voltage Range, VC4 to PACK (4 cells connection) ---------- V_{PACK} - 0.2V to V_{PACK} + 5V
- Output Voltage Range, CHG, DSG to VSS ---------- V_{BAT} to V_{BAT} + 12V
- Output Voltage Range, PCHG to VSS ---------- V_{VCC} - 8V to V_{VCC}
- Output Voltage Range, FUSE to VSS ---------- 0V to 26V
- Input Voltage Range, TS1, TS2, TS3, TS4, TS5 to VSS ---------- 0V to 3.3V
- External Capacitor, PBI ---------- 2.2μF
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

13 Electrical Characteristics

(Typical values are at T_A = 25°C and V_{BAT} = 14.4V, Min./Max. values are at T_A = –40°C to 85°C and 2.8V ≤ V_{BAT} ≤ 26V, unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
Normal Mode	I_{NORMAL}	CHG on. DSG on, no Flash write	--	240	--	μA
Sleep Mode	I_{SLEEP}	CHG off, DSG on, no SBS communication	--	125	--	μA
		CHG off, DSG off, no SBS communication	--	70	--	
Deep Sleep Mode	$I_{DEEPSLEEP}$	VOUT only	--	30	--	μA
Shutdown Mode	I_{SHDN}		--	1.6	--	μA
Power Supply Control						
BAT to VCC Switchover Voltage	$V_{SWITCHOVER-}$	V_{BAT} < $V_{SWITCHOVER–}$	2.55	2.65	2.75	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC to BAT Switchover Voltage	$V_{SWITCHOVER+}$	$V_{BAT} > V_{SWITCHOVER-} + V_{HYS}$	2.95	3.1	3.25	V
Switchover Voltage Hysteresis	V_{HYS}	$V_{SWITCHOVER+} - V_{SWITCHOVER-}$	--	450	--	mV
BAT Pin Leakage Current	I_{LK_BAT}	BAT pin, BAT = 0V, VCC = 25V, PACK = 25V	--	--	1	μA
VCC Pin Leakage Current	I_{LK_VCC}	VCC pin, BAT = 25V, VCC = 0V, PACK = 0V	--	--	1	μA
BAT and PACK Pin Leakage Current	$I_{LK\_BAT\_PACK}$	BAT and PACK terminals, BAT = 0V, VCC = 0V, PACK= 0V, PBI = 25V	--	--	1	μA
Internal Pull-Down Resistance	R_{PACK_PD}	$0.7V < V_{PACK} < 2V$	8.5	13.33	19	kΩ
Start-Up Voltage	V_{SU+}	$V_{PACK} > V_{SHUTDOWN+}$	2.65	--	2.85	V
Shutdown Voltage	V_{SHDN-}	$V_{PACK} < V_{SHUTDOWN-}$	2.55	--	2.75	V
Current Wake Detector						
Wakeup Voltage Threshold	V_{WAKE}	$V_{CSP} - V_{CSN}$	±0.075	±0.15	±0.225	mV
			±0.15	±0.3	±0.45	mV
			±0.3	±0.6	±0.9	mV
			±0.6	±1.2	±1.8	mV
			±1.2	±2.4	±3.6	mV
			±2.4	±4.8	±7.2	mV
Time from Application of Current to Wake Interrupt	t_{WAKE}		--	0.2	0.5	ms
Wake Comparator Startup Time	t_{WAKE_SU}		--	3.35	--	ms
Cell Balancing						
Internal Cell Balancing Resistance	R_CB	$R_{DS(ON)}$ for internal MOSFET switch at $3V < V_{DS} < 4.5V$	--	100	200	Ω
SMBD and SMBC						
High-Level Input	V_{IH}		1.3	--	--	V
Low-Level Input	V_{IL}		--	--	0.8	V
Output Voltage Low	V_{OL}	I_{OL} = 1.5mA	--	--	0.4	V
Pull-Down Resistance	R_{PD}		0.6	1	1.5	MΩ
$\overline{\text{PRES}}$, BTP_INT, and $\overline{\text{DISP}}$						
High-Level Input	V_{IH}		1.3	--	--	V
Low-Level Input	V_{IL}		--	--	0.55	V
Output Voltage High	V_{OH}	$\overline{\text{PRES}}$, BTP_INT and $\overline{\text{DISP}}$, $V_{BAT} > 5.5V$, $I_{OH} = -0\mu A$	3.5	--	5	V
		$\overline{\text{PRES}}$, BTP_INT and $\overline{\text{DISP}}$, $V_{BAT} > 5.5V$, $I_{OH} = -10\mu A$	1.8	--	5	
Output Voltage Low	V_{OL}	I_{OL} = 1.5mA	--	--	0.4	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
$\overline{\text{PRES}}$ Input Leakage Current	I_{LK_PRES}	$\overline{\text{PRES}}$ pin, BAT = 2.8V, $\overline{\text{PRES}}$ = 26V	--	--	1	μA
BTP_INT Input Leakage Current	$I_{LK\_BTP\_INT}$	BTP_INT pin, BAT = 2.8V, BTP_INT = 26V	--	--	1	μA
$\overline{\text{DISP}}$ Input Leakage Current	I_{LK_DISP}	$\overline{\text{DISP}}$ pin, BAT = 2.8V, $\overline{\text{DISP}}$ = 26V	--	--	1	μA
Output Reverse Resistance	R_O	Between $\overline{\text{PRES}}$ or BTP_INT or $\overline{\text{DISP}}$ and PBI	8	20	--	kΩ
LEDCTLA, LEDCTLB, and LEDCTLC						
High-Level Input	V_{IH}		1.4	--	--	V
Low-Level Input	V_{IL}		--	--	0.5	V
Output Voltage High	V_{OH}	$V_{BAT} > 3.3V$, $I_{OH} = -22.5mA$	V_{BAT} - 1.6V	--	--	V
High-Level Output Current Protection	I_{SC}		–30	–45	–60	mA
Low-Level Output Current	I_{OL}	$V_{BAT} > 3.3V$, $V_{OH} = 0.4V$	19.5	26.25	33	mA
Input Leakage Current	I_{LK}	LEDCNTLA/B/C pin, LEDCNTLA/B/C = BAT = 25V	--	--	1	μA
Frequency of LED Pattern	$f_{LEDCNTLx}$		--	180	--	Hz
Current Measurement						
Input Voltage Range		V_{CSP} - V_{CSN}	–0.1	--	0.1	V
Offset Error	I_{OERR}	$\lvert V_{CSP} - V_{CSN}\rvert = 0mV$	–6	±3.5	6	μV
Gain Error	I_{GERR}	$\lvert V_{CSP} - V_{CSN}\rvert = 100mV$	–0.5	±0.2	0.5	%
Effective Input Resistance	R_{CC_IN}		--	2.7	--	MΩ
Conversion Time	t_{CC_CONV}	Single conversion in normal mode	--	125	--	ms
Voltage Measurement						
Input Voltage Range (Differential Cell Input Mode)	$V_{ADC\_IN\_CELLS}$		0	--	5	V
Input Voltage Range (Divider Measurement Mode)	$V_{ADC\_IN\_DIV}$	Applicable to divider measurements using the BAT, VC4 and PACK, pins relative to VSS.	0	--	26	V
Cell Voltage Measurement Accuracy	V_{CELL_ACC}	$V_{VC4} - V_{VC3}$, $V_{VC3} - V_{VC2}$, $V_{VC2} - V_{VC1}$, $V_{VC1} - V_{VSS}$	–10	±3	10	mV
		$V_{BAT} - V_{VC4}$, impedance between top node of 5th cell and the BAT pin is under 0.3Ω	–12.5	±5	12.5	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
MOSFET Voltage Drop Measurement Accuracy	V_{MOSFET_ACC}	$V_{BAT} – V_{PACK}$, Impedance between top node of 5th cell and the BAT pin is under 0.3Ω and without Schottky diode $7.5V < V_{BAT} \le 26V$	–12.5	±5	12.5	mV
		$V_{BAT} – V_{PACK}$, Impedance between top node of 5th cell and the BAT pin is under 0.3Ω and without Schottky diode $2.8V \le VBAT \le 7.5V$	–32.5	±20	32.5	
Stack Voltage Measurement Accuracy	V_{STACK_ACC}	$V_{VC4} – V_{VSS}$	–50	±15	50	mV
		$V_{BAT} – V_{VSS}$, Impedance between top node of 5th cell and the BAT pin is under 0.3Ω and without Schottky diode	–62.5	±25	62.5	mV
PACK Pin Voltage Measurement Accuracy	$V_{PACK\_ACC)}$=	$V_{PACK} – V_{VSS}$	–50	±15	50	mV
Effective Input Resistance	$R_{\_ADC\_IN)}$=		--	15.3	--	MΩ
Conversion Time	$t_{\_ADC\_CONV)}$=	Single conversion in normal mode	--	10	--	ms
High-Side N-MOSFET Drivers						
DSG MOSFET Turn-On Ratio	V_{DSG_RATIO}	Ratio = $(V_{DSG} – V_{BAT}) / V_{BAT}$, $3.4V < V_{BAT} < 5V$ Connect a 10MΩ resistor between PACK and DSG	2.133	2.333	2.433	
		Ratio = $(V_{DSG} – V_{BAT}) / V_{BAT}$, $2.8V \le V_{BAT} \le 3.4V$ Connect a 10MΩ resistor between PACK and DSG	1.93	2.18	2.433	
CHG MOSFET Turn-On Ratio	V_{CHG_RATIO}	Ratio = $(V_{CHG} – V_{BAT}) / V_{BAT}$, $3.4V < V_{BAT} < 5V$ Connect a 10MΩ resistor between BAT and CHG	2.133	2.333	2.433	
		Ratio = $(V_{CHG} – V_{BAT}) / V_{BAT}$, $2.8V \le V_{BAT} \le 3.4V$ Connect a 10MΩ resistor between BAT and CHG	1.93	2.08	2.23	
DSG MOSFET Turn-On Voltage	V_{DSGON}	$V_{DSGON} = V_{DSG} – V_{BAT}$, $V_{BAT} \ge 5V$, connect a 10MΩ resistor between PACK and DSG	10.5	11.5	12.5	V
CHG MOSFET Turn-On Voltage	V_{CHGON}	$V_{CHGON} = V_{CHG} – V_{BAT}$, $V_{BAT} \ge 5V$, connect a 10MΩ resistor between BAT and CHG	10.5	11.5	12.5	V
DSG MOSFET Turn-Off Voltage	V_{DSGOFF}	$V_{DSGOFF} = V_{DSG} – V_{PACK}$, connect a 10MΩ resistor between PACK and DSG	–0.4	--	0.4	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CHG MOSFET Turn-Off Voltage	V_{CHGOFF}	$V_{CHGOFF} = V_{CHG} - V_{BAT}$, V_{GS} resistor = 10MΩ	–0.4	--	0.4	V
DSG Rise Time (0% to 35% V_{DSGON})	t_{R_DSG}	Connect a C_L = 4.7nF between DSG and PACK, a 5.1kΩ resistor between DSG and C_L, a 10MΩ resistor between PACK and DSG	--	200	500	μs
CHG Rise Time (0% to 35% V_{CHGON})	t_{R_CHG}	Connect a C_L = 4.7nF between CHG and BAT, a 5.1kΩ resistor between CHG and C_L, a 10MΩ resistor between BAT and CHG	--	200	500	μs
DSG Fall Time (V_{DSGON} to 1V)	t_{F_DSG}	Connect a C_L = 4.7nF between DSG and PACK, a 5.1kΩ resistor between DSG and C_L, a 10MΩ resistor between PACK and DSG	--	40	100	μs
CHG Fall Time (V_{DSGON} to 1V)	t_{F_CHG}	Connect a C_L = 4.7nF between CHG and BAT, a 5.1kΩ resistor between CHG and C_L, a 10MΩ resistor between BAT and CHG	--	40	100	μs
PCHG P-MOSFET Drivers						
PCHG MOSFET Turn-On Voltage	V_{PCHGON}	$V_{PCHGON} = V_{VCC} - V_{PCHG}$, V_{GS} resistor = 10MΩ	6	7	8	V
PCHG MOSFET Turn-Off Voltage	$V_{PCHGOFF}$	$V_{PCHGOFF} = V_{VCC} - V_{PCHG}$, V_{GS} resistor = 10MΩ	–0.4	--	0.4	V
PCHG Rise Time (10% to 90% V_{PCHGON})	t_{R_PCHG}	$V_{VCC} \geq 8V$, connect a C_L = 4.7nF between PCHG and VCC, a 5.1kΩ resistor between PCHG and C_L, a 10MΩ resistor between PCHG and VCC	--	40	200	μs
PCHG Fall Time (90% to 10% V_{PCHGON})	t_{F_PCHG}	$V_{VCC} \geq 8V$, connect a C_L = 4.7nF between PCHG and VCC, a 5.1kΩ resistor between PCHG and C_L, a 10MΩ resistor between PCHG and VCC	--	40	200	μs
Fuse Driver						
Output Voltage High	V_{OH}	$V_{BAT} \geq 8V$, C_L = 1nF, I_{OH} = 0μA	8	9.6	10.7	V
		$V_{BAT} < 8V$, C_L = 1nF, I_{OH} = 0μA	V_{BAT} – 0.1V	--	V_{BAT}	V
Output Voltage Low	V_{OL}	I_{OL} = 1.5mA	--	--	0.4	V
High-Level Input	V_{IH}		1.5	2	2.5	V
Low-Level Input	V_{IL}		--	--	0.54	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Internal Pull-Up Current	$I_{AFEFUSE\_PU}$	$V_{BAT} \geq 8V$, $V_{AFEFUSE}$ = VSS	100	150	330	nA
Output Impedance	$R_{AFEFUSE}$		1.4	2	2.6	kΩ
Fuse Trip Detection Delay	t_{DLY}		128	--	256	µs
Fuse Output Rise Time	t_R	$V_{BAT} \geq 8V$, C_L = 1nF, V_{OH} = 0V to 5V	--	5	20	µs
Internal Temperature Sensor						
Internal Temperature Measurement Error	INT_{GERR}		--	±3	--	°C
TS1, TS2, TS3, TS4, and TS5						
Input Voltage Range	V_{IN}		–0.3	--	3.3	V
Internal Resistance	R_{TS}	Pull-up resistance	--	15	--	kΩ
		Pull-down resistance	--	30	--	kΩ
PTC and PTCEN						
PTC Trip Resistance	R_{TRIP}		1.3	2.1	4	MΩ
PTC Trip Voltage	V_{PTC_TRIP}	$V_{PTC\_TRIP} = V_{PTCEN} - V_{PTC}$	490	540	645	mV
Internal PTC Current Bias	I_{PTC}		160	260	375	nA
PTC Delay Time	t_{DLY_PTC}		40	80	145	ms
Program Flash						
Data Retention			10	--	--	Years
Flash Programming Write Cycles			100k	--	--	Cycles
Word Programming Time	$t_{PROGWORD}$		--	--	10	µs
Mass-Erase Time	$t_{MASSERASE}$		--	--	100	ms
Page-Erase Time	$t_{PAGEERASE}$		--	--	6	ms
Flash-Read Current	$I_{FLASHREAD}$		--	3.37	4	mA
Flash-Write Current	$I_{FLASHWRITE}$		--	--	2.7	mA
Flash-Erase Current	$I_{FLASHERASE}$		--	--	1.2	mA
Data Flash						
Data Retention			10	--	--	Years
Flash Programming Write Cycles			100k	--	--	Cycles
Word Programming Time	$t_{PROGWORD}$		--	--	10	µs
Mass-Erase Time	$t_{MASSERASE}$		--	--	40	ms
Page-Erase Time	$t_{PAGEERASE}$		--	--	6	ms
Flash-Read Current	$I_{FLASHREAD}$		--	--	4	mA
Flash-Write Current	$I_{FLASHWRITE}$		--	--	2.7	mA
Flash-Erase Current	$I_{FLASHERASE}$		--	--	1.2	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OCD, SCC, SCD1, and SCD2 Current Protection Thresholds						
OCD Detection Threshold Voltage Range	V_{OCD}	$V_{CSP} – V_{CSN}$, extend range	–32	--	–92	mV
		$V_{CSP} – V_{CSN}$, normal range	–2	--	–32	
OCD Detection Threshold Voltage Program Step	ΔV_{OCD}	$V_{CSP} – V_{CSN}$, extend range	--	–4	--	mV
		$V_{CSP} – V_{CSN}$, normal range	--	–2	--	
SCD1 Detection Threshold Voltage Range	V_{SCD1}	$V_{CSP} – V_{CSN}$, extend range	–80	--	–220	mV
		$V_{CSP} – V_{CSN}$, normal range	–10	--	–80	
SCD1 Detection Threshold Voltage Program Step	ΔV_{SCD1}	$V_{CSP} – V_{CSN}$, extend range	--	–20	--	mV
		$V_{CSP} – V_{CSN}$, normal range	--	–10	--	
SCD2 Detection Threshold Voltage Range	V_{SCD2}	$V_{CSP} – V_{CSN}$, extend range	–80	--	–220	mV
		$V_{CSP} – V_{CSN}$, normal range	–10	--	–80	
SCD2 Detection Threshold Voltage Program Step	ΔV_{SCD2}	$V_{CSP} – V_{CSN}$, extend range	--	–20	--	mV
		$V_{CSP} – V_{CSN}$, normal range	--	–10	--	
SCC Detection Threshold Voltage Range	V_{SCC}	$V_{CSP} – V_{CSN}$, extend range	80	--	220	mV
		$V_{CSP} – V_{CSN}$, normal range	10	--	80	
SCC Detection Threshold Voltage Program Step	ΔV_{SCC}	$V_{CSP} – V_{CSN}$, extend range	--	20	--	mV
		$V_{CSP} – V_{CSN}$, normal range	--	10	--	
OCD, SCC, SCD1, and SCD2 Current Protection Timing						
OCD Detection Delay Time	t_{OCD}		1	--	31	ms
OCD Detection Delay Time Program Step	Δt_{OCD}		--	2	--	ms
SCD1 Detection Delay Time	t_{SCD1}	Extend delay time	0	--	1850	µs
		Normal delay time	0	--	915	
SCD1 Detection Delay Time Program Step	Δt_{SCD1}	Extend delay time	--	121	--	µs
		Normal delay time	--	61	--	
SCD2 Detection Delay Time	t_{SCD2}	Extend delay time	0	--	915	µs
		Normal delay time	0	--	458	
SCD2 Detection Delay Time Program Step	Δt_{SCD2}	Extend delay time	--	61	--	µs
		Normal delay time	--	30.5	--	
SCC Detection Delay Time	t_{SCC}		0	--	915	µs
SCC Detection Delay Time Program Step	Δt_{SCC}		--	61	--	µs
Current Fault Delay Time Accuracy	t_{ACC}	$V_{CSP} – V_{CSN} = V_T – 3mV$ for OCD, SCD1, and SC2, $V_{CSP} – V_{CSN} = V_T + 3mV$ for SCC	--	--	160	µs
OCD, SCC, SCD1, and SCD2 Current Protection Accuracy						
OCD Detection Accuracy	V_{OCD_ACC}	|Setting| < 32mV	–1	--	1	mV
		|Setting| = 32mV to 64mV	–2	--	2	
		|Setting| = 64mV to 92mV	–4	--	4	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCD1, SCD2 Detection Accuracy	V_{SCD_ACC}	|Setting| < 40mV	–1	--	1	mV
		|Setting| = 40mV to 80mV	–2	--	2	
		|Setting| = 80mV to 150mV	–4	--	4	
		|Setting| > 150mV	–7	--	7	
SCC Detection Accuracy	V_{SCC_ACC}	|Setting| < 40mV	–1	--	1	mV
		|Setting| = 40mV to 80mV	–2	--	2	
		|Setting| = 80mV to 150mV	–4	--	4	
		|Setting| > 150mV	–7	--	7	
Load Detection						
Load Remove Threshold	V_{LD}	$V_{PACK} > V_{LD}$	0.9	1	1.1	V
Internal Current from BAT to PACK for Load Detection	I_{SOURCE}		9	10	11	μA
			18	20	22	
			27	30	33	
			36	40	44	
Detection Delay Time	t_{DLY_LD}		--	10	--	ms
Charger Detection						
Charger Remove Threshold	V_{CD}	$V_{BAT} > V_{PACK}$	0.07	0.1	0.15	V
Detection Delay Time	t_{DLY_CD}		--	2	--	ms
Low Frequency Oscillator						
Operating Frequency Low	f_{OSC_LOW}		--	262.14	--	kHz
Operating Accuracy Low	f_{ERR_LOW}		–2.5	±0.25	2.5	%
High Frequency Oscillator						
Operating Frequency High	f_{OSC_HIGH}		--	4	--	MHz
Operating Accuracy High	f_{ERR_HIGH}		–10	--	10	%
Auxiliary LDO Power Supply						
Programming Output Voltage	V_{OUT}	$C_L = 1\mu F$	3.14	3.30	3.47	V
			2.85	3.00	3.15	
			2.38	2.50	2.63	
			1.71	1.80	1.89	
			1.425	1.5	1.575	
Output Current	I_{OUT}	$C_L = 1\mu F$	--	--	2	mA
The Time for V_{OUT} Ready	t_{RDY}	$C_L = 1\mu F$	--	--	1	ms
Output Short Circuit Current Limit	$I_{LIM\_VOUT\_SC}$	V_{OUT} = VSS, $C_L = 1\mu F$	8	--	20	mA
SMBus, 100kHz						
Clock Operating Frequency	f_{SMB}	Slave mode, SMBC duty cycle = 50%	10	--	100	kHz
Clock Operating Frequency	f_{MAS}	Master mode	--	51.2	--	kHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Bus Free Time STOP to START	t_{BUF}		4.7	--	--	µs
START Condition Hold Time	$t_{HD:START}$		4.0	--	--	µs
Setup Repeated START	$t_{SU:START}$		4.7	--	--	µs
Setup Time STOP Condition	$t_{SU:STOP}$		4.0	--	--	µs
Data Hold Time	$t_{HD:DAT}$		0	--	--	ns
Data Setup Time	$t_{SU:DAT}$		250	--	--	ns
Error Signal Detect Time	$t_{TIMEOUT}$		25	--	35	ms
Low Period of the SMBC Clock	t_{LOW}		4.7	--	--	µs
High Period of the SMBC Clock	t_{HIGH}		4	--	--	µs
Clock Rise Time	t_R	10% to 90%	--	--	1000	ns
Clock Fall Time	t_F	90% to 10%	--	--	300	ns
Cumulative Clock Low Slave Extend Time	t_{LOW_SEXT}		--	--	25	ms
Cumulative Clock Low Master Extend Time	t_{LOW_MEXT}		--	--	10	ms
SMBus, 400kHz						
Clock Operating Frequency	f_{SMB}	Slave mode, SMBC duty cycle = 50%	--	--	400	kHz
Bus Free Time STOP to START	t_{BUF}		1.3	--	--	µs
START Condition Hold Time	$t_{HD:START}$		0.6	--	--	µs
Setup Repeated START	$t_{SU:START}$		0.6	--	--	µs
Setup Time STOP Condition	$t_{SU:STOP}$		0.6	--	--	µs
Data Hold Time	$t_{HD:DAT}$		0	--	--	ns
Data Setup Time	$t_{SU:DAT}$		100	--	--	ns
Error Signal Detect Time	$t_{TIMEOUT}$		25	--	35	ms
Low Period of the SMBC Clock	t_{LOW}		1.3	--	--	µs
High Period of the SMBC Clock	t_{HIGH}		0.6	--	--	µs
Clock Rise Time	t_R	10% to 90%	20	--	300	ns
Clock Fall Time	t_F	90% to 10%	20	--	300	ns
Cumulative Clock Low Slave Extend Time	t_{LOW_SEXT}		--	--	25	ms
Cumulative Clock Low Master Extend Time	t_{LOW_MEXT}		--	--	10	ms
SMBus, 1MHz						
Clock Operating Frequency	f_{SMB}	Slave mode, SMBC duty cycle = 50%	--	--	1	MHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Bus Free Time STOP to START	t_{BUF}		0.5	--	--	μs
START Condition Hold Time	$t_{HD:START}$		0.26	--	--	μs
Setup Repeated START	$t_{SU:START}$		0.26	--	--	μs
Setup Time STOP Condition	$t_{SU:STOP}$		0.26	--	--	μs
Data Hold Time	$t_{HD:DAT}$		0	--	--	ns
Data Setup Time	$t_{SU:DAT}$		50	--	--	ns
Error Signal Detect Time	$t_{TIMEOUT}$		25	--	35	ms
Low Period of the SMBC Clock	t_{LOW}		0.5	--	--	μs
High Period of the SMBC Clock	t_{HIGH}		0.26	--	--	μs
Clock Rise Time	t_R	10% to 90%	--	--	120	ns
Clock Fall Time	t_F	90% to 10%	20	--	120	ns
Cumulative Clock Low Slave Extend Time	t_{LOW_SEXT}		--	--	25	ms
Cumulative Clock Low Master Extend Time	t_{LOW_MEXT}		--	--	10	ms

14 Timing Diagram

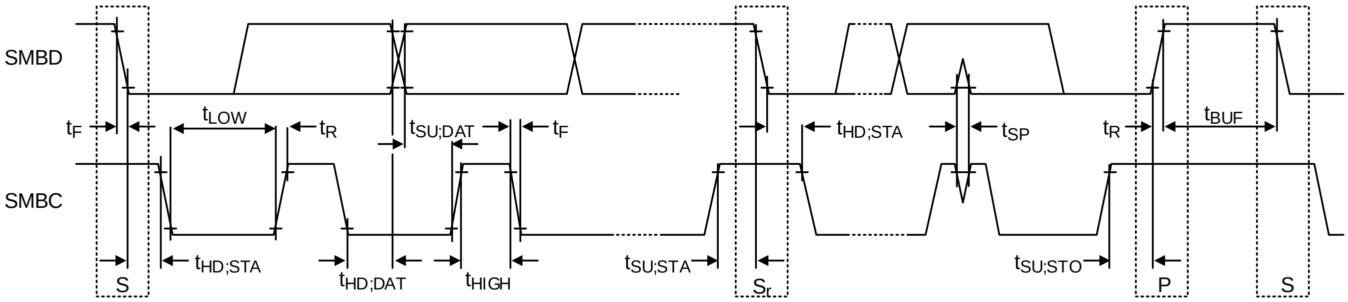


Figure 1. SMBus Timing Diagram

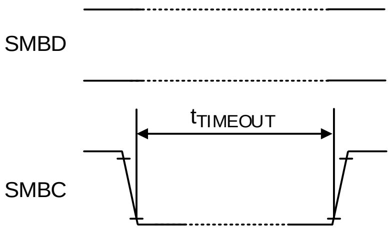
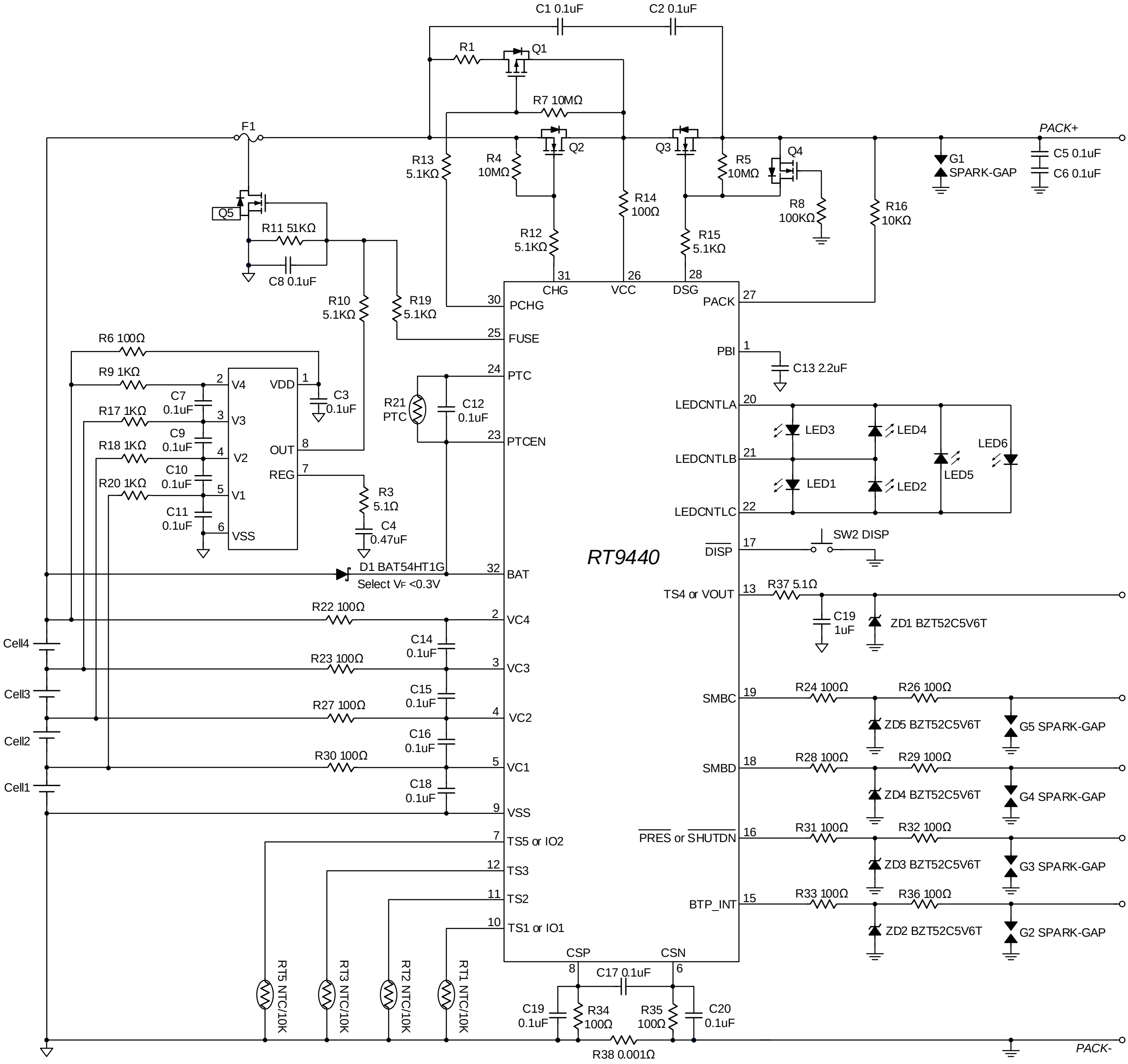
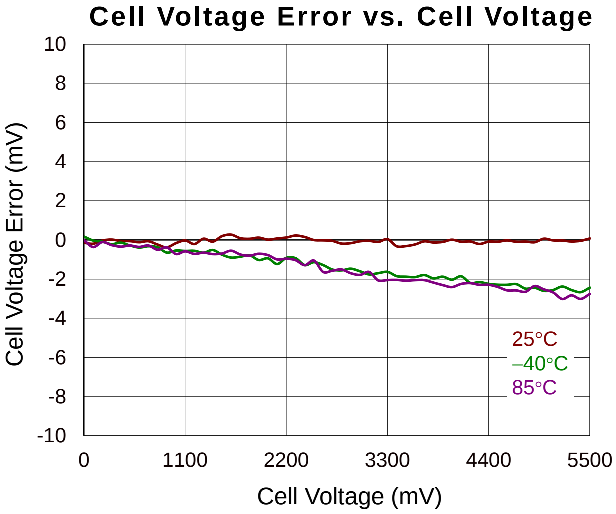


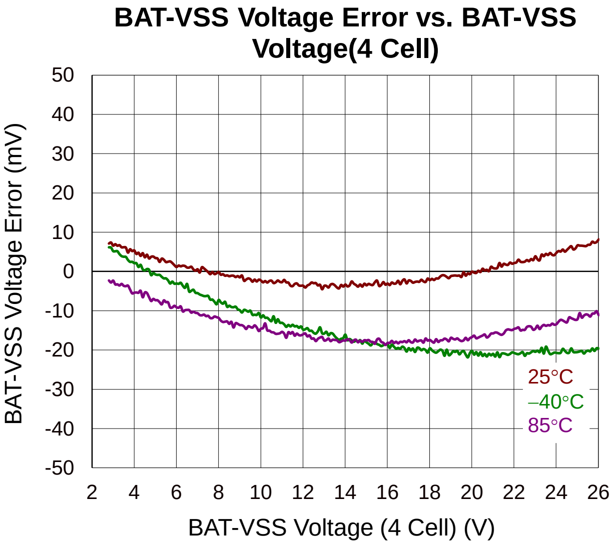
Figure 2. SMBus Timeout Condition

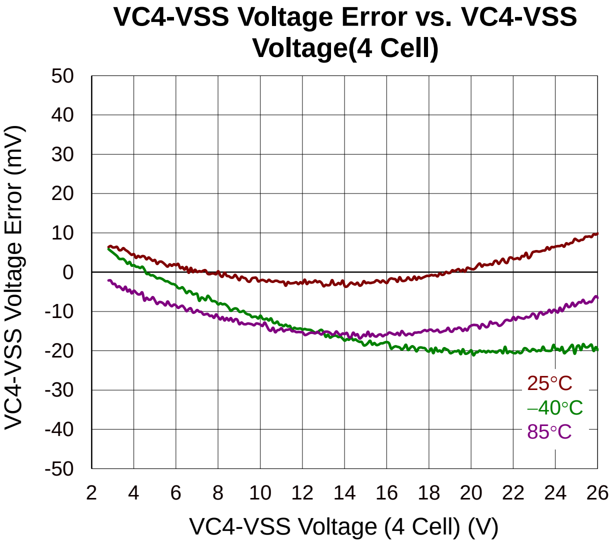
15 Typical Application Circuit

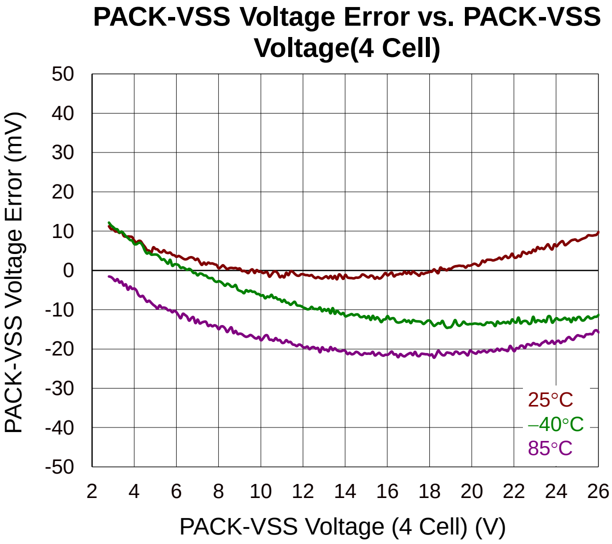


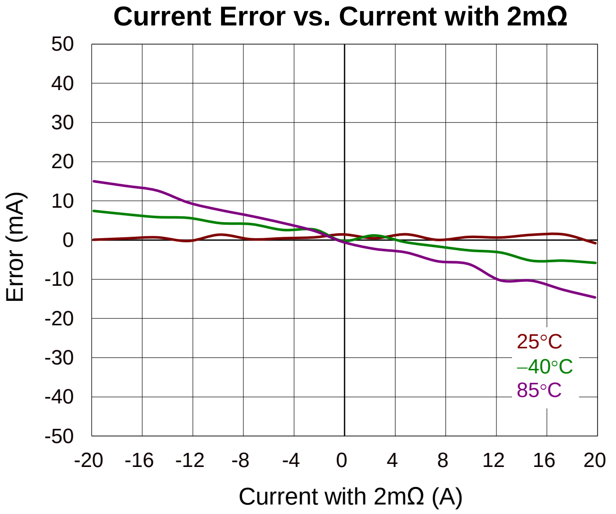
16 Typical Operating Characteristics

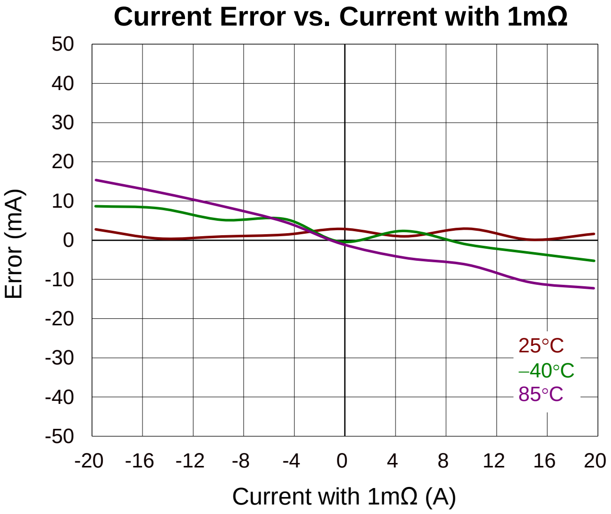












17 Application Information

(Note 6)

The RT9440 device provides a complete fuel gauging solution for 2-to-5 series cell battery pack applications. It also fully integrates cell balancing, protection, charger control, and authentication for 2-to-5 series cell battery packs.

17.1 Fuel Gauge

The RT9440 uses the VGCS algorithm to calculate the state of charge in battery cells. The VGCS algorithm is a hybrid fuel gauge algorithm with voltage-based core (VoltaicGauge^{TM}), iterating battery voltage and dynamic difference of battery voltage. Then it is optimized with current information to adjust the delta SOC and integrate it into the overall SOC. The VGCS algorithm also includes temperature and load compensation, and aging compensation functions, providing both short-term accurate and long-term stability in SOC results.

17.2 Power Mode

The RT9440 supports four power modes to decrease power usage.

- In normal mode, the RT9440 performs measurements, calculations, protection decisions, and data updates at 250ms intervals. Between these intervals, the RT9440 is in idle status to reduce power consumption.
- In sleep mode, the RT9440 performs measurements, calculations, protection decisions, and data updates at adjustable intervals (default 5 second). Between these intervals, the RT9440 is in idle status to decrease power usage. The RT9440 has a wake function that enables exit from sleep mode when current flow or failure is detected.
- In deep sleep mode, the RT9440 turns off all MOSFETs and hardware current protection, and executes measurements, calculations, and data updates at adjustable intervals (default 60 seconds). Between these intervals, the RT9440 is in idle status to reduce power consumption and turns off SMBus communication. The RT9440 has a wake function that enables exit from deep sleep mode when a charger is plugged in.
- In shutdown mode, the RT9440 is completely disabled.

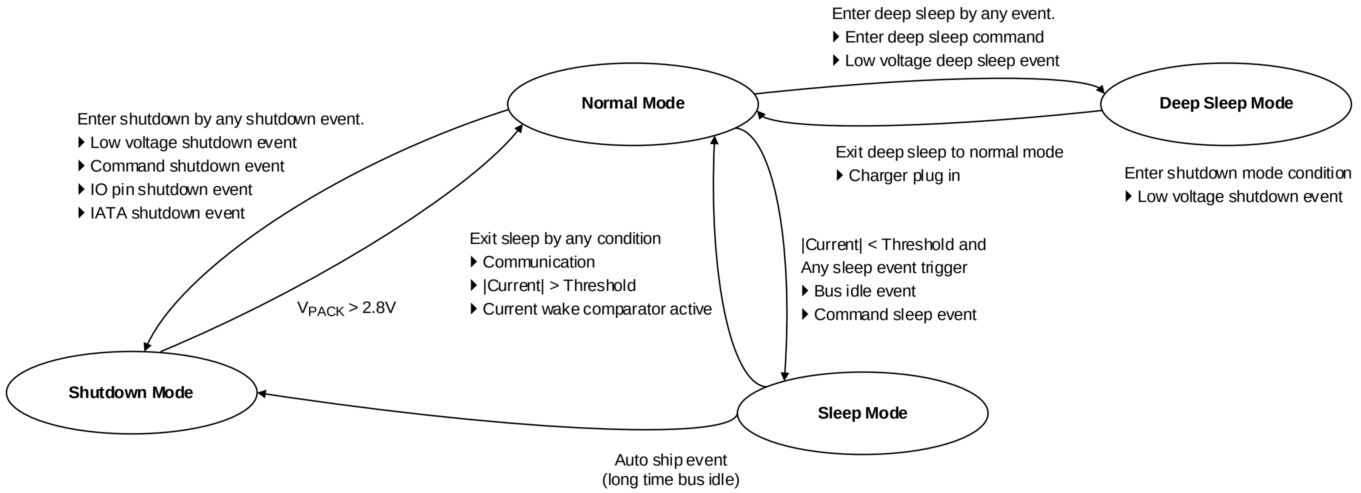


Figure 3. Power Mode State Machine

17.3 Measurement

The RT9440 supports voltage, current and temperature measurements.

The RT9440 uses internal ADC to measure voltage and updates the voltage every 0.25 seconds in the normal mode. This data is also used to calculate the VGCS gas gauging.

- Up to 5 cell voltage measurement
- Stack cell voltage
- Pack pin voltage
- High-side MOSFET drop voltage measurement

The RT9440 uses the CSP and CSN inputs to measure and calculate the battery charge and discharge current.

- Supports current measurement with 0.5mΩ to 10mΩ current sense resistance.

The RT9440 has an internal temperature sensor and inputs for up to 5 external temperature sensors.

- Supports up to 5 channels of external NTC temperature measurement.
- TS1, TS2, TS3, TS4, and TS5 can be optionally configured for general ADC measurement, with a measurement range of 0V to 3.3V.
- Internal temperature measurement.

TS1, TS2, TS3, TS4 and TS5 can be individually enabled and configured for cell or MOSFET temperature usage and use a different thermistor profile.

17.4 Primary (1st Level) Safety Features

The RT9440 supports a full coverage of battery and system protection features that can be easily configured. For detailed descriptions of each protection function, refer to the RT9440 Technical Reference Manual.

It includes two types of protection: hardware protection and software protection.

- Hardware protection
  - Overcurrent in discharge protection
  - Short circuit in charge protection
  - Short circuit in discharge protection with 2 levels
- Software protection
  - Cell overvoltage protection
  - Cell undervoltage protection
  - Overcurrent in charge protection in 2 levels
  - Overcurrent in discharge protection in 2 levels
  - Over-temperature in charge protection
  - Over-temperature in discharge protection
  - Under-temperature in charge protection
  - Under-temperature in discharge protection
  - Over-temperature MOSFET protection
  - Pre-charge timeout protection
  - Host watchdog timeout protection
  - Fast charge timeout protection
  - Overcharge protection
  - Overcharging voltage protection
  - Overcharging current protection
  - Over pre-charge current protection

- Overcurrent protection by CHG+DSG MOSFET drop voltage

17.5 Secondary (2nd Level) Safety Features

The secondary safety features of the RT9440 can be used to indicate more serious faults via the FUSE pin. This pin is used to blow an in-line fuse and permanently disable the battery pack.

For detailed descriptions of each protection function, refer to the RT9440 Technical Reference Manual.

- Safety cell overvoltage permanent failure
- Safety cell undervoltage permanent failure
- Safety overcurrent in charge permanent failure
- Safety overcurrent in discharge permanent failure
- Safety overtemperature cell permanent failure
- Safety overtemperature MOSFET permanent failure
- Cell balancing permanent failure
- Qmax imbalance permanent failure
- Capacity degradation permanent failure
- Voltage imbalance at rest permanent failure
- Voltage imbalance active permanent failure
- Charge MOSFET permanent failure
- Discharge MOSFET permanent failure
- Fuse failure permanent failure
- AFE register permanent failure
- 2nd protection permanent failure
- PTC permanent failure
- Open thermistor permanent failure
- Program memory checksum permanent failure
- Data memory permanent failure
- AFE communication permanent failure

The RT9440 charge control features include:

- Supports JEITA temperature ranges and reports the charging voltage and the charging current according to the active temperature and voltage range
- 7-stage programmable temperature range
- 3-stage programmable voltage range
- Bidirectional hysteresis for temperature and voltage

17.6 Charge Control

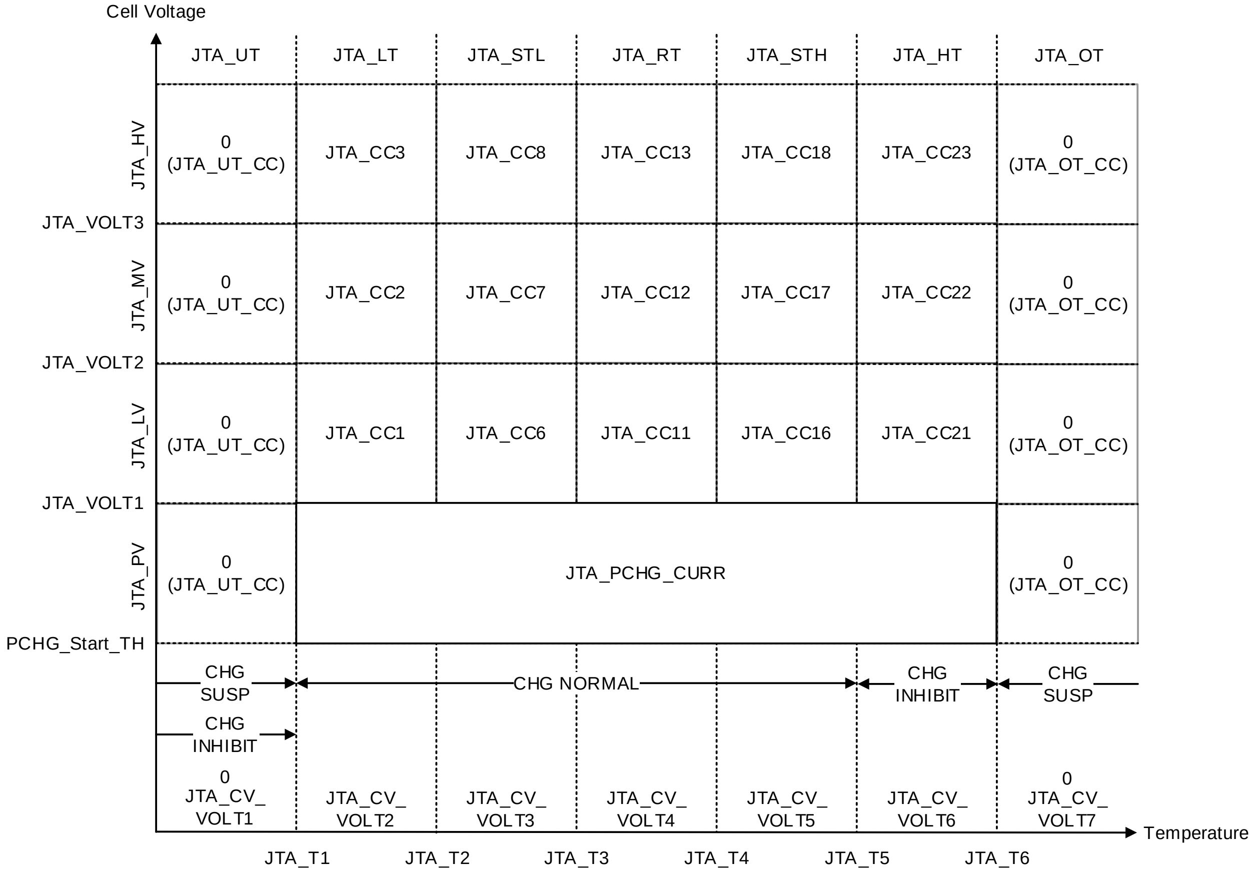


Figure 4. JEITA Temperature and Voltage Range

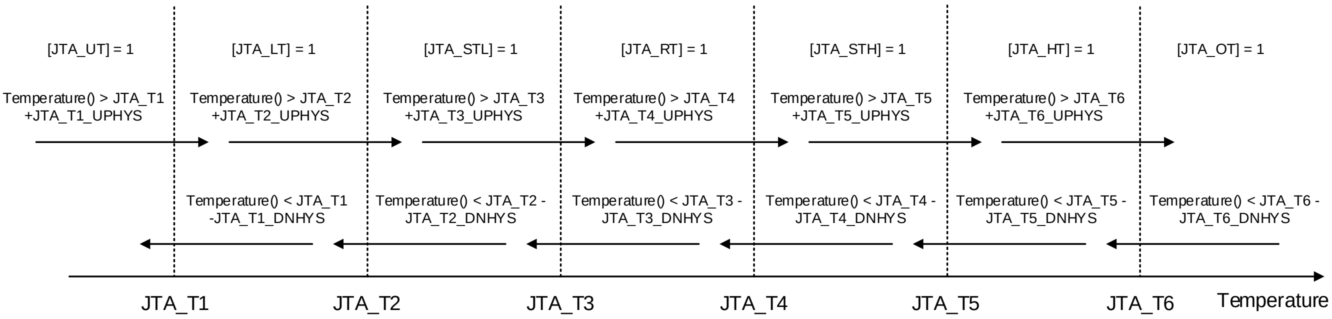


Figure 5. Bidirectional Hysteresis

- Report the charging current and charging voltage after compensation to a smart charger using SMBus broadcasts.
  - Report the compensated charging voltage for voltage drop of MOSFET.
  - Report the compensated charging voltage due to degradation by temperature and voltage to prevent cell swelling.
  - Report the compensated charging voltage and charging current due to degradation by cycle, SOH or runtime.
- Supports pre-charging and zero-voltage charging.
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range.
- Reports charging fault and also indicates charge status via charge and discharge alarms.

17.7 Cell Balancing Control

The RT9440 supports passive cell balancing with embedded bypass switches and can balance multiple cells simultaneously during charging or rest. The cell balance algorithm determines the capacity needed to be bypassed to balance of all cells. The RT9440 also supports voltage-base cell balancing. With up to 10mA bypass current using internal bypass switches, the device can achieve higher cell balance current by using an external cell balancing circuit.

17.8 Auxiliary LDO Provides Two Features

The auxiliary LDO provides a configurable output voltage from 1.5V to 3.3V and delivers up to 6mA output current. It can drive the always-on circuit, such as the RTC power and it is also used for GPIO power source.

- The RT9440 can work in deep sleep mode to reduce quiescent but keep VOUT to drive always-on circuits (e.g., RTC).
- VOUT turns off when cell voltage is lower than configurable threshold to prevent over discharge, over-temperature, under-temperature, battery removal, or abnormal current consumption.

17.9 Load Detection and Charger Detection

The load and charge detection feature stops the MOSFETs from toggling on and off continuously when there is a persistent faulty condition.

- Load detection can monitor the PACK pin voltage. If the PACK pin voltage is over 1V, the load is considered removed.
- The device integrates a source current to detect the PACK pin voltage. The current level can be configured from 10μA to 40μA.

For example, if the BAT voltage is 16V, the load equivalent resistance is 30kΩ, and the configured load detection source current is 20μA:

- If the load is present, the PACK voltage is 0.8V (under 1V).
- If the load is removed, the PACK voltage is 16V (over 1V).

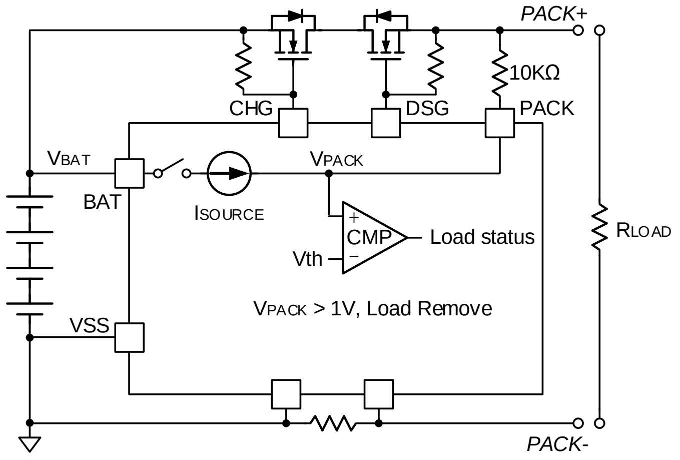


Figure 6. Load Detection

- Charger detection can compare the BAT pin voltage with the PACK pin voltage. If the differential voltage between the BAT pin voltage and the PACK pin voltage is over 0.1V, the charger is considered removed.

For example, if the BAT voltage is 16V and the charger CV is 17.6V:

- If the charger is present, the differential voltage between the BAT pin voltage and the PACK pin voltage is 1.6V.
- If the charger is removed, the differential voltage between the BAT pin voltage and the PACK pin voltage is 0.7V (body diode forward voltage).

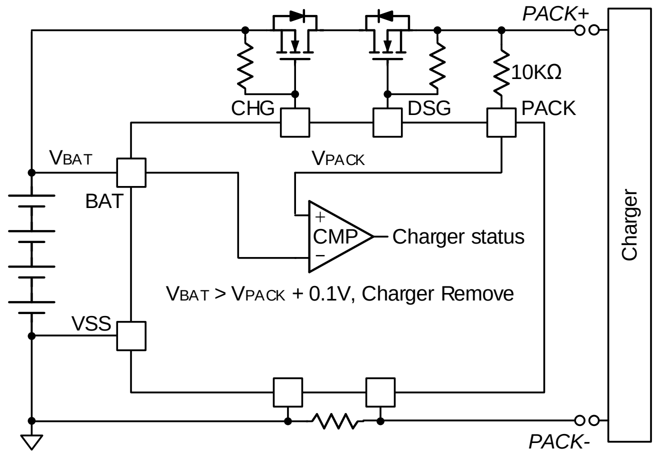


Figure 7. Charger Detection

17.10 Black Box Recorder

- Record the last three safety statuses to black box when permanent failure occurs.
- Update the lifetime log when a permanent failure occurs.
- Record additional three permanent failure statuses to black box after the first permanent failure occurs.

17.11 Lifetime Data Log

The RT9440 supports lifetime logging of important battery data. The following data are updated every 10 hours if a difference is detected between values in RAM and data flash:

- Maximum and minimum cell voltages
- Maximum delta cell voltage

- Maximum charge current
- Maximum discharge current
- Maximum average discharge current
- Maximum average discharge power
- Maximum and minimum cell temperature
- Maximum delta cell temperature
- Maximum and minimum internal sensor temperature
- Maximum MOSFET temperature
- Number of safety events occurrences and the last cycle of the occurrence
- Number of valid charge termination and the last cycle of the valid charge termination
- Number of Qmax updates and the last cycle of the Qmax updates
- Number of shutdown events
- Cell balancing time for each cell
- Total FW runtime and time spent in each temperature range.

17.12 Intel® Dynamic Battery Power Technology (DBPT V2.0)

The RT9440 supports DBPT V2.0 by providing the available max power and max current to prevent system reset or trigger termination voltage under peak loading.

17.13 IATA Support

The RT9440 supports several commands and procedures to satisfy the IATA criteria when the battery pack is in shipping.

17.14 LED Display

The RT9440 can drive up to 6-segment LED display for remaining capacity indication and/or a permanent failure code indication.

17.15 FUSE Driver

The RT9440 can use FUSE driver to blow an in-line fuse and permanently disable the battery pack.

17.16 PTC Permanent Failure

The RT9440 supports PTC overtemperature detection. Place PTC close to the CHG and DSG MOSFETs to monitor the temperature of MOSFETs. The PTC pin monitors the voltage at the pin and will trip if the thermistor resistance exceeds the defined threshold. To connect both PTC and PTCEN to VSS to disable PTC function.

17.17 Battery Trip Point (BTP)

The RT9440 supports the Battery Trip Point (BTP) feature that indicates when the Relative State of Charge (RSOC) has depleted to a set value in a data flash. This feature allows a host to program two capacity-based thresholds that govern the triggering of a BTP interrupt on the BTP_INT pin.

17.18 Emergency Shutdown

The emergency shutdown feature enables a push button action that connects the $\overline{\text{SHUTDN}}$ pin to shut down the battery pack system before removing the battery. A high-to-low signal on the $\overline{\text{SHUTDN}}$ pin turns off the CHG and DSG MOSFETs, disconnecting the power from the system to safely remove the battery pack. The CHG and DSG

MOSFETs can be turned on again by another high-to-low signal detected by the $\overline{\text{SHUTDN}}$ pin or when a data flash configurable timeout is reached.

17.19 System Present Operation

The RT9440 checks $\overline{\text{PRES}}$ periodically (every 1 second). If $\overline{\text{PRES}}$ input is pulled to ground by the external system, the RT9440 detects this as the system being present.

17.20 2-Series, 3-Series, 4-Series, or 5-Series Cell Configuration

In a 2-series cell configuration, VC4 is shorted to VC3, VC3, and VC2. In a 3-series cell configuration, VC4 is shorted to VC3.

17.21 Communication

The RT9440 uses SMBus in MASTER mode with packet error checking (PEC) options, in accordance with the SBS specification.

17.22 SMBus On and Off State

The RT9440 detects an SMBus off state when both SMBC and SMBD are low for two or more seconds, then enters sleep mode. Clearing this state requires either SMBC or SMBD to transition high, which will cause and device to enter normal mode from sleep mode.

17.23 SBS Commands

Refer to the RT9440 Technical Reference Manual for detailed description.

17.24 Authentication

The RT9440 supports three authentications.

- HMAC SHA1 authentication
  - Key 16 bytes and challenge 20 bytes
  - Execution time 1ms
- HMAC SHA256 authentication
  - Key 32 bytes and challenge 32 bytes
  - Execution time 2ms
- ECC authentication
  - Use SECG recommended ECC curve

163 bit ECC signature execution time is within 150ms, and 233 bit ECC is within 250ms.

17.25 Cell Voltage Measurement Circuit

- Place an input RC filter between VCx pin for ESD protection and filter unwanted voltage transients.
- Please select 100Ω resistor for R22, R23, R27 and R30. The resistors can be traded off for cell balancing current requirements. Select a 0.1μF capacitor for C14, C15, C16, and C18.
- The impedance of VC4, VC3, VC2, VC1 and VSS must be as minimal as possible. Make Kelvin sense connections to each cell’s positive and negative terminals to minimize the IR drop effect on voltage measurement accuracy.
- The impedance between the positive terminal of the top cell and the BAT pin must be as minimal as possible (under 0.3Ω).

- For applications with fewer than 4 cells. It is suggested to use a Schottky diode with a forward voltage under 0.3V for D1.

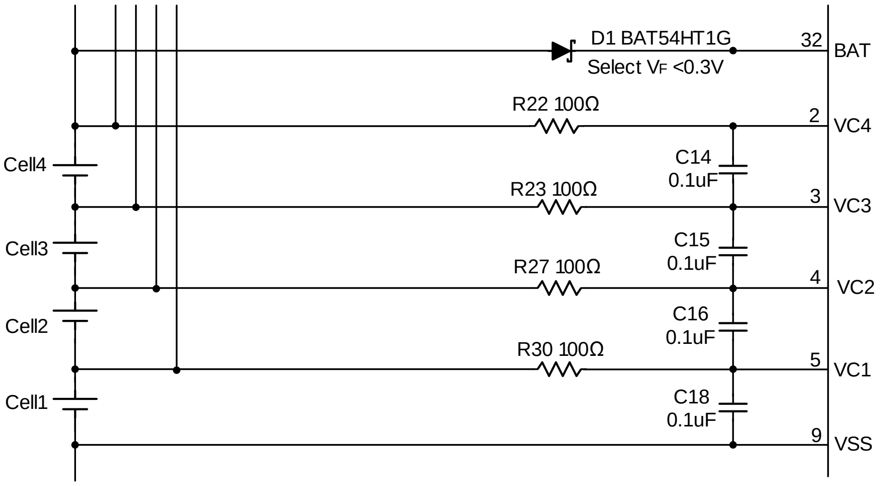


Figure 8. Cell Voltage Measurement Circuit

17.26 Current Measurement Circuit

- The CSP and CSN pins monitor the voltage of current sensing resistor R38, with a resistor value range is from 0.5mΩ to 10mΩ, depending on the current protection and thermal requirements. It is suggested to minimize the impedance between CSP and VSS to keep the voltage of VCSP - VSS, and VCSN – VSS under the ROC requirement (±0.2V) when a short circuit occurs.
- The current sensing resistor must have a low temperature coefficient (<50ppm) to minimize the current drift with temperature.
- Place a low-pass filter for input noise. Select a 100Ω resistor for R34 and R35, and 0.1μF for C17. 0.1μF capacitors C19 and C20 can be used a Y filter to reduce specific interferences or noise sources, further improving the accuracy of current measurements.
- The CSN and CSP paths must make Kelvin Sense connection to R38 to avoid the IR drop effect on current measurement accuracy.

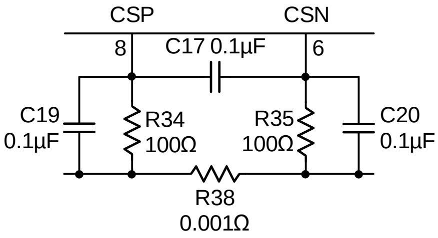


Figure 9. Current Measurement Circuit

17.27 External Temperature Measurement Circuit

- ADC voltage measurement pins (TS1, TS2, TS3, TS4, TS5) are assigned for NTC thermistors.
- Each pin can be enabled with an integrated pull-up resistor (typical 15kΩ) and a pull-down resistor (typical 30kΩ) to support the use of a 10kΩNTC external thermistor at 25°C (B = 3435k) for RT1 to RT5. Also, place an NTC for monitor temperature for high-side MOSFET.
- TS4 is a multi-function pin and disables ADC measurement function when AUX LDO is enabled.

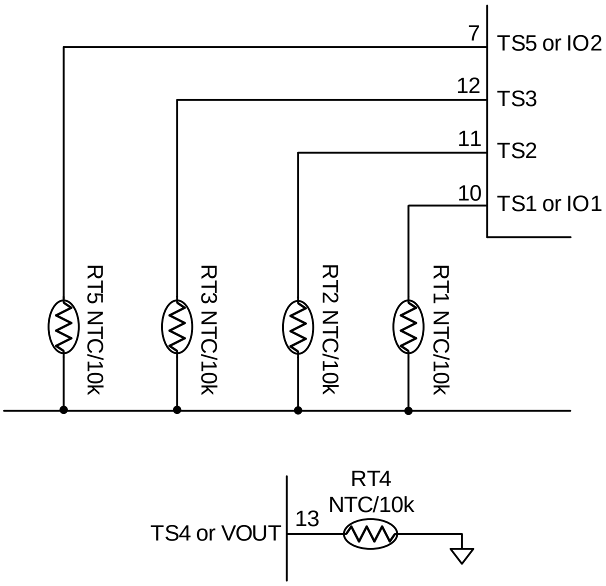


Figure 10. External Temperature Measurement Circuit

17.28 PACK Detection Circuit

- The VCC pin provides power to RT9440 when the PACK pin detects a charger plug-in. The device integrates a PACK detection circuit to monitor the charger status.
- It is recommended to use a 10kΩ resistor for R16.

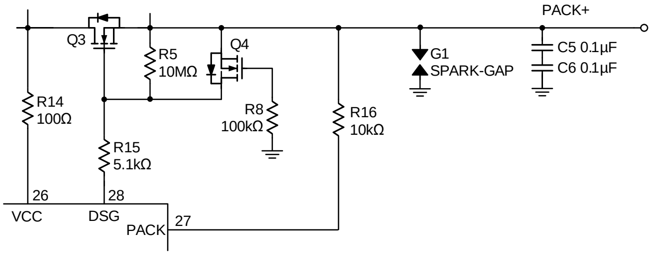


Figure 11. PACK Detection Circuit

17.29 PBI Capacitor

- The device has internal LDO power without external capacitor.
- The PBI pin provides a power supply backup function, supplying power during short transient power outages.
- It is necessary to place a 2.2µF capacitor for C13.

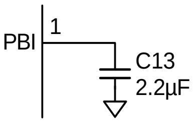


Figure 12. PBI Capacitor

17.30 High-Side N-MOSFETs and P-MOSFET Control Circuit

- N-MOSFETs (Q2 and Q3) are used for charge and discharge current path switch. The MOSFETs should be 30V devices with low Ron to address thermal issues. The gate driver voltage and AMR should consider the RT9440 VCHGON or VDSGON design voltage.
- P-MOSFET (Q1) for pre-charge operation and R1 is for limiting the pre-charge current.

- R12, R13 and R15 are used for gate protection and Q1/Q2/Q3 MOSFETs noise reduction. A 5.1kΩ resistor is recommended to provide a microsecond switching time constant.
- R7, R4 and R5 are used to fix Q1/Q2/Q3 MOSFETs gate voltage to keep them in a stable off state when turned off. A 10MΩ resistor is recommended to prevent voltage drop.
- Q4 is located between gate and source of Q3 to turn off Q3 when the charger is reversely connected.
- C1 and C2 can protect the MOSFETs for ESD. Use two capacitors to ensure normal operation if one shorts.

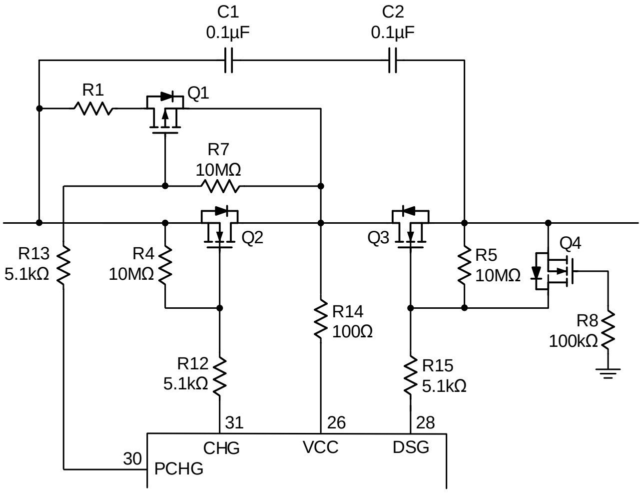


Figure 13. High-Side N-MOSFETs and P-MOSFET Control Circuit

17.31 Fuse Pin Control Circuit

- The FUSE pin is designed to ignite the chemical fuse if any safety event occurs and also monitors the 2nd protection IC. The fuse will blow when the FUSE pin or the OUT pin of the 2nd protection IC is high, causing Q5 to turn on.
- The R10, R11 and R19 need to ensure that the divided voltage from the OUT pin or the FUSE pin voltage is high enough to provide a gate driver voltage to turn on Q5.
- It is recommended to use 5.1kΩ resistors for R10 and R19, and a 51kΩ resistor for R11.
- Connect the FUSE pin to VSS if not used.

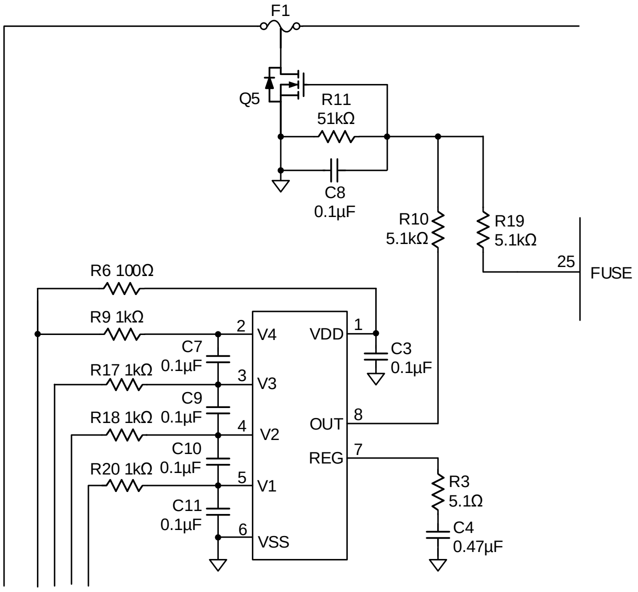


Figure 14. FUSE Pin Control Circuit

17.32 PTC Over-Temperature Detection Circuit

- PTC circuit to monitor temperature when PTCEN connects to the BAT pin. Connect PTCEN to GND if not used.
- It is recommended to place PTC thermistor (R21) close to the CHG/DSG MOSFETs to monitor the temperature.
- The PTC pin monitors the voltage of PTC thermistor and will trip if the thermistor resistance exceeds the defined threshold.

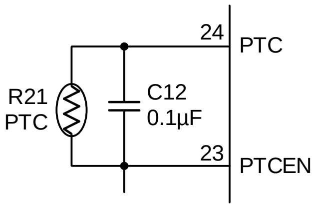


Figure 15. PTC Circuit

17.33 LEDs Control Circuit

- LED control pins can provide sink current to driver external LEDs.
- Supports up to six LEDs.
- For applications with six LEDs, it is suggested to use LEDs with low forward voltage to reduce the forward current of other LEDs when one LED is on.
- Let the LEDCNTL pins float if not used, and connect the $\overline{\text{DISP}}$ pin to GND if not used.

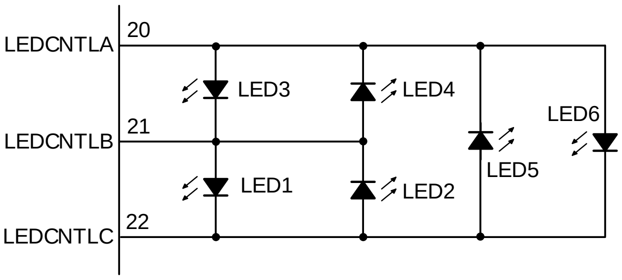


Figure 16. LEDs Control Circuit

17.34 VOUT Circuit

- The TS4 pin is a multi-function pin and can be configured for the VOUT function.
- VOUT can provide power to drive the always-on circuits, such as the RTC, when the AUX LDO is enabled.
- Place a 4.9Ω to 5.1Ω resistor for R37 and a 1μF capacitor for C19 to keep the output voltage stable. ZD1 is for ESD protection.

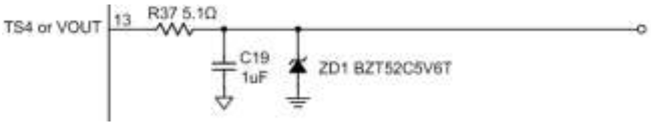


Figure 17. VOUT Circuit

17.35 SMBus Circuit

- For robust ESD protection, the ESD protection diodes (ZD4, ZD5) and resistor (R24, R26, R28, R29) are recommended.
- Use 100Ω resistors for R24, R26, R28, and R29.

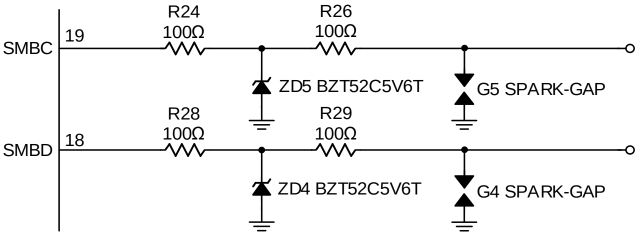


Figure 18. SMBus Circuit

17.36 System Present Circuit

- For a removable system host, the $\overline{\text{PRES}}$ pin can detect the system connection status.
- The $\overline{\text{PRES}}$ pin pulls up every 250ms and records the pin status. If the device continuously counts four low statuses, it detects the system as present.
- A resistor can be used to pull the pin low and a 20kΩ or lower resistor is recommended.
- For robust ESD protection, it is recommended to use an ESD protection diodes (ZD3) and resistors (R31, R32).
- Use 100Ω resistors for R31 and R32.

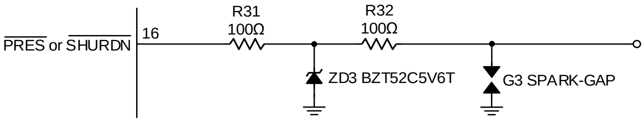


Figure 19. System Present Circuit

17.37 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a VQFN-32L 4x4 package, the thermal resistance, θ_{JA}, is 27.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (27.8°C/W) = 3.59W for a VQFN-32L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 20 allows the designer to estimate the effect of rising ambient temperature on the maximum power dissipation.

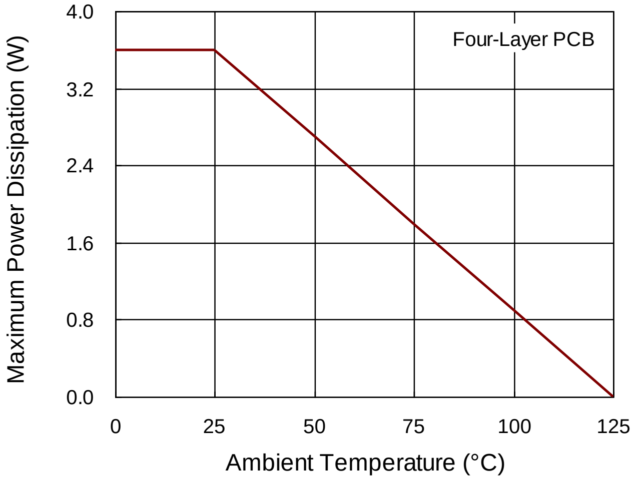


Figure 20. Derating Curve of Maximum Power Dissipation

17.38 Layout Considerations

1. The capacitor for the PBI pin must be placed as close as possible to the pin.

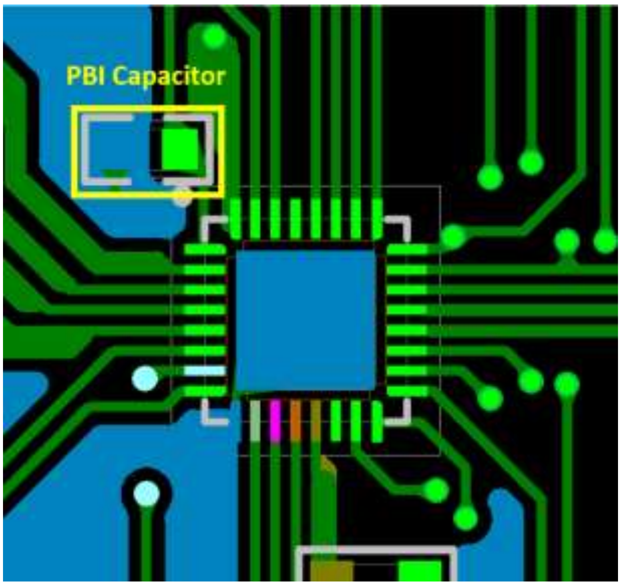
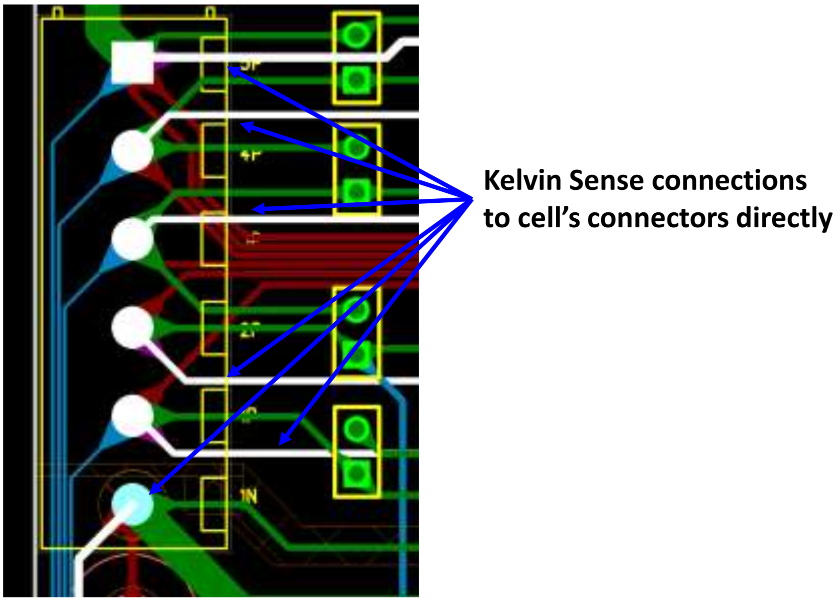


Figure 21. PBI Capacitor

2. The BAT, VC4, VC3, VC2, VC1 and VSS paths must make Kelvin sense connections to each cell's positive and negative terminals to minimize the IR drop effect on voltage measurement accuracy.



Kelvin Sense connections to cell’s connectors directly

Figure 22. Cell Voltage Sense Circuit

3. The CSN and CSP paths must make Kelvin Sense connections to RS to avoid the IR drop effect on current measurement accuracy.
    - Layout traces should be symmetrical for minimum current offset and noise pickup.
    - The Input filter should be placed as close as possible to the IC.

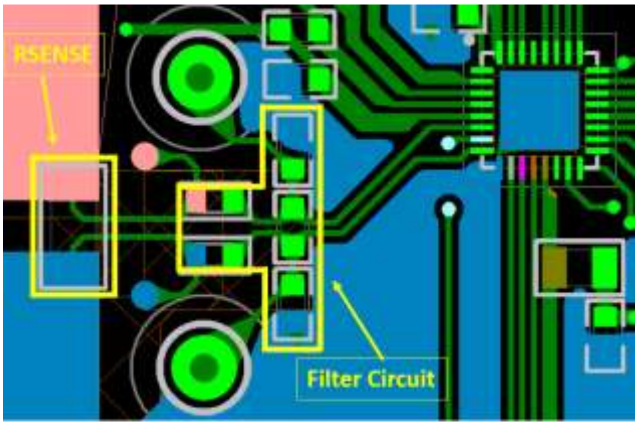


Figure 23. Current Sense Circuit

4. Place a spark gap at the communication connector to protect SMBC and SMBD from the system ESD.
    - It is suggested that the spacing between the points be 0.2mm.
    - The spark gap must be placed on outer layer of the PCB and cannot be coated with any protective covering.

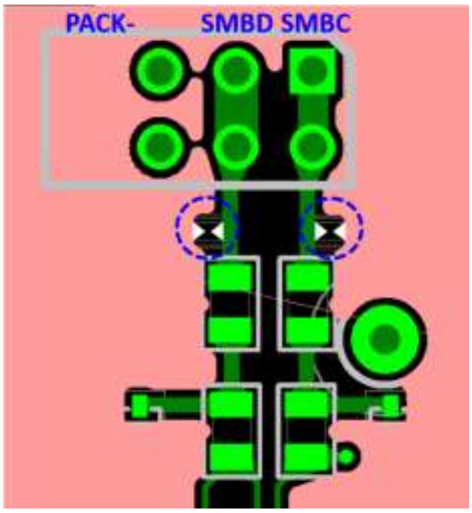


Figure 24. ESD Protection for Communication Interface

5. Place wide copper traces to eliminate the inductance of the CHG/DSG MOSFET Bypass and pack terminal bypass capacitor.

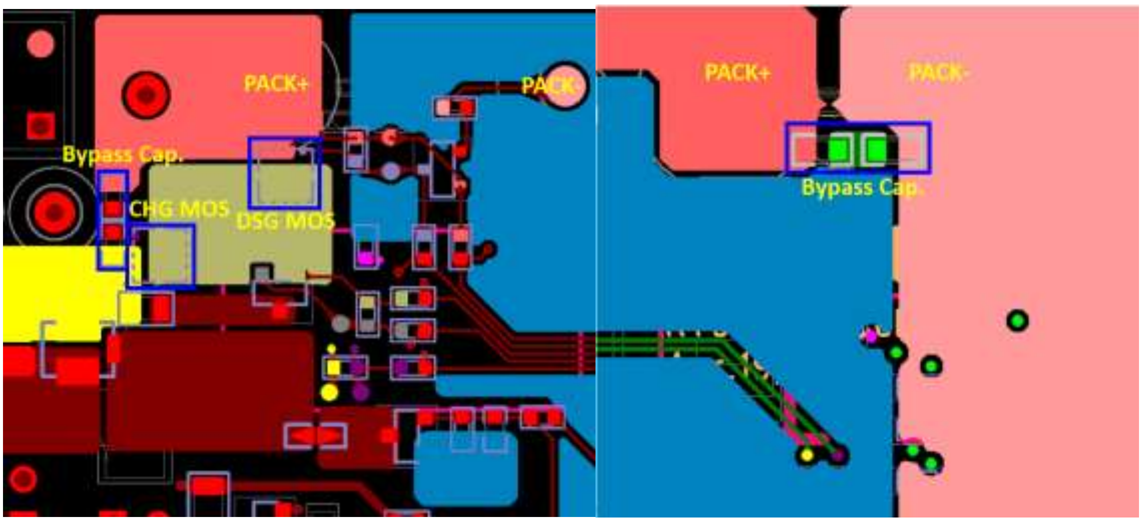


Figure 25. CHG/DSG MOSFET Circuit

6. The impedance between the top node of the top cell and the BAT pin must be as minimal as possible (under 0.3Ω for 5 cells).
    - The BAT trace must be wide and short.

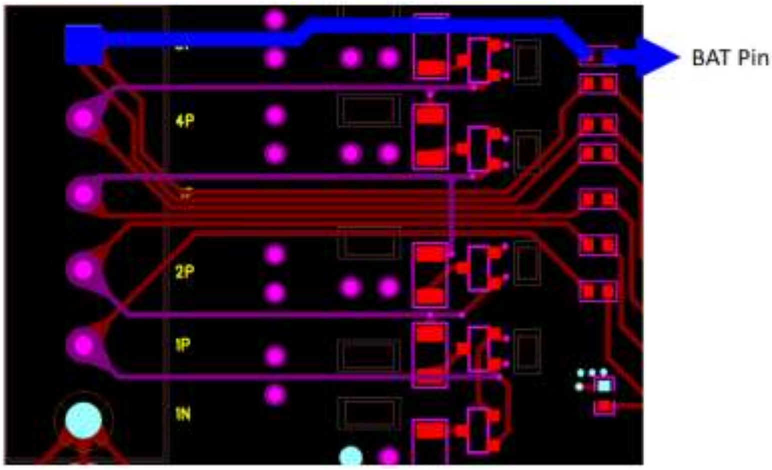


Figure 26. The BAT Power Pin

7. The impedance (RPCB) between CSP and VSS must be minimized.

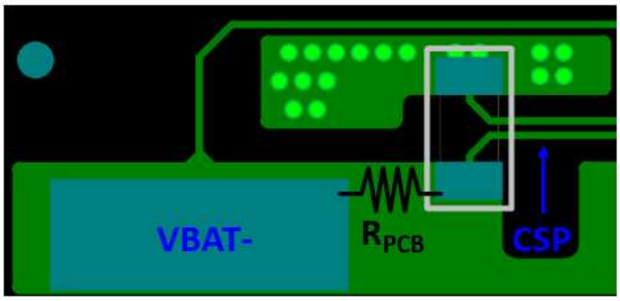


Figure 27. Impedance Minimization between VSS to CSP

8. Layout example

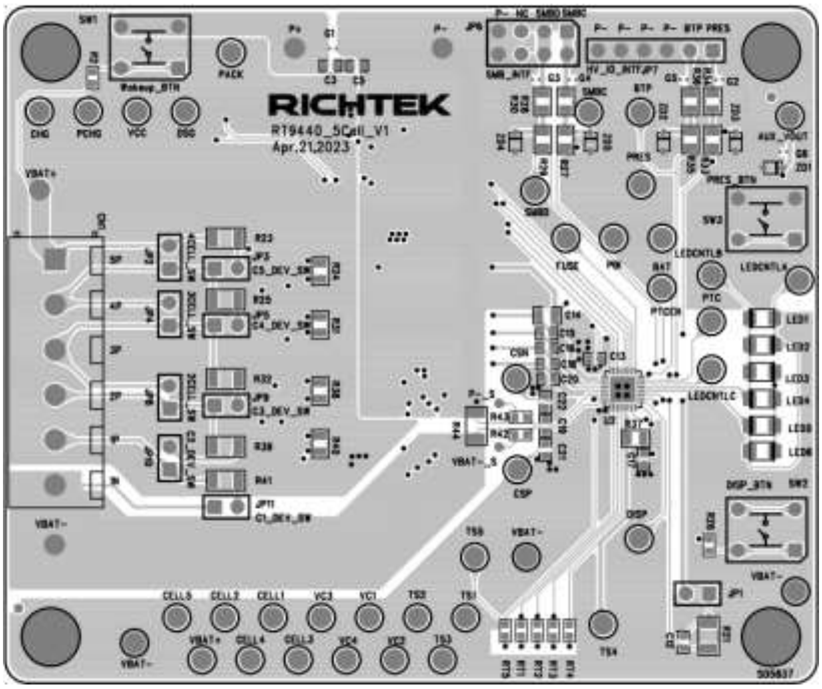


Figure 28. Top Layer

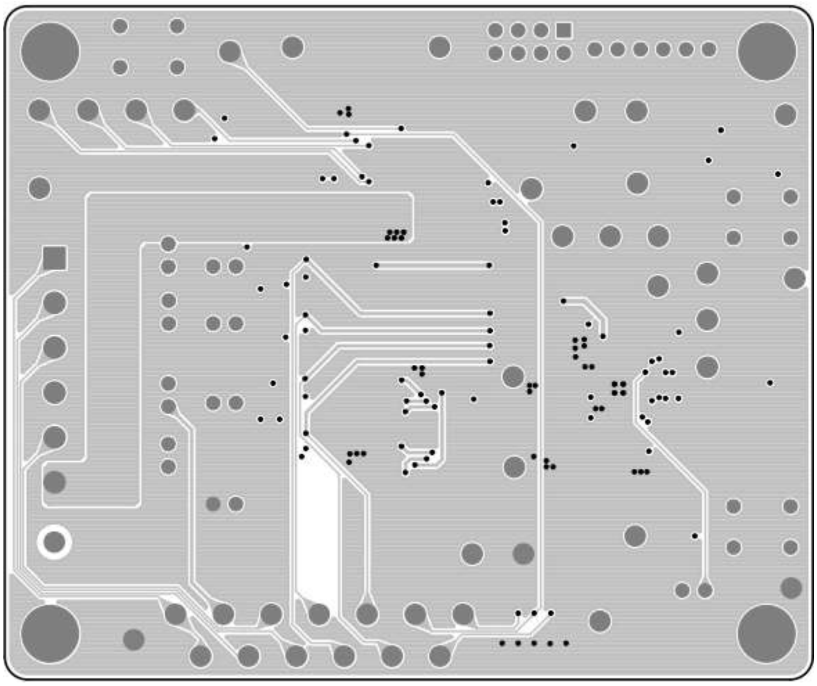


Figure 29. 2nd Layer

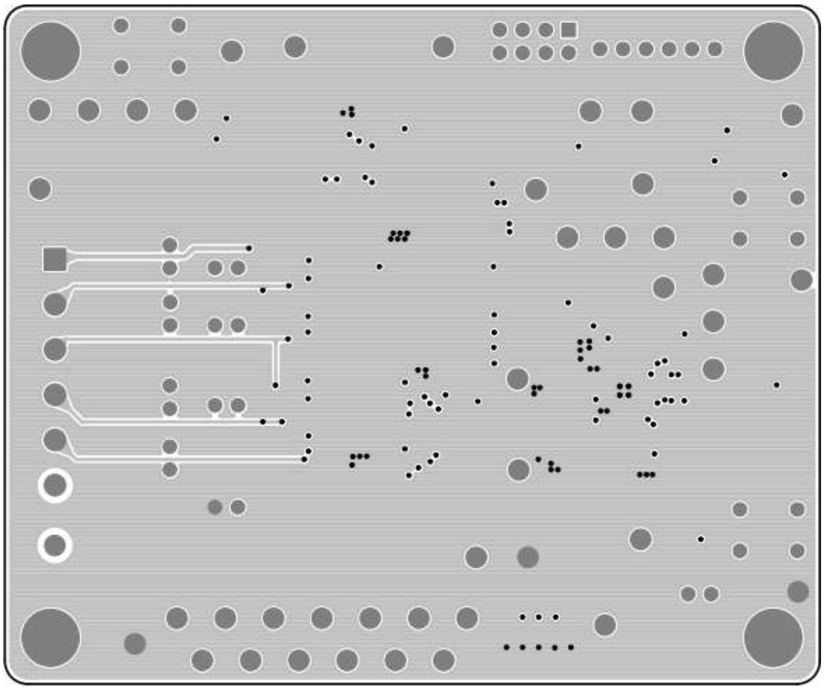


Figure 30. 3rd Layer

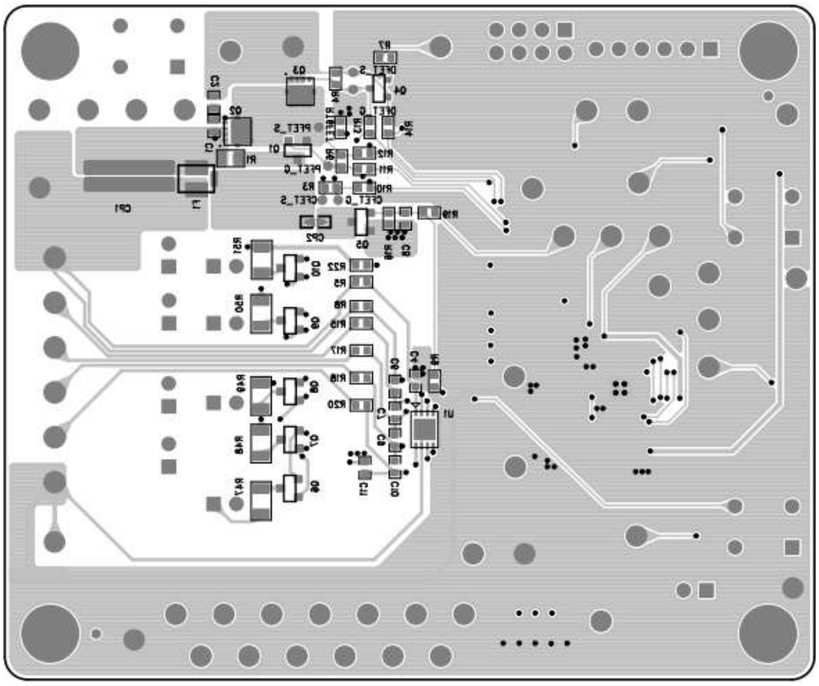
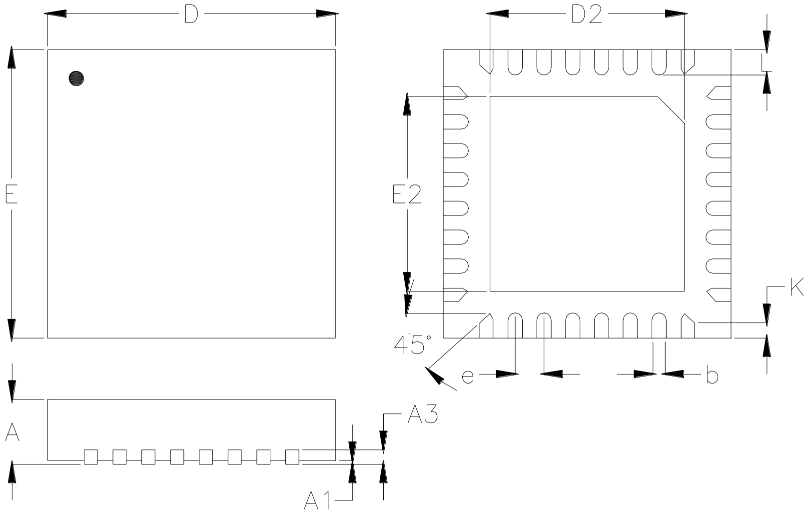
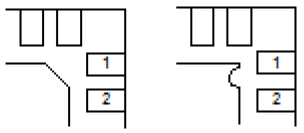


Figure 31. Bottom Layer

Note 6. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

18 Outline Dimension





DETAIL A

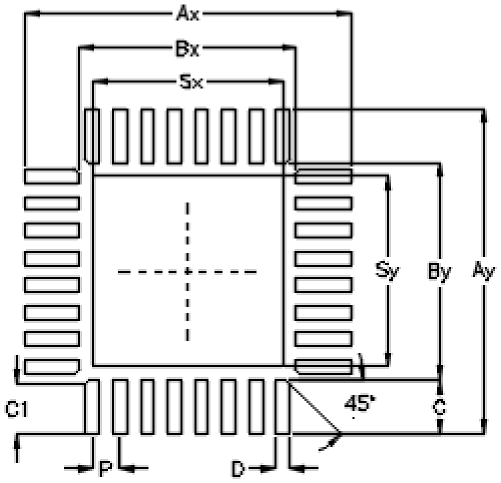
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	3.950	4.050	0.156	0.159
D2	2.650	2.750	0.104	0.108
E	3.950	4.050	0.156	0.159
E2	2.650	2.750	0.104	0.108
e	0.400		0.016	
L	0.300	0.400	0.012	0.016
K	0.200		0.008	

V-Type 32L QFN 4x4 Package

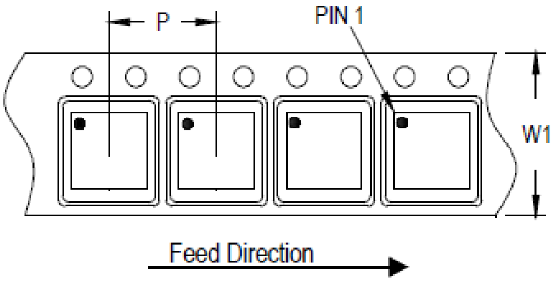
19 Footprint Information

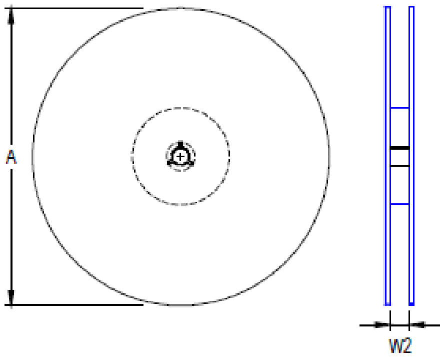


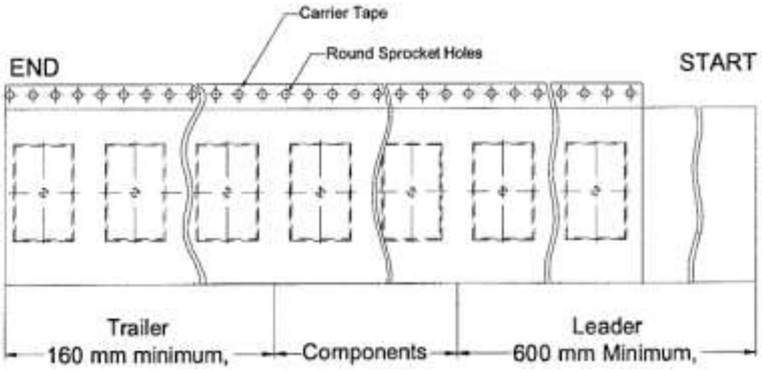
Package	Number of Pin	Footprint Dimension (mm)										Tolerance
		P	Ax	Ay	Bx	By	C*32	C1*8	D	Sx	Sy	
V/W/U/XQFN4*4-32	32	0.40	4.80	4.80	3.20	3.20	0.80	0.75	0.20	2.80	2.80	±0.05

20 Packing Information

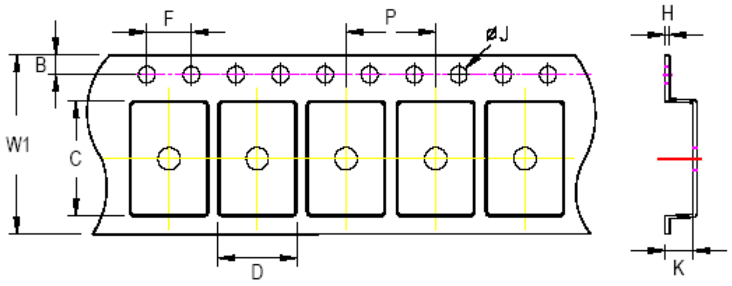
20.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 4x4	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN/DFN 4x4	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description
00	2024/6/17	*General Description* *Ordering Information* *Features* *Marking Information* *Simplified Application Circuit* *Functional Pin Description* *Pin Block Diagram* *Electrical Characteristics* *Typical Application Circuit* *Typical Operating Characteristics* *Application Information* *Packing Information*
01	2025/6/4	Ordering Information - Modified ordering information Simplified Application Circuit Pin Block Diagram Electrical Characteristics Typical Application Circuit Application Information Packing Information - Added Tape Size “K”