RICHTEK®

RT9441

2-to-4 Series Cell Fuel Gauge with Integrated Protection Solution for Li-Ion Battery Packs

1 General Description

The RT9441 device is a highly accurate and integrated, 2 to 4 series cell fuel gauge and protection solution. It features autonomous cell balancing, protection, and charger control.

The RT9441 integrates highly accurate analog peripherals to measure and maintain an accurate record of available capacity, voltage, current, and temperature. It reports the battery pack parameters to the system host controller via the SMBus interface.

The RT9441 is available in a WQFN-32L 4x4 package. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Ordering Information

RT9441 □-□□

Packing
A: Standard

Customized Firmware Code AABBX(1)
AA: Firmware Application Code
BB: Hardware Model Code
X: Firmware Version Code

Package Type(2)
N: WQFN-32L 4x4 (W-Type)
(Exposed Pad: Option 2)

Note 1.

- Marked with (1) indicates if the firmware code is empty, this field will be removed.
- Marked with (2) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

3 Applications

- Notebooks
- Power Tools
- Drones
- Tablets
- UPS/Battery Backup Systems
- Medical Equipment
- Handheld Vacuum Cleaners and Vacuum Robots

4 Features

- **State of Charge (SOC) Calculated by VoltaicGauge with Current Sensing (VGCS)**
- **Voltage Measurement Accuracy: ±3mV**
- **Current Measurement Accuracy: ±0.35%**
- **Battery Temperature Measurement Accuracy: ±1°C (T_A = 0°C to 45°C)**
- **Autonomous Cell Balancing**
- **Configurable Protection Levels and Delay Times for Voltage, Temperature, Current Protection**
- **Support Both Voltage-Based and SOC-Based Cell Balancing**
- **High-Side N-Channel MOSFET Drivers**
- **Low Power Consumption**
- **Normal Mode: 150μA**
- **Sleep Mode with DSG ON: 65μA**
- **Shutdown Mode: 0.5μA**
- **Low Value Sense Resistor: 1mΩ to 10mΩ**
- **SHA-1/SHA-256/Hardware ECC Authentication**
- **Support Intel Dynamic Battery Power Technology (DBPT V2.0)**
- **Lifetime Data Log and Black Box Recorder**
- **FUSE Driver**
- **Support up to 1MHz SMBus Interface**
- **IATA Support**
- **32 Pin WQFN Package with 0.4mm Pitch**

5 Marking Information

KG=: Product Code
YMDAN: Date Code

6 Simplified Application Circuit

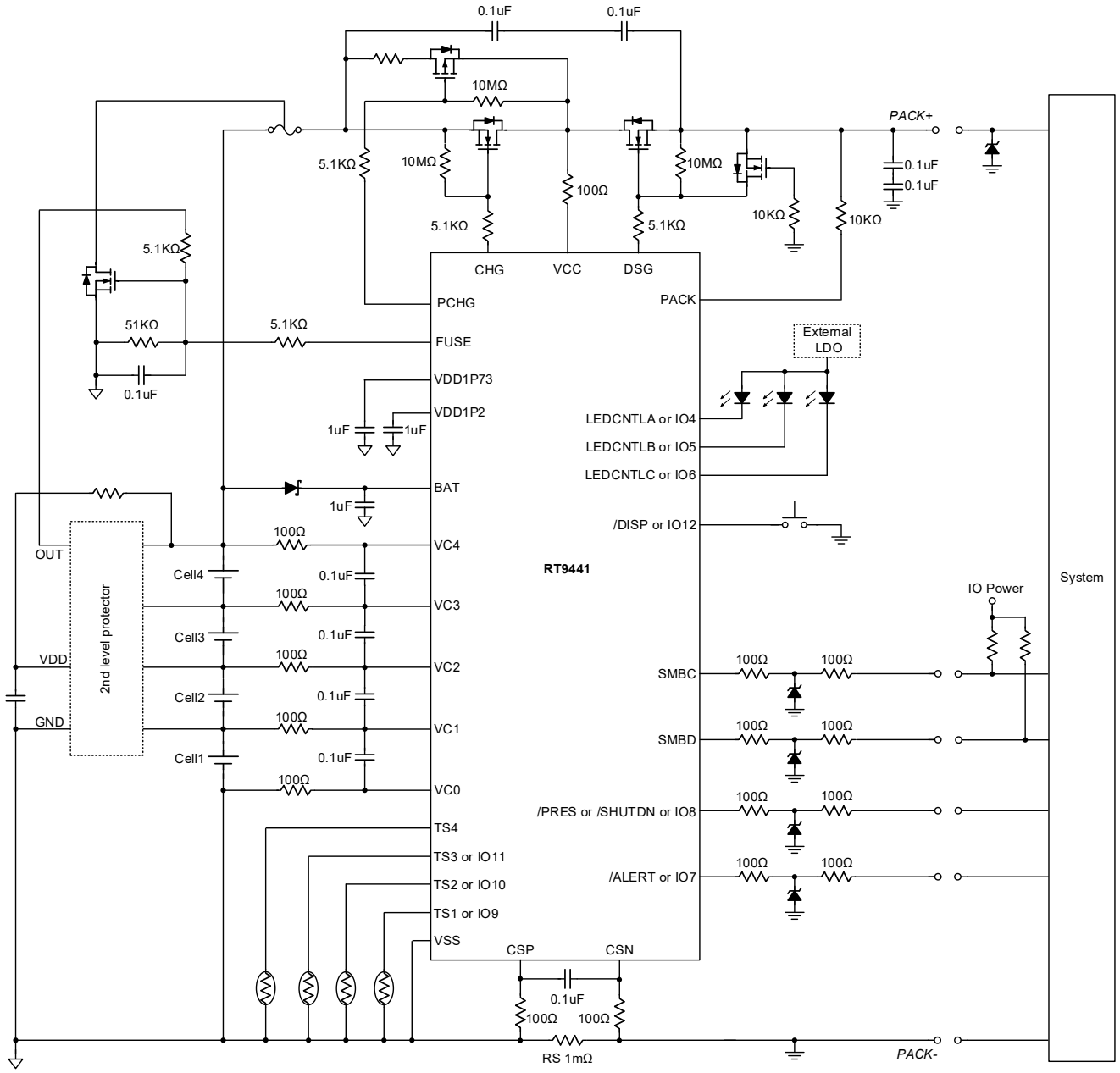
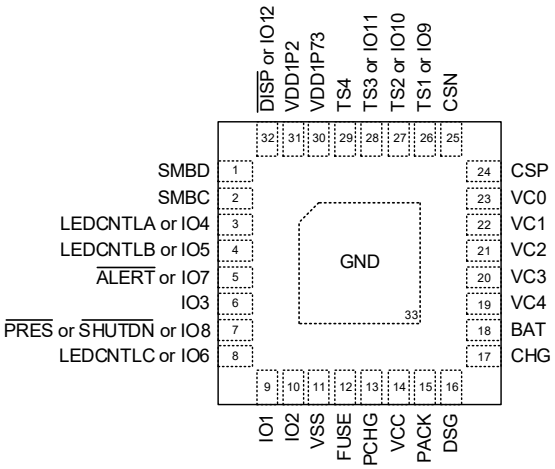


Table of Contents

7 Pin Configuration

(TOP VIEW)



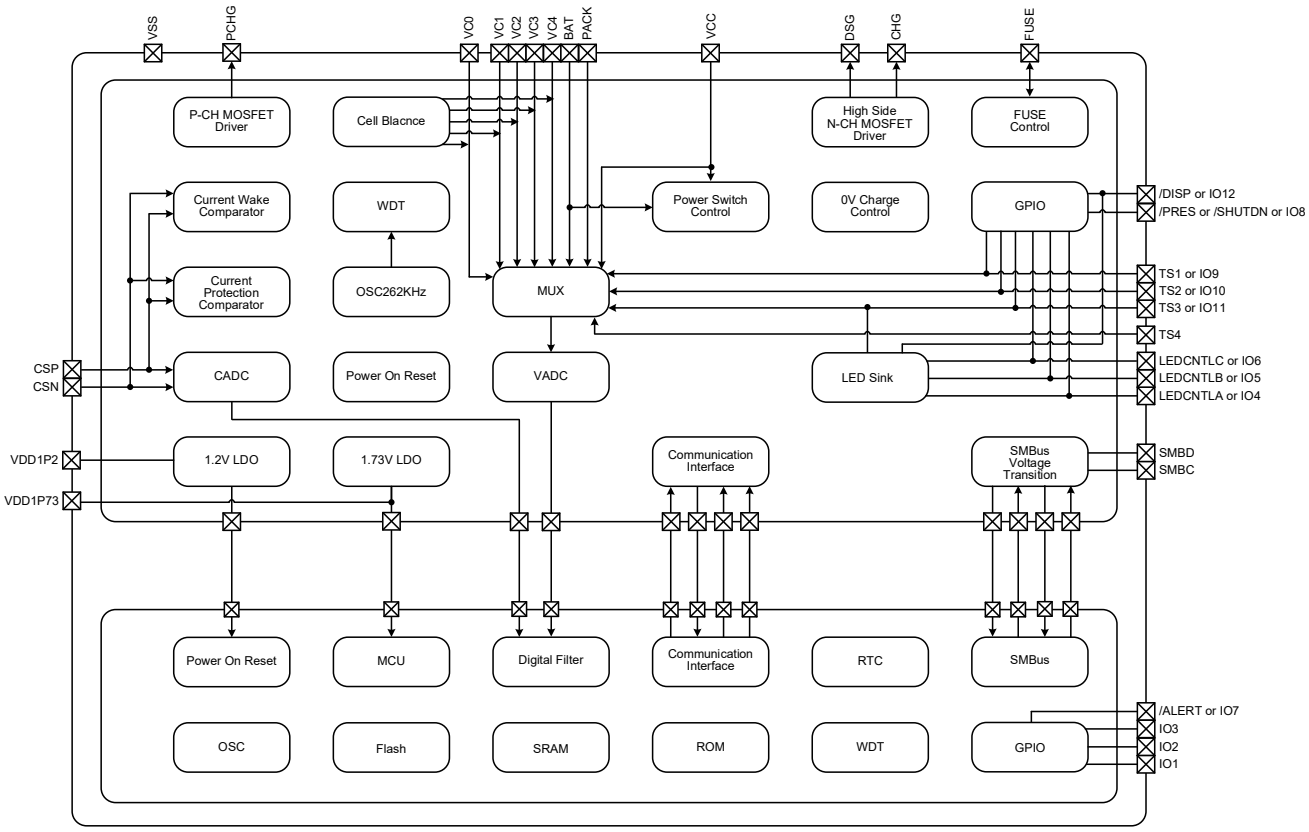
WQFN-32L 4x4

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	SMBD	SMBus data pin
2	SMBC	SMBus clock pin
3	LEDCNTLA or IO4	LED display segment drives external LEDs using an internal sink current. It can also be optionally function as a multi-function GPIO. It should be left floating or connected to VSS if it is not used.
4	LEDCNTLB or IO5	LED display segment drives external LEDs using an internal sink current. It can also be optionally function as a multi-function GPIO. It should be left floating or connected to VSS if it is not used.
5	$\overline{\text{ALERT}}$ or IO7	The alert output pin, or multi-function GPIO. It should be left floating if it is not used.
6	IO3	Multi-function GPIO. It should be left floating if it is not used.
7	$\overline{\text{PRES}}$ or $\overline{\text{SHUTDN}}$ or IO8	Host system presents input for removable battery pack or emergency shutdown for non-removable battery pack input pin. No external pull-up resistor is required. It can also be optionally function as multi-function GPIO. It should be left floating or connected to VSS if it is not used.
8	LEDCNTLC or IO6	LED display segment drives external LEDs using an internal sink current. It can also be optionally functioned as multi-function GPIO. It should be left floating or connected to VSS if it is not used.
9	IO1	Multi-function GPIO. It should be left floating if it is not used.
10	IO2	Multi-function GPIO. It should be left floating if it is not used.
11	VSS	Ground.
12	FUSE	Fuse drive output pin. It should be connected to VSS if it is not used.

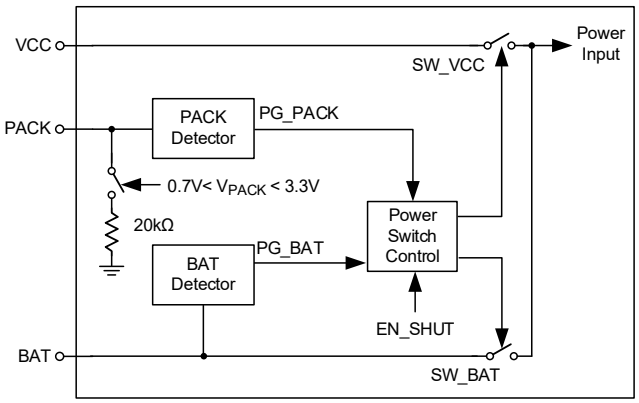
Pin No.	Pin Name	Pin Function
13	PCHG	PMOS pre-charge MOSFET drive output pin. It should be left floating if it is not used.
14	VCC	Secondary power supply input pin.
15	PACK	Pack sense input pin.
16	DSG	N-Channel MOSFET driving output pin for discharge MOSFET control.
17	CHG	N-Channel MOSFET driving output pin for charge MOSFET control.
18	BAT	Primary power supply input pin. Select a 1μF capacitor connected to VSS.
19	VC4	The voltage input pin is for the 4th cell. The balance current input is for the 4th cell.
20	VC3	The voltage input pin is for the 3rd cell. The balance current input is for the 3rd cell and return the balance current for the 4th cell.
21	VC2	The voltage input pin is for the 2nd cell. The balance current input is for the 2nd cell and return the balance current for the 3rd cell.
22	VC1	The voltage input pin is for the 1st cell. The balance current input is for the 1st cell and return the balance current for the 2nd cell.
23	VC0	The voltage input pin for the negative terminal of the 1st cell. Return the balance current for the 1st cell.
24	CSP	Battery current sensing positive input.
25	CSN	Battery current sensing negative input.
26	TS1 or IO9	Temperature sensor 1 measurement input pin, or multi-function GPIO. It should be left floating or connected to VSS if it is not used.
27	TS2 or IO10	Temperature sensor 2 measurement input pin, or multi-function GPIO. It should be left floating or connected to VSS if it is not used.
28	TS3 or IO11	Temperature sensor 3 measurement input pin, or multi-function GPIO. LED display segment that drives the external LEDs by an internal sink current. It should be left floating or connected to VSS if it is not used.
29	TS4	Temperature sensor 4 measurement input pin. It should be left floating or connected to VSS if it is not used.
30	VDD1P73	Internal regulator output. Select a 1μF capacitor connected to VSS.
31	VDD1P2	Internal regulator output. Select a 1μF capacitor connected to VSS.
32	$\overline{\text{DISP}}$ or IO12	LED display segment drives external LEDs using an internal sink current. It can also be optionally function as multi-function GPIO. It should be left floating or connected to VSS if it is not used.
33 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

9 Functional Block Diagram

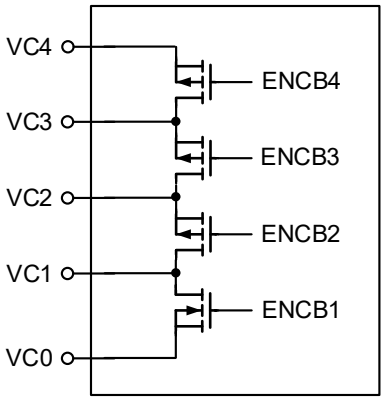


10 Pin Block Diagram

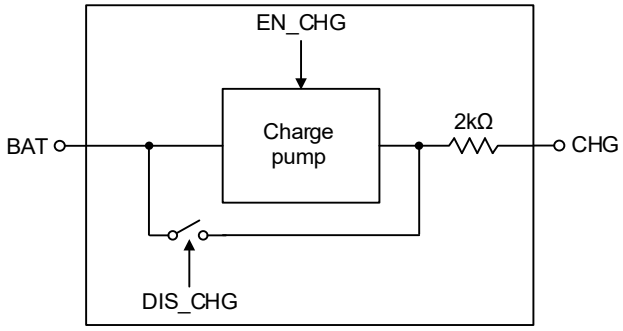
Power Switch Control



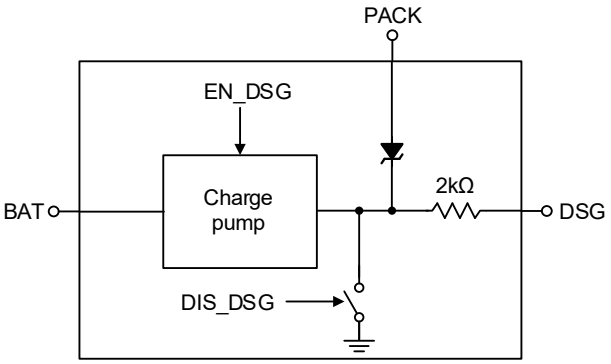
Cell Balancing



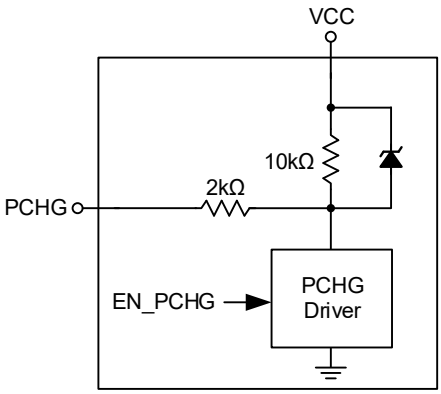
CHG Driver



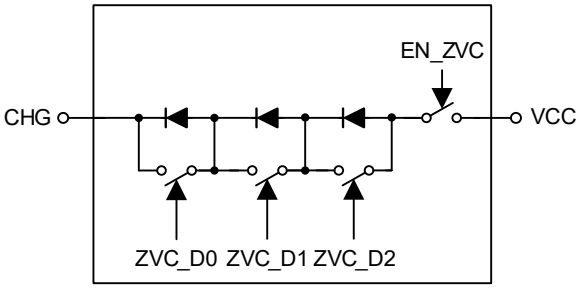
DSG Driver



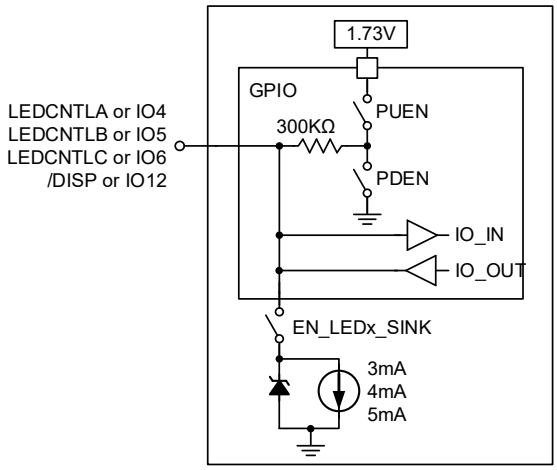
PCHG Driver



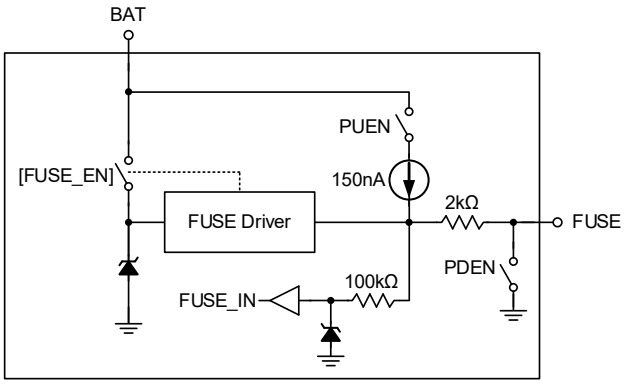
Zero Voltage Control



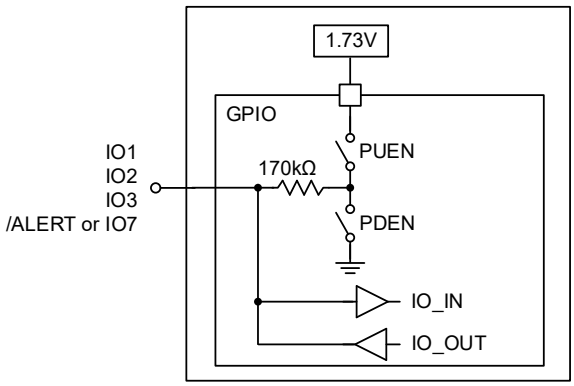
LEDCNTLA or IO4, LEDCNTLB or IO5, LEDCNTLC or IO6, /DISP or IO12



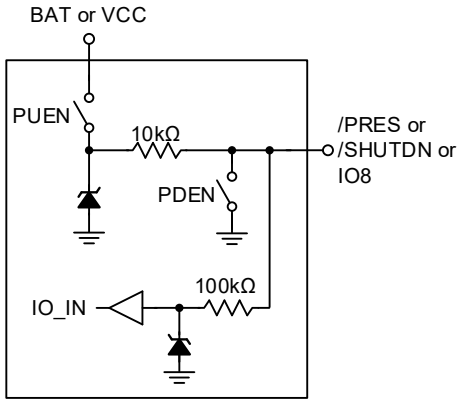
FUSE Control



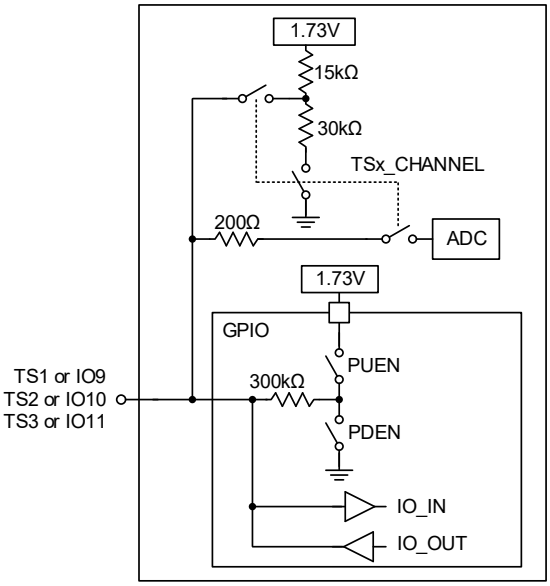
IO1, IO2, IO3 and /ALERT or IO7



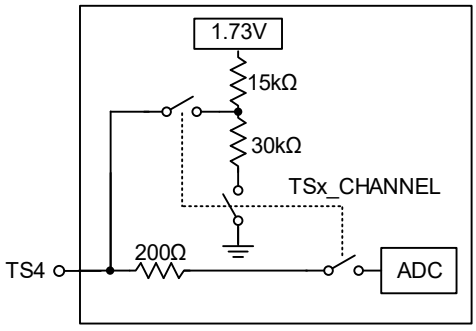
IO8 or /PRES



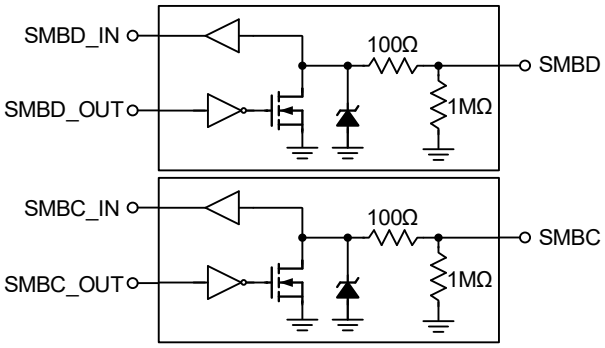
TS1 or IO9, TS2 or IO10, and TS3 or IO11



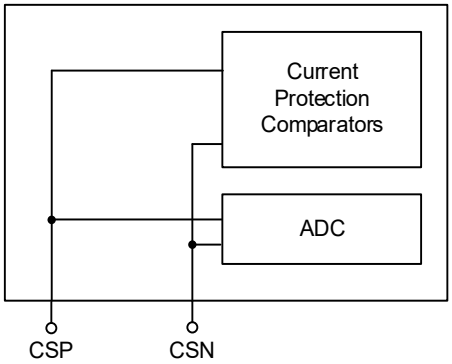
TS4



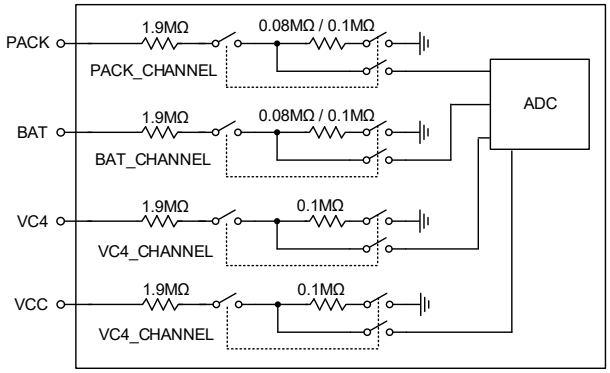
SMBD and SMBC



OCD1, OCD2, OCC, SCD Comparators, and CADC



VC4, BAT, VCC, and PACK Dividers



11 Absolute Maximum Ratings

(Note 2)

- Supply Voltage on VCC to VSS ---------- –0.3V to 30V
- Input Voltage on PACK, BAT, $\overline{\text{PRES}}$ or $\overline{\text{SHUTDN}}$ or IO8 to VSS ---------- –0.3V to 30V
- Input Voltage on SMB, SMBD to VSS ---------- –0.3V to 30V
- Input Voltage on $\overline{\text{ALERT}}$ or IO7, IO1, IO2, IO3 to VSS ---------- –0.3V to 3.63V
- Input Voltage on LEDCNTLA or IO4, LEDCNTLB or IO5, LEDCNTLC or IO6, $\overline{\text{DISP}}$ or IO12 to VSS ---------- –0.3V to 6V
- Input Voltage on CSP, CSN to VSS ---------- –0.3V to 2V
- Input Voltage on VC4 ---------- VC3 – 0.3V to VC3 + 8.5V or VSS + 30V
- Input Voltage on VC3 ---------- VC2 - 0.3V to VC2 + 8.5V or VSS + 30V
- Input Voltage on VC2 ---------- VC1 – 0.3V to VC1 + 8.5V or VSS + 30V
- Input Voltage on VC1 ---------- VSS - 0.3V to VSS + 8.5V or VSS + 30V
- Input Voltage on VC0 ---------- –0.3V to 6V
- Output on CHG, DSG to VSS ---------- –0.3V to 36V
- Output on PCHG, FUSE to VSS ---------- –0.3V to 30V
- Output on VDD1P73, VDD1P2 to VSS ---------- –0.3V to 2V
- Input Voltage on TS1 or IO9, TS2 or IO10, TS3 or IO11, TS4 to VSS ---------- –0.3V to 6V
- Functional Temperature ---------- –40°C to 85°C
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-32L 4x4 ---------- 3.59W
- Package Thermal Resistance (Note 3)
  WQFN-32L 4x4, θ_{JA} ---------- 27.8°C/W
  WQFN-32L 4x4, θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 5)

- Voltage on BAT, VCC Pin to VSS ---------- 2.8V to 26V
- Input Voltage Range, PACK, SMBC, SMBD to VSS ---------- 0V to 26V
- Input Voltage Range, LEDCNTLA or IO4, LEDCNTLB or IO5, LEDCNTLC or IO6 to VSS---0V to 5.5V
- Input Voltage Range, CSP, CSN to VSS ---------- –0.25V to 0.5V
- Input Voltage Range, VC4 ---------- V_{VC3} to V_{VC3} + 5V
- Input Voltage Range, VC3 ---------- V_{VC2} to V_{VC2} + 5V
- Input Voltage Range, VC2 ---------- V_{VC1} to V_{VC1} + 5V
- Input Voltage Range, VC1 ---------- V_{VC0} to V_{VC0} + 5V
- Input Voltage Range, VC0 ---------- 0V to 5V
- Output Voltage Range, CHG, DSG to VSS ---------- V_{BAT} to V_{BAT} + 12V
- Output Voltage Range, PCHG to VSS ---------- V_{VCC} – 9.7V to V_{VCC}
- Output Voltage Range, FUSE to VSS ---------- 0V to 26V
- Input Voltage Range, TS1 or IO9, TS2 or IO10, TS3 or IO11, TS4 to VSS ---------- 0V to 5V
- Input Voltage Range, $\overline{\text{PRES}}$ or $\overline{\text{SHUTDN}}$ or IO8, $\overline{\text{DISP}}$ or IO12 to VSS ---------- 0V to 5.5V
- Input Voltage Range, $\overline{\text{ALERT}}$ or IO7, IO1, IO2, IO3 to VSS ---------- 0V to VDD1P73
- Output Voltage Range, VDD1P73 to VSS ---------- 1.65V to 1.8V
- Output Voltage Range, VDD1P2 to VSS ---------- 1.16V to 1.24V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

13 Electrical Characteristics

(Typical values are at T_A = 25°C and V_{BAT} = 14.4 V, Min/Max values are at T_A = –40°C to 85°C and 2.8V ≤ V_{BAT} ≤ 26V, unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
Normal Mode	I_{NORMAL}	CHG on. DSG on, no Flash write	--	150	--	μA
Sleep Mode	I_{SLEEP}	CHG off, DSG on, no SBS communication	--	65	--	μA
Shutdown Mode	I_{SHDN}		--	0.5	--	μA
Power Supply Control						
BAT to VCC Switchovervoltage	$V_{SWITCHOVER-}$	V_{BAT} < $V_{SWITCHOVER–}$	2.55	2.65	2.75	V
VCC to BAT Switchovervoltage	$V_{SWITCHOVER+}$	V_{BAT} > $V_{SWITCHOVER–}$ + V_{HYS}	2.95	3.1	3.25	V
Switchovervoltage Hysteresis	V_{HYS}	$V_{SWITCHOVER+}$ – $V_{SWITCHOVER–}$	--	450	--	mV
BAT Pin Leakage Current	I_{LK_BAT}	BAT pin, BAT = 0V, VCC = 25V, PACK = 25V	--	--	1	μA
VCC Pin Leakage Current	I_{LK_VCC}	VCC pin, BAT = 25V, VCC = 0V, PACK = 0V	--	--	1	μA
BAT and PACK Pin Leakage Current	$I_{LK\_BAT\_PACK}$	BAT and PACK terminals, BAT = 0V, VCC = 0V, PACK= 0V, PBI = 25V	--	--	1	μA
Internal Pull-Down Resistance	R_{PACK_PD}	0.7V< V_{PACK} < 2V	8.5	13.33	19	kΩ
Battery Pack+ Start-Up Voltage	V_{SU+_PACK+}	V_{PACK+} > V_{SU+_PACK+}	5.2	5.95	7.25	V
Fuel Gauge Start-Up Voltage	V_{SU+}	V_{PACK} > V_{SU+}	3.2	3.4	3.6	V
Fuel Gauge Shutdown Voltage	$V_{SHDN–}$	V_{PACK} < $V_{SHDN–}$	3	3.2	3.4	V
1.73V LDO						
Output Voltage	$V_{REG1P73}$	C_{OUT} = 0.47μF to 2.2μF, Typ.= 1μF +/- 20%	1.65	1.73	1.8	V
Temp. Regulation$\Delta V_{REG1P73}/V_{REG1P73}$	$\Delta V_{REG1P73TEMP}$	$I_{REG1P73}$ = 1mA	–1	--	1	%
Line Regulation$\Delta V_{REG1P73}/V_{BAT}$	$\Delta V_{REG1P73LINE}$	$I_{REG1P73}$ = 1mA	–1	--	1	%
Load Regulation $\Delta V_{REG1P73}/V_{REG1P73}$	$\Delta V_{REG1P73LOAD}$	$I_{REG1P73}$ = 1 to 5mA	–2.5	--	2.5	%
Load Regulation $\Delta V_{REG1P73}/V_{REG1P73}$	$\Delta V_{REG1P73LOAD}$	$I_{REG1P73}$ = 1 to 19mA	–10	--	10	%
Output Short Circuit Current Limit	$I_{OUT\_SC\_LIMIT}$	$V_{REG1P73}$ = VSS, C_{OUT} = 1μF	7	--	17	mA
1.2V LDO						
Output Voltage	V_{REG1P2}	C_{OUT} = 0.47μF to 2.2μF, Typ.=1μF +/- 20%	1.16	1.2	1.24	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Temp. Regulation $\Delta V_{REG1P2}/V_{REG1P2}$	$\Delta V_{REG1P2TEMP}$	I_{REG1P2} = 1 mA	–1	--	1	%
Line Regulation $\Delta V_{REG1P2}/V_{BAT}$	$\Delta V_{REG1P2LINE}$	I_{REG1P2} = 1 mA	–1	--	1	%
Load Regulation $\Delta V_{REG1P2}/V_{REG1P2}$	$\Delta V_{REG1P2LOAD}$	I_{REG1P2} = 1 to 5mA	–2.5	--	2.5	%
Output Short Circuit Current Limit	$I_{OUT\_SC\_LIMIT}$	V_{REG1P2} = VSS, C_{OUT} = 1μF	18	--	36	mA
Current Wake Detector						
Wakeup Voltage Threshold	V_{WAKE}	$V_{CSP} – V_{CSN}$	±0.25	±0.5	±0.75	mV
			±0.75	±1	±1.25	
			±1.25	±1.5	±1.75	
			±1.75	±2	±2.25	
			±2.25	±2.5	±2.75	
			±2.75	±3	±3.25	
			±3.25	±3.5	±3.75	
			±3.75	±4	±4.25	
			±4.25	±4.5	±4.75	
			±4.75	±5	±5.25	
			±5.25	±5.5	±5.75	
			±5.75	±6	±6.25	
			±6.25	±6.5	6.75	
			±6.75	±7	±7.25	
			±7.25	±7.5	±7.75	
Wakeup Delay Time	t_{WAKE}		2	--	9	ms
Wakeup Detection Delay Time Program Step	$\triangle t_{WAKE}$		--	1	--	ms
Cell Balancing						
Internal Cell Balancing Resistance	R_{CB}	$R_{DS(ON)}$ for internal FET switch at 3V< V_{DS} <4.5V	50	100	180	Ω
SMBD, SMBC						
High-Level Input	V_{IH}		1.3	--	--	V
Low-Level Input	V_{IL}		--	--	0.8	V
Output Voltage Low	V_{OL}	I_{OL} = –3mA	--	--	0.4	V
Pull-Down Resistance	R_{PD}		0.6	1	1.5	MΩ
IO1, IO2, IO3, IO4, IO5, IO6, IO7, IO9, IO10, IO11, IO12						
High-Level Input	V_{IH}	VDD = VDD1P73 IO1, IO2, IO3, IO4, IO5, IO6, IO7, IO9, IO10, IO11, IO12	0.7 x VDD	--	--	V
Low-Level Input	V_{IL}	VDD = VDD1P73 IO1, IO2, IO3, IO4, IO5, IO6, IO7, IO9, IO10, IO11, IO12	--	--	0.3x VDD	V
Output Voltage High	V_{OH}	VDD = VDD1P73, I_{OH} = –1mA IO1, IO2, IO3, IO4, IO5, IO6, IO7, IO9, IO10, IO11, IO12	VDD – 0.2	--	--	V
Output Voltage Low	V_{OL}	VDD = VDD1P73, I_{OL} = 3 mA IO1, IO2, IO3, IO4, IO5, IO6, IO7, IO9, IO10, IO11, IO12	--	--	0.4	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{LK}				1	μA
/PRES or IO8						
Output Voltage High	V_{OH}	V_{BAT} > 5.5V, I_{OH} = –0μA	3.5	--	5	V
		V_{BAT} > 5.5V, I_{OH} = –10μA	1.8	--	5	
Output Voltage Low	V_{OL}	I_{OL} = 1.5mA	--	--	0.4	V
Input Leakage Current	I_{LK}				1	μA
LEDCNTLA, LEDCNTLB, LEDCNTLC, TS3						
LED Sink Current	I_{CS}		2.1	3	3.9	mA
			2.8	4	5.2	
			3.5	5	6.5	
Input Leakage Current	I_{LK}		--	--	1	μA
Current Measurement						
Input Voltage Range		V_{CSP} - V_{CSN}	–200	--	200	mV
Offset Error	I_{CC1_OERR}	|V_{CSP} - V_{CSN}| = 0mV, T_A = –25°C to 65°C	-3.5	±2.5	3.5	μV
		|V_{CSP} - V_{CSN}| = 0mV, T_A = –40°C to 85°C	-4	±2.5	4	
Gain Error	I_{CC1_GERR}	|V_{CSP} - V_{CSN}| = 200mV, T_A = –25°C to 65°C	-0.15	±0.1	0.15	%
		|V_{CSP} - V_{CSN}| = 200mV, T_A = –40°C to 85°C	-0.2	±0.1	0.2	
Effective Input Resistance	$R_{ADC\_IN\_CURR}$	When measuring	2.5	--	--	MΩ
Conversion Time	t_{CC1_CONV}	Single conversion in normal mode	--	250	--	ms
Voltage Measurement						
Input Voltage Range (Differential Cell Input Mode)	$V_{ADC\_IN\_CELLS}$		0	--	5	V
Input Voltage Range (Divider Measurement Mode)	$V_{ADC\_IN\_DIV}$	Applicable to divider measurements using the BAT, VC4 and PACK, pins relative to VSS.	0	--	25	V
Cell Voltage Measurement Accuracy	V_{CELL_ACC}	V_{VC4} – V_{VC3}, V_{VC3} – V_{VC2}, V_{VC2} – V_{VC1}, V_{VC1} – V_{VC0}, T_A = –25°C to 65°C	–3	±0.5	3	mV
		V_{VC4} – V_{VC3}, V_{VC3} – V_{VC2}, V_{VC2} – V_{VC1}, V_{VC1} – V_{VC0}, T_A = –40°C to 85°C	–8	±0.5	8	
Stack Voltage Measurement Accuracy	V_{STACK_ACC}	V_{BAT} – V_{VSS}, T_A = –25°C to 65°C	–25	±10	25	mV
		V_{BAT} – V_{VSS}, T_A = –40°C to 85°C	–30	±10	30	
PACK Pin Voltage Measurement Accuracy	V_{PACK_ACC}	V_{PACK} – V_{VSS},T_A = –25°C to 65°C	–25	±10	25	mV
		V_{PACK} – V_{VSS},T_A = –40°C to 85°C	–30	±10	30	
TS1, TS2, TS3, TS4 Pin Voltage Measurement Accuracy	V_{TS_ACC}	V_{TS} ≤ 5V, T_A = –25°C to 65°C	–3	±0.5	3	mV
		V_{TS} ≤ 5V, T_A = –40°C to 85°C	–8	±0.5	8	
Effective Input Resistance	$R_{ADC\_IN\_CELL}$	When measuring	1	--	--	MΩ
Cell Voltage Conversion Time	t_{CELL_CONV}		--	8	--	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
BAT, PACK, Voltage Conversion Time	t_{LVMUX_CONV}		--	4	--	ms
TS1, TS2, TS3, TS4 Conversion Time	t_{TS_CONV}		--	2	--	ms
High-Side FET Drivers						
Output Voltage CHG and DSG On	V_{FETON_LOBAT}	2.8V ≤ V_{BAT} < 5V, V_{PACK} ≤ V_{DSG} Connect a 10MΩ between PACK and DSG, connect a 10MΩ between BAT and CHG	3.95	--	12	V
	V_{FETON}	$V_{DSG(ON)}$ = V_{DSG} – V_{BAT}, V_{BAT} ≥ 5V, Connect a 10MΩ between PACK and DSG $V_{CHG(ON)}$ = V_{CHG} – V_{BAT}, V_{BAT} ≥ 5V, Connect a 10MΩ between BAT and CHG	8.5	10	12	
DSG MOSFET Turn-Off Voltage	V_{DSGOFF}	V_{DSGOFF} = V_{DSG} – V_{PACK}, C_L = 10nF, Connect a 10MΩ between PACK and DSG	--	--	0.4	V
CHG MOSFET Turn-Off Voltage	V_{CHGOFF}	V_{CHGOFF} = V_{CHG} – V_{BAT}, connect a 10MΩ between BAT and CHG	--	--	0.7	V
DSG Rise Time (0% to 35% V_{DSGON})	t_{R_DSG}	Connect a C_L = 10nF between DSG and PACK, a 5.1kΩ between DSG and C_L, a 10MΩ between PACK and DSG	--	90	200	μs
CHG Rise Time (0% to 35% V_{CHGON})	t_{R_CHG}	Connect a C_L = 10nF between CHG and BAT, a 5.1kΩ between CHG and C_L, a 10MΩ between BAT and CHG	--	90	200	μs
DSG Fall Time (V_{DSGON} to 1V)	t_{F_DSG}	Connect a C_L = 10nF between DSG and PACK, a 5.1kΩ between DSG and C_L, a 10MΩ between PACK and DSG	--	40	100	μs
CHG Fall Time (V_{DSGON} to 1V)	t_{F_CHG}	Connect a C_L = 10nF between CHG and BAT, a 5.1kΩ between CHG and C_L, a 10MΩ between BAT and CHG	--	40	100	μs
PCHG FET Drivers						
PCHG MOSFET Turn-On Voltage	V_{PCHGON}	$V_{PCHG(ON)}$ = VCC – V_{PCHG}, VCC ≥ 8V, V_{BAT} ≥ 5V	7.1	8.4	9.7	V
		$V_{PCHG(ON)}$ = VCC– V_{PCHG}, 5V ≤ VCC < 8V, VCC > V_{BAT}	V_{PACK} – 1.4	--	V_{PACK}	
Current Sink Capability	$I_{PULLDOWN}$	PCHG enable, V_{BAT} = 14.4V	--	50	--	μA
PCHG Rise Time (10% to 90% V_{PCHGON})	t_R	V_{VCC} ≥ 8V, C_L = 1nF between PCHG and VCC, a 5.1kΩ between PCHG and C_L, a 10MΩ between PCHG and VCC	--	30	100	μs

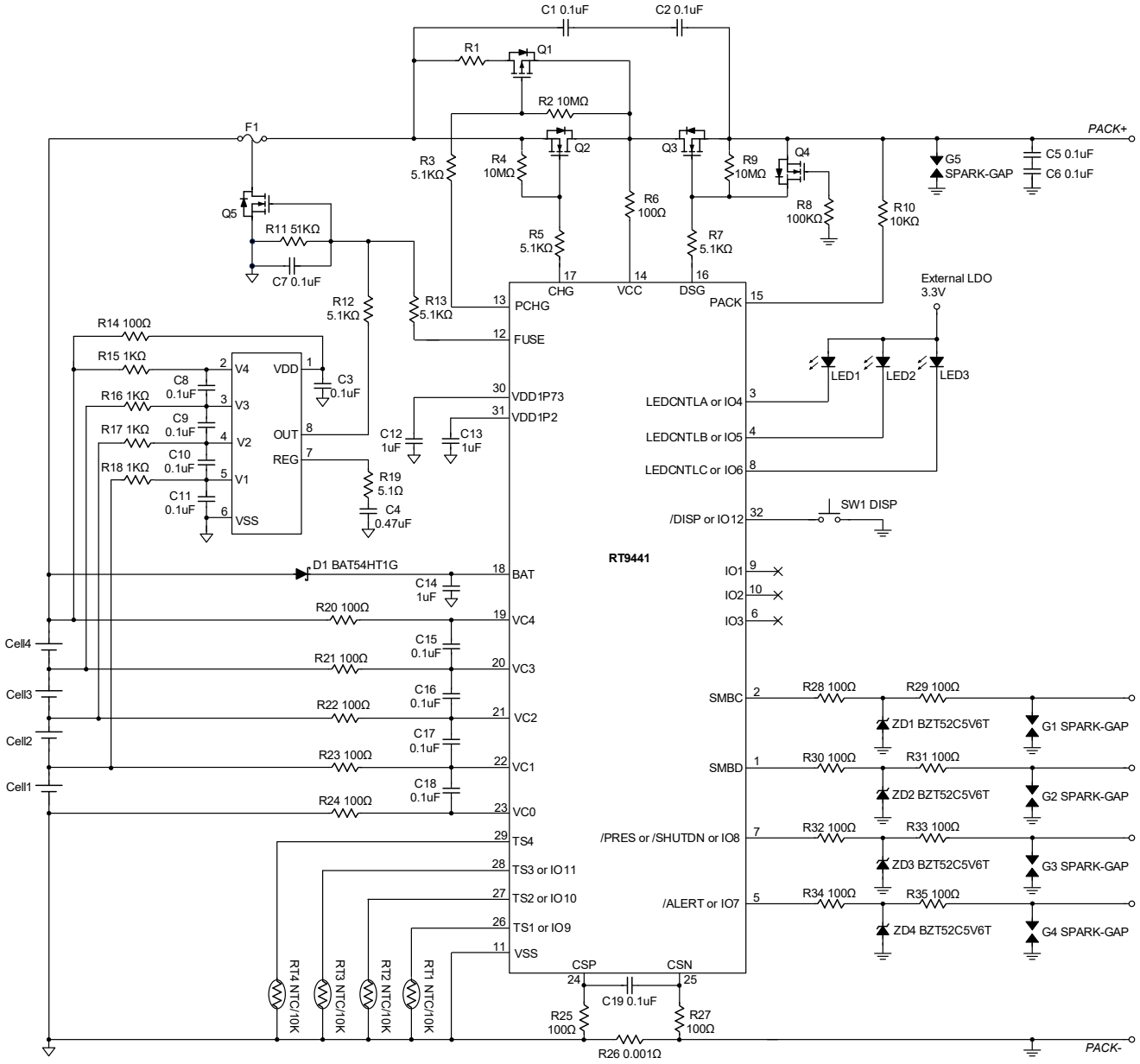
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PCHG Fall Time (90% to 10% V_{PCHGON})	t_F	$V_{VCC} \geq 8V$, C_L = 1nF between PCHG and VCC, a 5.1kΩ between PCHG and C_L, a 10MΩ between PCHG and VCC	--	60	200	μs
Fuse Driver						
Output Voltage High	V_{OH}	$V_{BAT} \geq 7.5V$, C_L = 10nF, 5kΩ load	6	6.8	7.5	V
		$2.8V \leq V_{BAT} < 7.5V$, C_L = 10nF, 5KΩ load.	V_{BAT} – 1.5V	--	V_{BAT}	
High-Level Input	V_{IH}	Maximum current limitation 2mA	2	--	--	V
Low-Level Input	V_{IL}		--	--	0.6	V
Fuse Output Rise Time	t_{RISE}	$V_{BAT} \geq 7.5V$, C_L = 10nF, R_{SERIES} = 100Ω, R_{LOAD} = 51kΩ, V_{OH} = 10% to 90% of final voltage	--	9	--	μs
Internal Temperature Sensor						
Internal Temperature Measurement Error	INT_{GERR}		--	±3	--	°C
TS1, TS2, TS3, TS4						
Input Voltage Range	V_{IN}		−0.3	--	5	V
Internal Resistance	R_{TS}	Pullup resistance	--	15	--	kΩ
		Pulldown resistance	--	30	--	kΩ
Program Flash						
Data Retention			10	--	--	Years
Flash Programming Write Cycles			100k	--	--	Cycles
Word Programming Time	$t_{PROGWORD}$		--	--	10	μs
Mass-Erase Time	$t_{MASSERASE}$		--	--	100	ms
Page-Erase Time	$t_{PAGEERASE}$		--	--	6	ms
Flash-Read Current	$I_{FLASHREAD}$		--	3.37	4	mA
Flash-Write Current	$I_{FLASHWRITE}$		--	--	2.7	mA
Flash-Erase Current	$I_{FLASHERASE}$		--	--	1.2	mA
Data Flash						
Data Retention			10	--	--	Years
Flash Programming Write Cycles			100k	--	--	Cycles
Word Programming Time	$t_{PROGWORD}$		--	--	10	μs
Mass-Erase Time	$t_{MASSERASE}$		--	--	40	ms
Page-Erase Time	$t_{PAGEERASE}$		--	--	6	ms
Flash-Read Current	$I_{FLASHREAD}$		--	--	4	mA
Flash-Write Current	$I_{FLASHWRITE}$		--	--	2.7	mA
Flash-Erase Current	$I_{FLASHERASE}$		--	--	1.2	mA
Data Retention			10	--	--	Years

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OCD1, OCD2, SCD, OCC Current Protection Thresholds						
OCD1 Detection Threshold Voltage Range	V_{OCD1}	$V_{CSP} - V_{CSN}$	–2	--	–254	mV
OCD1 Detection Threshold Voltage Program Step	ΔV_{OCD1}	$V_{CSP} - V_{CSN}$	--	–2	--	mV
OCD2 Detection Threshold Voltage Range	V_{OCD2}	$V_{CSP} - V_{CSN}$	–2	--	–254	mV
OCD2 Detection Threshold Voltage Program Step	ΔV_{OCD2}	$V_{CSP} - V_{CSN}$	--	–2	--	mV
SCD Detection Threshold Voltage Range	V_{SCD}	$V_{CSP} - V_{CSN}$	–2	--	–254	mV
SCD Detection Threshold Voltage Program Step	ΔV_{SCD}	$V_{CSP} - V_{CSN}$	--	–2.5	--	mV
OCC Detection Threshold Voltage Range	V_{OCC}	$V_{CSP} - V_{CSN}$	2	--	254	mV
OCC Detection Threshold Voltage Program Step	ΔV_{OCC}	$V_{CSP} - V_{CSN}$	--	2	--	mV
OCD1, OCD2, SCD, OCC Current Protection Timing						
OCD1 Detection Delay Time	t_{OCD1}	$V_{CSP} - V_{CSN}$	1	--	32	ms
OCD1 Detection Delay Time Program Step	Δt_{OCD1}	$V_{CSP} - V_{CSN}$	--	1	--	ms
OCD2 Detection Delay Time	t_{OCD2}	$V_{CSP} - V_{CSN}$	1	--	32	ms
OCD2 Detection Delay Time Program Step	Δt_{OCD2}	$V_{CSP} - V_{CSN}$	--	1	--	ms
SCD Detection Delay Time	t_{SCD}	$V_{CSP} - V_{CSN}$	61	--	3873.5	µs
SCD Detection Delay Time Program Step	Δt_{SCD}	$V_{CSP} - V_{CSN}$	--	30.5	--	µs
OCC Detection Delay Time	t_{SCC}	$V_{CSP} - V_{CSN}$	1	--	32	ms
OCC Detection Delay Time Program Step	Δt_{SCC}	$V_{CSP} - V_{CSN}$	--	1	--	ms
Current Fault Detect Time Accuracy	t_{DETECT}	$V_{CSP} - V_{CSN}$ = VT – 3 mV for OCD1, OCD2 $V_{CSP} - V_{CSN}$ = VT + 3 mV for OCC	--	--	176	µs
		$V_{CSP} - V_{CSN}$ = VT – 3 mV for SCD,	--	--	51	µs
Delay Time Accuracy	t_{ACC}	Delay time ≤ 1ms	–10	--	10	%
		Delay time > 1ms	–5	--	5	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OCD1, OCD2, SCD, OCC Current Protection Accuracy						
OCD1, OCD2, SCD, OCC Detection Voltage Accuracy	V_{ACC_OFFSET}	$\|V_{CSP} - V_{CSN}\|$ = 2mV to 254mV	−1.5	--	1.5	mV
	V_{ACC_GAIN}		−3.5	--	3.5	%
Low Frequency Oscillator						
Operating Frequency Low	f_{OSC_LOW}		--	262.14	--	kHz
Operating Accuracy Low	f_{ERR_LOW}		−2.5	±0.25	2.5	%
SMBus, 100kHz						
Clock Operating Frequency	f_{SMB}	Slave mode, SMBC duty cycle = 50%	10	--	100	kHz
Clock Operating Frequency	f_{MAS}	Master mode	--	51.2	--	kHz
Bus Free Time STOP to START	t_{BUF}		4.7	--	--	µs
START Condition Hold Time	$t_{HD:STA}$		4.0	--	--	µs
Setup Repeated START	$t_{SU:STA}$		4.7	--	--	µs
Setup Time STOP Condition	$t_{SU:STO}$		4.0	--	--	µs
Data Hold Time	$t_{HD:DAT}$		0	--	--	ns
Data Setup Time	$t_{SU:DAT}$		250	--	--	ns
Error Signal Detect Time	$t_{TIMEOUT}$		25	--	35	ms
Low Period of the SMBC Clock	t_{LOW}		4.7	--	--	µs
High Period of the SMBC Clock	t_{HIGH}		4.0	--	--	µs
Clock Rise Time	t_R	10% to 90%	--	--	1000	ns
Clock Fall Time	t_F	90% to 10%	--	--	300	ns
Cumulative Clock Low Slave Extend Time	$t_{LOW(SEXT)}$		--	--	25	ms
Cumulative Clock Low Master Extend Time	$t_{LOW(MEXT)}$		--	--	10	ms
SMBus, 400kHz						
Clock Operating Frequency	f_{SMB}	Slave mode, SMBC duty cycle = 50%	--	--	400	kHz
Bus Free Time STOP to START	t_{BUF}		1.3	--	--	µs
START Condition Hold Time	$t_{HD:STA}$		0.6	--	--	µs
Setup Repeated START	$t_{SU:STA}$		0.6	--	--	µs
Setup Time STOP Condition	$t_{SU:STO}$		0.6	--	--	µs
Data Hold Time	$t_{HD:DAT}$		0	--	--	ns
Data Setup Time	$t_{SU:DAT}$		100	--	--	ns
Error Signal Detect Time	$t_{TIMEOUT}$		25	--	35	ms
Low Period of the SMBC Clock	t_{LOW}		1.3	--	--	µs
High Period of the SMBC Clock	t_{HIGH}		0.6	--	--	µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Rise Time	t_R	10% to 90%	20	--	300	ns
Clock Fall Time	t_F	90% to 10%	20	--	300	ns
Cumulative Clock Low Slave Extend Time	t_{LOW_SEXT}		--	--	25	ms
Cumulative Clock Low Master Extend Time	t_{LOW_MEXT}		--	--	10	ms
SMBus, 1MHz						
Clock Operating Frequency	f_{SMB}	Slave mode, SMBC duty cycle = 50%	--	--	1	MHz
Bus Free Time STOP to START	t_{BUF}		0.5	--	--	µs
START Condition Hold Time	$t_{HD:STA}$		0.26	--	--	µs
Setup Repeated START	$t_{SU:STA}$		0.26	--	--	µs
Setup Time STOP Condition	$t_{SU:STO}$		0.26	--	--	µs
Data Hold Time	$t_{HD:DAT}$		0	--	--	ns
Data Setup Time	$t_{SU:DAT}$		50	--	--	ns
Error Signal Detect Time	$t_{TIMEOUT}$		25	--	35	ms
Low Period of the SMBC Clock	t_{LOW}		0.5	--	--	µs
High Period of the SMBC Clock	t_{HIGH}		0.26	--	--	µs
Clock Rise Time	t_R	10% to 90%	--	--	120	ns
Clock Fall Time	t_F	90% to 10%	20	--	120	ns
Cumulative Clock Low Slave Extend Time	t_{LOW_SEXT}		--	--	25	ms
Cumulative Clock Low Master Extend Time	t_{LOW_MEXT}		--	--	10	ms

14 Typical Application Circuit



15 Timing Diagram

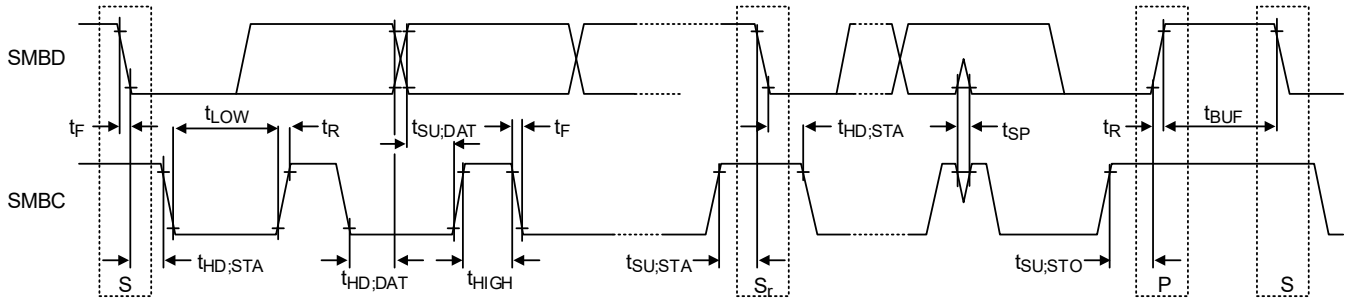


Figure 1. SMBus Timing Diagram

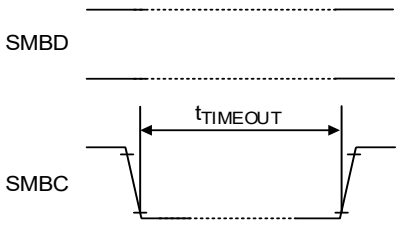
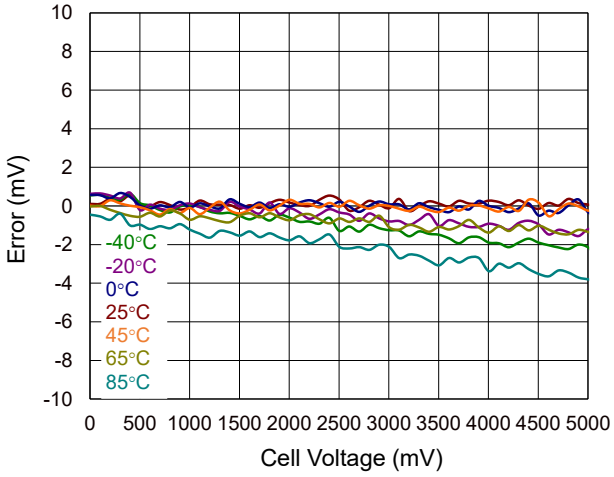


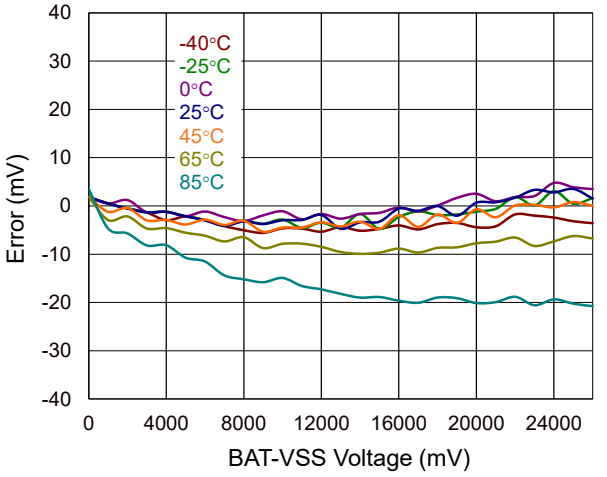
Figure 2. SMBus Timeout Condition

16 Typical Operating Characteristics

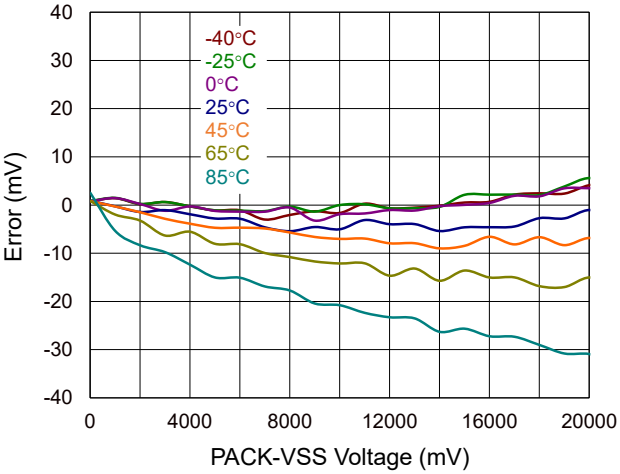
Cell Voltage Error vs. Cell Voltage



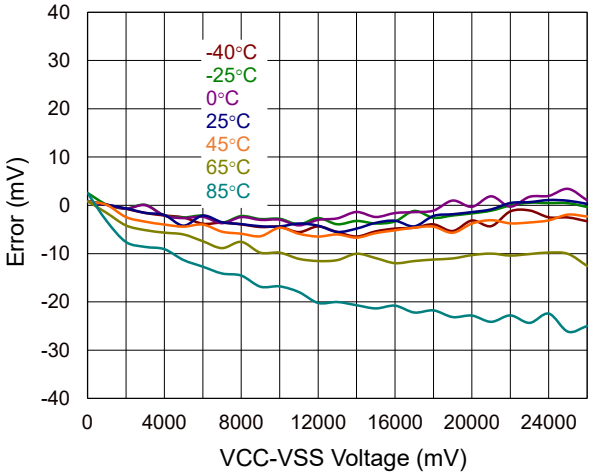
BAT-VSS Voltage Error vs. BAT-VSS Voltage



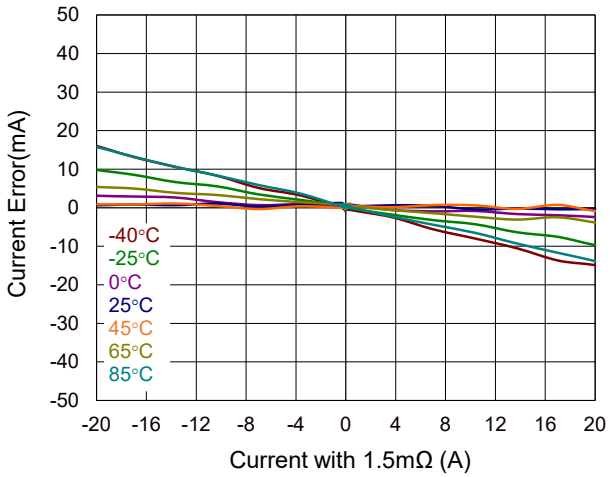
PACK-VSS Voltage Error vs. PACK-VSS Voltage



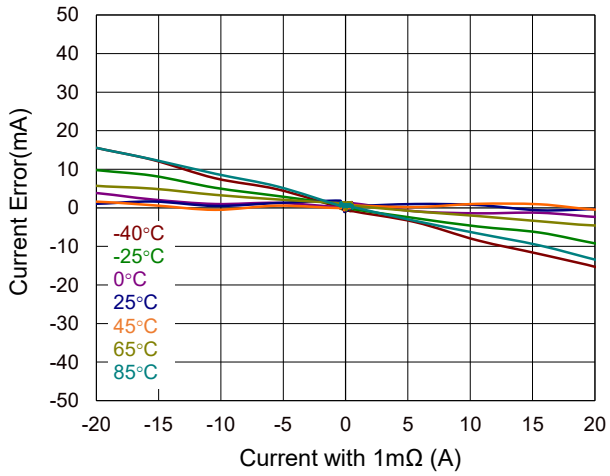
VCC-VSS Voltage Error vs. VCC-VSS Voltage



Current Error vs. Current with 1.5mΩ



Current Error vs. Current with 1mΩ



17 Operation

17.1 Cell Voltage Measurement Circuit

- Place an input RC filter between VCx pins for ESD protection and filter unwanted voltage transients.
- Select 100Ω resistors for R20, R21, R22, R23, and R24. The resistors can be adjusted based on cell balancing current requirements. Select 0.1μF capacitors for C15, C16, C17, and C18.
- The impedance of VC4, VC3, VC2, VC1, and VC0 must be minimized. Use Kelvin sense connections to each cell's positive and negative terminals to reduce IR drop and improve voltage measurement accuracy.
- The BAT input is isolated and decoupled from the cells by diode D1 to protect against transient voltage dips caused by short circuits.

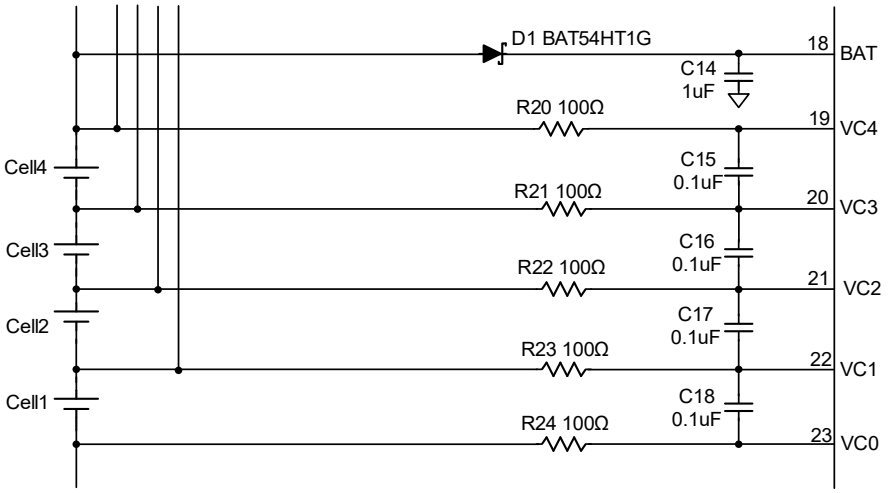


Figure 3. Cell Voltage Measurement Circuit

17.2 Current Measurement Circuit

- The CSP and CSN pins monitor the voltage of current sensing resistor R26, with a recommended resistor value range from 1mΩ to 10mΩ, depending on the current protection and thermal requirements. Minimize the impedance between CSP and VSS to ensure that the voltages of VCSP - VSS and VCSN – VSS remain within the ROC requirement during a short circuit event.
- The current sensing resistor must have a low temperature coefficient (<50ppm) to minimize the current drift due to temperature variations.
- Place a low-pass filter to reduce input noise. Select 100Ω resistors for R25 and R27, and 0.1μF for C19. 0.1μF capacitors C20 and C21 can be used as a Y-filter to reduce specific interferences or noise sources, further improving the accuracy of current measurements.
- The CSN and CSP paths must use Kelvin sense connections to R26 to avoid the IR drop effects and maintain current measurement accuracy.

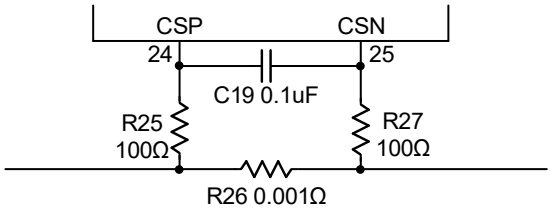


Figure 4. Current Measurement Circuit

17.3 External Temperature Measurement Circuit

- TS1, TS2, TS3, and TS4 pins are used to measure external NTC thermistors.
- Each pin can be enabled with an integrated pull-up resistor (typical 15kΩ) and a pull-down resistor (typical 30kΩ) to support the use of a 10kΩ NTC thermistor at 25°C (B = 3435k) for RT1 to RT4. Also, place an NTC thermistor to monitor the temperature of the high-side MOSFET.

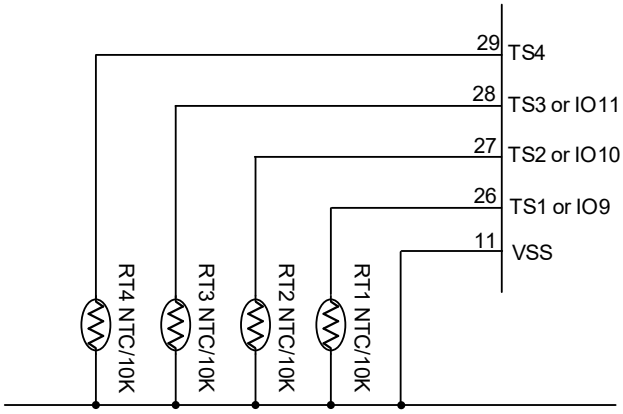


Figure 5. External Temperature Measurement Circuit

17.4 PACK Detection Circuit

- The VCC pin provides power to the RT9441 when the PACK pin detects a charger plug-in. The device integrates a PACK detection circuit to monitor the charger status.
- It is recommended to use a 10kΩ resistor for R10.

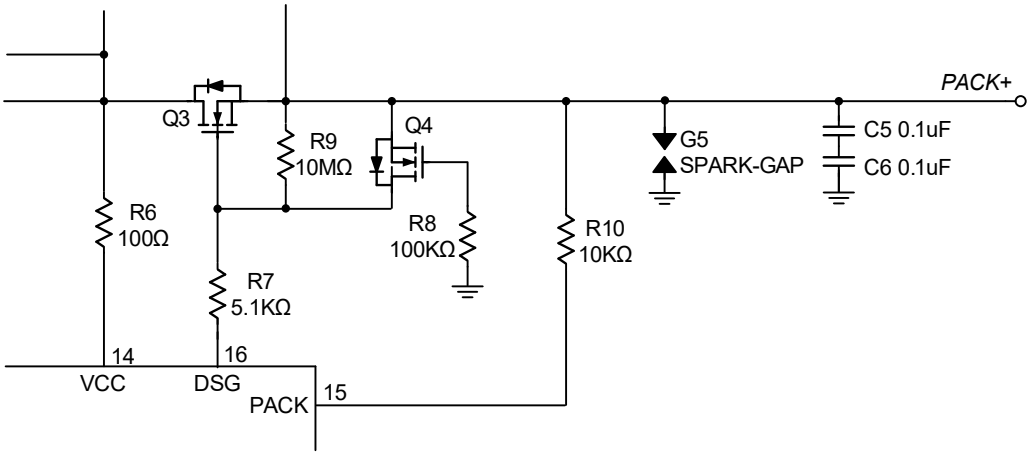


Figure 6. PACK Detection Circuit

17.5 High-Side N-MOSFETs and P-MOSFET Control Circuit

- N-MOSFETs (Q2 and Q3) are used as switches for charge and discharge current paths. The MOSFETs should be 30V devices with low $R_{DS(ON)}$ to address thermal concerns. The gate driver voltage and AMR should be selected according to the RT9441 VCHGON or VDSGON design voltage.
- The P-MOSFET (Q1) is used for pre-charge operation, with R1 limiting the pre-charge current.
- R3, R5, and R7 are used for gate protection and to reduce noise in the Q1/Q2/Q3 MOSFETs. A 5.1kΩ resistor is recommended to provide a microsecond switching time constant.

- R2, R4, and R9 are used to fix Q1/Q2/Q3 MOSFETs gate voltage to keep them in a stable off state when turned off. A 10MΩ resistor is recommended to prevent voltage drop.
- Q4 is placed between the gate and source of Q3 to turn off Q3 when the charger is reversely connected.
- C1 and C2 provide ESD protection for the MOSFETs. Use two capacitors to ensure normal operation if one fails short.

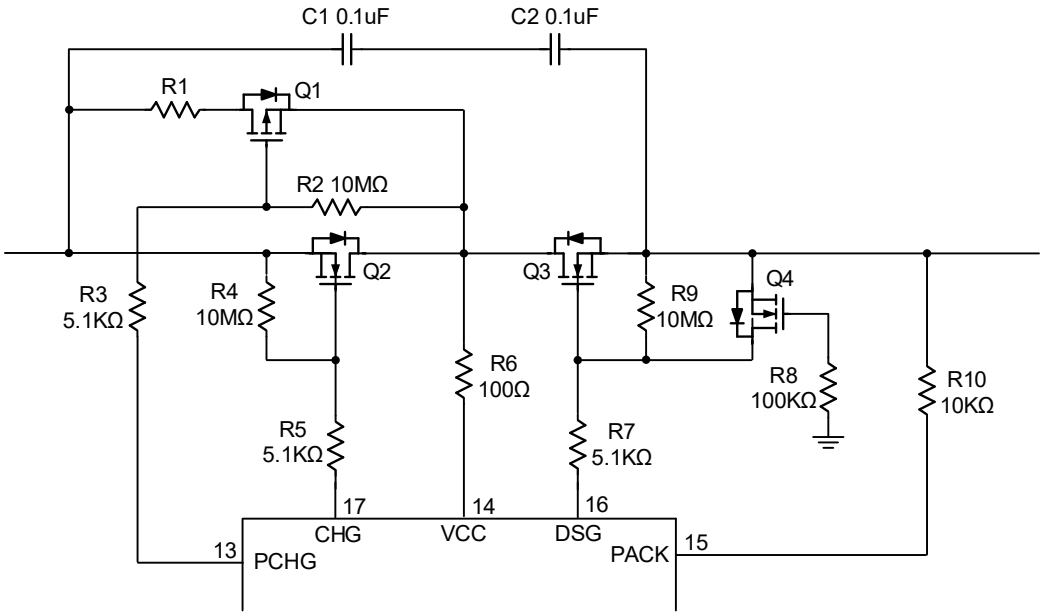


Figure 7. High-Side N-MOSFETs and P-MOSFET Control Circuit

17.6 Fuse Pin Control Circuit

- The FUSE pin is designed to ignite the chemical fuse in the event of a safety incident and also monitors the 2nd protection IC. The fuse will blow when either the FUSE pin or the OUT pin of the 2nd protection IC is high, causing Q5 to turn on.
- R11, R12 and R13 need to ensure that the divided voltage from the OUT pin or the FUSE pin is sufficient to provide the gate driver voltage to turn on Q5.
- It is recommended to use 5.1kΩ resistors for R12 and R13, and a 51kΩ resistor for R11.
- Connect the FUSE pin to VSS if not used.

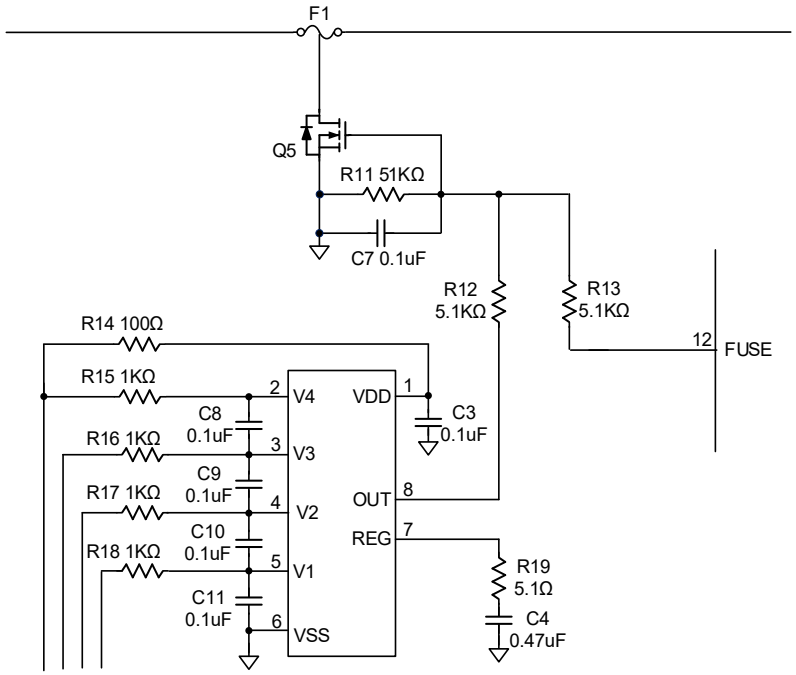


Figure 8. FUSE Pin Control Circuit

17.7 LEDs Control Circuit

- Select an external LDO to provide the required voltage and drive current for the external LEDs
- The LEDCNTLA, LEDCNTLB, and LEDCNTLC pins can provide sink current for external LEDs.
- If necessary, the TS3 pin and $\overline{\text{DISP}}$ pin can also be configured as LED control pins.
- Let the LEDCNTL pins floating if not used, and connect the $\overline{\text{DISP}}$ pin to GND if not used.

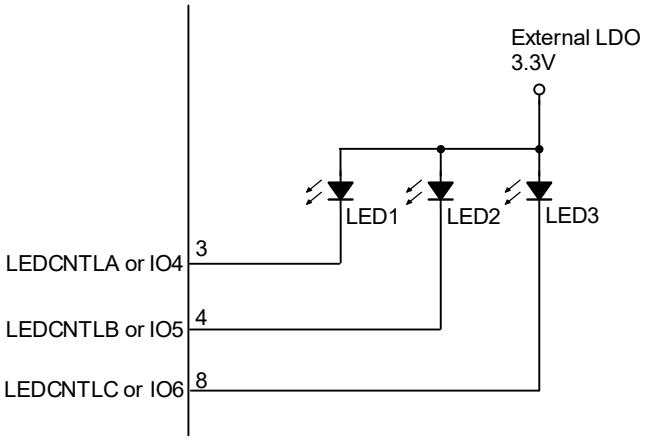


Figure 9. LEDs Control Circuit

17.8 SMBus Circuit

- For robust ESD protection, the ESD protection diodes (ZD1, ZD2) and resistor (R28, R29, R30, R31) are recommended.
- Use 100Ω resistors for R28, R29, R30, and R31.

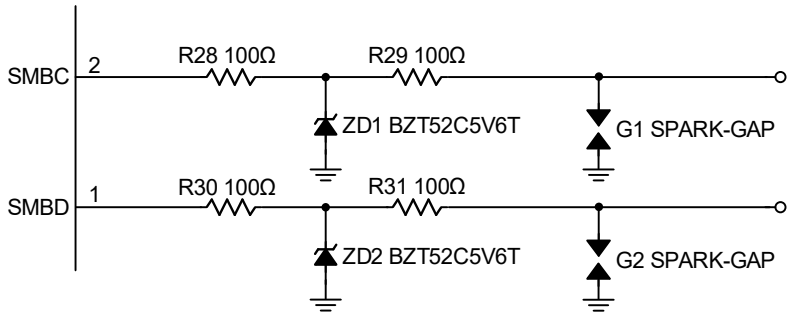


Figure 10. SMBus Circuit

17.9 System Present Circuit

- For a removable system host, the $\overline{\text{PRES}}$ pin can be used to detect the system connection status.
- The $\overline{\text{PRES}}$ pin is pulled up every 250ms and its status is recorded. If the device continuously detects four low states, the system is considered present.
- A resistor can be used to pull the pin low and a 20kΩ or lower resistor is recommended.
- For robust ESD protection, it is recommended to use an ESD protection diodes (ZD3) and resistors (R32, R33).
- Use 100Ω resistors for R32 and R33.

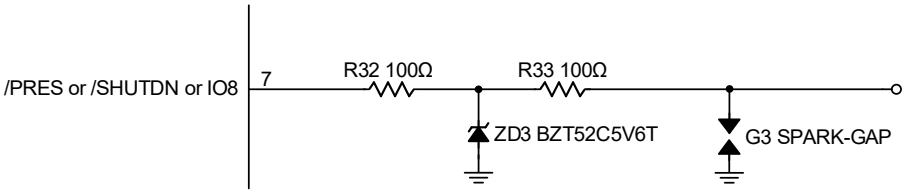


Figure 11. System Present Circuit

18 Application Information

(Note 6)

The RT9441 device provides a complete fuel gauging solution for 2-to-4 series cell battery pack applications. It also fully integrates cell balancing, protection, charger control, and authentication for 2-to-4 series cell battery packs.

18.1 Fuel Gauge

The RT9441 uses the VGCS algorithm to calculate the state of charge in battery cells. The VGCS algorithm is a hybrid fuel gauge algorithm with voltage-based core (VoltaicGauge), iterating battery voltage and dynamic difference of battery voltage. Then it is optimized with current information to adjust the delta SOC and integrate it into the overall SOC. The VGCS algorithm also includes temperature and load compensation, and aging compensation functions, providing both short-term accurate and long-term stability in SOC results.

18.2 Power Mode

The RT9441 supports three power modes to decrease power usage.

- In normal mode, the RT9441 performs measurements, calculations, protection decisions, and data updates at 250ms intervals. Between these intervals, the RT9441 is in idle status to reduce power consumption.
- In sleep mode, the RT9441 performs measurements, calculations, protection decisions, and data updates at adjustable intervals (default 5 seconds). Between these intervals, the RT9441 is in idle status to decrease power usage. The RT9441 has a wake function that enables exit from sleep mode when current flow or failure is detected.
- In shutdown mode, the RT9441 is completely disabled.

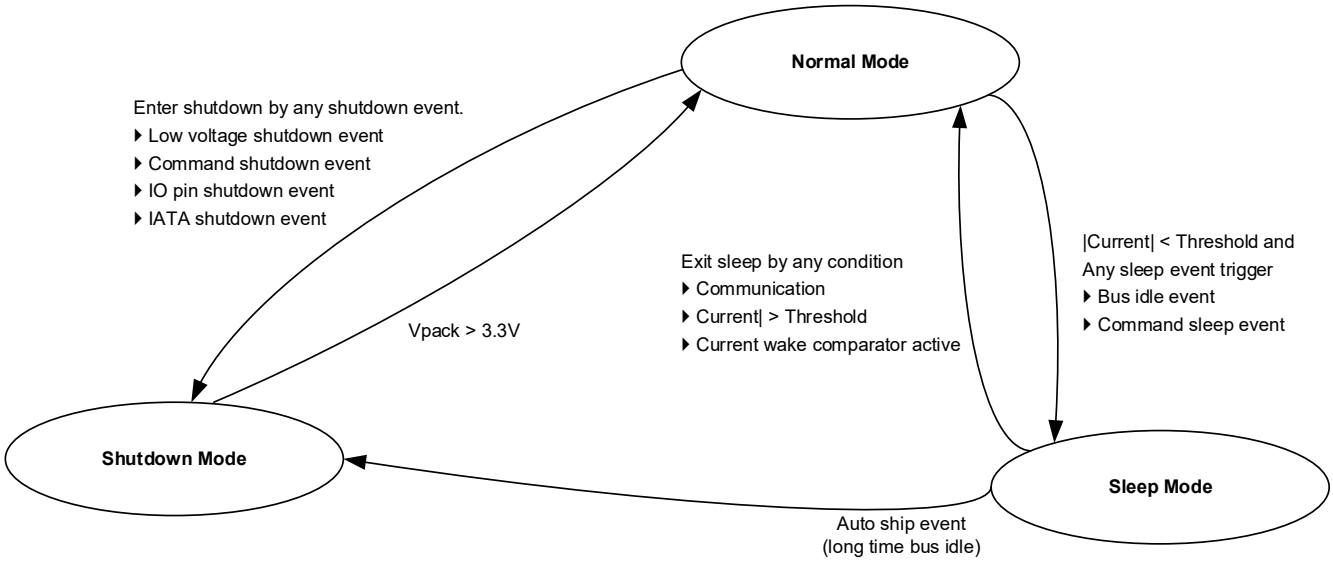


Figure 12. Power Mode State Machine

18.3 Measurement

The RT9441 supports voltage, current, and temperature measurements.

The RT9441 uses internal ADC to measure voltage and updates the voltage every 0.25 seconds in the normal mode. This data is also used to calculate the VGCS gas gauging.

- Up to 4 cell voltage measurement
- Stack cell voltage
- Pack pin voltage
- VCC pin voltage

The RT9441 uses the CSP and CSN input pins to measure and calculate the battery charge and discharge current.

- Supports current measurement with 1mΩ to 10mΩ current sense resistance.

The RT9441 has an internal temperature sensor and inputs for up to 4 external temperature sensors.

- Supports up to 4 channels of external NTC temperature measurement.
- TS1, TS2, TS3, and TS4 can be optionally configured for general ADC measurement, with a measurement range of 0V to 5V.
- Internal temperature measurement.

TS1, TS2, TS3, and TS4 can be individually enabled and configured for cell or MOSFET temperature usage and use a different thermistor profile.

18.4 Primary (1st Level) Safety Features

The RT9441 supports a full coverage of battery and system protection features that can be easily configured. For detailed descriptions of each protection function, refer to the RT9441 Technical Reference Manual.

It includes two types of protection: hardware protection and software protection.

- Hardware protection
- Overcurrent in discharge protection with 2 levels
- Overcurrent in charge protection
- Short circuit in discharge protection
- Software protection
- Cell overvoltage protection
- Cell undervoltage protection
- Overcurrent in charge protection in 2 levels
- Overcurrent in discharge protection in 2 levels
- Over-temperature in charge protection
- Over-temperature in discharge protection
- Under-temperature in charge protection
- Under-temperature in discharge protection
- Over-temperature MOSFET protection
- Pre-charge timeout protection
- Host watchdog timeout protection
- Fast charge timeout protection
- Overcharge protection
- Overcharging voltage protection
- Overcharging current protection
- Over pre-charge current protection

18.5 Secondary (2nd Level) Safety Features

The secondary safety features of the RT9441 can be used to indicate more serious faults via the FUSE pin. This pin is used to blow an in-line fuse and permanently disable the battery pack.

For detailed descriptions of each protection function, refer to the RT9441 Technical Reference Manual.

- Safety cell overvoltage permanent failure
- Safety cell undervoltage permanent failure
- Safety overcurrent in charge permanent failure
- Safety overcurrent in discharge permanent failure
- Safety overtemperature cell permanent failure
- Safety overtemperature MOSFET permanent failure
- Cell balancing permanent failure
- Qmax imbalance permanent failure
- Capacity degradation permanent failure
- Voltage imbalance at rest permanent failure
- Voltage imbalance active permanent failure
- Charge MOSFET permanent failure
- Discharge MOSFET permanent failure
- Fuse failure permanent failure
- AFE register permanent failure
- 2nd protection permanent failure
- Open thermistor permanent failure
- Program memory checksum permanent failure
- Data memory permanent failure
- AFE communication permanent failure

The RT9441 charge control features include:

- Supports JEITA temperature ranges and reports the charging voltage and the charging current according to the active temperature and voltage range
- 7-stage programmable temperature range
- 3-stage programmable voltage range
- Bidirectional hysteresis for temperature and voltage

18.6 Charge Control

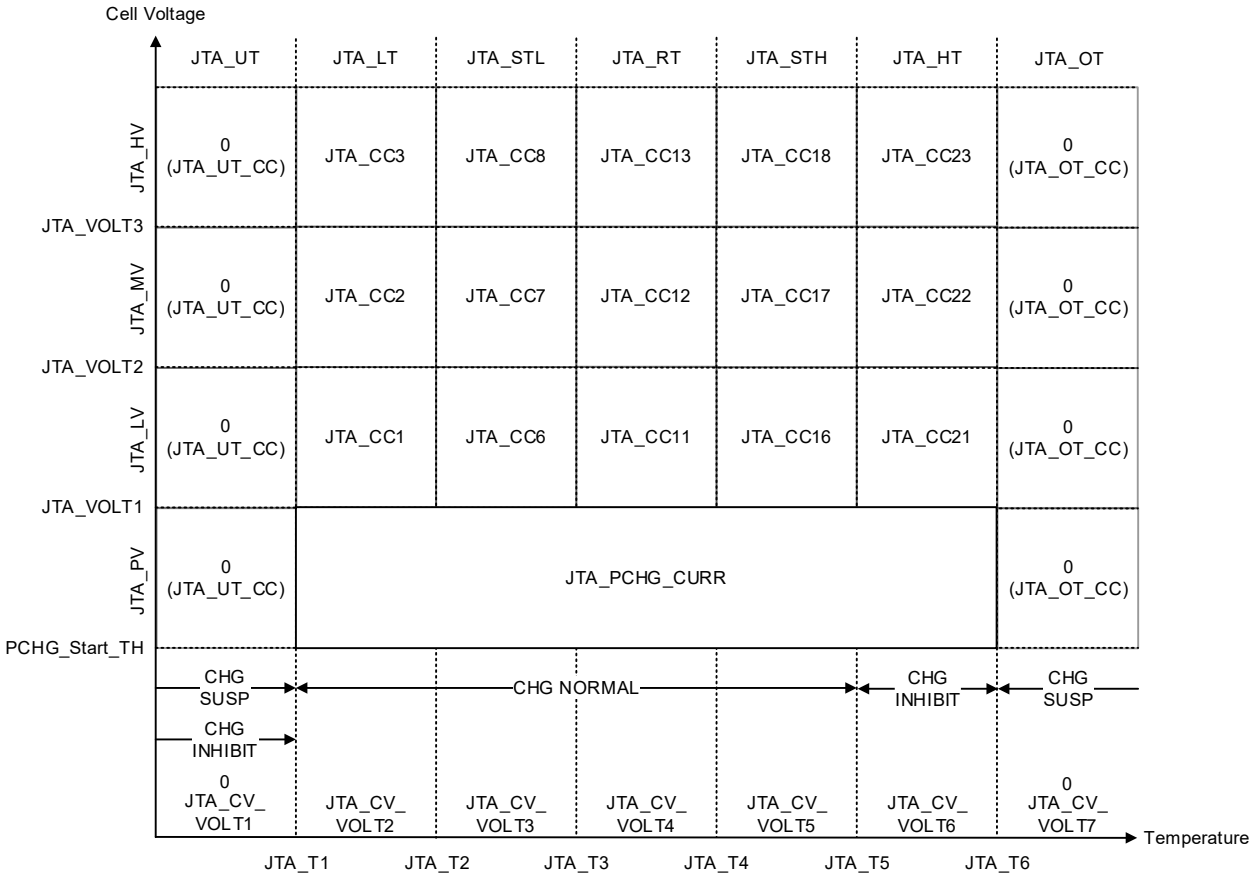


Figure 13. JEITA Temperature and Voltage Range

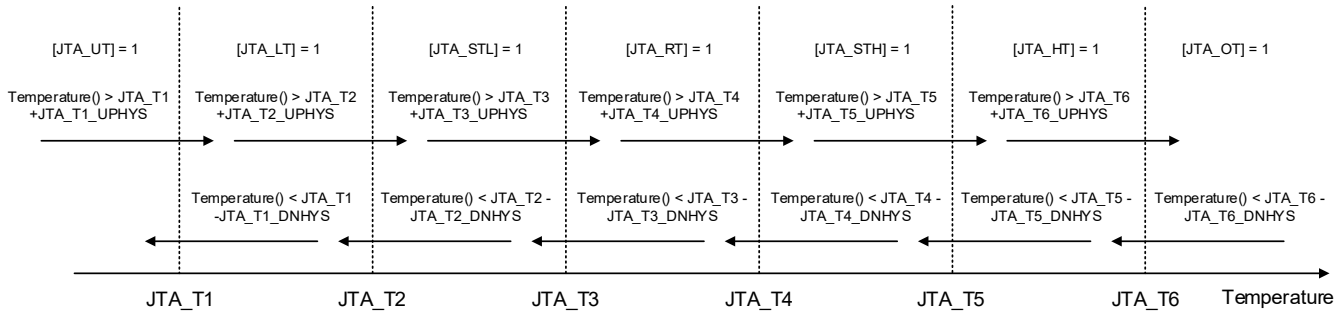


Figure 14. Bidirectional Hysteresis

- Report the charging current and charging voltage after compensation to a smart charger using SMBus broadcasts.
- Report the compensated charging voltage for voltage drop of MOSFET.
- Report the compensated charging voltage due to degradation by temperature and voltage to prevent cell swelling.
- Report the compensated charging voltage and charging current due to degradation by cycle, SOH or runtime.
- Supports pre-charging and zero-voltage charging.
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range.
- Reports charging fault and also indicates charge status via charge and discharge alarms.

18.7 Cell Balancing Control

The RT9441 supports passive cell balancing with embedded bypass switches and can balance multiple cells simultaneously during charging or rest. The cell balancing algorithm determines the capacity needed to be bypassed to balance of all cells. The RT9441 also supports voltage-based cell balancing. It can achieve higher cell balance current by using an external cell balancing circuit.

18.8 Black Box Recorder

- Record the last three safety statuses to black box when permanent failure occurs.
- Update the lifetime log when a permanent failure occurs.
- Record additional three permanent failure statuses to black box after the first permanent failure occurs.

18.9 Lifetime Data Log

The RT9441 supports lifetime logging of important battery data. The following data are updated every 10 hours if a difference is detected between values in RAM and data flash:

- Maximum and minimum cell voltages
- Maximum delta cell voltage
- Maximum charge current
- Maximum discharge current
- Maximum average discharge current
- Maximum average discharge power
- Maximum and minimum cell temperature
- Maximum delta cell temperature
- Maximum and minimum internal sensor temperature
- Maximum MOSFET temperature
- Number of safety events occurrences and the last cycle of the occurrence
- Number of valid charge termination and the last cycle of the valid charge termination
- Number of Qmax updates and the last cycle of the Qmax updates
- Number of shutdown events
- Cell balancing time for each cell
- Total FW runtime and time spent in each temperature range.

18.10 Intel Dynamic Battery Power Technology (DBPT V2.0)

The RT9441 supports DBPT V2.0 by providing the available max power and max current to prevent system reset or trigger termination voltage under peak loading.

18.11 IATA Support

The RT9441 supports several commands and procedures to satisfy the IATA criteria when the battery pack is in shipping.

18.12 LED Display

The RT9441 can drive up to 4-segment LED display for remaining capacity indication and/or a permanent failure code indication.

18.13 FUSE Driver

The RT9441 can use FUSE driver to blow an in-line fuse and permanently disable the battery pack.

18.14 Emergency Shutdown

The emergency shutdown feature enables a push button action that connects the $\overline{\text{SHUTDN}}$ pin to shut down the battery pack system before removing the battery. A high-to-low signal on the $\overline{\text{SHUTDN}}$ pin turns off the CHG and DSG MOSFETs, disconnecting the power from the system to safely remove the battery pack. The CHG and DSG MOSFETs can be turned on again by another high-to-low signal detected by the $\overline{\text{SHUTDN}}$ pin or when a data flash configurable timeout is reached.

18.15 System Present Operation

The RT9441 checks $\overline{\text{PRES}}$ periodically (every 1 second). If $\overline{\text{PRES}}$ input is pulled to ground by the external system, the RT9441 detects this as the system being present.

18.16 2-Series, 3-Series, or 4-Series Cell Configuration

- In a 2-series cell configuration, VC4 is shorted to VC3, and VC3 is shorted to VC2.
- In a 3-series cell configuration, VC4 is shorted to VC3.

18.17 Communication

The RT9441 uses SMBus in MASTER mode with packet error checking (PEC) options, in accordance with the SBS specification.

18.18 SMBus On and Off State

The RT9441 detects an SMBus off state when both SMBC and SMBD are low for two or more seconds, then enters sleep mode. Clearing this state requires either SMBC or SMBD to transition high, which will cause and device to enter normal mode from sleep mode.

18.19 SBS Commands

Refer to the RT9441 Technical Reference Manual for detailed description.

18.20 Authentication

The RT9441 supports three authentications.

- HMAC SHA1 authentication

- Key 16 bytes and challenge 20 bytes
- Execution time 1ms

- HMAC SHA256 authentication
  - Key 32 bytes and challenge 32 bytes
  - Execution time 2ms
- ECC authentication
  - ECC algorithm with ECDSA 256 bits, and signature execution time is within 100ms.

18.21 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-32L 4x4 package, the thermal resistance, θ_{JA}, is 27.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (27.8°C/W) = 3.59W for a WQFN-32L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 15 allows the user to estimate the effect of rising ambient temperature on the maximum power dissipation.

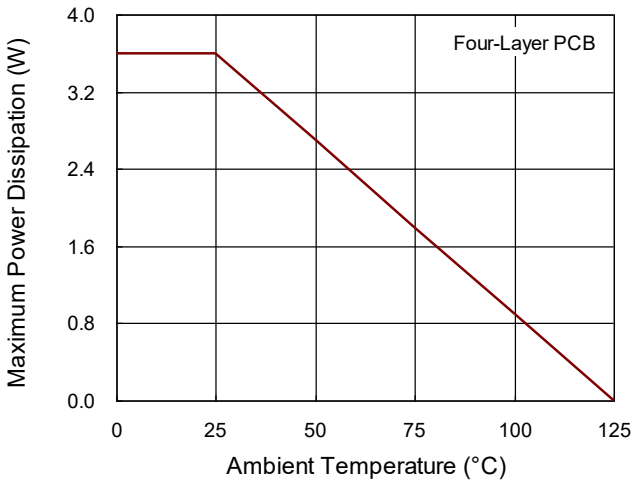


Figure 15. Derating Curve of Maximum Power Dissipation

18.22 Layout Considerations

1. The capacitor for the BAT pin must be placed as close as possible to the pin.
2. The capacitors for the VDD1P73 and VDD1P2 pins must be placed as close as possible to the pin.

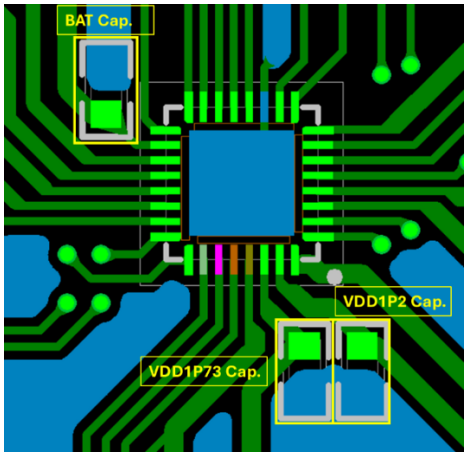


Figure 16. BAT, VDD1P73 & VDD1P2 Capacitors

3. The VC4, VC3, VC2, VC1 and VC0 paths must make Kelvin sense connections to each cell's positive and negative terminals to minimize the IR drop effect on voltage measurement accuracy.
   - The Input filter should be placed as close as possible to the IC.

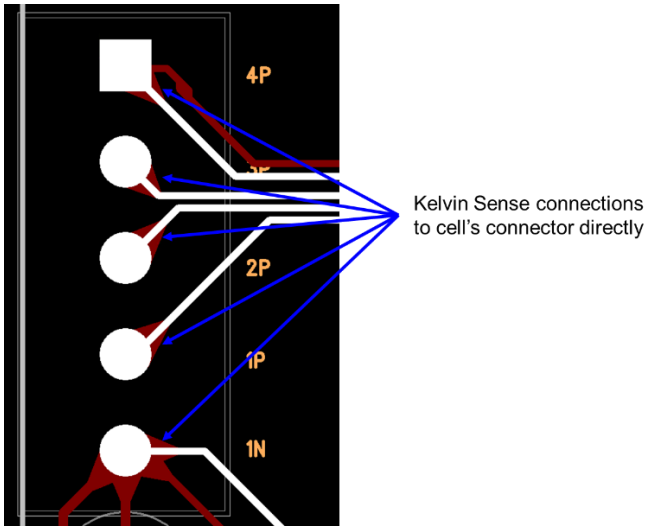


Figure 17. Cell Voltage Sense Circuit

4. The CSN and CSP paths must make Kelvin sense connections to RS to avoid the IR drop effect on current measurement accuracy.
   - Layout traces should be symmetrical for minimum current offset and noise pickup.
   - The Input filter should be placed as close as possible to the IC.

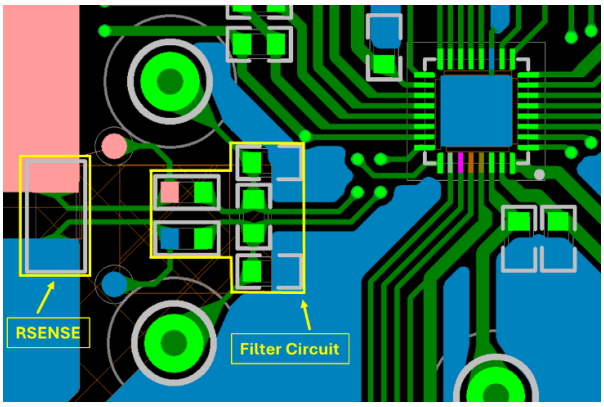


Figure 18. Current Sense Circuit

5. Place a spark gap at the communication connector to protect SMBC and SMBD from the system ESD.
   - It is suggested that the spacing between the points be 0.2mm.
   - The spark gap must be placed on outer layer of the PCB and cannot be coated with any protective covering.

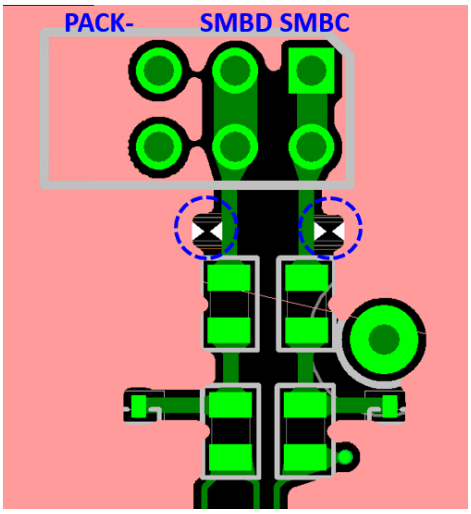


Figure 19. ESD Protection for Communication Interface

6. Use wide copper and short traces to minimize inductance in the CHG/DSG MOSFET bypass and pack terminal bypass capacitor connections.

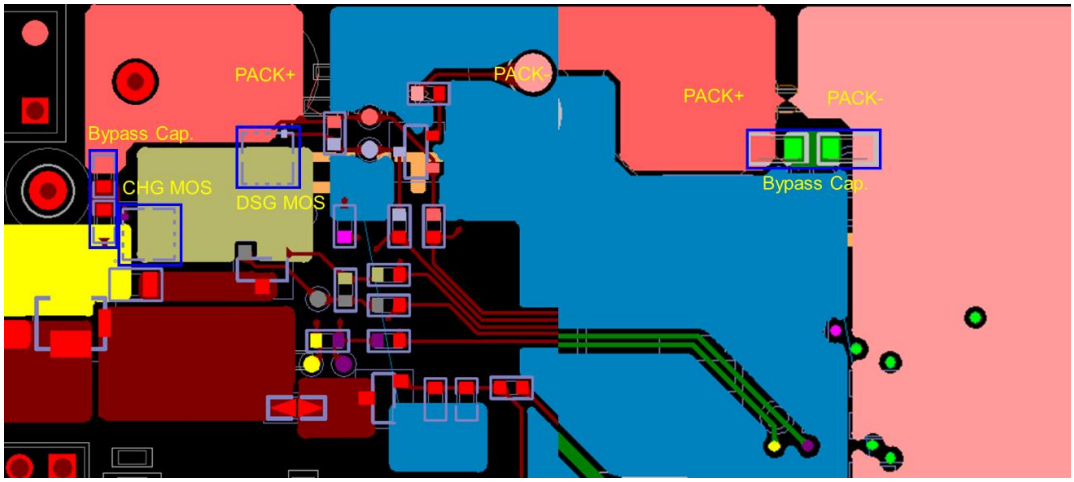


Figure 20. CHG/DSG MOSFET Circuit

7. The impedance (RPCB) between CSP and VSS must be minimized.

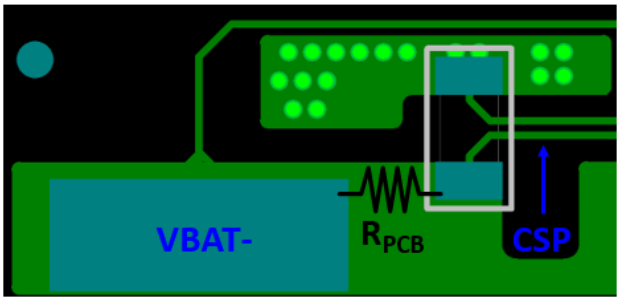


Figure 21. Impedance Minimization between VSS to CSP

Layout example

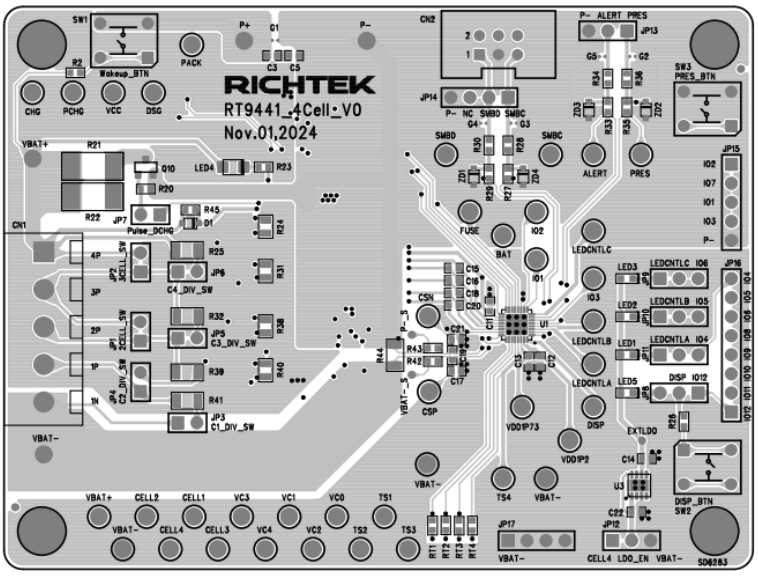


Figure 22. Top Layer

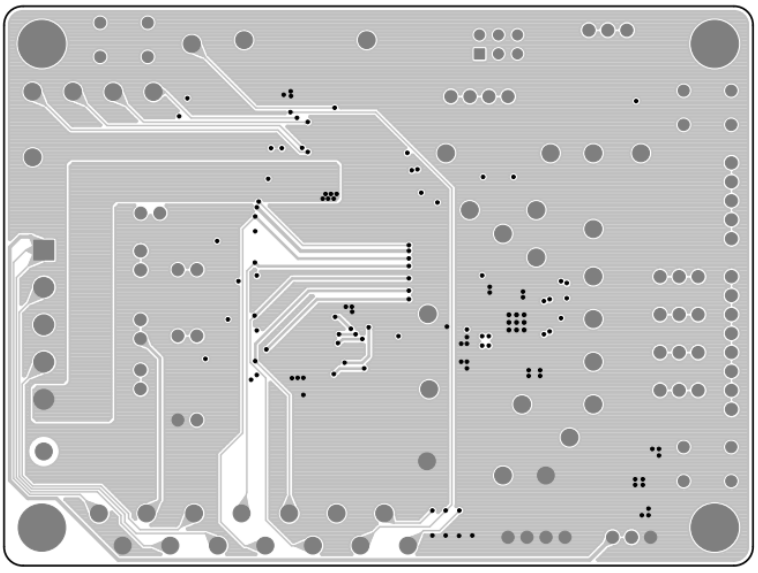


Figure 23. 2nd Layer

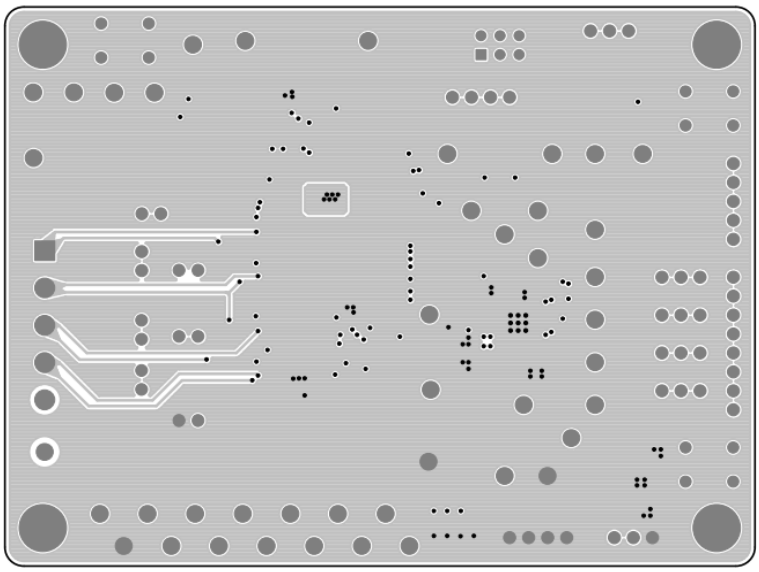


Figure 24. 3rd Layer

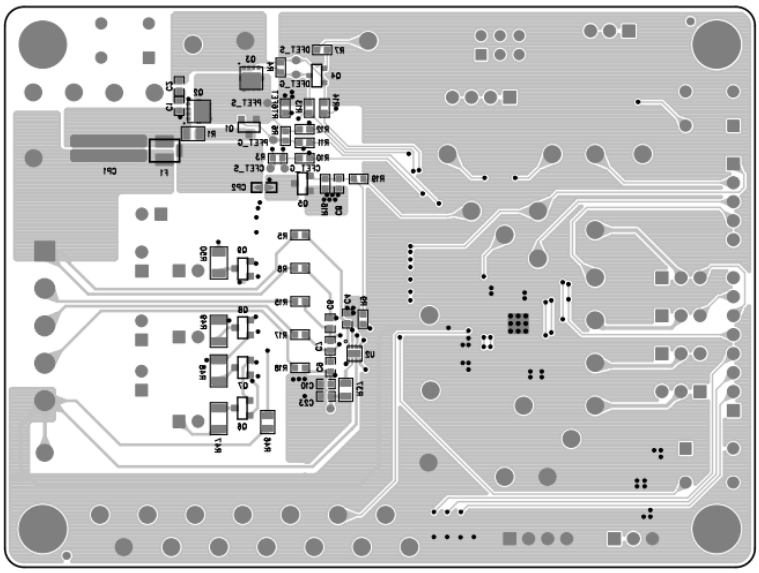
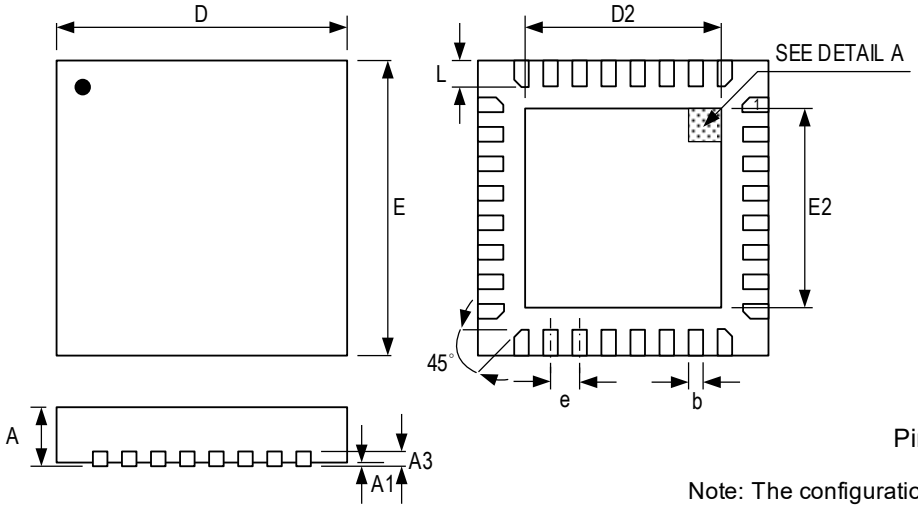
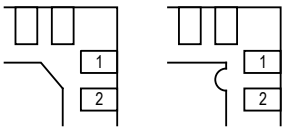


Figure 25. Bottom Layer

Note 6. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

19 Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

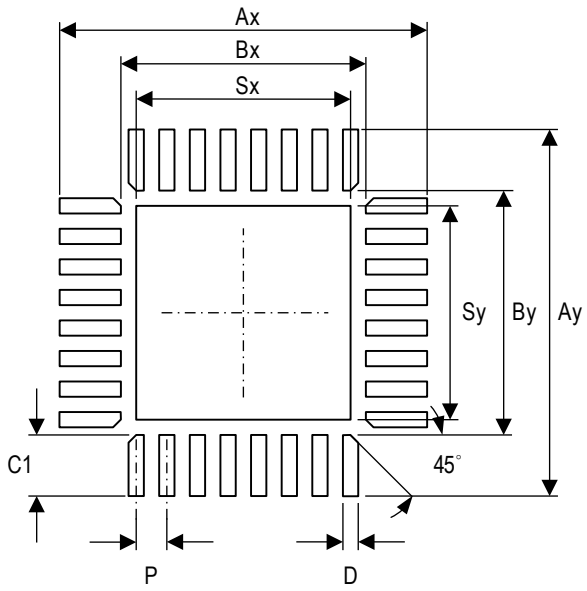
Note: The configuration of the Pin #1 identifier is optional. but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.150	0.250	0.006	0.010
D		3.900	4.100	0.154	0.161
D2	Option 1	2.650	2.750	0.104	0.108
	Option 2	2.750	2.850	0.108	0.112
E		3.900	4.100	0.154	0.161
E2	Option 1	2.650	2.750	0.104	0.108
	Option 2	2.750	2.850	0.108	0.112
e		0.400		0.016	
L		0.300	0.400	0.012	0.016

W-Type 32L QFN 4x4 Package

Note 7. The package of the RT9441 uses Option 2.

20 Footprint Information

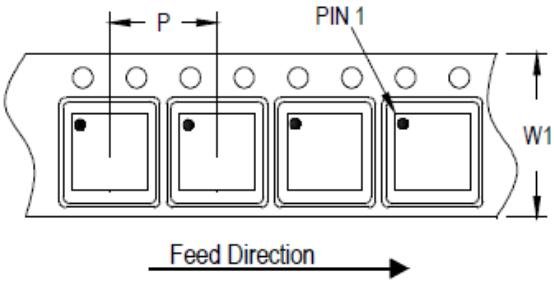


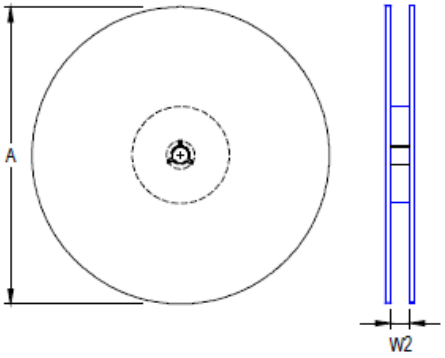
Package		Number of Pins	Footprint Dimension (mm)										Tolerance
			P	Ax	Ay	Bx	By	C*32	C1*8	D	Sx	Sy	
V/W/U/XQFN4*4-32	Option1	32	0.40	4.80	4.80	3.20	3.20	0.80	0.75	0.20	2.80	2.80	±0.05
	Option2												

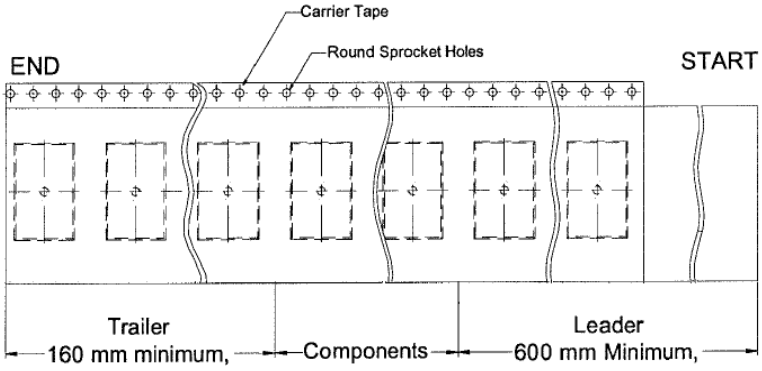
Note 8. The package of the RT9441 uses Option 2.

21 Packing Information

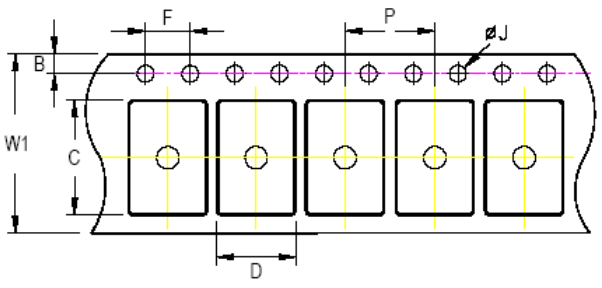
21.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 4x4	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN/DFN 4x4	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm²	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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22 Datasheet Revision History

Version	Date	Description
00	2026/5/14	First Edition