RICHTEK®

RT9478

24V Input for 2 to 4 Cell NVDC Buck-Boost Battery Charge Controller with PSYS, PROCHOT, IBAT, and IBUS Pins, and SMBus

1 General Description

The RT9478 is a 4-switch bidirectional buck-boost Narrow Voltage DC (NVDC) charge controller, designed to charge 2- to 4-cell batteries from a wide range of DC power sources, including USB-C Power Delivery (PD) sources, conventional AC-DC charger adapters, and mobile batteries. It also compliant with Intel IMVP 9.2 features.

The device's SMBus serial communication interface enables flexible programming of various parameters, including charging current, charging voltage, IMVP features, and protection thresholds for overvoltage and undervoltage conditions affecting the input, battery, and system outputs.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

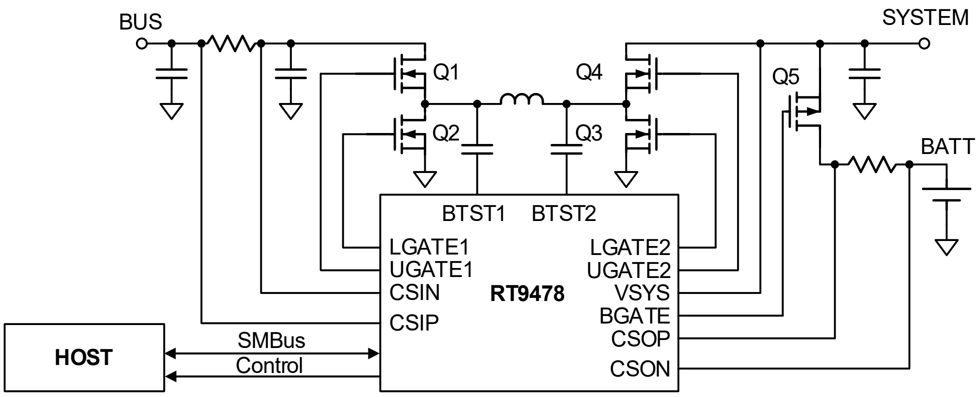
2 Applications

- Notebook PCs
- Tablets/Chromebooks
- Drones
- Portable Speakers
- Portable Devices and Accessories

3 Features

- **Programmable Frequency: 720kHz/800kHz/1.2MHz**
- **Wide Input Voltage Range from 3.8V to 24V**
- **Average Input Current Regulation (AICR)**
- **Minimum Input Voltage Regulation (MIVR)**
- **Support 10mΩ and 5mΩ Sensing Resister**
- **High Accuracy for 2% Battery Charge Current and 0.5% Voltage Regulation**
- **Wide Battery Regulation Voltage Range from 5V to 19.2V**
- **Support IMVP 9.2 Compliant Features**
- **Multi-Level Input Current Limit**
- **Vmin Active Protection (VAP)**
- **PROCHOT Open-Drain Output**
- **System Power Monitor (PSYS)**
- **Support USB On-The-Go (OTG)**
- **5V NMOSFET Gate Driver**
- **8-Bit A/D Converter for Monitor Functions**
- **Input, System and Battery Voltage**
- **Input (IBUS) and Battery (IBAT) Current**
- **System Power**
- **Independent Comparator Input Voltage**
- **Low Battery Quiescent Current**
- **Programmable System Overvoltage Protection**
- **Protection**
- **Input, System and Battery Overvoltage Protection**
- **System Undervoltage Protection**
- **Input and Battery Overcurrent Protection**
- **Over-Temperature Protection**
- **SMBus Compliant Serial Communication**

4 Simplified Application Circuit



5 Ordering Information

RT9478□-□□

Packing
B: Pin 1 Orientation
(Quadrant 2, Follow EIA-481)

Option Code
A: SDA/SCL; VIH = 1.4V, VIL = 0.8V
SMBus Slave Address; 0x09
B: SDA/SCL; VIH = 1.3V, VIL = 0.4V
SMBus Slave Address; 0x6B

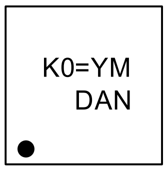
Package Type[1]
N: WQFN-32L 4x4 (W-Type)
(Exposed Pad: Option 2)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with [1] indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

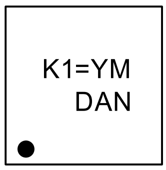
6 Marking Information

RT9478N-AB



K0=: Product Code
YMDAN: Date Code

RT9478N-BB



K1=: Product Code
YMDAN: Date Code

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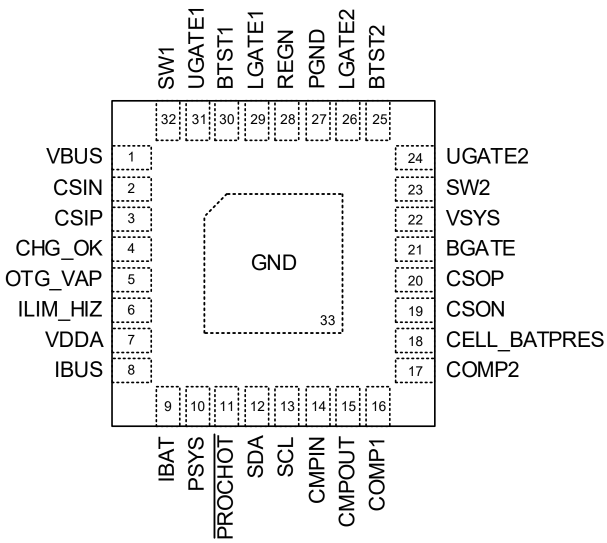
7 Pin Configuration

(TOP VIEW)



WQFN-32L 4x4

8 Functional Pin Description

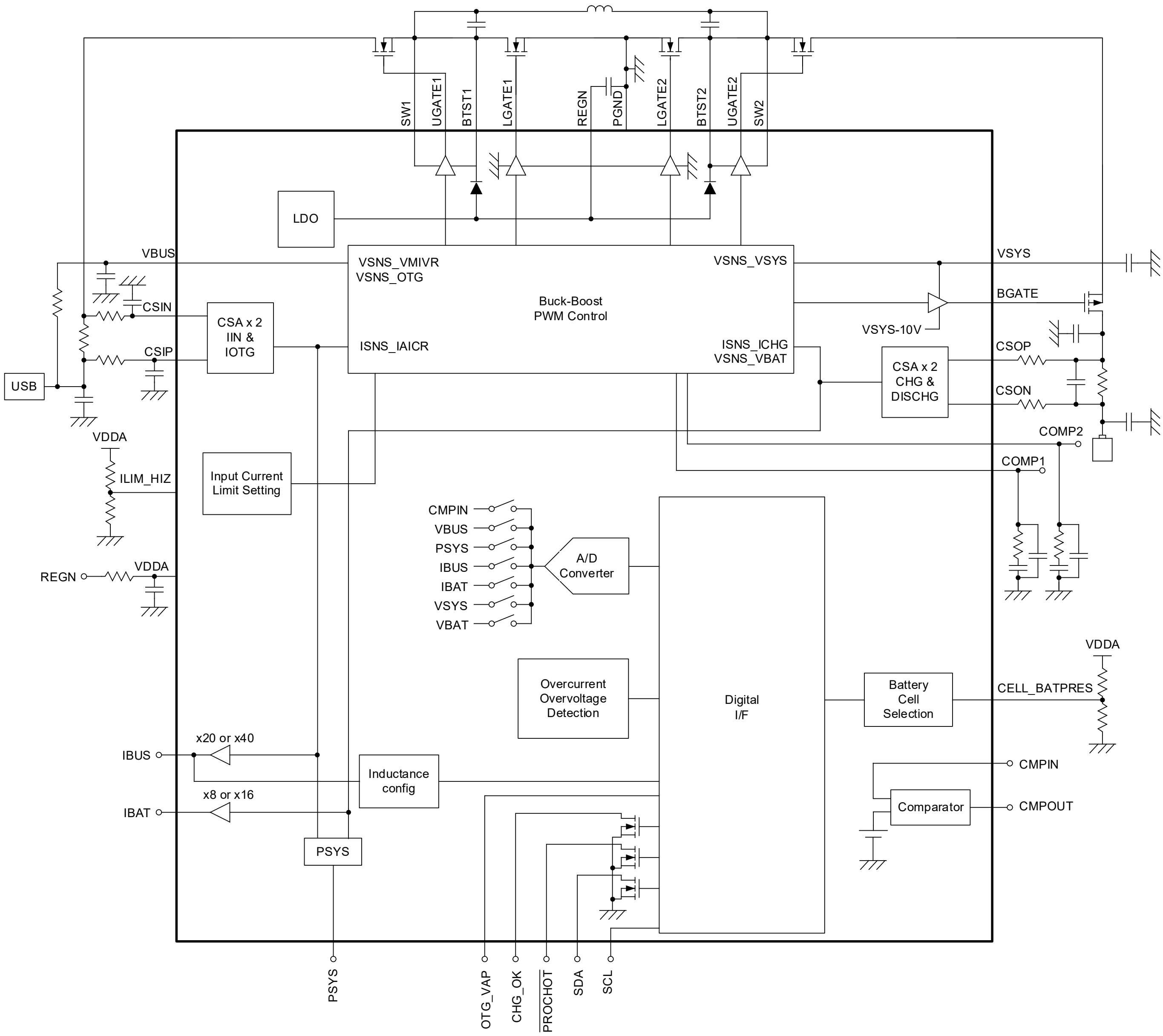
Pin No.	Pin Name	I/O	Pin Function
1	VBUS	PWR	Charger input voltage.
2	CSIN	I	Input current sense negative input.
3	CSIP	I	Input current sense positive input.
4	CHG_OK	O	Open drain, active high indicator to inform the system for charging.
5	OTG_VAP	I	Mode enables pin for OTG/VAP in reverse mode. If OTG and VAP are not used, this pin can be connected to GND.
6	ILIM_HIZ	I	Input current limit programming and HiZ mode enable input pin.
7	VDDA	PWR	Internal power supply pin. Connect REGN through a filter.
8	IBUS	O	Input current monitor analog output pin. This pin is also used to detect inductor value.
9	IBAT	O	Battery current monitor analog output pin. This pin can be unconnected if the battery current monitor is not used.
10	PSYS	O	System power monitor analog output pin. This pin can be unconnected if system power monitor is not used.
11	$\overline{\text{PROCHOT}}$	O	Processor hot indicator open drain output.
12	SDA	I/O	Open drain data signal input/output pin of the SMBus interface.
13	SCL	I	Clock signal input pin of the SMBus interface.
14	CMPIN	I	Independent comparator input pin. This pin can be connected to GND if independent comparator is not used.
15	CMPOUT	O	Open drain output of independent comparator. This pin can be unconnected if independent comparator is not used.
16	COMP1	I	Buck-boost converter compensation pin 1.

Pin No.	Pin Name	I/O	Pin Function
17	COMP2	I	Buck-boost converter compensation pin 2.
18	CELL_BATPRES	I	Battery cell selection pin for 2- to 4-cell battery setting. This pin should be biased from VDDA through a resister divider. This pin is also used for battery removal detection.
19	CSON	I	Battery charge current sense negative input. Positive in case of battery discharge.
20	CSOP	I	Battery charge current sense positive input. Negative in case of battery discharge.
21	BGATE	O	P-channel battery FET (BATFET) gate driver output. Connect to the gate of the battery P-MOSFET, Q5 in the simplified application circuit.
22	VSYS	PWR	System sensing voltage input.
23	SW2	PWR	Boost mode switch node. Connect to the power inductor.
24	UGATE2	O	Boost mode high-side gate driver output. Connect to the gate of high-side N-MOSFET, Q4 in the simplified application circuit.
25	BTST2	PWR	Boost mode supplies for high-side Q4 gate drivers. Connect a 47nF bootstrap capacitor from this pin to the SW2 pin.
26	LGATE2	O	Boost mode low-side gate driver output. Connect to the gate of low-side N-MOSFET, Q3 in the simplified application circuit.
27	PGND	GND	Power Ground.
28	REGN	PWR	5V LDO output supplied from VBUS or VSYS. Connect a 2.2μF capacitor from this pin to GND. This output is internally used for gate drives only.
29	LGATE1	O	Buck mode low-side gate driver output. Connect to gate of low-side N-MOSFET, Q2 in the simplified application circuit.
30	BTST1	PWR	Buck mode supplies for high-side Q1 gate driver. Connect a 47nF bootstrap capacitor from this pin to the SW1 pin.
31	UGATE1	O	Buck mode high-side gate driver output. Connect to the gate of high-side N-MOSFET, Q1 in the simplified application circuit.
32	SW1	PWR	Buck mode switch node. Connect to the power inductor.
33 (Exposed Pad)	GND	GND	Ground. The exposed pad must be soldered to a large PCB pattern to achieve sufficient thermal performance.

8.1 IO Type Definition

- PWR: Power Pin
- GND: Ground Pin
- I: Input Pin
- O: Output Pin
- I/O: Input/Output Pin

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2, Note 3)

- BTST1, BTST2, UGATE1, UGATE2 ---------- –0.3V to 35V
- BGATE ---------- –0.3V to 30V
- LGATE1, LGATE2 ---------- –0.3V to 6V
- SW1, SW2 ---------- –2V (50ns), –0.3V (DC) to 30V
- CSIP, CSIN, CSOP, CSON ---------- –0.3V to 30V
- CSIP to CSIN, CSOP to CSON ---------- –0.5V to 0.5V
- VBUS, VSYS ---------- –0.3V to 30V
- CHG_OK, OTG_VAP, REGN, VDDA, ILIM_HIZ, SDA, SCL, $\overline{\text{PROCHOT}}$, CELL_BATPRES, CMPIN, CMPOUT, COMP1, COMP2 ---------- –0.3V to 6V
- IBUS, IBAT, PSYS ---------- –0.3V to 3.6V
- BTST1 to SW1, BTST2 to SW2, UGATE1 to SW1, UGATE2 to SW2 ---------- –0.3V to 6V
- VSYS to BGATE ---------- 15V to –0.3V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-32L 4x4 ---------- 2.82W
- Package Thermal Resistance (Note 4)
  WQFN-32L 4x4, θ_{JA} ---------- 35.43°C/W
  WQFN-32L 4x4, θ_{JC} ---------- 0.95°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 5)
  HBM (Human Body Model) ---------- 2kV
  CDM (Charged Device Model) ---------- 500V

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. Absolute Maximum Ratings and ESD Susceptibility are guaranteed at T_J = 25°C.

Note 4. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package

Note 5. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 6)

- VBUS -- 0V to 24V
- CSON (Battery Voltage) --- 0V to 19.2V
- CHG_OK, OTG_VAP, SDA, SCL, PROCHOT, CMPIN, CMPOUT ----------------------------- 0V to 5.5V
- Ambient Temperature Range --- –40°C to 85°C
- Junction Temperature Range -- –40°C to 125°C

Note 6. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

($V_{BUS\_UVLO\_R}$ < V_{BUS} < $V_{BUS\_OVP\_F}$, –40°C < T_J < 125°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VSYS Voltage Regulation						
System Voltage Regulation Accuracy (Charge Disabled and OOA Disabled)	$V_{SYS\_REG\_ACC}$	VBAT_REG (0x15[14:3]) = 0x41A0 (16.8V)	V_{CSON} + 30	V_{CSON} + 150	V_{CSON} + 480	mV
		VBAT_REG (0x15[14:3]) = 0x3138 (12.6V)	V_{CSON} + 30	V_{CSON} + 150	V_{CSON} + 400	mV
		VBAT_REG (0x15[14:3]) = 0x20D0 (8.4V)	V_{CSON} + 30	V_{CSON} + 150	V_{CSON} + 400	mV
Minimum System Voltage Regulation Range	$V_{SYS\_MIN\_REG\_RNG}$		5	--	19.2	V
Minimum System Voltage Regulation Accuracy (V_{CSON} below Reg 0x3E setting, EN_OOA = 0b)	$V_{SYS\_MIN\_REG\_ACC}$	VSYS_MIN (0x3E[15:8]) = 0x7B00	--	12.3	--	V
			–2	--	2	%
		VSYS_MIN (0x3E[15:8]) = 0x5C00	--	9.2	--	V
			–2	--	2	%
		VSYS_MIN (0x3E[15:8]) = 0x4200	--	6.6	--	V
			–3	--	3	%
Battery Voltage Regulation						
Battery Voltage Regulation Range	$V_{BAT\_REG\_RNG}$		5	--	19.2	V
Battery Voltage Regulation Accuracy (Charge Enable)	$V_{BAT\_REG\_ACC}$	VBAT_REG (0x15[14:3]) = 0x41A0, T_J = 0 to 85°C	--	16.8	--	V
			–0.5	--	0.5	%
		VBAT_REG (0x15[14:3]) = 0x3138, T_J = 0 to 85°C	--	12.6	--	V
			–0.5	--	0.5	%
		VBAT_REG (0x15[14:3]) = 0x20D0, T_J = 0 to 85°C	--	8.4	--	V
			–0.6	--	0.6	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Battery Current Regulation						
Battery Current Regulation Differential Voltage Range	$V_{CHG\_REG\_RNG}$	$V_{CSO} = V_{CSOP} – V_{CSON}$	0	--	81.28	mV
Charge Battery Current Regulation Accuracy	$I_{CHG\_REG\_ACC}$	ICHG_CTRL (0x14[12:6]) = 0x1000, T_J = 0 to 85°C	--	4.096	--	A
			–3	--	2	%
		ICHG_CTRL (0x14[12:6]) = 0x0800, T_J = 0 to 85°C	--	2.048	--	A
			–4	--	3	%
		ICHG_CTRL (0x14[12:6]) = 0x0400, T_J = 0 to 85°C	--	1.024	--	A
			–5	--	6	%
		ICHG_CTRL (0x14[12:6]) = 0x0200, T_J = 0 to 85°C	--	0.512	--	A
			–12	--	12	%
Pre-Charge Battery Current Limit	I_{LIM_PRECHG}	V_{CSON} < VSYS_MIN (0x3E[15:8])	--	384	--	mA
Pre-Charge Battery Current Regulation Accuracy with R_{SENSE_IN} = 10mΩ	$I_{PRECHG\_REG\_ACC}$	ICHG_CTRL (0x14[12:6]) = 0x0180, T_J = 0 to 85°C	--	384	--	mA
			–15	--	15	%
		ICHG_CTRL (0x14[12:6]) = 0x0100, T_J = 0 to 85°C	--	256	--	mA
			–20	--	20	%
		ICHG_CTRL (0x14[12:6]) = 0x00C0, T_J = 0 to 85°C	--	192	--	mA
			–25	--	25	%
		ICHG_CTRL (0x14[12:6]) = 0x0080, T_J = 0 to 85°C	--	128	--	mA
			–30	--	30	%
CSOP, CSON Leakage Current Mismatch	$I_{LK\_DIFF\_CSOP\_CSON}$		–45	--	–9.5	μA
Average Input Current Regulation (AICR)						
AICR Differential Voltage Range with R_{SENSE_IN} = 10mΩ	$V_{AICR\_REG\_RNG}$	Differential voltage: $V_{CSIP} – V_{CSIN}$	0.5	--	64	mV
AICR Accuracy with 10mΩ CSIP/CSIN Series Resistor	$I_{AICR\_REG\_ACC}$	AICR_HOST (0x3F[14:8]) = 0x4E00, T_J = –40 to 105°C	3800	3900	4000	mA
		AICR_HOST (0x3F[14:8]) = 0x3A00, T_J = –40 to 105°C	2800	2900	3000	mA
		AICR_HOST (0x3F[14:8]) = 0x1C00, T_J = –40 to 105°C	1300	1400	1500	mA
		AICR_HOST (0x3F[14:8]) = 0x0800, T_J = –40 to 105°C	300	400	500	mA
CSIP, CSIN Leakage Current Mismatch	$I_{LK\_DIFF\_CSIP\_CSIN}$	$V_{CSIP} = V_{CSIN}$ = 11V	–37.5	--	–13	μA
Setting Voltage Range for AICR (ILIM_HIZ Pin)	$V_{AICR\_RNG\_ILIM\_HIZ}$		0.958	--	3.333	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
AICR Setting Voltage Accuracy on the ILIM_HIZ pin	$I_{AICR\_REG\_ACC\_ILIM\_HIZ}$	V_{ILIM_HIZ} = 2.166V T_J = –40 to 105°C	3800	4000	4200	mA
		V_{ILIM_HIZ} = 1.833V T_J = –40 to 105°C	2800	3000	3200	mA
		V_{ILIM_HIZ} = 1.333V T_J = –40 to 105°C	1300	1500	1700	mA
		V_{ILIM_HIZ} = 1.0 V T_J = –40 to 105°C	300	500	700	mA
ILIM_HIZ Pin Leakage Current	$I_{LK\_ILIM\_HIZ}$	V_{ILIM_HIZ} = 5V	–1	--	1	μA
Minimum Input Voltage Regulation (MIVR)						
MIVR Range	$V_{MIVR\_REG\_RNG}$		3.2	--	19.52	V
MIVR Accuracy	$V_{MIVR\_REG\_ACC}$	VMIVR (0x3D[13:6]) = 0x3C80	--	18.688	--	V
			–2	--	2	%
		VMIVR (0x3D[13:6]) = 0x7B00	--	10.88	--	V
			–2.5	--	2.5	%
		VMIVR (0x3D[13:6]) = 0x0500	--	4.48	--	V
			–5	--	5	%
OTG Current Regulation						
OTG Output Current Regulation Differential Voltage Range	$V_{OTG\_REG\_RNG}$		0	--	63.5	mV
OTG Output Current Regulation Accuracy	I_{OTG_ACC}	OTG_CUR (0x3C[14:8]) = 0x3C00	2.8	3	3.2	A
		OTG_CUR (0x3C[14:8]) = 0x1E00	1.3	1.5	1.7	
		OTG_CUR (0x3C[14:8]) = 0x0A00	0.3	0.5	0.7	
OTG Voltage Regulation						
OTG Voltage Regulation Range (OOA Disabled)	$V_{OTG\_REG\_RNG}$		3	--	24	V
OTG Voltage Regulation Accuracy (OOA Disabled)	$V_{OTG\_REG\_ACC}$	OTG_VOL (0x3B[13:2]) = 0x2710	--	20	--	V
			–2	--	2	%
		OTG_VOL (0x3B[13:2]) = 0x1770	--	12	--	V
			–2	--	2	%
		OTG_VOL (0x3B[13:2]) = 0x09C4	--	5	--	V
			–3	--	3	%
REGN Regulator						
REGN Regulator Voltage	V_{REGN_REG}	V_{BUS} = 10V	4.75	5	5.25	V
REGN Voltage in Drop Out Mode	V_{REGN_DROP}	V_{BUS} = 5V, I_{REGN} = 20mA	--	100	200	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
REGN Current Limit when Converter is Enabled	I_{LIM_REGN}	V_{BUS} = 10V	65	78	--	mA
REGN Undervoltage	$V_{REGN\_UVLO\_F}$		3	3.1	3.2	V
Quiescent Current						
Device Powered by Battery. BATFET On	$I_{Q\_BATFET\_ON}$	Low power mode V_{BAT} = 18V, EN_LPWR (0x12[15]) = 1 (Low power mode), EN_PROCHOT_LPWR = 0 (PROCHOT disabled)	--	18	45	μA
		Low power mode with PROCHOT V_{BAT} = 18V, EN_LPWR (0x12[15]) = 1 (Low power mode), EN_PROCHOT_LPWR = 1 (PROCHOT enabled), PSYS_CONFIG (0x30[13:12]) = 11 (PSYS disabled)	--	24	60	
		Performance mode without PSYS V_{BAT} = 18V, EN_LPWR (0x12[15]) = 0 (Performance mode), PSYS_CONFIG (0x30[13:12]) = 11 (PSYS disabled)	--	850	1170	
		Performance mode with PSYS V_{BAT} = 18V, EN_LPWR (0x12[15]) = 0 (Performance mode), PSYS_CONFIG (0x30[13:12]) = 00 (PSYS enabled)	--	920	1270	
Device Powered VBUS BATFET Off (Note 7)	$I_{Q\_STBY\_BUCK}$	V_{BUS} = 20V, V_{BAT} = 12.6V, Qg = 7.5nC, no load, EN_OOA (0x12[10]) = 0 (OOA disabled)	--	1.4	--	mA
	$I_{Q\_STBY\_BOOST}$	V_{BUS} = 5V, V_{BAT} = 8.4V, Qg = 7.5nC, no load, EN_OOA (0x12[10]) = 0 (OOA disabled)	--	3.6	--	mA
	$I_{Q\_STBY\_BB}$	V_{BUS} = 12V, V_{BAT} = 12V, Qg = 7.5nC, no load, EN_OOA (0x12[10]) = 0 (OOA disabled)	--	2.1	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Device Powered by Battery, OTG Mode (Note 7)	$I_{Q\_STBY\_OTG}$	V_{BAT} = 8.4V, VOTG_REG (0x3B[13:2]) = 0x09C4 (5V), Qg = 7.5nC, no load, EN_OOA (0x12[10]) = 0 (OOA disabled)	--	1.8	--	mA
		V_{BAT} = 8.4V, VOTG_REG (0x3B[13:2]) = 0x1770 (12V), Qg = 7.5nC, no load, EN_OOA (0x12[10]) = 0 (OOA disabled)	--	3.0	--	
		V_{BAT} = 8.4V, VOTG_REG (0x3B[13:2]) = 0x2710 (20V), Qg = 7.5nC, no load, EN_OOA (0x12[10]) = 0 (OOA disabled)	--	5.3	--	
Input Current and Battery Current Monitor						
Input Common Mode Range	$V_{CSIP\_CSIN\_RNG}$		3.8	--	24	V
IBUS Output Clamp Voltage	V_{IBUS_CLAMP}		3.1	3.2	3.3	V
IBUS Output Current	I_{IBUS}		--	--	1	mA
Input Current Sensing Gain	A_{IBUS}	IBUS_GAIN (0x12[4]) = 0	--	20	--	V/V
		IBUS_GAIN (0x12[4]) = 1	--	40	--	
Input Current Monitor Accuracy	V_{IBUS_ACC}	$V_{(CSIP-CSIN)}$ = 40.96mV	–2	--	2	%
		$V_{(CSIP-CSIN)}$ = 20.48mV	–3	--	3	
		$V_{(CSIP-CSIN)}$ = 10.24mV	–6	--	6	
		$V_{(CSIP-CSIN)}$ = 5.12mV	–10	--	10	
Maximum Capacitance at the IBUS Pin (Note 7)	C_{IBUS_MAX}		--	--	100	pF
Input Common Mode Range	$V_{CSOP\_CSON\_RNG}$		3.8	--	19.2	V
IBAT Output Clamp Voltage	V_{IBAT_CLAMP}		3.1	3.2	3.3	V
IBAT Output Current	I_{IBAT}		--	--	1	mA
Charge and Discharge Current Sensing Gain	A_{IBAT}	IBAT_GAIN (0x12[3]) = 0	--	8	--	V/V
		IBAT_GAIN (0x12[3]) = 1	--	16	--	
Charge and Discharge Current Monitor Accuracy	V_{IBAT_ACC}	$V_{(CSOP-CSON)}$ = 40.96mV	–2	--	2	%
		$V_{(CSOP-CSON)}$ = 20.48mV	–4	--	4	
		$V_{(CSOP-CSON)}$ = 10.24mV	–7	--	7	
		$V_{(CSOP-CSON)}$ = 5.12mV	–15	--	15	
Maximum Capacitance at the IBAT Pin (Note 7)	C_{IBAT_MAX}		--	--	100	pF

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System Power (PSYS) Monitor						
PSYS Clamp Voltage	V_{PSYS_CLAMP}		3.1	3.2	3.3	V
PSYS Output Current Range	I_{PSYS_RNG}		0	--	160	μA
PSYS System Gain	A_{PSYS}	I(PSYS)/(P(BUS) +P(BAT)), PSYS_CONFIG (0x30[13:12]) = 00 (PBUS + PBAT), PSYS_RATIO (0x30[9]) = 1 (1μA/W)	--	1	--	μA/W
		I(PSYS)/P(BUS), PSYS_CONFIG (0x30[13:12]) = 01 (PBUS), PSYS_RATIO (0x30[9]) = 1 (1μA/W)	--	1	--	
PSYS Gain Accuracy	A_{PSYS_ACC}	PSYS_CONFIG (0x30[13:12]) = 00 (PBUS + PBAT), VBUS = 19.5V, 45W PSYS_RATIO (0x30[9]) = 1 (1μA/W), CSIP – CSIN = 23.077mV, CSOP – CSON = 0V, R_{SENSE_IN} = 10mΩ, R_{SENSE_BAT} = 10mΩ, T_J = 0 to 85°C	–5	--	5	%
		PSYS_CONFIG (0x30[13:12]) = 00 (PBUS + PBAT), VBAT = 11V, 44W PSYS_RATIO (0x30[9]) = 1 (1μA/W), CSIP – CSIN = 0V, CSON – CSOP = 40mV, R_{SENSE_IN} = 10mΩ, R_{SENSE_BAT} = 10mΩ, T_J = 0 to 85°C	–5	--	5	
		PSYS_CONFIG (0x30[13:12]) = 01 (PBUS), VBUS = 19.5V, 45W PSYS_RATIO (0x30[9]) = 1 (1μA/W), CSIP – CSIN = 23.077mV, R_{SENSE_IN} = 10mΩ, R_{SENSE_BAT} = 10mΩ, T_J = 0 to 85°C	–5	--	5	
Vmin Active Protection PROCHOT Comparator						
VAP VSYS Rising Threshold 1	$V_{SYS\_VAP1\_R}$	VSYS_TH1 (0x33 [7:2]) = 100000	6.3	6.5	6.65	V
VAP VSYS Falling Threshold 1	$V_{SYS\_VAP1\_F}$	VSYS_TH1 (0x33 [7:2]) = 100000	6.2	6.4	6.65	V
VAP VSYS Threshold 1 Hysteresis	$V_{SYS\_VAP1\_HYS}$		--	100	--	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VSYS Threshold 1 Falling Deglitch for VAP Shooting	$t_{DEGLITCH\_VSYS\_VAP1}$		--	4	--	μs
VAP VSYS Rising Threshold 2	$V_{SYS\_VAP2\_R}$	VSYS_TH2 (0x37 [7:2]) = 0x011011	5.8	6	6.15	V
VAP VSYS Falling Threshold 2	$V_{SYS\_VAP2\_F}$	VSYS_TH2 (0x37 [7:2]) = 0x011011	5.7	5.9	6.05	V
VAP VSYS Threshold 2 Hysteresis	$V_{SYS\_VAP2\_HYS}$		--	100	--	mV
VSYS Threshold 2 Falling Deglitch for Throttling	$t_{DEGLITCH\_VSYS\_VAP2}$		--	4	--	μs
VAP Mode VBUS Rising Threshold	$V_{BUS\_VAP\_R}$	VBUS_VAP_TH (0x37[15:9]) = 0000101	3.65	3.85	4.0	V
VAP Mode VBUS Falling Threshold	$V_{BUS\_VAP\_F}$	VBUS_VAP_TH (0x37[15:9]) = 0000101	3.5	3.7	3.85	V
VAP Mode VBUS Threshold Hysteresis	$V_{BUS\_VAP\_HYS}$		--	150	--	mV
VBUS Falling Deglitch for Throttling	$t_{DEGLITCH\_VBUS\_VAP}$		--	4	--	μs
Protection Comparators						
VSYS Undervoltage Rising Threshold	$V_{SYS\_UVP\_R}$	VSYS_UVP (0x36[15:13]) = 001	3.7	3.8	3.9	V
VSYS Undervoltage Falling Threshold	$V_{SYS\_UVP\_F}$	VSYS_UVP (0x36[15:13]) = 001	3.55	3.65	3.75	V
VSYS Undervoltage Hysteresis	$V_{SYS\_UVP\_HYS}$		--	150	--	mV
VBUS Undervoltage Rising Threshold	$V_{BUS\_UVLO\_R}$		3.1	3.2	3.3	V
VBUS Undervoltage Falling Threshold	$V_{BUS\_UVLO\_F}$		3	3.1	3.2	V
VBUS Undervoltage Hysteresis	$V_{BUS\_UVLO\_HYS}$		--	100	--	mV
VBUS Converter Enable Rising Threshold	$V_{BUS\_CONVEN\_R}$		3.7	3.8	3.9	V
VBUS Converter Enable Falling Threshold	$V_{BUS\_CONVEN\_F}$		3.4	3.5	3.6	V
VBUS Converter Enable Hysteresis	$V_{BUS\_CONVEN\_HYS}$		--	300	--	mV
VBUS Overvoltage Rising Threshold	$V_{BUS\_OVP\_R}$		26	26.8	27.7	V
VBUS Overvoltage Falling Threshold	$V_{BUS\_OVP\_F}$		25	25.8	26.7	V
VBUS Overvoltage Hysteresis	$V_{BUS\_OVP\_HYS}$		--	1	--	V
VBUS Deglitch Overvoltage Rising	$t_{DEGLITCH\_VBUS\_OVP\_R}$		--	100	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBUS Deglitch Overvoltage Falling	$t_{DEGLITCH\_VBUS\_OVP\_F}$		--	1	--	ms
VBUS (OTG) Undervoltage Falling Threshold	$V_{BUS\_OTG\_UVP\_F}$	As percentage of OTG_VOL (0x3B[13:2])	--	85	--	%
VBUS (OTG) Undervoltage Deglitch Time	$t_{DEGLITCH\_VBUS\_OTG\_UVP}$		--	7	--	ms
VBUS (OTG) Overvoltage Rising Threshold	$V_{BUS\_OTGOVP\_R}$	As percentage of OTG_VOL (0x3B[13:2])	--	110	--	%
VBUS (OTG) Overvoltage Deglitch Time	$t_{DEGLITCH\_VBUS\_OTG\_UVP}$		--	10	--	ms
VBAT Undervoltage Rising Threshold	$V_{BAT\_UVLO\_R}$	V_{CSON} rising	3.58	3.7	3.82	V
VBAT Undervoltage Falling Threshold	$V_{BAT\_UVLO\_F}$	V_{CSON} falling	3.46	3.58	3.7	V
VBAT Undervoltage Hysteresis	$V_{BAT\_UVLO\_HYS}$		--	120	--	mV
VBAT OTG Enable Rising Threshold	$V_{BAT\_OTGEN\_R}$	V_{CSON} rising	4.28	4.4	4.52	V
VBAT OTG Enable Falling Threshold	$V_{BAT\_OTGEN\_F}$	V_{CSON} falling	3.93	4.05	4.17	V
VBAT OTG Enable Hysteresis	$V_{BAT\_OTGEN\_HYS}$		--	350	--	mV
VBAT Overvoltage Rising Threshold	$V_{BAT\_OVP\_R}$	As percentage of VBAT_REG(0x15[14:3]), $6.5V \leq V_{BAT} < 7.4V$	102	104	106	%
		As percentage of VBAT_REG(0x15[14:3]), $7.4V \leq V_{BAT} < 11V$	102.5	104	105.5	
		As percentage of VBAT_REG(0x15[14:3]), $11V \leq V_{BAT}$	103	104	105	
VBAT Overvoltage Falling Threshold	$V_{BAT\_OVP\_F}$	As percentage of VBAT_REG(0x15[14:3]), $6.5V \leq V_{BAT} < 7.4V$	100	102	104	%
		As percentage of VBAT_REG(0x15[14:3]), $7.4V \leq V_{BAT} < 11V$	100.5	102	103.5	
		As percentage of VBAT_REG(0x15[14:3]), $11V \leq V_{BAT}$	101	102	103	
VBAT Overvoltage Hysteresis	$V_{BAT\_OVP\_HYS}$	As percentage of VBAT_REG(0x15[14:3])	--	2	--	%
Discharge Current during BATOVP	$I_{DISCHG\_BAT\_OVP}$	Discharge current through the VSYS pin	--	40	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System Overvoltage Rising Threshold to Turn Off Converter	$V_{SYS\_OVP\_R}$	VSYS_OVP (0x40[14:12]) = 000 (Depends on cell count), 2s by CELL_BATPRES	11.7	12	12.2	V
		VSYS_OVP (0x40[14:12]) = 000 (Depends on cell count), 3s by CELL_BATPRES	19	19.5	20	
		VSYS_OVP (0x40[14:12]) = 000 (Depends on cell count), 4s by CELL_BATPRES	19	19.5	20	
System Overvoltage Hysteresis	$V_{SYS\_OVP\_HYS}$		--	200	--	mV
Discharge Current during SYSOVP	$I_{DISCHG\_SYS\_OVP}$	Discharge current through the VSYS pin	--	40	--	mA
Pre-Charge to Fast Charge Transition						
Pre-Charge to Fast Charge Mode Transient Threshold, V_{CSON} Rising	V_{PRECHG_R}	As percentage of VSYS_MIN (0x3E[15:8]), VBAT < 6.5V	97.5	100	102.5	%
		As percentage of VSYS_MIN (0x3E[15:8]), VBAT $\geq$ 6.5V	98	100	102	
Pre-Charge to Fast Charge Mode Transient Threshold, V_{CSON} Falling	V_{PRECHG_F}	As percentage of VSYS_MIN (0x3E[15:8])	--	97.5	--	%
Fast Charge to Pre-Charge Mode Transient Threshold Hysteresis	V_{PRECHG_HYS}	As percentage of VSYS_MIN (0x3E[15:8])	--	2.5	--	%
Input Overcurrent Comparator						
CSIP to CSIN Rising Threshold	$I_{BUS\_OCP1\_R}$	As percentage of IAICR2 (0x33[15:11]), IBUS_OCP1_TH (0x31[2]) = 1 (200% of IAICR2), I_{AICR2} > 2A	180	200	220	%
Rising Deglitch Time	$t_{DEGLITCH\_BUS\_OCP1\_R}$		--	250	--	μs
Relax Time	$t_{RELAX\_BUS\_OCP1}$		--	250	--	ms
Converter Overcurrent Comparator						
Converter Overcurrent Limit Across Q2 MOSFET Drain to Source Voltage	$V_{LIM\_Q2\_OCP}$	Q2_OCP (0x31[5]) = 1	--	150	--	mV
		Q2_OCP (0x31[5]) = 0	--	210	--	
	$V_{LIM\_Q2\_OCP\_S}$	Q2_OCP (0x31[5]) = 1 (150mV), V_{SYS} < $V_{SYS\_UVLO\_F}$ or V_{CSON} < $V_{BAT\_UVLO\_R}$	--	45	--	mV
		Q2_OCP (0x31[5]) = 0 (210mV), V_{SYS} < $V_{SYS\_UVLO\_F}$ or V_{CSON} < $V_{BAT\_UVLO\_R}$	--	60	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Converter Overcurrent Limit Across CSIP - CSIN Input Current Sensing Resistor	V_{BUS_OCP2}	IBUS_OCP2_TH (0x31[4]) = 1, RSNS_IN (0x30[11]) = 0 (10mΩ)	--	150	--	mV
		IBUS_OCP2_TH (0x31[4]) = 0, RSNS_IN (0x30[11]) = 0 (10mΩ)	--	280	--	
		IBUS_OCP2_TH (0x31[4]) = 0, V_{SYS} < $V_{SYS\_UVLO\_F}$ or V_{CSON} < $V_{BAT\_UVLO\_R}$	--	150	--	
		IBUS_OCP2_TH (0x31[4]) = 1, V_{SYS} < $V_{SYS\_UVLO\_F}$ or V_{CSON} < $V_{BAT\_UVLO\_R}$	--	90	--	
Ship-Mode Discharge Current						
Discharge VBAT Cap	I_{CSON_DISCHG}	EN_SHIP_DCHG (0x30[1]) = 1 (enabled)	--	10	--	mA
	I_{CSOP_DISCHG}	EN_SHIP_DCHG (0x30[1]) = 1 (enabled)	--	10	--	
Over-Temperature Protection (OTP)						
Over-Temperature Protection Rising Threshold (Note 7)	T_{OTP_R}		--	140	--	°C
Over-Temperature Protection Falling Threshold (Note 7)	T_{OTP_F}		--	125	--	°C
Over-Temperature Protection Threshold Hysteresis (Note 7)	T_{OTP_HYS}		--	15	--	°C
Over-Temperature Protection Rising Deglitch	$t_{DEGLITCH\_OTP\_R}$		--	100	--	μs
Over-Temperature Protection Falling Deglitch	$t_{DEGLITCH\_OTP\_F}$		--	12	--	ms
ICRIT PROCHOT Comparator						
Input Current Rising Threshold for Throttling as 10% above I_{AICR2}	I_{CRIT}	Only when I_{AICR2} setting is higher than 2A	105	110	117	%
INOM PROCHOT Comparator						
INOM Rising Threshold as 10% above I_{LIM1}	I_{NOM}	Only when I_{AICR1} setting is higher than 2A	105	110	116	%
Battery Discharge Current Limit PROCHOT Comparator						
I_{DCHG} Threshold1	$I_{DISCHG1}$	IDCHG_TH1 (0x34[15:10]) = 010000, with 10mΩ R_{SENSE_BAT}	--	8192	--	mA
			96	--	103	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I_{DCHG} Threshold1 Deglitch Time	$t_{DEGLITCH\_DISCHG1}$	IDCHG_DEG1 (0x34[9:8]) = 01	1.0625	1.25	1.4375	s
I_{DCHG} Threshold2	$I_{DISCHG2}$	IDCHG_TH1 (0x34[15:10]) = 010000, IDCHG_TH2 (0x36[5:3]) = 001 (150% of IDCHG1_TH1) with 10mΩ R_{SENSE_BAT}	--	12288	--	mA
			96	--	103	%
I_{DCHG} Threshold2 Deglitch Time	$t_{DEGLITCH\_DISCHG2}$	IDCHG_DEG2 (0x36[7:6]) = 01	--	1.6	--	ms
Independent Comparator						
Independent Comparator Threshold	V_{CMPIN_F}	CMP_REF (0x30[7]) = 1, CMPIN falling	1.17	1.2	1.23	V
		CMP_REF (0x30[7]) = 0, CMPIN falling	2.27	2.3	2.33	
Independent Comparator Hysteresis	V_{CMPIN_HYS}	CMPIN rising	--	100	--	mV
Independent Comparator Threshold in Low Power Mode	$V_{CMPIN\_LPWR\_F}$	CMPIN rising, EN_PROCHOT_LPWR (0x30[14]) = 1 (enabled)	--	1.2	--	V
Converter Switching Frequency						
Converter Switching Frequency	f_{SW}	PWM_FREQ (0x12[9]) = 0	1020	1200	1260	kHz
		PWM_FREQ (0x12[9]) = 1	680	800	840	
		PWM_LOWFREQ (0x40[10]) = 1	612	720	756	
Converter OOA Minimum Frequency	$f_{SW\_OOA\_MIN}$	EN_OOA (0x12[10]) = 1 (OOA enabled)	--	25	--	kHz
Frequency Dither Configuration	f_{SW_DITHER}	DITHER_EN (0x36[12:11]) = 00	--	Disable	--	%
		DITHER_EN (0x36[12:11]) = 01	--	±2	--	
		DITHER_EN (0x36[12:11]) = 10	--	±4	--	
		DITHER_EN (0x36[12:11]) = 11	--	±6	--	
BATFET Gate Driver						
Gate Drive Voltage on BATFET	V_{BGATE_ON}	V_{BGATE} = V_{VSYS} – V_{BGATE}	8.5	10	11.5	V
Drain-Source Voltage on BATFET during Ideal Diode Operation	V_{F_IDEAL}	V_{F_IDEAL} = V_{CSON} – V_{VSYS}	--	30	--	mV
BATFET Turn-On Resistance	R_{BGATE_ON}	Measured by sourcing 10μA and 100μA current to BGATE	1.5	2.5	4	kΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
BATFET Turn-Off Resistance	R_{BGATE_OFF}	Measured by sinking 10μA current from BGATE	--	0.8	2.1	kΩ
Input High-Side Driver (UGATE1)						
High-Side Driver (Q1) Turn-On Resistance	$R_{DS\_ON\_Q1}$	$V_{BTST1} - V_{SW1}$ = 5V, DIS_STRGDRV (0x12[8]) = 1 (strong drive disabled)	--	3.1	--	Ω
		$V_{BTST1} - V_{SW1}$ = 5V, DIS_STRGDRV (0x12[8]) = 0 (strong drive enabled)	--	1.6	--	
High-Side Driver (Q1) Turn-Off Resistance	$R_{DS\_OFF\_Q1}$	$V_{BTST1} - V_{SW1}$ = 5V, DIS_STRGDRV (0x12[8]) = 1 (strong drive disabled)	--	0.8	--	Ω
		$V_{BTST1} - V_{SW1}$ = 5V, DIS_STRGDRV (0x12[8]) = 0 (strong drive enabled)	--	0.5	--	
Input High-Side Driver (UGATE2)						
High-Side Driver (Q4) Turn-On Resistance	$R_{DS\_ON\_Q4}$	$V_{BTST2} - V_{SW2}$ = 5V, DIS_STRGDRV (0x12[8]) = 1 (strong drive disabled)	--	3.2	--	Ω
		$V_{BTST2} - V_{SW2}$ = 5V, DIS_STRGDRV (0x12[8]) = 0 (strong drive enabled)	--	1.7	--	
High-Side Driver (Q4) Turn-Off Resistance	$R_{DS\_OFF\_Q4}$	$V_{BTST2} - V_{SW2}$ = 5V, DIS_STRGDRV (0x12[8]) = 1 (strong drive disabled)	--	0.8	--	Ω
		$V_{BTST2} - V_{SW2}$ = 5V, DIS_STRGDRV (0x12[8]) = 0 (strong drive enabled)	--	0.5	--	
Input Low-Side Driver (LGATE1)						
Low-Side Driver (Q2) Turn-On Resistance	$R_{DS\_ON\_Q2}$	V_{REGN} = 5V	--	1.7	--	Ω
Low-Side Driver (Q2) Turn-Off Resistance	$R_{DS\_OFF\_Q2}$	V_{REGN} = 5V	--	0.7	--	Ω
Output Low-Side Driver (LGATE2)						
Low-Side Driver (Q3) Turn-On Resistance	$R_{DS\_ON\_Q3}$	V_{REGN} = 5V	--	1.8	--	Ω
Low-Side Driver (Q3) Turn-Off Resistance	$R_{DS\_OFF\_Q3}$	V_{REGN} = 5V	--	0.3	--	Ω
Integrated Bootstrap Switch (BTST1/BTST2)						
On Resistance	R_{BTST_ON}		1	2.1	4	Ω
Reverse Breakdown Voltage	V_{BTST_RBD}		25	--	--	V
Internal Soft-Start During Charge Enable						
Charge Current Soft-Start Rate	SR_{ICHG}		--	64	--	A/s
Converter Soft-Start						

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VSYS Slew Rate	SR_{SYS}	V_{CSON} < VSYS_MIN (0x3E[15:8])	--	12.5	--	V/ms
VBUS Slew Rate (In OTG Mode)	SR_{BUS}		--	8	--	V/ms
Logic Pins (CHG_OK, OTG_VAP, and ILIM_HIZ or SCL/SDA if Specified)						
Input Low Threshold	V_{IL_SMBUS}	SCL/SDA Option Code A	--	--	0.8	V
		SCL/SDA Option Code B	--	--	0.4	V
Input High Threshold	V_{IH_SMBUS}	SCL/SDA Option Code A	1.4	--	--	V
		SCL/SDA Option Code B	1.3	--	--	V
Output Low Voltage	V_{OL_SMBUS}	SCL/SDA Drain current = 5mA	--	--	0.4	V
Leakage Current	I_{LK_SMBUS}	Pin voltage = 5V	--	--	1	μA
Output Low Voltage	V_{OL_OD}	Drain current = 5mA At CHG_OK and CMPOUT pins	--	--	0.3	V
Leakage Current	I_{LK_OD}	Pin voltage = 5V At CHG_OK and CMPOUT pins	--	--	1	μA
Output Low Voltage	$V_{OL\_PROCHOT}$	50Ω is pulled up to 1.05V/5mA	--	--	0.3	V
Leakage Current	$I_{LK\_PROCHOT}$	Pin voltage = 5V At PROCHOT pin	--	--	1	μA
Input Low Threshold	V_{IL_LOGIC}	At OTG_VAP pin	--	--	0.8	V
Input High Threshold	V_{IH_LOGIC}	At OTG_VAP pin	1.4	--	--	V
Analog Inputs (CELL_BATPRES Pin and ILIM_HIZ Pin)						
Voltage to Exit HiZ Mode Rising Threshold	$V_{IL\_ILIM\_HIZ}$	At the ILIM_HIZ pin	0.8	--	--	V
Voltage to Enter HiZ Mode Falling Threshold	$V_{IH\_ILIM\_HIZ}$	At the ILIM_HIZ pin	--	--	0.4	V
4S Setting Condition	V_{CELL_4S}	At CELL_BATPRES pin voltage as % of the VDDA pin	68.4	75	81.5	%
3S Setting Condition	V_{CELL_3S}		51.7	55	65	%
2S Setting Condition	V_{CELL_2S}		18.4	40	48.5	%
Battery Present Rising Threshold	$V_{CELL\_BATPRES\_R}$	At CELL_BATPRES pin voltage as % of the VDDA pin	18	--	--	%
Battery Removed Falling Threshold	$V_{CELL\_BATPRES\_F}$		--	--	15	%
SMBus Timing Characteristics (Note 7)						
Clock/Data Rise Time	t_R		--	--	300	ns
Clock/Data Fall Time	t_F		--	--	300	ns
Clock High Period	t_{HIGH}		0.6	--	50	μs
Clock Low Period	t_{LOW}		1.3	--	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
START Condition Setup Time	$t_{SU;STA}$		0.6	--	--	μs
Hold Time After START Condition	$t_{HD;STA}$		0.6	--	--	μs
Data Setup Time	$t_{SU;DAT}$		100	--	--	ns
Data Hold Time	$t_{HD;DAT}$		0	--	--	ns
STOP Condition Setup Time	$t_{SU;STO}$		0.6	--	--	μs
Bus Free Time Between START and STOP	t_{BUF}		1.3	--	--	μs
Bus Operating Frequency	f_{SCL}		10	--	400	kHz
SMBus Host Communication Error						
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	--	35	ms
Watchdog Timeout						
Watchdog Timeout Period	t_{WDI}	WATCHDOG (0x12[14:13]) = 00	--	Disable	--	s
		WATCHDOG (0x12[14:13]) = 01	4.25	5	5.75	
		WATCHDOG (0x12[14:13]) = 10	74.8	88	101.2	
		WATCHDOG (0x12[14:13]) = 11	148.75	175	201.25	

Note 7. Guaranteed by design.

RICHTEK

13 Typical Application Circuit

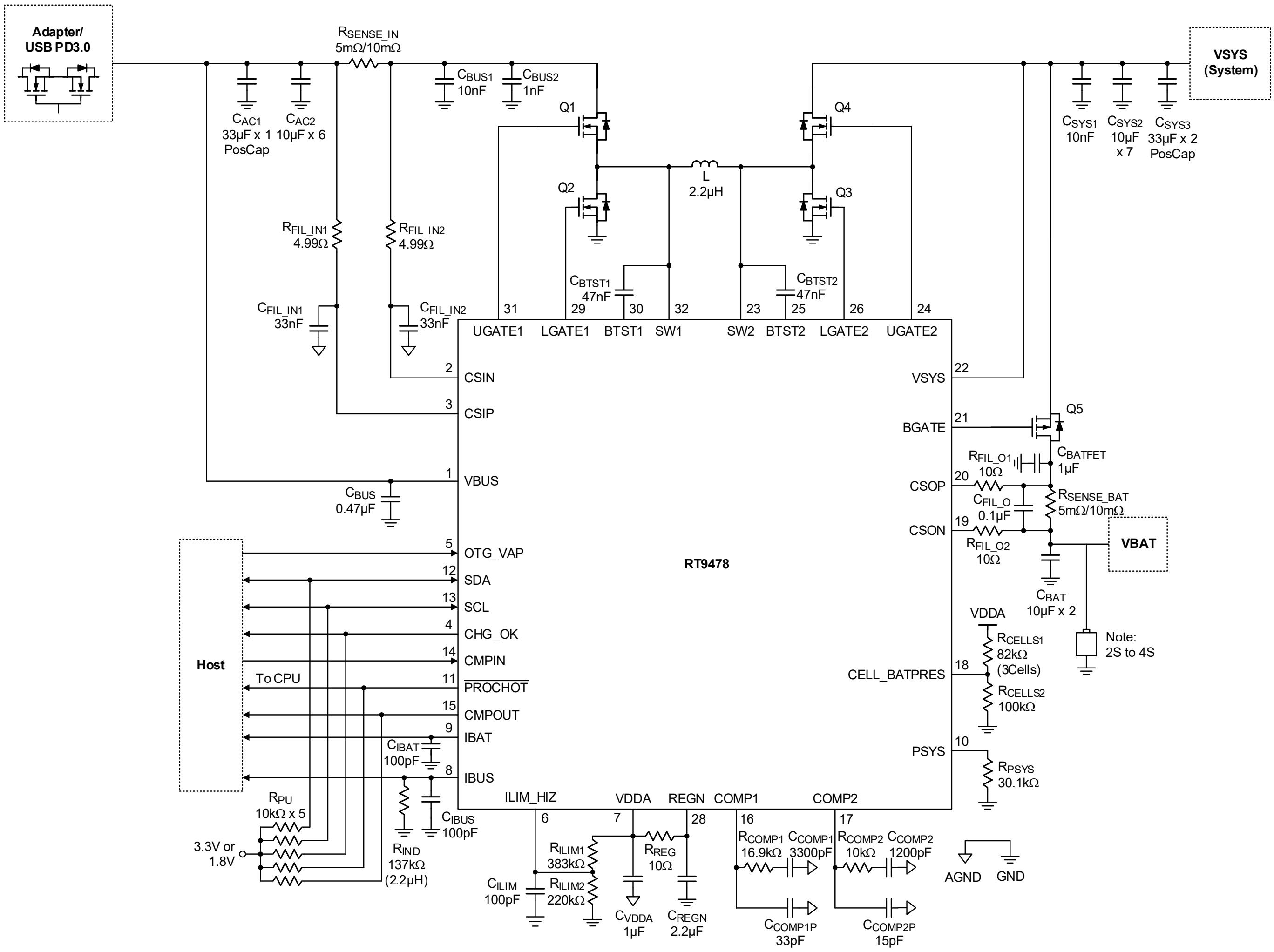
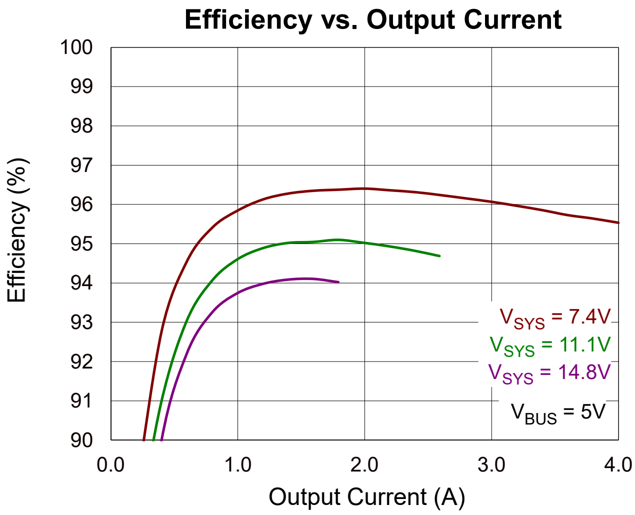


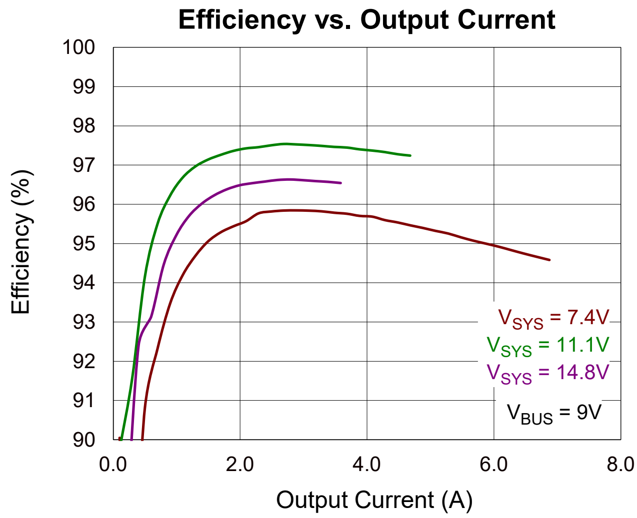
Table 1. Recommended Components Information

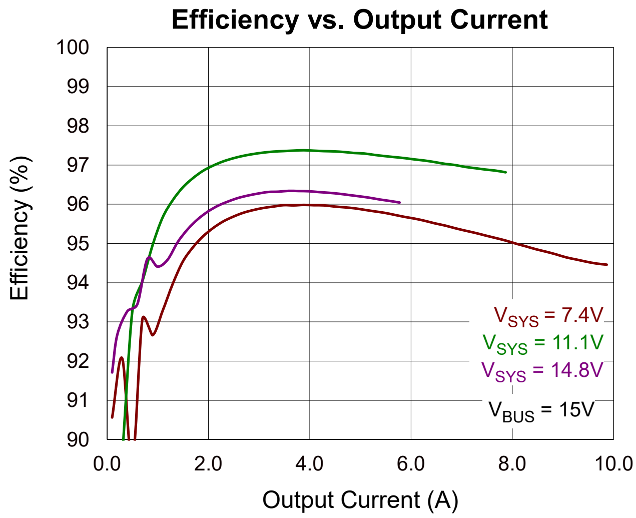
Name	Part Number	Description	Package	Manufacturer
C_{BUS}	0603B474K500CT	0.47μF/50V/X7R	0603	WALSIN
C_{AC1}	T521D336M035ATE065	33μF/35V	7343-31	KEMET
C_{AC2}	GRM21BR6YA106KE43L	10μF/35V/X5R	0805	MURATA
C_{BUS1}	0603B103K500CT	10nF/50V/X7R	0603	WALSIN
C_{BUS2}	0402B102K500CT	1nF/50V/X7R/	0402	WALSIN
C_{BTST1}, C_{BTST2}	0603B473K500CT	47nF/50V/X7R	0603	WALSIN
C_{SYS1}	0603B103K500CT	10nF/50V/X7R	0603	WALSIN
C_{SYS2}	GRM21BR61E106KA73L	10μF/25V/X5R	0805	MURATA
C_{SYS3}	T521D336M035ATE065	33μF/35V	7343-31	KEMET
C_{BAT}	GRM188R61E106KA73	10μF/25V/X5R	0603	MURATA
C_{BATFET}	0603X105K250CT	1μF/25V/X5R	0603	WALSIN
C_{REGN}	GRM155R61A225KE01	2.2μF/10V/X5R	0603	WALSIN
C_{VDDA}	0402X105K100CT	1μF/10V/X5R	0402	WALSIN
C_{FIL_IN1}, C_{FIL_IN2}	0603B333K500CT	33nF/50V/X7R	0603	WALSIN
C_{IBAT}, C_{IBUS}, C_{ILIM}	UMK105CH101JV-F	100pF/50V/C0H	0402	TAIYO YUDEN
C_{COMP1}	GRM155R71H332KA01D	3300pF/50V/X7R	0402	MURATA
C_{COMP2}	GRM155R71H122KA01D	1200pF/50v/X7R	0402	MURATA
C_{COMP1P}	0402N330J500CT	33pF/50V/NPO	0402	WALSIN
C_{COMP2P}	GRM1555C1H150JA01D	15pF/50V/C0G	0402	MURATA
Q_1, Q_2, Q_3, Q_4	AONR36368	Vds = 30V/Id = 32A	DFN3X3	ALPHA & OMEGA
Q_5	AONR21307	Vds = -30V/Id = -24A	DFN3X3	ALPHA & OMEGA
L	BMRHDY1010302R2MA1	2.2μH	101030	CHILISIN
R_{SENSE_IN}, R_{SENSE_BAT}	WW12NR010FTL	0.01/1W/1%	1206	WALSIN
R_{PSYS}	WR06X3012FTL	30.1K/1%	0603	WALSIN
R_{COMP1}	RE0402FRE0716K9L	16.9K/0402/1%	0402	YAGEO
R_{COMP2}	WR04X1002FTL	10K/0402/1%	0402	WALSIN

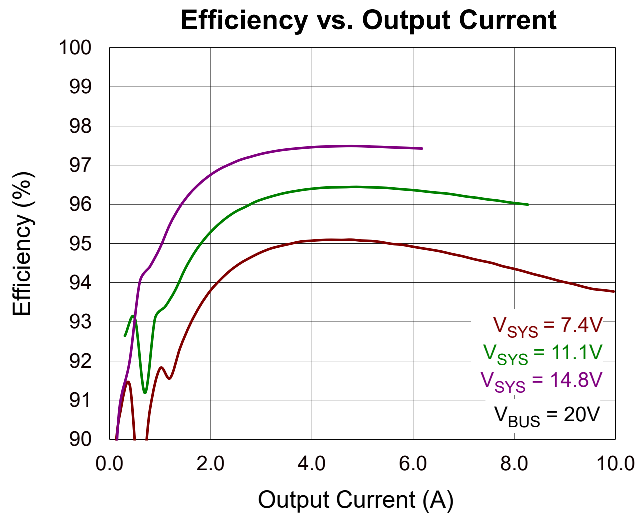
14 Typical Operating Characteristics

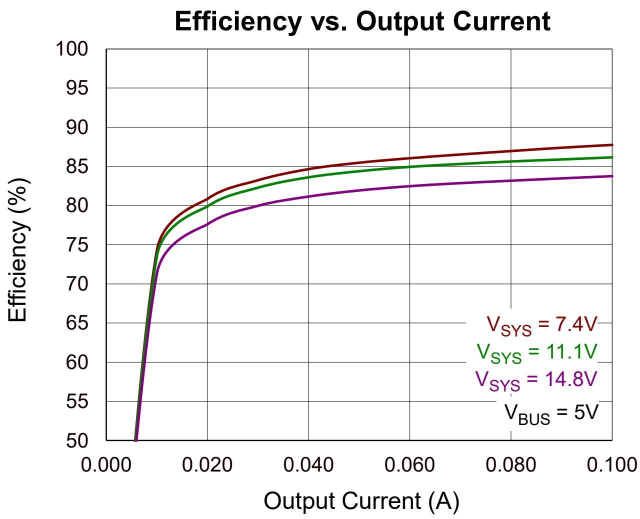
R_{SENSE_IN} = 10mΩ, R_{SENSE_BAT} = 10mΩ, f_{SW} = 800kHz, L = 2.2μH, RDC = 8mΩ, Q1 to Q4: AONR36368 (Note 8)

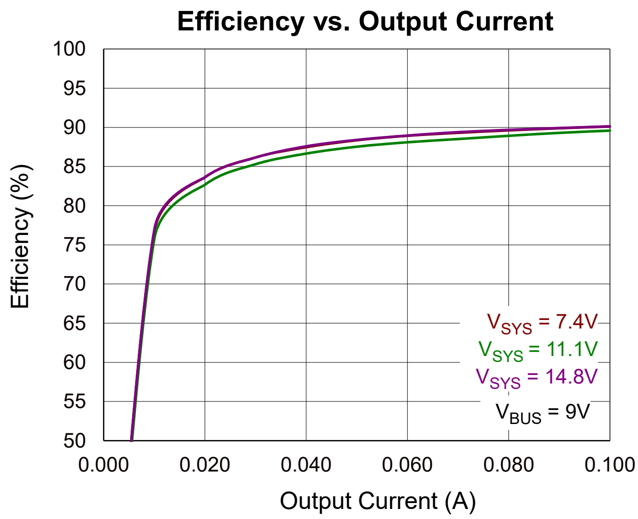


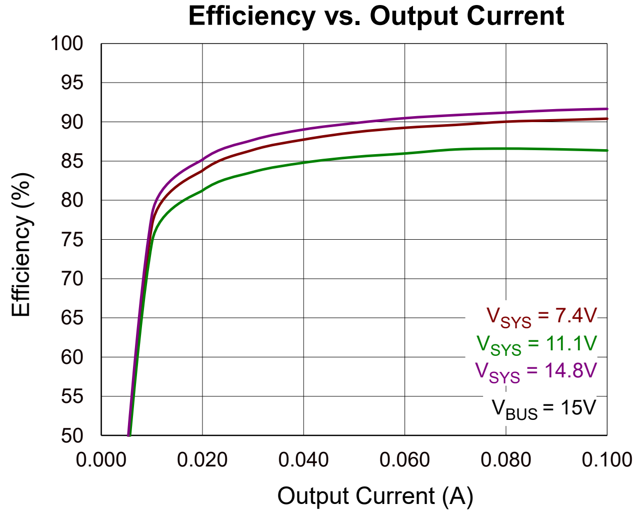


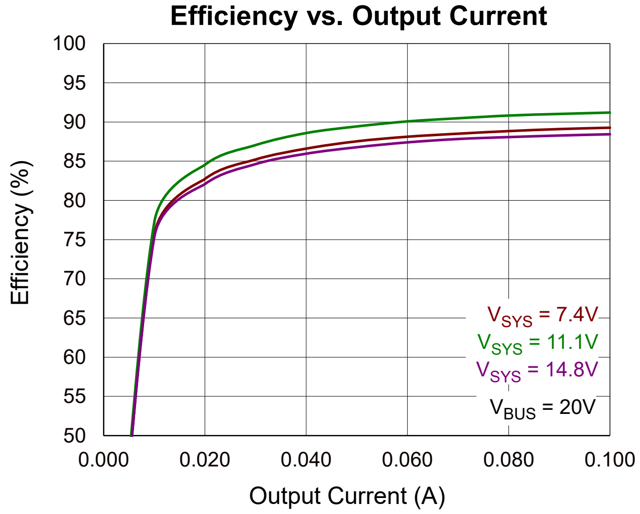


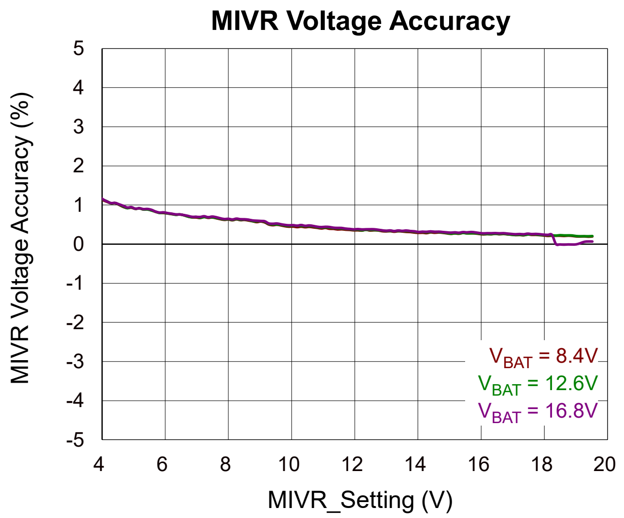


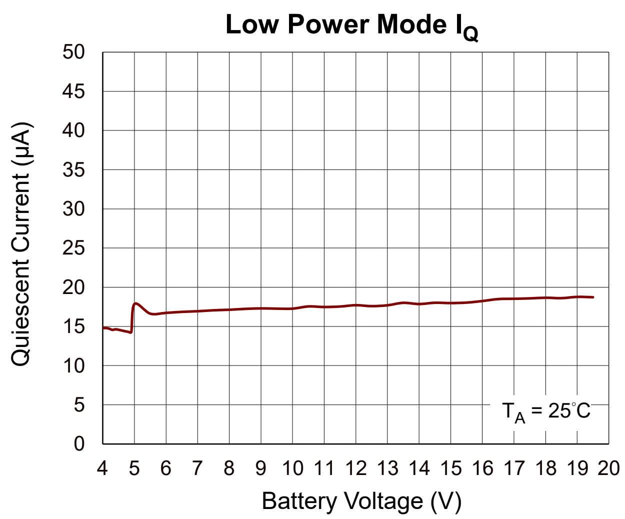


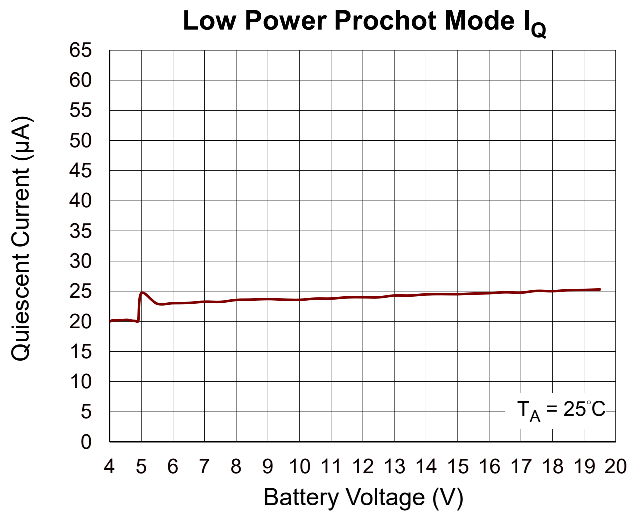


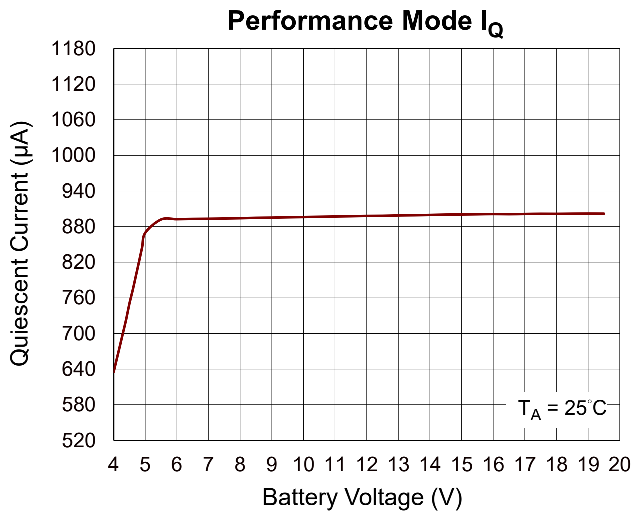

Efficiency vs. Output Current
Efficiency (%)
Output Current (A)
VSYS = 7.4V
VSYS = 11.1V
VSYS = 14.8V
VBUS = 15V

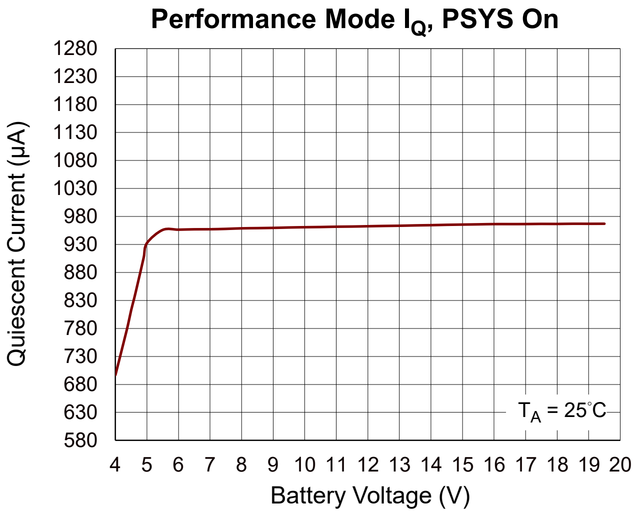

Efficiency vs. Output Current
Efficiency (%)
Output Current (A)
VSYS = 7.4V
VSYS = 11.1V
VSYS = 14.8V
VBUS = 20V

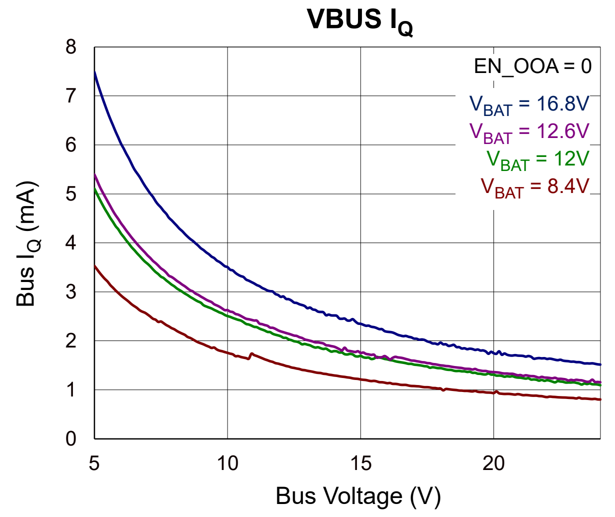

MIVR Voltage Accuracy
MIVR Voltage Accuracy (%)
MIVR_Setting (V)
VBAT = 8.4V
VBAT = 12.6V
VBAT = 16.8V

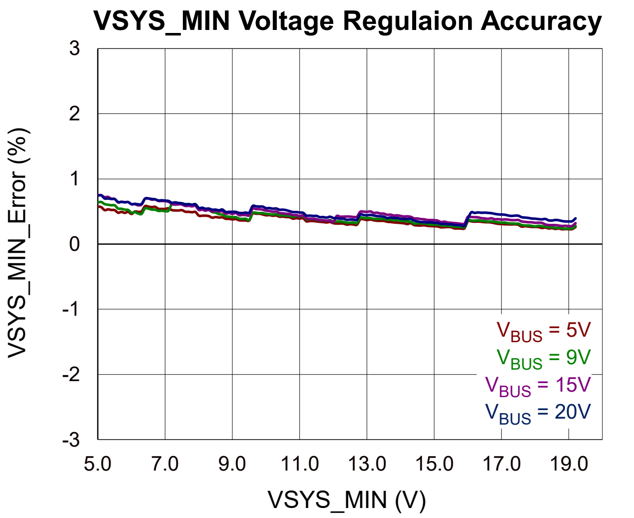

Low Power Mode IQ
Quiescent Current (μA)
Battery Voltage (V)
TA = 25°C

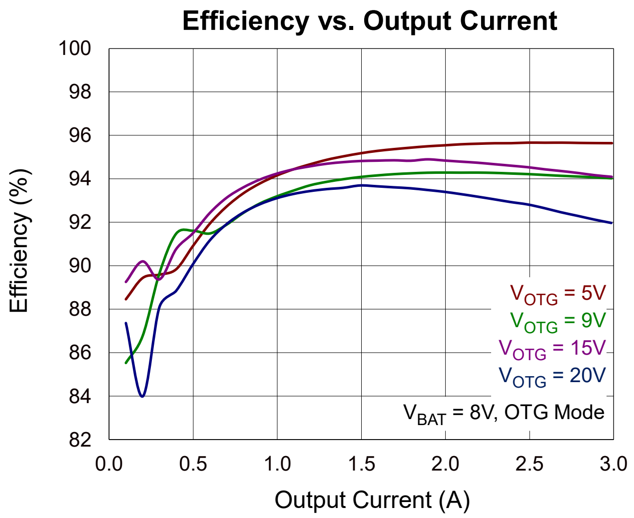

Low Power Prochot Mode IQ
Quiescent Current (μA)
Battery Voltage (V)
TA = 25°C

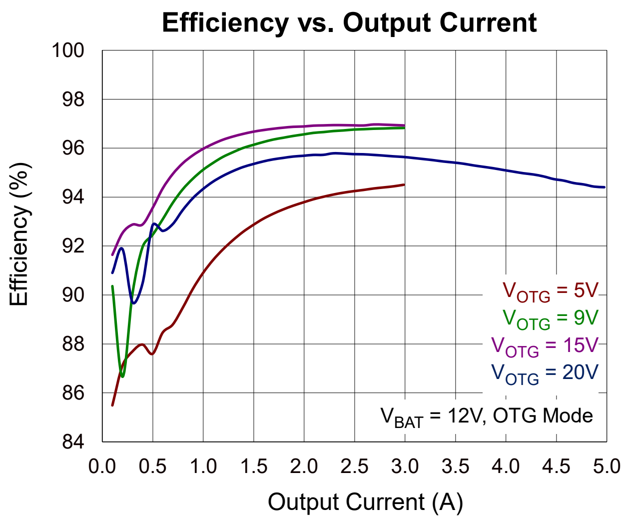

Performance Mode IQ
Quiescent Current (μA)
Battery Voltage (V)
TA = 25°C

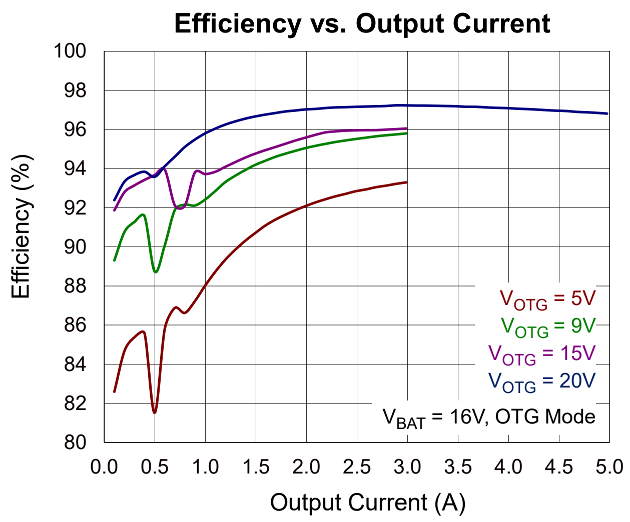












Note 8. Sense resister loss is not included in efficiency data.

15 Operation

15.1 Overview

The RT9478 is an NVDC battery charger, and the typical application circuit is shown in 13 Typical Application Circuit. The device has 9 operation modes: Low Power Mode, Performance Mode, Active VBUS Mode, Charging Mode, Supplement Mode, OTG Mode, VAP Mode, HiZ Mode, and Learn Mode. Mode transitions are shown in Figure 1.

15.1.1 Low Power Mode

In low power mode, the system is powered only by the battery, and EN_LPWR (0x12[15] = 1). All functions, except for SMBus communication, are disabled to obtain a minimum quiescent current (18μA, typical). If low power PROCHOT is enabled by setting the EN_PROCHOT_LPWR (0x30[14]) register bit to 1, PROCHOT can be asserted by an independent comparator output status with a typical quiescent current of 24μA.

15.1.2 Performance Mode

In performance mode, the system is powered by the battery. Current monitors and A/D converter can be enabled, but the buck-boost converter is disabled.

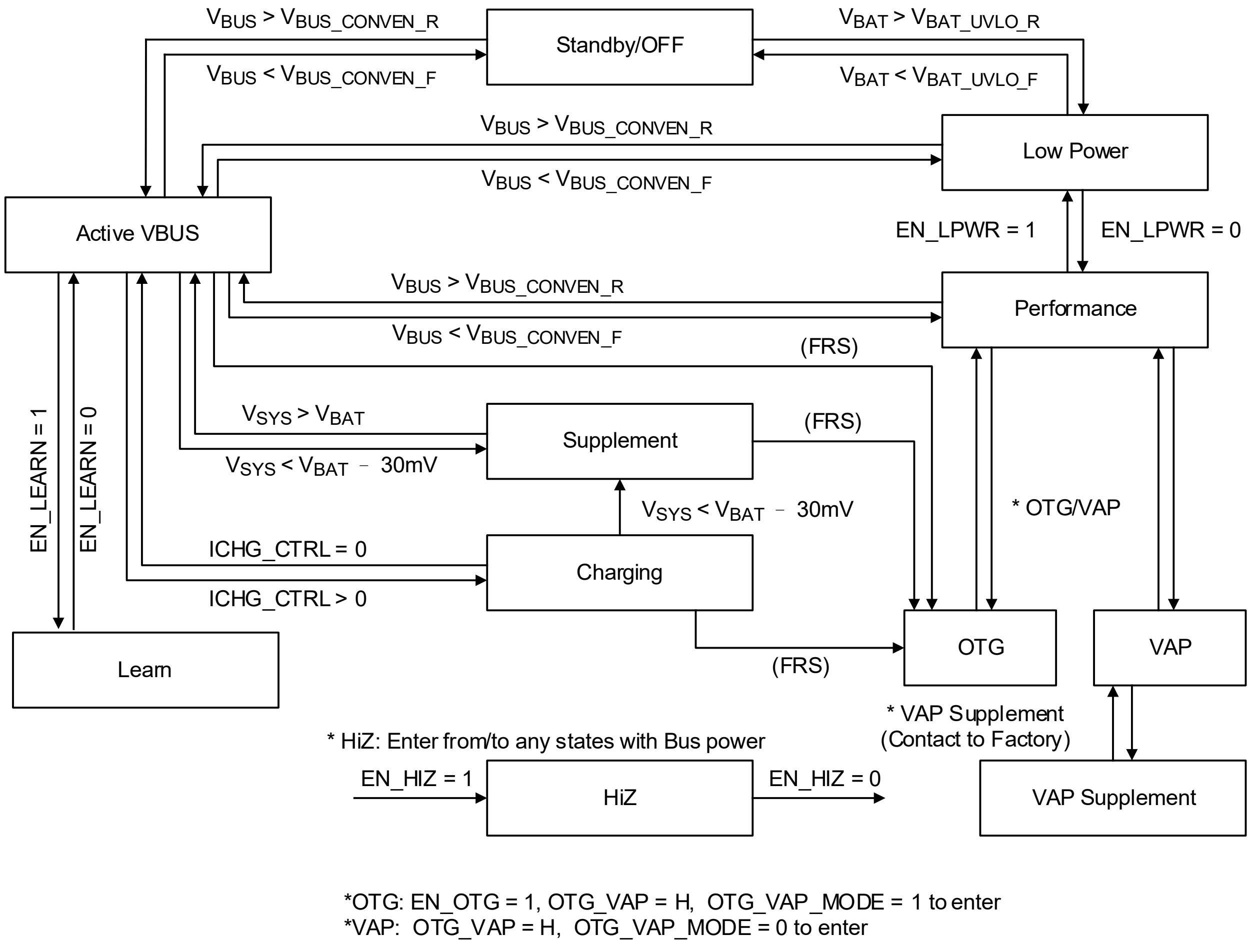


Figure 1. Operation State Diagram

15.1.3 Active VBUS Mode

When a valid power source is connected to VBUS, the buck-boost converter is enabled to regulate the system voltage. Refer to 15.3.3 System Voltage for details.

15.1.4 Charging Mode

In charging mode, the battery is charged using a CC-CV profile as shown in Figure 3. The battery charge current is set by the ICHG_CTRL (0x14[12:6]) register, while the battery regulation voltage is configured by the VBAT_REG (0x15[14:3]) register. If the battery voltage drops below the threshold set by the VSYS_MIN (0x3E[15:8]) register, the device operates in pre-charge mode. Refer to 15.4 Charging Battery for details.

15.1.5 Supplement Mode

When the system load is high and the bus power supply input current is insufficient, the system will activate MIVR (Minimum Input Voltage Regulation) or AICR (Average Input Current Regulation). If the VSYS drops below the battery voltage (CSON voltage), the charger immediately enters supplement mode. In this mode, both the buck-boost converter and the battery supply power to the system to meet the system load requirements.

15.1.6 OTG Mode

In OTG (USB On-The-Go) mode, power is supplied to the bus side from the battery. Refer to 15.8 OTG Mode (USB On-The-Go) for details.

15.1.7 Vmin Active Protection (VAP) Mode

In VAP (Vmin Active Protection) mode, battery power is charged into the input (bus-side) capacitor. During a system peak power spike, the bus-side capacitors can supplement the system to prevent the system voltage from dropping below a specific value. Refer to 15.9 Vmin Active Protection (VAP) for details.

15.1.8 HiZ Mode

In HiZ mode, the buck-boost converter is disabled, the A/D converter is disabled, but the REGN supply remains enabled. This mode can be transitioned to from any other VBUS mode by pulling down the ILIM_HIZ pin or setting the EN_HIZ (0x32[15]) register bit to 1. To exit HiZ mode and return to the previous mode, set the ILIM_HIZ pin to high and set the EN_HIZ register bit to 0. Refer to 15.10 HiZ Mode for details.

15.1.9 Learn Mode

In learn mode, the buck-boost converter is disabled, and the battery MOSFET is turned on. To enter learn mode, set the EN_LEARN (0x12[5]) register bit to 1. To exit, set the EN_LEARN register bit to 0 or pull down the CELL_BATPRES pin. This mode is used by the system to calibrate the battery gas gauge throughout a full discharge/charge cycle. Refer to 15.1.9 Learn Mode for details.

15.2 Power-Up Sequence

The RT9478 powers up from either the bus input voltage (VBUS) or the battery voltage (VBAT) on the CSON pin. The device powers up when VBUS exceeds VBUS_UVLO_R due to a power source being plugged in or when VBAT exceeds VBAT_UVLO_R due to battery connection. The host can access user registers within a maximum of 10ms after either VBUS or VBAT becomes valid.

15.2.1 Powered-Up from Bus Input

- When VBUS exceeds VBUS_UVLO_R with a 2ms deglitch time, the device becomes ready for SMBus communication.
- Once VBUS exceeds VBUS_CONVEN_R with a 45ms deglitch time, the REGN LDO is enabled and supplies power to the VDDA pin. The CHG_OK goes HIGH, and the VBUS_PG (0x20[15]) register is set to 1.
- The following functions and registers will be activated after powering up from VBUS:
- The battery cell count is detected at the CELL_BATPRES pin.
- The inductance in use is detected at the IBUS pin.
- The MIVR threshold is set by the no-load VBUS voltage.
- The AICR threshold is detected at the ILIM_HIZ pin voltage.
- The VBAT_REG (0x15[14:3]) register, VSYS_MIN (0x3E) register, and SYSOV threshold are loaded according to the cell count.
- Eventually, the device enters active VBUS mode, and the converter starts switching.

15.2.2 Powered-Up from Battery

- When the voltage at the CSON pin exceeds VBAT_UVLO_R, the device enters low power mode, and the BATFET is turned on.
- When the EN_LPWR (0x12[15]) register is set to 0, the device enters performance mode and the REGN LDO is enabled and supplies power to the VDDA pin. The battery cell count is detected at the CELL_BATPRES pin.

15.2.3 Battery Cell Count, SYSOVP Threshold, and VSYS_MIN Value

At power-up, the cell count is determined by the voltage at the CELL_BATPRES pin. The CELL_BATPRES pin is biased with a resistive ladder from VDDA to GND. The initial system minimum voltage (VSYS_MIN) and charge voltage (VBAT_REG) are loaded into the VSYS_MIN (0x3E[15:8]) register and the VBAT_REG (0x15[14:3]) register, respectively, and the system overvoltage protection (SYSOVP) threshold is set as shown in Table 2.

Table 2

CELL_BATPRES Pin Voltage (% of the VDDA Pin)	CELL COUNT	VBAT_REG (0x15[14:3])	SYSOVP Threshold (0x40[14:12] = 000b)	VSYS_MIN (0x3E[15:8])
68.4% - 81.5%	4s	16.8V	19.5V	12.3V
51.7% - 65.0%	3s	12.6V	19.5V	9.2V
18.4% - 48.5%	2s	8.4V	12V	6.6V
0% - 15%	Battery Removal	8.4V	25V	6.6V

The VBAT_REG and VSYS_MIN registers can be overwritten by the user. The SYSOVP threshold can be selected from 15V to 24V by setting the VSYS_OVP (0x40[14:12]) register.

15.2.4 Initial Minimum Input Voltage Regulation Voltage

At VBUS power-up, the initial Minimum Input Voltage Regulation (MIVR) value is set to VBUS – 1.28V and stored in the VMIVR (0x3D[13:6]) register. Refer to 15.5.1 Minimum Input Voltage Regulation (MIVR) for details.

15.2.5 Initial Average Input Current Limit

At VBUS power-up, the initial Average Input Current Regulation (AICR) value is set by the lower one of the AICR value set by the ILIM_HIZ pin voltage and the AICR_HOST (0x3F[14:8]) register. Refer to 15.5.2 Average Input Current Regulation (AICR) for details.

15.2.6 Inductance Detection

At VBUS power-up, the inductance value is set by the voltage at the IBUS pin. Appropriate inductance value needs to be provided to the charger for stable buck-boost converter operation. The required resistors for 1μH, 2.2μH, and 3.3μH inductances are 90.9kΩ, 137kΩ, and 169kΩ, respectively. A ±2% or better tolerance of the resistor is required for accurate inductance detection. The switching frequency must be chosen appropriately for the inductor.

If an additional sensing circuit is connected to the IBUS pin, it should have a high input impedance for 13ms after REGN startup to ensure accurate resistance detection and eliminate any disturbance.

Table 3 presents the recommended combinations of inductor value and frequency; other combinations are not recommended.

Table 3

Inductor in Use	Resistor on the IBUS Pin
1μH (for 1200kHz)	90.9kΩ
1.5μH (for 800kHz)	121kΩ
2.2μH (for 800kHz or 720kHz)	137kΩ or 140kΩ
3.3μH (for 800kHz or 720kHz)	169kΩ

15.3 Configuration

15.3.1 Switching Frequency and Compensation

The switching frequency is selected from 800kHz, 1200kHz or 720kHz by the PWM_FREQ (0x12[9]) register bit and PWM_LOWFREQ (0x40[10]). The device requires an appropriate external RC combination on the COMP1 pin and the COMP2 pin. The recommended value combinations are shown in Table 4.

Table 4

SW Frequency	Inductor	R_{COMP1}	C_{COMP1}	C_{COMP1P}	R_{COMP2}	C_{COMP2}	C_{COMP2P}
720kHz	3.3μH	16.9kΩ	3300pF	33pF	15kΩ	1200pF	15pF
720kHz	2.2μH	16.9kΩ	3300pF	33pF	10kΩ	1200pF	15pF
800kHz	3.3μH	16.9kΩ	3300pF	33pF	15kΩ	1200pF	15pF
800kHz	2.2μH	16.9kΩ	3300pF	33pF	10kΩ	1200pF	15pF
800kHz	1.5μH	16.9kΩ	3300pF	33pF	6.8kΩ	1200pF	15pF
1200kHz	1.0μH	16.9kΩ	3300pF	33pF	5kΩ	1200pF	15pF

15.3.2 Current Sense Resister

Two sense resistors are needed to detect input current and battery current. The input current sense resistor, R_{SENSE_IN} should be placed between the CSIP and CSIN pins. The battery current sense resistor, R_{SENSE_BAT}, should be placed between the CSOP and CSON pins. These resistors must be 10mΩ or 5mΩ. For proper operation, the sense resistor value must be set in the registers. The RSNS_IN (0x30[11]) register bit sets R_{SENSE_IN}, and the RSNS_BAT (0x30[10]) register bit sets R_{SENSE_BAT}.

15.3.3 System Voltage Setting

In active VBUS mode, the device controls VSYS depending on the V_{BAT} and the V_{SYS_MIN}. The V_{BAT} is detected at the CSON pin, and the V_{SYS_MIN} is set by the VSYS_MIN (0x3E) register.

If the battery voltage is lower than V_{SYS_MIN}, the target voltage is V_{SYS_MIN}. Once the battery voltage increases higher than V_{SYS_MIN}, the target voltage is changed to 150mV higher than V_{BAT}. Refer to Figure 2 for the relationship between V_{BAT} and V_{SYS} when VSYS_MIN is set to 6.6V.

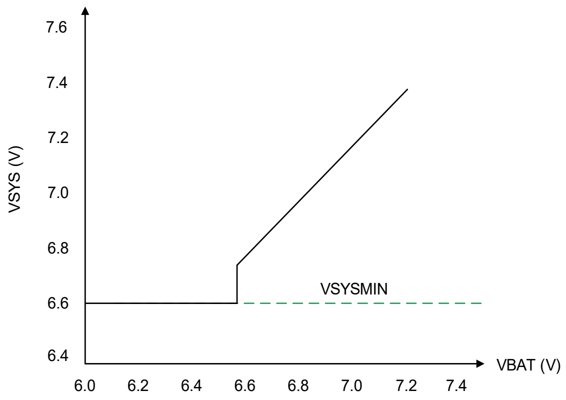


Figure 2. System Voltage and Battery Voltage Relationship in Active VBUS Mode

15.4 Charging Battery

15.4.1 Charging Start

When V_{BUS} is valid, the battery charge starts by writing a non-zero value to the ICHG_CTRL (0x14[12:6]) register. This register is 7-bit with an LSB of 64mA when R_{SENSE_BAT} is 10mΩ, and 128mA when R_{SENSE_BAT} is 5mΩ.

15.4.2 Charging Stop

The ICHG_CTRL is reset to 0 and battery charge stops in the following cases:

- Write 0 to the ICHG_CTRL (0x14[12:6]) register.
- Write 0 to the VBAT_REG (0x15[14:3]) register.
- Set the RESET_REG (0x32[14]) register bit to 1.
- The CELL_BATPRES pin is pulled low.
- VBUS is lower than $V_{BUS\_CONVEN\_F}$ (adapter removal).
- The watchdog timer (WDT) expires. Refer to 15.4.4 Watchdog Timer (WDT).

Note that once the VBAT_REG (0x15[11:0]) is written to 0, the VBAT_REG keeps its value and the ICHG_CTRL is set to 0.

In the following cases, the battery charge temporarily stops but the ICHG_CTRL keeps its value.

- The CHG_OK is low. Refer to 15.4.3 CHG_OK Indicator and Charge Condition for details.
- The CHG_INHIBIT (0x12[0]) register bit is written to be 1.
- Entering supplement mode.
- Entering learn mode by setting the EN_LEARN (0x12[5]) register to 1.
- Entering HiZ mode by pulling down the ILIM_HIZ pin to low or setting the EN_HIZ (0x32[15]) register to 1.

If the above conditions are removed, the battery charge restarts.

15.4.3 CHG_OK Indicator and Charge Condition

When the following conditions are satisfied, the system is ready to charge and the CHG_OK pin is pulled high.

- Bus voltage is present: $V_{BUS\_CONVEN\_R}$ < VBUS < $V_{BUS\_OVP\_F}$
- None of the following fault events are asserted: FORCE_CONV_OFF_FLT, BUSOC1_FLT, BUSOVP_FLT, BATOCP_FLT, OTP_FLT, SYSOVP_FLT, or SYSUVP_FLT
- Battery voltage is less than $V_{BAT\_OVP\_F}$

Also, the CHG_OK pin goes high in OTG mode if the OTG_ON_CHGOK (0x12[11]) register is set to 1. Refer to 15.8 OTG Mode (USB On-The-Go) for details.

15.4.4 Watchdog Timer (WDT)

To protect the battery, the RT9478 has a watchdog timer (WDT). Battery charging is terminated if the WDT expires. To reset the WDT, the host must write to the ICHG_CTRL register (0x14[12:6]) or the VBAT_REG (0x15[14:3]) register via SMBus within a WDT period. The period is selectable from 5s (01), 88s (10), and 175s (11, default) by setting the WATCHDOG (0x12[14:13]) register. If 00 is set in the WATCHDOG register, the watchdog timer is disabled.

15.4.5 Charging Profile

As described in 15.1.4 Charging Mode, the RT9478 supports a CC-CV profile.

The battery charging current is set by the ICHG_CTRL (0x14[12:6]) register.

If the battery voltage (V_{CSON}) is below the VSYS_MIN (0x3E[15:8]) register, the device operates in pre-charge mode, and the maximum charging current is limited to 384mA.

If the battery voltage is between VSYS_MIN register and the VBAT_REG (0x15[14:3]), the device operates in fast-charge mode.

When EN_LDO (0x12[2]) bit is written to 0, the device operates in fast-charge mode even if the V_{CSON} is less than VSYS_MIN register.

Once the battery voltage reaches the VBAT_REG register setting, the device enters CV (constant voltage) mode and maintains the battery voltage at the VBAT_REG register setting. Figure 3 shows a conceptual charging profile.

In fast-charge and pre-charge modes, the IN_FCHG (0x20[10]) or IN_PCHG (0x20[9]) bit is set to 1, respectively.

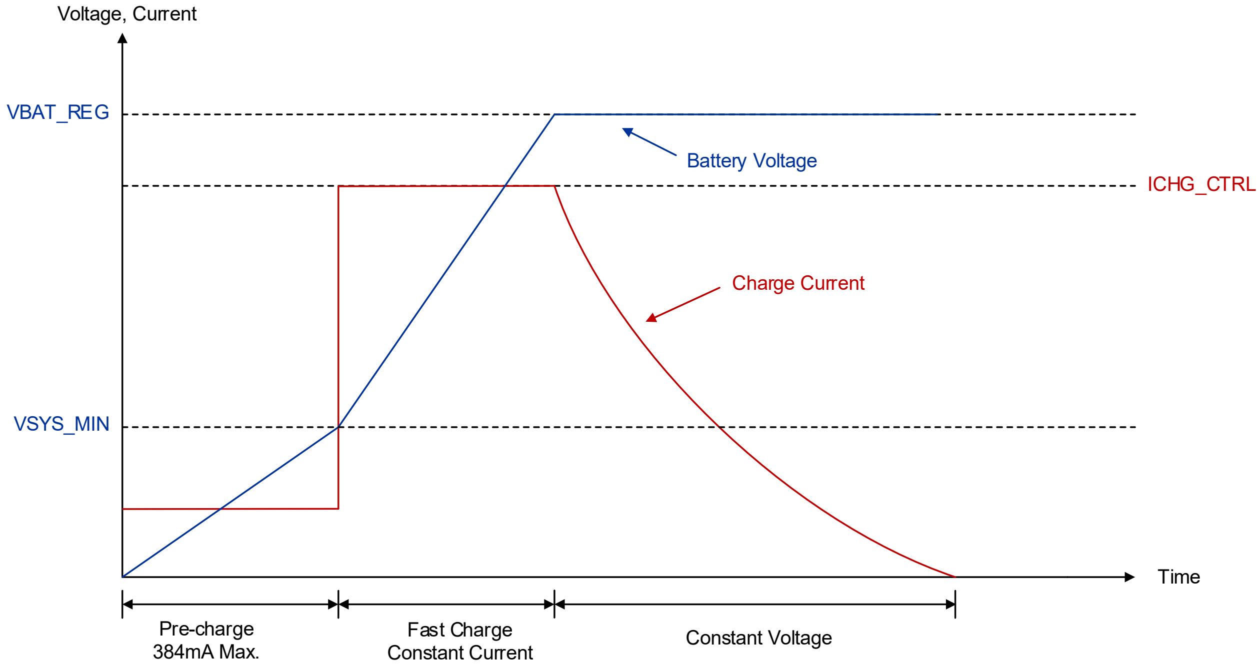


Figure 3. Charging Profile

15.5 Dynamic Power Management

The RT9478 offers two types of input current limit functions: Minimum Input Voltage Regulation (MIVR) and Average Input Current Regulation (AICR). AICR limits the input current to the specified level I_{AICR1}. The I_{AICR1} can be adjusted automatically by the Adaptive Input Current Control (AICC) function. Additionally, the peak power mode (two level AICR) function is available to periodically increase the AICR level to a higher value, I_{AICR2} to support peak system power.

15.5.1 Minimum Input Voltage Regulation (MIVR)

When the bus power supply is overloaded, the input bus voltage (V_{BUS}) is expected to drop due to the current limit function of the power supply. MIVR limits the input current to prevent the input voltage from dropping below the MIVR threshold.

When the V_{BUS} is connected, the MIVR threshold is set to V_{BUS} – 1.28V, and the threshold is stored in the VMIVR (0x3D[13:6]) register. However, the minimum setting of the MIVR threshold is limited to 3.904V by this automatic setting.

The host can adjust the MIVR threshold through the VMIVR register, ranging from 3.2V to 19.52V with an LSB of 64mV and a 3.2V offset. For example, if the host writes 10000 (0x20, or 16 in decimal) to the VMIVR, the threshold becomes 1.024V + 3.2V = 4.224V, instead of just 1.024V (64mV × 16 = 1024mV).

If the device is in MIVR, the IN_MIVR (0x20[12]) bit is set to 1.

15.5.2 Average Input Current Regulation (AICR)

AICR limits the input current to the value, I_{AICR1}. I_{AICR1} is defined in the IAICR (0x22[14:8]) register, but the host cannot write to the IAICR register directly. The IAICR register value and the I_{AICR1} are set in the following way, as shown in Figure 4:

- If the EN_EXT_ILIM (0x31[7]) register is set to 1 (default), the device sets lower of two values:
- AICR_HOST (0x3F[14:8]) register value.
- AICR value given by the ILIM_HIZ pin voltage

The relationship between AICR values and the ILIM_HIZ pin voltage is as follows.

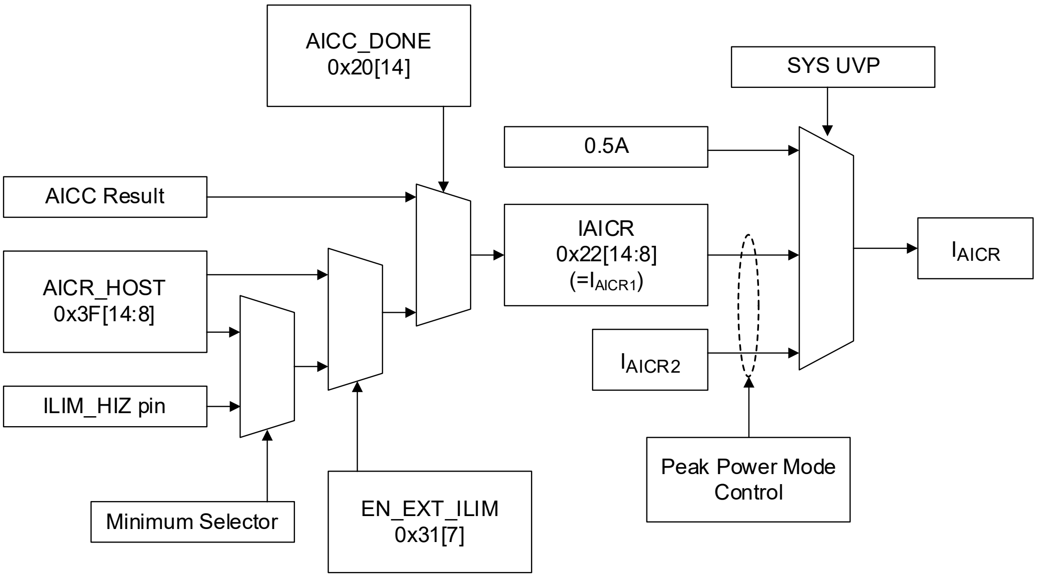


Figure 4. AICR Setting Selection Diagram

The I_{AICR1} is set by the ILIM_HIZ voltage:

$V_{ILIM\_HIZ} = 5/6 \times (1[V] + 40 \times I_{AICR1}[A] \times R_{SENSE\_IN})$

or,

$I_{AICR1} = (6/5 \times V_{ILIM\_HIZ} - 1[V]) / (40 \times R_{SENSE\_IN})$

For example, if the system needs to set the AICR value to 3.0A and R_{SENSE_IN} = 10mΩ,

$V_{ILIM\_HIZ}[V] = 5/6 \times (1[V] + 40 \times 3.0 \times 0.01) = 1.83[V]$

Therefore, 1.83V must be applied to the ILIM_HIZ pin externally.

Note that this ILIM_HIZ pin voltage is measured every time the V_{BUS} is connected.

- If the EN_EXT_ILIM register bit is set to 0, the charger reads the AICR_HOST (0x3F[14:8]) register and sets it to the IAICR register. If the system needs to set a specific AICR value, the EN_EXT_ILIM must be 0, and the host needs to write the desired value to the AICR_HOST register rather than to the IAICR register.
- The AICC result is prioritized over both the ILIM_HIZ pin and the AICR_HOST.
- If system under voltage protection (SYSUVP) is triggered, the AICR is temporarily clamped at 0.5A without modifying the IAICR register. The AICR is enabled during SYSUVP even when the EN_AICR (0x12[1]) is set to 0.
- If 0x00 (0mA) or 0x01 (50mA) is written to the AICR_HOST register and it is reflected in the IAICR register, I_{AICR1} is set to 100mA.

The AICR maximum value can be 6.3A, 6.35A or 10A. It depends on the inductance, input current sense resistor, and the EN_FAST_5MOHM (0x30[8]) register settings as shown in Table 5.

Table 5

Inductance	EN_FAST_5MOHM (0x30[8])	RSNS_IN (0x30[11])	Maximum I_{AICR}	Maximum IAICR (0x22[14:8])
1.0μH 1.5μH 2.2μH	X	0 (10mΩ)	6.35A	0x7F
	1	1 (5mΩ)	6.3A	0x3F
	0	1 (5mΩ)	10A	0x64
3.3μH	X	0 (10mΩ)	6.35A	0x7F
	X	1 (5mΩ)	10A	0x64

15.5.3 Adaptive Input Current Control (AICC)

If the end-user uses a nonstandard input power source, in some cases the AICR setting may be higher than the current limit of the input power source, causing the charger to operate in the MIVR loop. Therefore, the RT9478 offers a method to detect the input power source's current limit and the optimal input current limit level. This is called Adaptive Input Current Control (AICC).

AICC starts when the EN_AICC (0x32[11]) bit is set to 1 and the device is in MIVR (Minimum Input Voltage Regulation). During the AICC process, the internal AICR limit value is decreased until the bus input voltage recovers, and the input power source is no longer in MIVR operation. Once the optimal AICC threshold is found, the IAICR (0x22[14:8]) register is updated, and the AICC_DONE (0x20[14]) bit is asserted. Figure 5 shows the AICC operation.

Note that if the bus input is unplugged, the IAICR register value and EN_AICC are reset. If EN_AICC is reset to 0 during the AICC process, AICC is disabled.

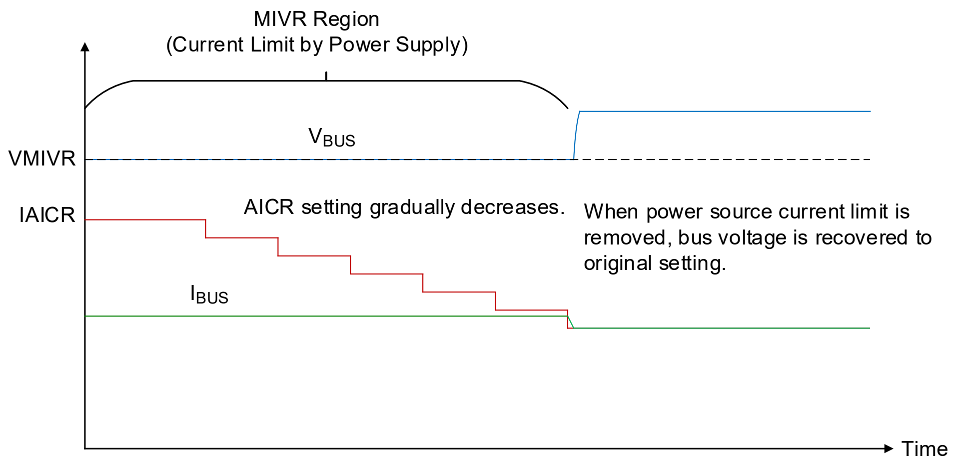


Figure 5. Adaptive Input Current Control (AICC) Operation

15.5.4 Peak Power Mode (Two Level AICR)

The peak power mode is designed to increase the input current limit for a short period to support peak system power.

Entry into peak power mode is detected under two conditions:

- I_{BUS} hits the IAICR (0x22[14:8]) register threshold, and the EN_PKPWR_AICR (0x31[13]) register bit is set to 1.
- V_{SYS} drops to 95% of the VSYS_MIN (0x3E[7:0]) register threshold, and the EN_PKPWR_VSYS (0x31[12]) register bit is set to 1.

When the peak power mode is triggered by I_{BUS} or V_{SYS}, the input current limit is temporarily changed to I_{AICR2} for a certain overloading period. The I_{AICR2} is set by the IAICR2 (0x33[15:11]) register, ranging between 110% and 450% of I_{AICR1}. The overloading period is selected from 1ms (default), 2ms, 5ms, or 10ms by the PKPWR_TOVLD_DEG (0x31[15:14]) register. After this overloading period (T_{OVLD}) elapses, the input current limit resumes to I_{AICR1} and operates in the relaxation period. The relaxation period (T_{RELAX}) is defined as the PKPWR_TMAX (0x31[9:8]) register setting minus the PKPWR_TOVLD_DEG (0x31[15:14]) register setting.

The cycle timer (T_{MAX}) of PKPWR_TMAX (0x31[9:8]) register can be selected from 20ms (default), 40ms, 80ms, and 1s. When the cycle time expires, the current limit is set to I_{AICR2} again and operates in a new cycle period.

During the overloading period, the PKPWR_OVLD_STAT (0x31[11]) register bit is set to 1. If overload is removed, the PKPWR_OVLD_STAT is set to 0. If PKPWR_OVLD_STAT is written to 0 during the overloading period, the device exits from the overloading state. During the relaxation period, the PKPWR_RELAX_STAT (0x31[10]) bit is set to 1 until the relaxation period expires. If PKPWR_RELAX_STAT is written to 0 during the relaxation period, the device exits from the relaxing state. Refer to Figure 6 for the operation of peak power mode.

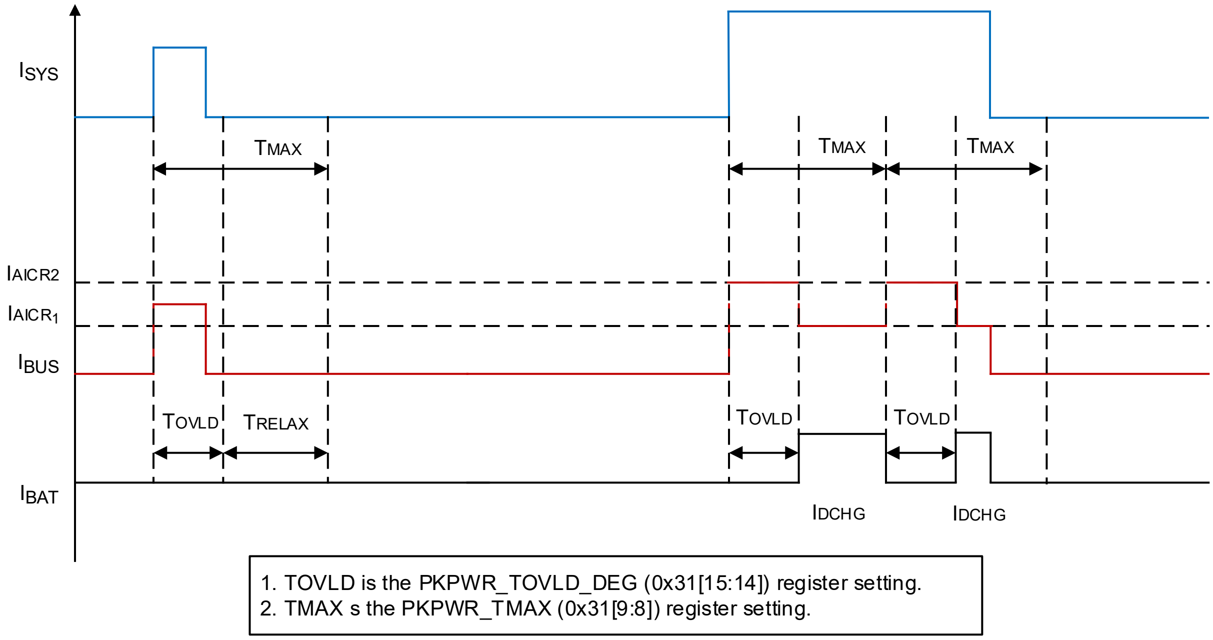


Figure 6. Peak Power Mode (Two Level Input Current Limit) Operation

15.6 Voltage, Current, and System Power Monitor

15.6.1 A/D Converter

The RT9478 features an 8-bit A/D converter for monitoring the following points: CMPIN pin, VBUS pin, PSYS pin, input current via the differential voltage of the CSIP and CSIN pins, VSYS pin, and battery voltage via the CSON pin. The battery discharge and charge current are measured via the differential voltage of the CSOP and CSON pins but are measured in 7-bit. A/D conversion begins when the ADC_START (0x35[14]) register is set to 1, and each channel conversion takes a maximum of 25ms.

If the ADC_CONV (0x35[15]) register is 0 (A/D conversion is one-shot) ADC_START resets to 0 after one set of conversions finishes.

If the ADC_CONV is 1, A/D conversion repeats at 1-second intervals, and the registers are continuously updated during this interval.

Desired conversion points must be enabled in the ADCOption (0x35) register. Each channel conversion result is stored in each dedicated register as shown in Table 6. The full-scale range for COMPIN and PSYS is selectable via the ADC_FULLSCALE (0x35[13]) register. The A/D converter is not activated in low power mode.

Table 6

Conversion Point	Enable Bit	Result Register	Unit (LSB)
CMPIN Pin	EN_ADC_VCOMP 0x35[7]	VCOMP 0x25[7:0]	8mV (ADC_FULLSCALE = 0) 12mV (ADC_FULLSCALE = 1)
VBUS Pin	EN_ADC_VBUS 0x35[6]	VBUS 0x23[15:8]	96mV
PSYS Pin	EN_ADC_PSYS 0x35[5]	PSYS 0x23[7:0]	8mV (ADC_FULLSCALE = 0) 12mV (ADC_FULLSCALE = 1)

Conversion Point	Enable Bit	Result Register	Unit (LSB)
CSIP − CSIN Pins Differential	EN_ADC_IBUS 0x35[4]	IBUS 0x25[15:8]	50mA (R_{SENSE_IN} = 10mΩ) 100mA (R_{SENSE_IN} = 5mΩ)
CSON − CSOP Pins Differential	EN_ADC_IBAT_DISCHG 0x35[3]	IBAT_DISCHG 0x24[6:0]	256mA (R_{SENSE_BAT} = 10mΩ) 512mA (R_{SENSE_BAT} = 5mΩ)
CSOP − CSON Pins Differential	EN_ADC_IBAT_ICHG 0x35[2]	IBAT_CHG 0x24[14:8]	64mA (R_{SENSE_BAT} = 10mΩ) 128mA (R_{SENSE_BAT} = 5mΩ)
VSYS Pin	EN_ADC_VSYS 0x35[1]	VSYS 0x26[15:8]	64mV Offset is 2.88V
CSON Pin	EN_ADC_VBAT 0x35[0]	VBAT 0x26[7:0]	64mV Offset is 2.88V

15.6.2 *IBUS and IBAT Pins Current Monitor*

The RT9478 has two current sense amplifiers to monitor input current during forward mode or output current during OTG mode via the IBUS pin, and battery charge/discharge current via the IBAT pin.

The IBUS pin voltage is 20x (default) or 40x of the differential voltage across the CSIP pin and CSIN pin, and the gain is selected by the IBUS_GAIN (0x12[4]) register. The IBAT pin voltage is 8x or 16x (default) the differential voltage across the CSOP pin and CSON pin, and the gain is selected by the IBAT_GAIN register bit (0x12[3]). The IBUS pin output is enabled during forward mode or OTG mode, and the IBAT pin output is enabled by the EN_IBAT_PIN (0x30[15]) register bit. If the ICHG_IDCHG_DIR (0x31[6]) register bit is set to 0 (default), the IBAT pin outputs the battery discharge current monitor. If the ICHG_IDCHG_DIR is set to 1, it outputs the battery charge current monitor. A maximum 100pF capacitor can be connected to the IBUS and IBAT pins for decoupling high-frequency noise.

The IBAT pin output is not enabled in low power mode even if the EN_IBAT_PIN register is set to 1.

15.6.3 *PSYS Pin System Power Monitor*

The PSYS pin provides a current output for real-time system power monitoring. The monitoring target can be selected using the PSYS_CONFIG (0x30[13:12]) and PSYS_OTG_IDCHG (0x32[1]) registers. Refer to Table 7 for detailed selection options. The output gain for the PSYS monitor can be configured to either 0.25μA/W or 1μA/W (default) via the PSYS_RATIO (0x30[9]) register. For accurate power monitoring, ensure that the RSNS_IN (0x30[11]) and RSNS_BAT (0x30[10]) registers are properly set to match the R_{SENSE_IN} and R_{SENSE_BAT} as described in 15.3.2 Current Sense Resister.

Table 7

PSYS_CONFIG (0x30[13:12])	PSYS_OTG_IDCHG (0x32[0])	PSYS Function in Forward Mode	PSYS Function in OTG Mode
00	0	PSYS = PBUS + PBAT	PSYS = PBAT - PBUS
00	1	PSYS = PBUS + PBAT	PSYS = PBAT
01	X	PSYS = PBUS	PSYS = 0
11	X	PSYS = 0 (Disabled)	PSYS = 0 (Disabled)
10 (Reserved)	X	PSYS = 0 (Reserved)	PSYS = 0 (Reserved)

The output voltage is clamped at 3.3V.

The PSYS power monitor is not activated in low power mode.

15.7 Independent Comparator

The RT9478 features a comparator with one input at the CMPIN pin and one output at the CMPOUT pin. The comparator's threshold voltage can be set to either 1.2V (default) or 2.3V using the CMP_REF (0x30[7]) register. The threshold is fixed at 1.2V in low power mode. This feature is enabled by setting the EN_CMP (0x32[2]) register bit to 1 (default).

Output polarity is determined by the CMP_POL (0x30[6]) register, where 0 represents CMPOUT is low when CMPIN is above the internal threshold (default) and 1 represents CMPOUT is low when CMPIN is below the internal threshold. The deglitch time for the comparator can be selected from 5μs, 2ms, 20ms, and 5s by the CMP_DEG (0x30[5:4]) register.

15.8 OTG Mode (USB On-The-Go)

15.8.1 OTG Mode

The RT9478 supports USB On-The-Go (OTG) functionality to deliver power from the battery to a USB-C port. In this mode, the buck-boost converter operates in reverse direction. The OTG output voltage is set by the VOTG_REG (0x3B[13:2]) register, and the current limit is set by the IOTG_REG (0x3C[14:8]) register. Both voltage and current settings must be greater than 0 to enable OTG functionality.

To enter OTG mode, the EN_LPWR (0x12[15]) must be set to 0. The device enters OTG mode 15ms after the OTG_VAP pin voltage is pulled high, the EN_OTG (0x32[12]) register is set to 1, and the OTG_VAP_MODE (0x32[5]) register is set to 1 (default). When the device enters OTG mode, the IN_OTG (0x20[8]) register bit is set to 1.

15.8.2 Fast Role Swap (FRS)

The USB-C PD specification includes a Fast Role Swap (FRS) feature, which enables a quick transition from the power sink role to the power source role. This ensures that power is provided to accessories on the bus input without a voltage drop when the original power source is disconnected. In accordance with the USB-C PD specification, the device is capable of providing 5V within 150μs after the bus voltage falls below 4.75V.

If the EN_FRS register (0x37[0]) is set to 1 and EN_LPWR (0x12[15]) is set to 0, the buck-boost converter operates regardless of whether the bus input voltage is present or not. The OTG_VAP_MODE (0x32[5]) register must be set to 1 (default), and the EN_OTG (0x32[12]) register will automatically be set when the EN_FRS register (0x37[0]) is set to 1. Do not set EN_FRS while OTG mode (when EN_OTG is already set to 1).

The EN_FRS will be reset to 0 if the EN_HIZ (0x32[15]) register is set to 1.

15.9 Vmin Active Protection (VAP)

In performance mode (0x12[15] = 0), system peak load may cause a battery voltage drop due to battery internal impedance, and the system voltage also drops. The Vmin Active Protection (VAP) feature supports this intermittent system voltage drop. In VAP mode, the buck-boost converter runs in reverse mode to charge the input bus bulk capacitor to store energy. Once the system voltage drops below the threshold, system voltage is supplied from the input side using stored energy.

15.10 HiZ Mode

The device enters HiZ mode if the ILIM_HIZ pin is driven low or the EN_HIZ (0x32[15]) register is set to 1 when the bus power is connected. In this mode, the buck-boost converter stops.

The device does not enter HiZ mode in battery-only operation, even in OTG or FRS.

The behavior of the battery MOSFET is controlled by the BATFETOFF_HIZ (0x32[1]) register. If BATFETOFF_HIZ is set to 1, the battery MOSFET is turned off in HiZ mode.

Setting the EN_HIZ register bit to 1 automatically resets the EN_FRS (0x37[0]) register to 0 (default).

15.11 Learn Mode

The device enters learn mode if the EN_LEARN (0x12[5]) register is set to 1 when the input bus voltage and battery voltage are present. In this mode, the buck-boost converter stops.

To exit learn mode, set EN_LEARN to 0 or pull the CELL_BATPRES pin low.

15.12 Force Converter Off Mode

The device enters force converter off mode when the EN_FORCE_CONV (0x30[3]) register is set to 1 and the CMPOUT pin is low. In this mode, the buck-boost converter stops, the FORCE_CONV_OFF_FLT (0x20[2]) register is set to 1, and the CHG_OK signal is driven low.

The FORCE_CONV_OFF_FLT is not cleared until the host reads it.

To exit force converter off mode, set EN_FORCE_CONV to 0. The device does not exit force converter off mode by unplugging the bus voltage.

15.13 Processor Hot (PROCHOT)

15.13.1 Processor Hot (PROCHOT) Overview

The RT9478 features a $\overline{\text{PROCHOT}}$ pin that notifies an overload of the load device, such as a CPU. Refer to Table 8 for monitoring events, enable bits, and status registers. Each monitor can be enabled individually.

Table 8

Monitor Event	Enable Register	Status Register
Input Current: Critical	PP_ICRIT (0x34[5])	ICRIT_PP_STAT (0x21[5])
Input Current: Nominal	PP_INOM (0x34[4])	INOM_PP_STAT (0x21[4])
Battery Discharge Current: Low (I_{DCHG1})	PP_IDCHG1 (0x34[3])	IDCHG1_PP_STAT (0x21[3])
Battery Discharge Current: High (I_{DCHG2})	PP_IDCHG2 (0x36[2])	IDCHG2_PP_STAT (0x36[1])
System Undervoltage	PP_VSYS (0x34[2])	VSYS_PP_STAT (0x21[2])
Input Bus Voltage (VAP mode)	PP_VBUS_VAP (0x36[9])	VBUS_VAP_PP_STAT (0x36[8])
VAP Exit	--	EXIT_VAP_PP_STAT (0x21[8])
Input Bus Power Removal	PP_VBUSOK (0x34[0])	VBUSOK_PP_STAT (0x21[0])
Battery Removal	PP_BATGONE (0x34[1])	BATGONE_PP_STAT (0x21[1])
Entering MIVR	PP_MIVR (0x34[7])	MIVR_PP_STAT (0x21[7])
Independent Comparator	PP_COMP (0x34[6]) EN_PROCHOT_LPWR (0x30[14])	COMP_PP_STAT (0x21[6])

All triggers are not active in low power mode, except for the low power independent comparator. VAP Exit is always enabled in VAP mode. If this PROCHOT is triggered, the $\overline{\text{PROCHOT}}$ pin generates a pulse with a minimum width, except in the case of PP_MIVR and EXIT_VAP. The minimum width can be selected from 100μs, 1ms, 5ms, and 10ms (default) by the PROCHOT_WIDTH (0x21[13:12]) register. If the EN_PROCHOT_EXT (0x21[14]) register is set to 1, the $\overline{\text{PROCHOT}}$ pin remains low until the host writes a 0 to the PROCHOT_CLR (0x21[11]) register.

Each status register bit is latched to 1 until the host reads it, except for PP_MIVR and EXIT_VAP. The host needs to write 0 to clear MIVR_PP_STAT and EXIT_VAP_PP_STAT.

15.13.2 Input Overcurrent PROCHOT (INOM, ICRIT)

When the input current exceeds the threshold, the $\overline{\text{PROCHOT}}$ pin is asserted. There are two thresholds: I_{NOM} and I_{CRIT}. This feature is enabled by the PP_INOM (0x34[4]) and PP_ICRIT (0x34[5]) register bits.

For I_{NOM} PROCHOT, the threshold is 110% of the I_{AICR1}, which is the IAICR (0x22[14:8]) register value. The deglitch time can be selected from 1ms (default) or 60ms by the INOM_DEG (0x33[1]) register.

For I_{CRIT} PROCHOT, the threshold is 110% of I_{AICR2}. I_{AICR2} is set between 110% and 450% of I_{AICR1} according to the IAICR2 (0x33[15:11]) register. The default is 150%. The deglitch time can be selected from 15μs, 100μs (default), 400μs, and 800μs by the ICRIT_DEG (0x33[10:9]) register.

The IAICR resister is not allowed to write by the host. Refer to 15.5.2 Average Input Current Regulation (AICR) for I_{AICR1} setting.

15.13.3 Battery Discharge Current PROCHOT (IDCHG1, IDCHG2)

When the battery discharge current exceeds the threshold, the $\overline{\text{PROCHOT}}$ pin is asserted. There are two thresholds: I_{DCHG1} and I_{DCHG2}. This feature is enabled by the PP_IDCHG1 (0x34[3]) or PP_IDCHG2 (0x36[2]) register bit and is not enabled in low power mode.

I_{DCHG1} is set from 0A to 32.256A in 512mA steps by the IDCHG_TH1 (0x34[15:10]) register. The deglitch time can be selected from 78ms, 1.25s (default), 5s, and 20s by the IDCHG_DEG1 (0x34[9:8]) register.

I_{DCHG2} is set from 125% to 400% of I_{DCHG1} by the IDCHG_TH2 (0x36[5:3]) register. The deglitch time can be selected from 100μs, 1.6ms (default), 6ms, and 12ms by the IDCHG_DEG2 (0x36[7:6]) register.

15.13.4 System Undervoltage PROCHOT (VSYS)

When the V_{SYS} drops below the threshold, the $\overline{\text{PROCHOT}}$ pin is asserted. The threshold is set by the VSYS_TH2 (0x37[7:2]) register. This feature is enabled by the PP_VSYS (0x34[2]) register.

If the EN_VSYSTH2_FOLLOW_VSYSTH1 (0x37[1]) register is set to 1, the VSYS_TH1 (0x33[7:2]) register determines the VSYS_TH2 threshold.

15.13.5 Input Bus Undervoltage in VAP PROCHOT (VBUS_VAP)

In VAP mode, the $\overline{\text{PROCHOT}}$ pin is asserted when V_{BUS} drops below the threshold. This feature is enabled by the PP_VBUS_VAP (0x36[9] register bit.

The threshold is set by the VBUS_VAP_TH register (0x37[15:9]).

15.13.6 Exit VAP PROCHOT (EXIT_VAP)

When the charger exits from VAP mode, the $\overline{\text{PROCHOT}}$ pin is asserted. This feature has no enable register and is always enabled in VAP mode. The host needs to write 0 to clear the EXIT_VAP_PP_STAT (0x21[8]) register bit.

15.13.7 Input Power Source Removal PROCHOT (VBUSOK)

When the V_{BUS} voltage drops below the threshold, the $\overline{\text{PROCHOT}}$ pin is asserted. This feature is enabled by the PP_VBUSOK (0x34[0]) register bit.

The threshold is $V_{BUS\_CONVEN\_F}$ (3.5V typical)

15.13.8 Battery Removal (BATGONE)

When battery removal is detected, the $\overline{\text{PROCHOT}}$ pin is asserted. This feature is enabled by the PP_BATGONE (0x34[1]) register bit.

This occurs when the CELL_BATPRES pin voltage drops below the $V_{CELL\_BATPREZ\_F}$ threshold.

15.13.9 MIVR PROCHOT

When the device enters MIVR mode, the $\overline{\text{PROCHOT}}$ pin is asserted. This feature is enabled by the PP_MIVR (0x34[7]) register bit.

The MIVR PROCHOT bus voltage threshold can be selected. If the LOWER_PROCHOT_MIVR (0x33[0]) register bit is set to 1 (default), the threshold can be selected from 83% or 91% of the MIVR threshold using the PROCHOT_MIVR_80_90 (0x33[8]) register bit and its minimum value is $V_{BUS\_CONVEN\_F}$. The host needs to write 0 to clear the MIVR_PP_STAT (0x21[7]) register bit.

15.13.10 Comparator Output PROCHOT

When the CMPUOT goes low, the $\overline{\text{PROCHOT}}$ pin is asserted.

This feature is enabled by the PP_COMP (0x34[6]) register bit, except in low power mode with EN_LPWR (0x12[15]) =1.

In low power mode, this feature is enabled by setting the EN_PROCHOT_LPWR (0x30[14]) register bit to 1 with EN_LPWR (0x12[15]) =1.

For comparator configuration, refer to 15.7 Independent Comparator.

15.14 Protection

15.14.1 Bus Overvoltage Protection (BUSOVP)

When the V_{BUS} exceeds $V_{BUS\_OVP\_R}$ (typically 26.8V) with a 100μs deglitch time, overvoltage protection (BUSOVP) is triggered. In BUSOVP, the buck-boost converter stops, the BUSOVP_FLT (0x20[7]) register bit is asserted, and the CHG_OK pin is pulled down.

Once the bus voltage drops below $V_{BUS\_OVP\_F}$ (typically 25.8V) with a 1ms deglitch time, the buck-boost converter resumes, and the CHG_OK pin is asserted again. The BUSOVP_FLT bit is cleared when the host reads it.

15.14.2 Battery Discharge Overcurrent Protection (BATOCP)

When the I_{BAT} discharge exceeds the threshold, the battery discharge overcurrent protection (BATOCP) is triggered. This feature is enabled by the EN_BATOC (0x31[1]) register bit.

The threshold is either 133% or 200% of I_{DCHG2}, according to the BATOC_VTH (0x31[0]) register bit. I_{DCHG2} is set from 125% to 400% of I_{DCHG1} by the IDCHG_TH2 register (0x36[5:3]). The I_{DCHG1} is set from 0A to 32.256A in 512mA increments by the IDCHG_TH1 (0x34[15:10]) register.

For example, if the IDCHG_TH1 register is set to 0x10 (16 in decimal), I_{DCHG1} is set to 8.192A. If the IDCHG_TH2 register is set to 0x01 (001), which indicates 150%, I_{DCHG2} becomes 8.192 × 150% = 12.288A. Under this setting, if BATOC_VTH is set to 1, which indicates 200%, the bus battery discharge overcurrent threshold is 12.288 × 200% = 24.576A.

The battery discharge overcurrent detection has a 250μs deglitch time.

In the case where R_{SENSE_BAT} is 10mΩ, the BATOCP threshold should not exceed 40A. In the case where R_{SENSE_BAT} is 5mΩ, the BATOCP threshold should not exceed 80A.

If BATOCP is triggered, the BATOCP_FLT (0x20[6]) register bit is asserted, and the buck-boost converter stops.

Once the battery discharge current drops below the threshold with a 250ms deglitch time, the buck-boost converter restarts, but the BATOCP_FLT bit is cleared when the host reads it.

15.14.3 Battery Overvoltage Protection (BATOVP)

When the CSON pin voltage exceeds $V_{BAT\_OVP\_R}$, battery overvoltage protection (BATOVP) is triggered. The threshold is 104% of the VBAT_REG (0x15[14:3]) registers value. If BATOVP is triggered in charging mode, the buck-boost converter stops but the ICHG_CTRL (0x14[12:6]) register remains unchanged. If BATOVP is triggered not in charging mode, the buck-boost converter does not stop. In either case, a 40mA discharge current, $I_{DISCHG\_BAT\_OVP}$, is drawn from the VSYS pin.

Once the CSON pin voltage drops below the threshold, the converter resumes. This falling threshold is 102% of the VBAT_REG register value.

This protection does not have an indicator register bit.

15.14.4 Bus Overcurrent Protection (BUS_OCP1)

When the I_{BUS} exceeds the first threshold, BUS_OCP1 is triggered. This feature is enabled only if the EN_IBUS_OCP1 (0x31[3]) register bit is set to 1. The first threshold is selected as either 133% or 200% of I_{AICR2} , according to the IBUS_OCP1_TH (0x31[2]). I_{AICR2} is set between 110% and 450% of I_{AICR1} according to the IAICR2 (0x33[15:11]) register, with the default being 150%. I_{AICR1} is defined by the IAICR (0x22[14:8]) register value.

For example, if the IAICR register is set to 0x3C (60 in decimal) and R_{SENSE_IN} is 10 mΩ, I_{AICR1} is set to 3.0A. If the IAICR2 register is set to 0x09 (01001), which indicates 150%, I_{AICR2} becomes 3.0 × 150% = 4.5A. Under this setting, if IBUS_OCP1_TH is set to 1, which indicates 200%, the bus overcurrent first threshold is 4.5 × 200% = 9.0A.

If BUS_OCP1 is triggered, the converter stops after a 250μs deglitch time and the BATOCP_FLT (0x20[6]) register bit is asserted. Once the overcurrent is resolved, the converter resumes switching automatically after a 250ms deglitch time.

15.14.5 Critical Bus Overcurrent Protection (BUS_OCP2)

When the I_{BUS} exceeds the second threshold, BUS_OCP2 is triggered. The threshold depends on the IBUS_OCP2_TH register (0x31[4]) bit, the RSNS_IN (0x30[11]) register, the system voltage and the battery voltage status. Refer to Table 9 for the threshold of CSIP – CSIN voltage. If BUS_OCP2 is triggered, the converter stops immediately.

Once the input current drops below the threshold, the converter resumes switching automatically after a 16ms deglitch time. If a system undervoltage occurs (V_{SYS} < $V_{SYS\_UVLO\_R}$ or V_{CSON} < $V_{BAT\_UVLO\_R}$) simultaneously, the limit is reduced.

Table 9. IBUS_OCP2 Threshold

IBUS_OCP2_TH (0x31[4])	RSNS_IN (0x30[11])	V_{SYS} < $V_{SYS\_UVLO\_R}$ or V_{CSON} < $V_{BAT\_UVLO\_R}$	CSIP – CSIN Differential Voltage
0	0 (10mΩ)	No	280mV
0	1 (5mΩ)	No	200mV
1	0 (10mΩ)	No	150mV
1	1 (5mΩ)	No	100mV
0	X	Yes	150mV
1	X	Yes	90mV

15.14.6 MOSFET Overcurrent Protection (Q2_OCP)

When Q2 is turned on and the V_{DS} of Q2 voltage exceeds the threshold, Q2_OCP is triggered. The threshold is selected from 210mV or 150mV (default) by the Q2_OCP (0x31[5]) register bit. In the case of system voltage or battery undervoltage, where V_{SYS} < $V_{SYS\_UVLO\_R}$ or V_{CSON} < $V_{BAT\_UVLO\_R}$, this threshold is reduced to 60mV or 45mV, respectively.

15.14.7 Inductor Average Overcurrent Protection (IL_AVG)

When the inductor average current exceeds the threshold, Inductor Average Overcurrent (IL_AVG) is triggered and the inductor average current is clamped. The threshold is selected from 6A, 10A,15A (default) or disabled by the IL_AVG (0x32[4:3]) register.

15.14.8 System Overvoltage Protection (SYSOVP)

If the V_{SYS} exceeds the threshold, system overvoltage protection (SYSOVP) is triggered. The threshold is selected by the VSYS_OVP (0x40[14:12]) register. By default, the threshold depends on the cell battery count. Refer to Table 10 for overvoltage thresholds.

Table 10. System Overvoltage Threshold

VSYS_OVP (0x40[14:12])	Cell Count	System Overvoltage Threshold
000 (default)	2s	12V
	3s, 4s	19.5V
	Battery Removal	25V
001	X	15V
010		16V
011		20V
100		21V
101		22V
110		23V
111		24V

If SYSOV is triggered, the buck-boost converter stops, the SYSOVP_FLT (0x20[4]) register bit is asserted, and a 40mA current, $I_{DISCHG\_SYS\_OVP}$, is pulled from the VSYS pin. Once the V_{SYS} drops below the threshold and SYSOVP_FLT is cleared by the host, the buck-boost converter resumes.

15.14.9 System Undervoltage Protection (SYSUVP)

If the V_{SYS} goes below the threshold, system undervoltage protection (SYSUVP) is triggered. This feature can be enabled by setting the ENZ_VSYS_UVP (0x12[6]) register to 0 (default).

The threshold is selected from 3.65V (default) to 8.0V by the VSYS_UVP (0x36[15:3]) register. SYSUVP detection has a 10μs deglitch time. If SYSUVP is triggered.

The behavior of the buck-boost converter depends on the VSYS_UVP_NO_HICCUP (0x36[10]) register setting.

If VSYS_UVP_NO_HICCUP is set to 1, the buck-boost converter is latched off after SYSUVP is detected and the SYSUVP_FLT (0x20[3]) register bit is asserted.

If VSYS_UVP_NO_HICCUP is set to 0, the buck-boost converter stops for 500ms and then tries to restart for 10ms. If V_{SYS} does not exceed the threshold during the trial, the buck-boost converter stops for 500ms again. If this restart trial occurs seven times in 90 seconds, the buck-boost converter is latched off and the SYSUVP_FLT register bit is asserted. During SYSUVP hiccup, AICR is always enabled regardless of the EN_AICR setting. The IAICR value is temporarily set to 0.5A.

Once the SYSUVP is cleared by the host, the buck-boost converter resumes.

15.14.10 OTG Output Overvoltage Protection (OTGOVP)

If the V_{OTG} voltage exceeds the threshold in OTG mode, OTG output overvoltage protection (OTGOVP) is triggered with a 10ms deglitch time. The threshold is 110% of the VOTG_REG (0x3B[13:2]) register setting. If OTGOVP is triggered, the buck-boost converter stops, the OTGOVP_FLT (0x20[1]) register bit is asserted, the EN_OTG (0x32[12]) register is cleared to 0, and the device exits from OTG mode. The OTGOVP_FLT is cleared when the host reads it.

15.14.11 OTG Output Undervoltage Protection (OTGUVP)

If the V_{OTG} voltage drops below the threshold in OTG mode, OTG output undervoltage protection (OTGUVP) is triggered with a 7ms deglitch time. The threshold is 85% of the VOTG_REG (0x3B[13:2]) register setting. If OTGUVP is triggered, the buck-boost converter stops, the OTGUVP_FLT (0x20[0]) register bit is asserted, and the EN_OTG (0x32[12]) register is cleared to 0, and the device exits from OTG mode. The OTGUVP_FLT is cleared when the host reads it.

15.14.12 Over-Temperature Protection (OTP)

If the junction temperature of the device exceeds 140°C, the over-temperature protection (OTP) is triggered. If OTP is triggered, the buck-boost converter stops and the OTP_FLT (0x21[10]) register bit is asserted. During OTP, the REGN LDO current limit is reduced to 24mA, and the battery MOSFET remains on. Once the temperature decreases below 125°C, the buck-boost converter and REGN LDO current limit resume.

15.14.13 Regulator Undervoltage Protection (REGNUVP)

If the REGN voltage falls below the threshold, regulator undervoltage protection (REGNUVP) is triggered. If REGNUVP is triggered, the buck-boost converter stops, and the A/D converter, current monitors, and power monitor are disabled. Once the REGN and VDDA voltage exceeds the threshold, these functions resume.

15.15 Other Features

15.15.1 Frequency Dithering

The RT9478 has a frequency dithering function to improve EMI performance. This feature is enabled by the DITHER_EN (0x36[12:11]) register bit. The dithering range is selectable from disable (00), ±2% (01), ±4% (10), or ±6% (11) of the center frequency.

15.15.2 Strong Gate Drive

The RT9478 has a two-step gate drive capability for the high-side MOSFET driver. By setting the DIS_STRGDRV register (0x12[8]) to 0, strong gate drive is enabled.

15.15.3 Out of Audio Operation (OOA)

Under light-load conditions, the charger operates in pulse frequency modulation (PFM) mode to improve efficiency. In PFM mode, the effective switching frequency decreases as the system load reduces. If the EN_OOA (0x12[10]) register is set to 1, the device operates in out-of-audio mode, and the minimum PFM frequency is limited to 25kHz to prevent audible noise.

15.15.4 Resetting Registers

If the RESET_REG (0x32[14]) register is set to 1, all register values are reset to their default values except for the VMIVR (0x3D[13:6]). The VBAT_REG (0x15[14:3]) and the VSYS_MIN (0x3E[15:8]) revert to default values based on the CELL_BATPRES pin status.

15.15.5 Auto Wakeup

If EN_AUTO_WAKEUP (0x30[0]) is set to 1 and V_{BAT} is lower than the VSYS_MIN (0x3E[15:8]) setting value, the device charges the battery for 30mins with a 128mA charging current.

This automatic charging stops and EN_AUTO_WAKEUP resets to 0 in following cases:

- When the VBAT exceeds the VSYS_MIN setting value.
- The host writes a new charge current value higher than 0 to the ICHG_CTRL (0x14[12:6]).

If the host writes charge current value, the device goes to pre-charge operation.

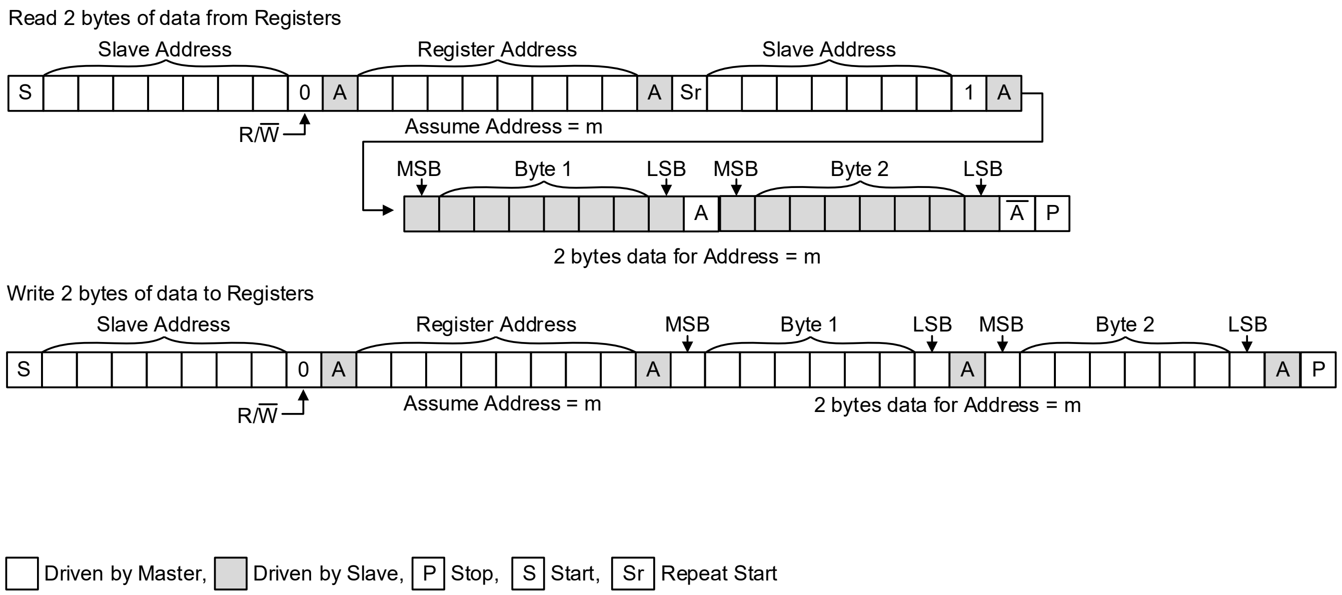
Note that the WDTMR_ADJ (0x12[14:13]) register must be set to 0 to disable watchdog timer.

15.15.6 Discharge for Shipping Mode

If EN_SHIP_DCHG (0x30[1]) is set to 1, current is sunk from each CSOP pin and CSON pin. Each pin sinks 10mA. This discharge continues for 140ms. When 140ms expire, the discharge stops and EN_SHIP_DCHG automatically resets to 0.

15.16 SMBus Communication Interface

The RT9478 uses an SMBus-compatible interface by a 2-wire line (SCL and SDA) to communicate with the host. The SCL and SDA pins are open drain, which need to be connected to the supply voltage via pull-up resistors. The device operates as an SMBus slave device with a 7-bit address of 0x09 for option code A and 0x6B for option code B, supporting up to 400kHz. To start an SMBus communication, begin with the START (S) condition, and then the host sends the slave address. This address is 7-bit long, followed by an eighth bit which is a data direction bit (RW). The second byte is the register address. Following bytes contain data for the selected register. End with the STOP (P) condition.



16 Application Information

(Note 9)

16.1 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-32L 4x4 package, the thermal resistance, θ_{JA}, is 35.43°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C − 25°C) / (35.43°C/W) = 2.82W for a WQFN-32L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 7 allows the user to see the effect of rising ambient temperature on the maximum power dissipation.

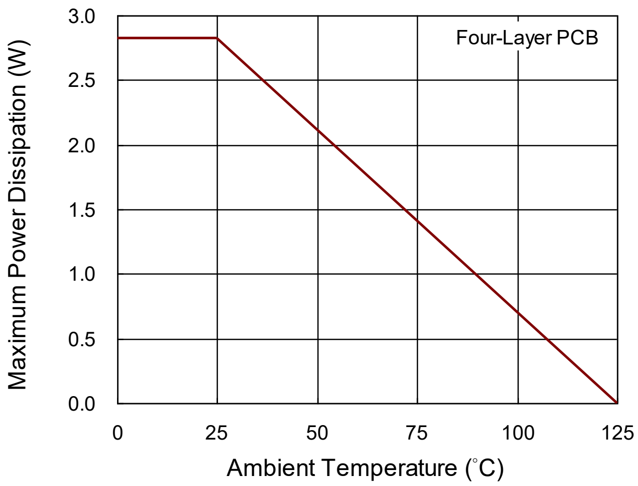


Figure 7. Derating Curve of Maximum Power Dissipation

16.2 Register to be Reset by Input Power is Unplugged

Register bits shown in Table 11 are reset to 0 when the input bus voltage drops below $V_{BUS\_CONVEN\_F}$.

Table 11

Register Name	Address	Note
ICHG_CTRL	0x14[12:6]	
SYSOVP_FLT	0x20[4]	Reset to 0 only in case of VSYS overvoltage being triggered while VBUS is available.
EN_PKPWR_AICR	0x31[13]	
EN_PKPWR_VSYS	0x31[12]	
EN_AICC	0x32[11]	
AICR_HOST	0x3F[14:8]	

16.3 Register to be Reset by the CELL_BATPRES Pin Pulled Down

Register bits shown in Table 12 are reset to 0 when the CELL_BATPRES pin is pulled down.

Table 12

Register Name	Address	Note
ICHG_CTRL	0x14[12:6]	
EN_LEARN	0x12[5]	

16.4 Power MOSFETs Selection

16.4.1 NMOSFET for 4-Switch Bidirectional Buck-Boost Converter

The RT9478 features a 4-switch non-inverted buck-boost switching regulator controller, which is part of the charger functions. This switching regulator requires four external NMOSFETs as power switches. The RT9478 drives the gates of these four external NMOSFETs using the REGN regulator voltage output, typically 5V.

Switching performance is critical for NMOSFETs used in switching regulators. The total gate charge (Q_g) serves as an indicator of gate driving losses. Slower gate driving increases the duration of switching events, thereby increasing total switching losses. To select suitable NMOSFET for the RT9478, ensure the gate driving power provided by the REGN regulator (minimum output capability $I_{LIM\_REGN\_min}$ = 65mA) is sufficient. The average gate driving current at a certain switching frequency (f_{SW}) can be estimated by: $I_{LIM\_REGN\_min} = Q_{g(Totally)} \times f_{SW\_MAX}$.

For example, if the switching frequency setting is 800kHz and the f_{SW_MAX} is 840kHz, the total gate charge (Q_g) for all NMOSFETs should be less than 77nC.

The RT9478 incorporates overvoltage protection (OVP) for both the VBUS and VSYS nodes. The OVP rise threshold for VBUS is specified at a maximum of 27.7V. The SYSOVP rise threshold ranges from 12V to 25V and is determined by the CELL_BATPREZ status and VSYS_OVP(0x40[14:12]) register configurations. It is recommended to select NMOSFET with a Drain-Source break down voltage (BV_{DSS}) greater than these OVP levels, with a reasonable safety margin. To match the RT9478's absolute maximum ratings for VBUS, VSYS, VBUS_OVP, and VSYS_OVP threshold settings, 30V breakdown voltage NMOSFET are recommended.

16.4.2 PMOSFET for Battery Path (BATFET)

The RT9478 requires a PMOSFET for the battery switch, also called the “BATFET”. The gate drive voltage for the BATFET is typically 10V. If VSYS is lower than 10V in system application, ensure the PMOSFET's V_{GS_TH} allows the device to turn on under these conditions.

The SYSOVP rise threshold ranges from 12V to 25V and is determined by the CELL_BATPREZ status and VSYS_OVP(0x40[14:12]) register configurations. Select a PMOSFET with a Drain-Source break down voltage (BV_{DSS}) greater than these OVP levels, with a reasonable safety margin. To match the RT9478's absolute maximum ratings and VSYS_OVP threshold settings, a 30V breakdown voltage PMOSFET is recommended. However, for 2-cell battery applications using the default VSYS_OVP, the $V_{SYS\_OVP\_R\_Max}$ is 12.2V; in this case, a PMOSFET with a lower breakdown voltage is suggested.

16.5 Capacitor Selection

16.5.1 Input Capacitor

Input capacitors absorb input switching current ripples, stabilize voltage during load transients, and decouple noise.

Ceramic capacitors (MLCC) are preferred for input decoupling (10nF and 1nF) and should be placed behind the RSENSE_IN, as close as possible to Q1 and Q2.

The input capacitors placed in front of R_{SENSE_IN} absorb input switching current ripple and stabilize voltage during load transients.

Refer to Section 13, Typical Application Circuit, for recommended values and placement for optimal performance.

The minimum effective capacitance on the near side depends on the input power of the application. The suggested minimum effective capacitance is 4μF for 65W input, 6μF for 90W input, 13μF for 130W input. However, customers need to verify the ripple and voltage stabilization during load transients, and other system performances requirements are met.

Ceramic capacitors (MLCC) exhibit a DC-bias effect, which can significantly reduce capacitance. Refer to the capacitor’s datasheet to evaluate this characteristic. Tantalum capacitors (POSCAP) are recommended to avoid the dc-bias effect.

The maximum OVP rise threshold for VBUS is 27.7V. Therefore, the capacitor voltage rating should be greater than this value.

If the system supports OTG function, the minimum effective capacitance is 50μF.

16.5.2 Output Capacitor

Output capacitors absorb output switching ripples and stabilize voltage during load transients.

Refer to 13 Typical Application Circuit, for recommended values and placement for optimal performance.

The minimum effective capacitance is 50μF. However, customers need to verify the ripple and voltage stabilization during load transients, and other system performance requirements are met.

Ceramic capacitors (MLCC) exhibit a DC-bias effect, which can significantly reduce capacitance. Refer to the capacitor’s datasheet to evaluate this characteristic. Tantalum capacitors (POSCAP) are recommended to avoid the dc-bias effect.

The maximum OVP rise threshold for VSYS is 25V. Therefore, the capacitor voltage rating should be greater than this value. However, if the VSYS_OVP setting is lower than 25V, the capacitor voltage rating can be chosen to be lower, but a reasonable safety margin should be reserved.

It is required to place two 10μF MLCC capacitors behind RSENSE_BAT.

16.6 Layout Considerations

- Place C_{AC1}, C_{AC2}, R_{SENSE_IN}, C_{BUS1}, C_{BUS2} Q1 and Q2 as close to the RT9478 as possible to minimize the switching loop. The C_{AC1} and C_{AC2} should be placed in front of R_{SENSE_IN}, while C_{BUS1} and C_{BUS2} should be placed behind R_{SENSE_IN}. Depending on the application, this loop's cooper should be as wide as possible to reduce parasitic resistance and support the required current capability. If this power loop is not on a single layer, ensure that the number of via is sufficient to support the application's current capability.
- Place the inductor (L), C_{BTST1}, and C_{BTST2} as close to the RT9478 as possible to minimize the loop. It is highly recommended that this placement remains on the same layer. Connect these components directly to the RT9478's SW1, SW2, BTST1, and BTST2.
- Place C_{SYS1}, C_{SYS2}, C_{SYS3}, Q3, and Q4 as close to the RT9478 as possible to minimize the switching loop. The C_{SYS1} should be placed in front of the C_{SYS2} and C_{SYS3}, and C_{SYS3} should be placed behind the C_{SYS2}. This loop's cooper should be as wide as possible to reduce parasitic resistance and support the required current capability. If this power loop is not on a single layer, ensure that the number of vias is sufficient to support the application's current capability.
- Place Q5 and R_{SENSE_BAT} as close to the battery terminal as possible. The path from the battery to VSYS, through the R_{SENSE_BAT} and Q5, should be as wide as possible to reduce parasitic resistance and support the required current capability. If this power loop is not on a single layer, ensure that the number of vias is sufficient to support the application's current capability. The RT9478 detects the battery voltage through the CSON pin. Therefore, the CSON connection should be as close to the battery terminal as possible.
- Use Kelvin-sensing connections for R_{SENSE_IN} and R_{SENSE_BAT} current sensing resistors. The traces should be connected from R_{SENSE_IN} and R_{SENSE_BAT} terminals and routed as differential pairs.
- Pin27 (PGND) should be connected to Pin33 (Exposed Pad, GND) by trace directly, and the exposed pad must be soldered to a large PCB pattern with added via for improved thermal performance.
- It is recommended to separate AGND and PGND. PGND should be used for all power stage ground nets, including VBUS, VSYS, and REGN. AGND should be used for sensing, and compensation ground. The following pins should use AGND as their reference: CSIN, CSIP, CMPIN, IBAT, IBUS, ILIM_HIZ, VDDA, COMP1, COMP2, PSYS, CELL_BATPRES, OTG/VAP, CSOP, and CSON. Connect AGND and PGND together using a power pad as the signal connection point.
- If the application has thermal concerns with the MOSFETs, it is suggested to add vias underneath Q1 to Q5 and use a wider multi-layer copper area beneath Q1 to Q5.

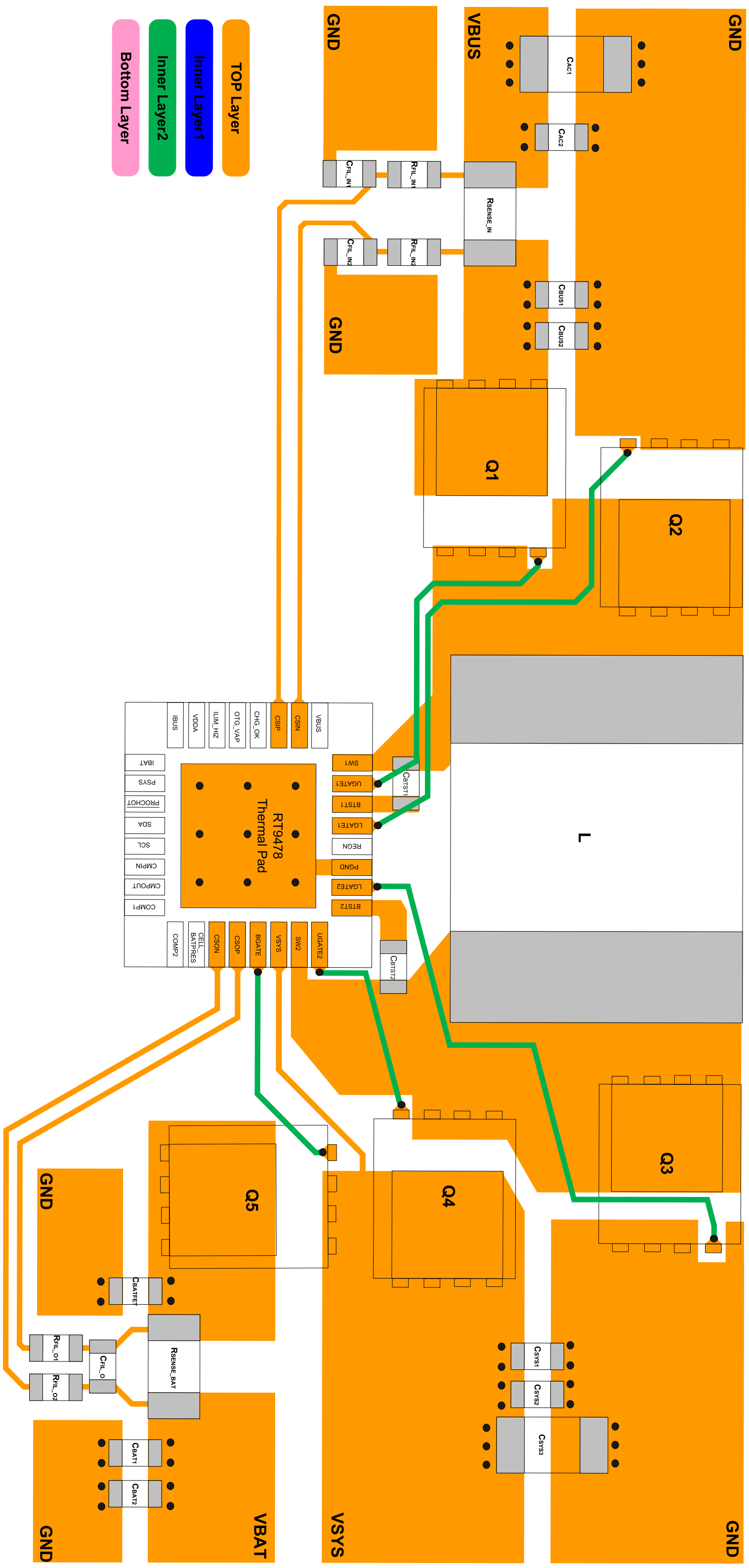


Figure 8. PCB Layout Guide for the RT9478

Note 9. The information provided in this section is for reference only. Richtek does not warrant its accuracy or completeness. The customer is solely responsible for designing, validating, and testing any system applications functionality incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

17 Functional Register Description

Table 13. SMBus Address

Option Code	7-bit Address
A	0x09
B	0x6B

Table 14. Register Type

Type	Abbreviation	Description
Read Only	R	This bit can be read by software. Writes have no effect.
Read/Write	RW	This bit can be read or written by host.
Read Once Clear	RWC	This bit can be read by software and resets to 0.

Table 15. Register List

Address	Register Name	Default	Type	Description
0x12	ChargeOption0	0xE30E	RW	
0x14	ChargeCurrent	0x0000	RW	
0x15	ChargeVoltage	0x0000	RW	
0x20	ChargerStatus	0x0000	R, RWC	
0x21	ProchotStatus	0xB800	R, RW, RWC	
0x22	AICR	0x4100	R	
0x23	ADCVBUS/PSYS	0x0000	R	
0x24	ADCIBAT	0x0000	R	
0x25	ADCIINCMPIN	0x0000	R	
0x26	ADCVSYSVBAT	0x0000	R	
0x30	ChargeOption1	0x3300	RW	
0x31	ChargeOption2	0x00B7	RW	
0x32	ChargeOption3	0x0634	RW	
0x33	ProchotOption0	0x4A81	RW	
0x34	ProchotOption1	0x41A0	RW	
0x35	ADCOption	0x2000	RW	
0x36	ChargeOption4	0x2048	R, RW, RWC	
0x37	VminActiveProtection	0x0A6C	RW	
0x3B	OTGVoltage	0x09C4	R, RW	
0x3C	OTGCurrent	0x3C00	R, RW	
0x3D	MIVR	0x0000	R, RW	
0x3E	VsysMin	0x0000	R, RW	
0x3F	AICRHost	0x4100	R, RW	
0x40	AuxFunction	0x8100	R, RW	
0xFE	MfgID	0x001E	R	
0xFF	DeviceID	0x001C	R	

Table 16. ChargeOption0

Address: 0x12
Description: Configure operation options

Bit	15	14	13	12	11	10	9	8
Field	EN_LPWR	WATCHDOG		AICR_ AUTO_ DIS	OTG_ON_ CHGOK	EN_OOA	PWM_ FREQ	DIS_ STRGDRV
Default	1	1	1	0	0	0	1	1
Type	RW	RW		RW	RW	RW	RW	RW
Bit	7	6	5	4	3	2	1	0
Field	EN_CMP_ LATCH	ENZ_ VSYS_ UVP	EN_ LEARN	IBUS_ GAIN	IBAT_GAIN	EN_LDO	EN_AICR	CHG_ INHIBIT
Default	0	0	0	0	1	1	1	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Bit Name	Default	Type	Description
15	EN_LPWR	1	RW	Enable low power mode. This bit is effective only when the device is in battery-only mode. 0: Disable 1: Enable (default)
14:13	WATCHDOG[1:0]	11	RW	Set the WDT (watchdog timer) for battery charge. The WDT is reset by writing any value to either reg 0x14 or reg 0x15. Once the WDT expires, reg 0x14 is reset to 0. 00: Disable WDT 01: 5s 10: 88s 11: 175s (default)
12	AICR_AUTO_DIS	0	RW	AICR auto disables when the CELL_BATPRES pin is pulled down. 0: Disable this function. AICR is not disabled when CELL_BATPRES goes LOW. (default) 1: Enable this function. AICR is disabled when CELL_BATPRES goes LOW.
11	OTG_ON_CHGOK	0	RW	Add OTG to CHRG_OK. Drive CHRG_OK high when the device is in OTG mode 0: Disable (default) 1: Enable
10	EN_OOA	0	RW	Out of audio function. 0: Disable (default) 1: Enable
9	PWM_FREQ	1	RW	Switching frequency selection. 0: 1200kHz 1: 800kHz (default)

Bit	Bit Name	Default	Type	Description
8	DIS_STRGDRV	1	RW	Disable strong gate drive. Configure the high-side MOSFET to turn on with strong gate drive. 0: Enable strong gate drive 1: Disable strong gate drive (default)
7	EN_CMP_LATCH	0	RW	Independent comparator output latch. 0: The independent comparator output does not latch when it is low. (default) 1: The independent comparator output does latch when it is low. The host can clear the COMPOUT pin by setting this REG 0x12[7] to 0. If enabled in the PP_COMP (0x34[6]) = 1, COMP_PP_STAT (0x21[6]) remains 1b after being triggered until read by host and cleared.
6	ENZ_VSYS_UVP	0	RW	VSYS undervoltage protection (VSYSUVP) enable (Negative Logic) 0: Enable (default) 1: Disable
5	EN_LEARN	0	RW	Learn mode enable. When enabled, the device enters learn mode. 0: Disable (default) 1: Enable
4	IBUS_GAIN	0	RW	Bus current sense pin (CSIP − CSIN) to IBUS output amplifier gain. 0: x20 (default) 1: x40
3	IBAT_GAIN	1	RW	Battery current sense pin (CSOP − CSON) to IBAT output amplifier gain. 0: x8 1: x16 (default)
2	EN_LDO	1	RW	LDO charging enable. Controls battery charges current if the battery voltage is less than VSYS_MIN. 0: Disable; BATFET is fully turned on and the charge current is set by the buck-boost regulator. 1: Enable; battery charge current is clamped at 384mA by LDO charging. (default)
1	EN_AICR	1	RW	Enable AICR. This bit is automatically set to 0 if AICR_AUTO_DIS (0x12[12]) is enabled and CELL_BAT_BATPRES goes to 0. 0: Disable 1: Enable (default)
0	CHG_INHIBIT	0	RW	Charge inhibits. If enabled, battery charging is stopped. 0: Disable (default) 1: Enable

Table 17. ChargeCurrent

Address: 0x14 **Description:** Set the battery charge current								
Bit	15	14	13	12	11	10	9	8
Field	Reserved			ICHG_CTRL				
Default	0	0	0	0	0	0	0	0
Type	R			RW				
Bit	7	6	5	4	3	2	1	0
Field	ICHG_CTRL		Reserved					
Default	0	0	0	0	0	0	0	0
Type	RW		R					

Bit	Bit Name	Default	Type	Description
15:13	Reserved	000	R	Reserved
12:6	ICHG_CTRL [6:0]	0000000	RW	Charging current setting in 7 bits; LSB = 64mA. (R_{SENSE_BAT} = 10mΩ), 128mA (R_{SENSE_BAT} = 5mΩ)
5:0	Reserved	000000	R	Reserved

Table 18. ChargeVoltage

Address: 0x15 **Description:** Set the battery charge termination voltage								
Bit	15	14	13	12	11	10	9	8
Field	Reserved	VBAT_REG						
Default	0	0	0	0	0	0	0	0
Type	R	RW						
Bit	7	6	5	4	3	2	1	0
Field	VBAT_REG					Reserved		
Default	0	0	0	0	0	0	0	0
Type	RW					R		

Bit	Bit Name	Default	Type	Description
15	Reserved	0	R	Reserved
14:3	VBAT_REG [11:0]	00000000 0000	RW	Battery charge termination voltage setting in 12 bits: LSB = 8mV. The effective range is 5.0V (0x271) to 19.2V (0x960). Writing values outside of this range will be ignored.
2:0	Reserved	000	R	Reserved

Table 19. ChargerStatus

Address: 0x20 **Description:** Charger status indicator								
Bit	15	14	13	12	11	10	9	8
Field	VBUS_PG	AICC_ DONE	IN_VAP	IN_MIVR	IN_AICR	IN_FCHG	IN_PCHG	IN_OTG
Default	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Field	BUSOVP _FLT	BATOCP _FLT	BUSOCP1 _FLT	SYSOVP _FLT	SYSUVP _FLT	FORCE_ CONV_ OFF_FLT	OTGOVP _FLT	OTGUVP _FLT
Default	0	0	0	0	0	0	0	0
Type	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC

Bit	Bit Name	Default	Type	Description
15	VBUS_PG	0	R	VBUS status. 0: VBUS is not present (default) 1: VBUS is present
14	AICC_DONE	0	R	Adaptive Input Current Control (AICC) is done. 0: AICC is not completed (default) 1: AICC completed
13	IN_VAP	0	R	0: Charger is not in VAP mode (default) 1: Charger is in VAP mode
12	IN_MIVR	0	R	0: Charger is not in MIVR. (default) 1: Charger is in MIVR during forward mode or in voltage regulation during OTG mode.
11	IN_AICR	0	R	0: Charger is not in AICR. (default) 1: Charger is in AICR during forward mode or IOTG_CC is hit during OTG mode.
10	IN_FCHG	0	R	0: Charger is not in fast charge (default) 1: Charger is in fast charge
9	IN_PCHG	0	R	0: Charger is not in pre-charge (default) 1: Charger is in pre-charge
8	IN_OTG	0	R	0: Charger is not in OTG (default) 1: Charge is in OTG
7	BUSOVP_FLT	0	RWC	0: No fault (default) 1: VBUS OV This bit is cleared to 0 when the register is read.
6	BATOCP_FLT	0	RWC	Fault indicator for BATOC only during normal operation. 0: No fault (default) 1: BATOC is triggered This bit is cleared to 0 when the register is read.
5	BUSOCP1_FLT	0	RWC	0: No fault (default) 1: BUS OC This bit is cleared to 0 when the register is read.

Bit	Bit Name	Default	Type	Description
4	SYSOVP_FLT	0	RWC	0: No fault (default) 1: SYS OVP This bit needs to be set to 0 to be cleared.
3	SYSUVP_FLT	0	RWC	0: No fault (default) 1: SYS UVP This bit needs to be set to 0 to be cleared.
2	FORCE_CONV_OFF_FLT	0	RWC	0: No fault (default) 1: Force converter off triggered (when FORCE_CONV_OFF (0x30[3] = 1) This bit is cleared to 0 when the register is read.
1	OTGOVP_FLT	0	RWC	0: No fault (default) 1: OTG OVP This bit is cleared to 0 when the register is read.
0	OTGUVP_FLT	0	RWC	0: No fault (default) 1: OTG UVP This bit is cleared to 0 when the register is read.

Table 20. ProchotStatus

Address: 0x21 **Description:** PROCHOT behavior settings and fault indicator								
Bit	15	14	13	12	11	10	9	8
Field	Reserved	EN_ PROCHOT _EXT	PROCHOT_WIDTH		PROCHO T_CLR	OTP_FLT	VAP_FAIL _STAT	EXIT_ VAP_PP_ STAT
Default	1	0	1	1	1	0	0	0
Type	R	RW	RW		RW	R	RW	RW
Bit	7	6	5	4	3	2	1	0
Field	MIVR_ PP_ STAT	COMP_ PP_STAT	ICRIT_ PP_STAT	INOM_ PP_ STAT	IDCHG1_ PP_STAT	VSYS_ PP_ STAT	BAT GONE_ PP_STAT	VBUSOK _PP_ STAT
Default	0	0	0	0	0	0	0	0
Type	RW	RWC	RWC	RWC	RWC	RWC	RWC	RWC

Bit	Bit Name	Default	Type	Description
15	Reserved	1	R	Reserved
14	EN_PROCHOT_ EXT	0	RW	PROCHOT pulse extension 0: Disable (default) 1: Enable
13:12	PROCHOT_ WIDTH [1:0]	11	RW	PROCHOT minimum pulse width. 00: 100μs 01: 1ms 10: 5ms 11: 10ms (default)
11	PROCHOT_CLR	1	RW	PROCHOT clear. 0: Clear PROCHOT 1: Idle (default) Need to write 0 to reset PROCHOT if pulse extension is enabled (0x21[14] = 1).
10	OTP_FLT	0	R	Over-Temperature Protection (OTP). 0: OTP is not triggered (default) 1: OTP is triggered
9	VAP_FAIL_STAT	0	RW	If VAP exits due to VBUS experiencing 7 consecutive undervoltage events, not only can the VAP_FAIL_STAT assert, but the EXIT_VAP_PP_STAT can assert as well. 0: No fail (default) 1: In the VAP failure event, it is latched until the host writes 0.
8	EXIT_VAP_PP_ STAT	0	RW	If this bit is set to 1, the charger exits VAP in following conditions: Disabled by ACOV, BATUV ($C_{SON} < V_{BAT\_OTGEN\_F}$), OTG_VAP = "L" and OTG_VAP_MODE (0x32[5]) = 1. 0: PROCHOT_EXIT_VAP is not active (default) 1: PROCHOT_EXIT_VAP is active and latched until the host writes 0.

Bit	Bit Name	Default	Type	Description
7	MIVR_PP_STAT	0	RW	PROCHOT profile MIVR status bit 0: Not triggered (default) 1: Triggered, the $\overline{PROCHOT}$ pin remains low until the host writes this status bit to 0 when PP_MIVR = 1.
6	COMP_PP_STAT	0	RWC	PROCHOT profile CMPOUT status bit. 0: Not triggered (default) 1: Triggered This bit is cleared to 0 when the register is read.
5	ICRIT_PP_STAT	0	RWC	PROCHOT profile ICRIT status bit 0: Not triggered (default) 1: Triggered This bit is cleared to 0 when the register is read.
4	INOM_PP_STAT	0	RWC	PROCHOT profile INOM status bit. 0: Not triggered (default) 1: Triggered This bit is cleared to 0 when the register is read.
3	IDCHG1_PP_ STAT	0	RWC	PROCHOT profile IDCHG1 status bit. 0: Not triggered (default) 1: Triggered This bit is cleared to 0 when the register is read.
2	VSYS_PP_STAT	0	RWC	PROCHOT profile VSYS status bit. 0: Not triggered (default) 1: Triggered This bit is cleared to 0 when the register is read.
1	BATGONE_PP_ STAT	0	RWC	PROCHOT profile Battery Removal status bit. 0: Not triggered (default) 1: Triggered This bit is cleared to 0 when the register is read.
0	VBUSOK_PP_ STAT	0	RWC	PROCHOT profile Adapter Removal status bit. 0: Not triggered (default) 1: Triggered This bit is cleared to 0 when the register is read.

Table 21. AICR

Address: 0x22
Description: Set AICR (Average Input Current Regulation) current

Bit	15	14	13	12	11	10	9	8
Field	Reserved	IAICR						
Default	0	1	0	0	0	0	0	1
Type	R	R						
Bit	7	6	5	4	3	2	1	0
Field	Reserved							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Bit Name	Default	Type	Description
15	Reserved	0	R	Reserved
14:8	IAICR [6:0]	1000001	R	AICR current setting in 7 bits; LSB = 50mA (R_{SENSE_IN} = 10mΩ), 100mA (R_{SENSE_IN} = 5mΩ) Note: This register is read only. Write setting value to AICR_HOST (0x3F[14:8]).
7:0	Reserved	00000000	R	Reserved

Table 22. ADCVbusPsys

Address: 0x23
Description: VBUS and PSYS voltage A/D conversion outputs

Bit	15	14	13	12	11	10	9	8
Field	VBUS							
Default	0	0	0	0	0	0	0	0
Type	R							
Bit	7	6	5	4	3	2	1	0
Field	PSYS							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Bit Name	Default	Type	Description
15:8	VBUS [7:0]	00000000	R	VBUS A/D conversion output in 8 bits: LSB = 96mV, up to 24.48V
7:0	PSYS [7:0]	00000000	R	PSYS A/D conversion output in 8 bits: LSB = 8mV (0x35[13] ADC_FULLSCALE = 0), up to 2.04V LSB = 12mV (0x35[13] ADC_FULLSCALE = 1), up to 3.06V

Table 23. ADCIbat

Address: 0x24 **Description:** Battery charge and discharge current A/D conversion outputs								
Bit	15	14	13	12	11	10	9	8
Field	Reserved	IBAT_CHG						
Default	0	0	0	0	0	0	0	0
Type	R	R						
Bit	7	6	5	4	3	2	1	0
Field	Reserved	IBAT_DISCHG						
Default	0	0	0	0	0	0	0	0
Type	R	R						

Bit	Bit Name	Default	Type	Description
15	Reserved	0	R	Reserved
14:8	IBAT_CHG [6:0]	0000000	R	Battery charge current A/D conversion output in 7 bits: LSB = 64mA (0x30[10] RSNS_BAT = 0, R_{SENSE_BAT} = 10mΩ), up to 8.128A LSB = 128mA (0x30[10] RSNS_BAT = 1, R_{SENSE_BAT} = 5mΩ), up to 16.256A
7	Reserved	0	R	Reserved
6:0	IBAT_DISCHG [6:0]	0000000	R	Battery discharge current A/D conversion output in 7 bits: LSB = 256mA (0x30[10] RSNS_BAT = 0, R_{SENSE_BAT} = 10mΩ), up to 20.48A LSB = 512mA (0x30[10] RSNS_BAT = 1, R_{SENSE_BAT} = 5mΩ), up to 40.96A

Table 24. ADCIinCMPin

Address: 0x25 **Description:** BUS current and Comparator Input voltage A/D conversion outputs								
Bit	15	14	13	12	11	10	9	8
Field	IBUS							
Default	0	0	0	0	0	0	0	0
Type	R							
Bit	7	6	5	4	3	2	1	0
Field	VCOMP							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Bit Name	Default	Type	Description
15:8	IBUS [7:0]	00000000	R	BUS current A/D conversion output in 8 bits: LSB = 50mA (0x30[11] RSNS_IN = 0, R_{SENSE_IN} = 10mΩ), up to 12.75A LSB = 100mA (0x30[11] RSNS_IN = 1, R_{SENSE_IN} = 5mΩ), up to 25.5A
7:0	VCOMP [7:0]	00000000	R	The CMPIN pin voltage A/D conversion output in 8 bits: LSB = 8mV (0x35[13] ADC_FULLSCALE = 0), up to 2.04V LSB = 12mV (0x35[13] ADC_FULLSCALE = 1), up to 3.06V

Table 25. ADCVsysVbat

Address: 0x26 **Description:** SYS voltage and battery voltage A/D conversion outputs								
Bit	15	14	13	12	11	10	9	8
Field	VSYS							
Default	0	0	0	0	0	0	0	0
Type	R							
Bit	7	6	5	4	3	2	1	0
Field	VBAT							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Bit Name	Default	Type	Description
15:8	VSYS [7:0]	00000000	R	VSYS voltage A/D conversion output in 8 bits: LSB = 64mV, 2.88V to 19.2V
7:0	VBAT [7:0]	00000000	R	VBAT voltage A/D conversion output in 8 bits: LSB = 64mV 2.88V to 19.2V

Table 26. ChargeOption1

Address: 0x30
Description: Configure the operation options

Bit	15	14	13	12	11	10	9	8
Field	EN_IBAT_PIN	EN_PROCHOT_LPWR	PSYS_CONFIG		RSNS_IN	RSNS_BAT	PSYS_RATIO	EN_FAST_5MOHM
Default	0	0	1	1	0	0	1	1
Type	RW	RW	RW		RW	RW	RW	RW
Bit	7	6	5	4	3	2	1	0
Field	CMP_REF	CMP_POL	CMP_DEG		EN_FORCE_CONV	Reserved	EN_SHIP_DCHG	EN_AUTO_WAKEUP
Default	0	0	0	0	0	0	0	0
Type	RW	RW	RW		RW	R	RW	RW

Bit	Bit Name	Default	Type	Description
15	EN_IBAT_PIN	0	RW	Enable IBAT analog output 0: Disable (default) 1: Enable
14	EN_PROCHOT_LPWR	0	RW	Enable the external comparator and its PROCHOT in low power mode 0: Disable (default) 1: Enable
13:12	PSYS_CONFIG [1:0]	11	RW	PSYS configuration 00: PSYS = PBUS + PBAT 01: PSYS = PBUS 10: Reserved 11: Disable (default)
11	RSNS_IN	0	RW	Input sense resistor, R_{SENSE_IN} setting 0: 10mΩ (default) 1: 5mΩ
10	RSNS_BAT	0	RW	Battery sense resistor, R_{SENSE_BAT} setting 0: 10mΩ (default) 1: 5mΩ
9	PSYS_RATIO	1	RW	PSYS gain 0: 0.25μA/W 1: 1μA/W (default)
8	EN_FAST_5MOHM	1	RW	Enable fast compensation to increase bandwidth under 5mΩ R_{SENSE_IN} (RSNS_IN = 1b) for input current up to 6.4A application. The fast compensation will only work when IBUS pin is configured to less than 160kΩ. 0: Disable 1: Enable (default)
7	CMP_REF	0	RW	Independent comparator's internal reference 0: 2.3V (default) 1: 1.2V

Bit	Bit Name	Default	Type	Description
6	CMP_POL	0	RW	Independent comparator output polarity 0: Negative (default) 1: Positive
5:4	CMP_DEG [1:0]	00	RW	Independent comparator deglitch time. This setting is only applicable to the falling edge 00: 5μs (default) 01: 2ms 10: 20ms 11: 5s
3	EN_FORCE_CONV	0	RW	Force converter off 0: Disable (default) 1: Enable
2	Reserved	0	R	Reserved
1	EN_SHIP_DCHG	0	RW	Discharge the CSOP and CSON pins for shipping mode 0: Disable (default) 1: Enable
0	EN_AUTO_ WAKEUP	0	RW	Enable auto wakeup 0: Disable (default) 1: Enable

Table 27. ChargeOption2

Address: 0x31 **Description:** Configure the operation options								
Bit	15	14	13	12	11	10	9	8
Field	PKPWR_TOVLD_DEG		EN_PKPWR_AICR	EN_PKPWR_VSYS	PKPWR_OVLD_STAT	PKPWR_RELAX_STAT	PKPWR_TMAX	
Default	0	0	0	0	0	0	0	0
Type	RW		RW	RW	RW	RW	RW	
Bit	7	6	5	4	3	2	1	0
Field	EN_EXT_ILIM	ICHG_IDCHG_DIR	Q2_OCP	IBUS_OCP2_TH	EN_IBUS_OCP1	IBUS_OCP1_TH	EN_BATOC	BATOC_VTH
Default	1	0	1	1	0	1	1	1
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Bit Name	Default	Type	Description
15:14	PKPWR_TOVLD_DEG [1:0]	00	RW	Input overload time in peak power mode 00: 1ms (default) 01: 2ms 10: 5ms 11: 10ms
13	EN_PKPWR_AICR	0	RW	Enable peak power mode which is triggered by input current overshoot 0: Disable (default) 1: Enable
12	EN_PKPWR_VSYS	0	RW	Enable peak power mode which is triggered by system voltage undershoot. 0: Disable (default) 1: Enable
11	PKPWR_OVLD_STAT	0	RW	Peak power mode indicator. Write 0 to exit the overloading cycle timer. 0: Not in peak power mode. (default) 1: In peak power mode.
10	PKPWR_RELAX_STAT	0	RW	Indicator of peak power relaxation. Write 0 to exit relaxation cycle timer. 0: Not in relaxation cycle. (default) 1: In relaxation mode.
9:8	PKPWR_TMAX [1:0]	00	RW	Set the peak power mode's overload and relax cycle times. 00: 20ms (default) 01: 40ms 10: 80ms 11: 1s
7	EN_EXT_ILIM	1	RW	Use the ILIM_HIZ pin to set current limit. 0: Input current limit is set by AICR register. 1: Input current limit is set by the minimum value of the ILIM_HIZ pin or AICR register (0x22). (default)

Bit	Bit Name	Default	Type	Description
6	ICHG_IDCHG_DIR	0	RW	The IBAT pin direction 0: As discharge current (default) 1: As charge current
5	Q2_OCP	1	RW	Set the V_{DS} threshold for Q2 overcurrent protection 0: 210mV 1: 150mV (default)
4	IBUS_OCP2_TH	1	RW	VBUS sense resistor overcurrent protection at CSIP − CSIN 0: 280mV (RSNS_IN = 0) 200mV (RSNS_IN = 1) 1: 150mV (RSNS_IN = 0) (default) 100mV (RSNS_IN = 1) (default)
3	EN_IBUS_OCP1	0	RW	Enable the VBUS sense resistor overcurrent protection 0: Disable (default) 1: Enable the threshold; it depends on IBUS_OCP1_TH (0x31[2])
2	IBUS_OCP1_TH	1	RW	Set the VBUS sense resistor overcurrent protection value 0: 133% of IAICR2 1: 200% of IAICR2 (default)
1	EN_BATOC	1	RW	Battery discharge overcurrent (BATOC) protection 0: Disable 1: Enable the threshold; its threshold depends on BATOC_VTH (0x31[0]) (default)
0	BATOC_VTH	1	RW	Set the battery discharge overcurrent protection value 0: 133% of DCHG_TH2 1: 200% of DCHG_TH2 (default)

Table 28. ChargeOption3

<table>
<tr><td colspan="9">Address: 0x32
Description: Configure the operation options</td></tr>
<tr><td>Bit</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>Field</td><td>EN_HIZ</td><td>RESET_ REG</td><td>RESET_ MIVR</td><td>EN_OTG</td><td>EN_AICC</td><td>EN_ PORT_ CTRL</td><td>EN_VSYS_ MIN_SOFT _SR</td><td>EN_OTG_ BIGCAP</td></tr>
<tr><td>Default</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Type</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td></tr>
<tr><td>Bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Field</td><td>BATFET_ ENZ</td><td>EN_VBUS _VAP</td><td>OTG_VAP _MODE</td><td colspan="2">IL_AVG</td><td>EN_CMP</td><td>BATFET OFF_HIZ</td><td>PSYS_ OTG_ IDCHG</td></tr>
<tr><td>Default</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Type</td><td>RWC</td><td>RW</td><td>RW</td><td colspan="2">RW</td><td>RW</td><td>RW</td><td>RW</td></tr>
</table>

Bit	Bit Name	Default	Type	Description
15	EN_HIZ	0	RW	Enable HiZ mode 0: Disable (default) 1: Enable
14	RESET_REG	0	RW	Reset all registers except for the MIVR (0x3F) register. 0: Idle (default) 1: Reset; the value goes back to 0 after the reset.
13	RESET_MIVR	0	RW	Reset MIVR (0x3D) resister 0: Idle (default) 1: Converter is disabled to measure the MIVR threshold.
12	EN_OTG	0	RW	OTG mode 0: Disable (default) 1: Enable
11	EN_AICC	0	RW	Enable Adaptive Input Current Control (AICC) 0: Disable (default) 1: Enable
10	EN_PORT_CTRL	1	RW	Enable BATFET control. If disabled, BGATE become high impedance. 0: Disable 1: Enable (default) This bit is activated only if the UNLOCK_PORT_CTRL (0x40[7]) is set to 1.
9	EN_VSYS_MIN_ SOFT_SR	1	RW	VSYS_MIN soft slew rate transition. 0: Disable 1: Enable (default)
8	EN_OTG_ BIGCAP	0	RW	Enable OTG compensation for VBUS effective capacitance larger than 33μF. 0: Disable (default) 1: Enable

Bit	Bit Name	Default	Type	Description
7	BATFET_ENZ	0	RWC	BATFET force turns off at battery only mode. This bit is not written to 1 during bus voltage is available. This bit is forced to 0 in OTG mode. 0: Disable (default) 1: Enable
6	EN_VBUS_VAP	0	RW	VAP mode selection, enabled to operate in mode 2 and 3. 0: Mode 1 (default) 1: Mode 2 and 3
5	OTG_VAP_MODE	1	RW	OTG/VAP/FRS pin function assign 0: VAP 1: OTG (default)
4:3	IL_AVG [1:0]	10	RW	Converter inductor average current clamp. 00: 6A 01: 10A 10: 15A (default) 11: Disable
2	EN_CMP	1	RW	Enable independent comparator. 0: Disable 1: Enable (default)
1	BATFETOFF_HIZ	0	RW	Control BATFET on/off during charger HiZ mode. 0: BATFET on during charger HiZ mode (default) 1: BATFET off during charger HiZ mode
0	PSYS_OTG_ IDCHG	0	RW	PSYS function in OTG mode. 0: PSYS as battery discharge power minus OTG output power (default) 1: PSYS as battery discharge power only

Table 29. ProchotOption0

Address: 0x33
Description: Configure the PROCHOT options

Bit	15	14	13	12	11	10	9	8
Field	IAICR2					ICRIT_DEG		PROCHOT_MIVR_80_90
Default	0	1	0	0	1	0	1	0
Type	RW					RW		RW
Bit	7	6	5	4	3	2	1	0
Field	VSYS_TH1						INOM_DEG	LOWER_PROCHOT_MIVR
Default	1	0	0	0	0	0	0	1
Type	RW						RW	RW

Bit	Bit Name	Default	Type	Description
15:11	IAICR2 [4:0]	01001	RW	I_{AICR2} threshold. Trigger if the current hits the threshold: 00000: NA 00001 to 11001: 110% to 230%, step 5% 11010 to 11110: 250% to 450%, step 50% 11111: Out of range (ignored) 01001 (default) is 150%.
10:9	ICRIT_DEG [1:0]	01	RW	Typical ICRIT deglitch time to trigger PROCHOT. 00: 15μs 01: 100μs (default) 10: 400μs 11: 800μs
8	PROCHOT_MIVR_80_90	0	RW	Lower threshold of the PROCHOT_MIVR comparator When REG0x33[0] = 1, the threshold of the PROCHOT_MIVR comparator is determined by this bit setting. The minimum setting of 83%/91% of MIVR setting is clamped at VBUS_CONVENZ if the value is lower than VBUS_CONVENZ 0: 83% of MIVR (0x3D[13:6]) threshold (default) 1: 91% of MIVR (0x3D[13:6]) threshold
7:2	VSYS_TH1 [5:0]	100000	RW	VSYS threshold in VAP mode for VSYS capacitor voltage. 000000 to 111111: 3.2V to 9.5V in 100mV step 100000 (default) is 6.4V.
1	INOM_DEG	0	RW	INOM deglitch time 0: 1ms (default) 1: 60ms

Bit	Bit Name	Default	Type	Description
0	LOWER_ PROCHOT_MIVR	1	RW	Enable the lower threshold of the PROCHOT_MIVR comparator. 0: The threshold of the PROCHOT_MIVR comparator to follow the same MIVR (Reg 0x3D) setting. 1: The threshold of the PROCHOT_MIVR comparator is determined by the PROCHOT_MIVR_80_90bit (Reg 0x33[8]) setting. (default)

Table 30. ProchotOption1

Address: 0x34
Description: Configure the PROCHOT options

Bit	15	14	13	12	11	10	9	8
Field	IDCHG_TH1						IDCHG_DEG1	
Default	0	1	0	0	0	0	0	1
Type	RW						RW	
Bit	7	6	5	4	3	2	1	0
Field	PP_MIVR	PP_COMP	PP_ICRIT	PP_INOM	PP_ IDCHG1	PP_VSYS	PP_ BATGONE	PP_ VBUSOK
Default	1	0	1	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Bit Name	Default	Type	Description
15:10	IDCHG_TH1 [5:0]	010000	RW	IDCHG level 1 threshold in 6 bits: LSB = 512mA 010000 (default) is 8.192A
9:8	IDCHG_DEG1 [1:0]	01	RW	IDCHG level 1 deglitch time 00: 78ms 01: 1.25s (default) 10: 5s 11: 20s
7	PP_MIVR	1	RW	Enable MIVR PROCHOT 0: Disable 1: Enable (default)
6	PP_COMP	0	RW	Enable independent comparator PROCHOT. 0: Disable (default) 1: Enable
5	PP_ICRIT	1	RW	Enable ICRIT PROCHOT 0: Disable 1: Enable (default)
4	PP_INOM	0	RW	Enable INOM PROCHOT 0: Disable (default) 1: Enable
3	PP_IDCHG1	0	RW	Enable IDCHG1 PROCHOT 0: Disable (default) 1: Enable
2	PP_VSYS	0	RW	Enable VSYS PROCHOT 0: Disable (default) 1: Enable
1	PP_BATGONE	0	RW	Enable battery removal PROCHOT when the CELL_BATPRES pin is low 0: Disable (default) 1: Enable
0	PP_VBUSOK	0	RW	Enable adapter removal PROCHOT 0: Disable (default) 1: Enable

Table 31. ADCOption

Address: 0x35 **Description:** Enable the A/D converter								
Bit	15	14	13	12	11	10	9	8
Field	ADC_ CONV	ADC_ START	ADC_ FULL SCALE	Reserved				
Default	0	0	1	0	0	0	0	0
Type	RW	RW	RW	R				
Bit	7	6	5	4	3	2	1	0
Field	EN_ADC_ VCOMP	EN_ADC_ VBUS	EN_ADC_ PSYS	EN_ADC_ IBUS	EN_ADC_ IBAT_ DISCHG	EN_ADC_ IBAT_CHG	EN_ADC_ VSYS	EN_ADC_ VBAT
Default	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Bit Name	Default	Type	Description
15	ADC_CONV	0	RW	Enable A/D conversion repeat mode 0: One-shot (default) 1: Continuous (1sec cycle)
14	ADC_START	0	RW	A/D conversion starts in one-shot mode. Automatically reset to 0 after the one-shot update is complete. 0: Ready (default) 1: Start
13	ADC_FULLSCALE	1	RW	ADC input voltage full scale range for PSYS and CMPIN. 0: 2.04V 1: 3.06V (default)
12:8	Reserved	00000	R	Reserved
7	EN_ADC_VCOMP	0	RW	A/D conversion for independent comparator 0: Disable (default) 1: Enable
6	EN_ADC_VBUS	0	RW	A/D conversion for BUS voltage 0: Disable (default) 1: Enable
5	EN_ADC_PSYS	0	RW	A/D conversion for PSYS output 0: Disable (default) 1: Enable
4	EN_ADC_IBUS	0	RW	A/D conversion for BUS current 0: Disable (default) 1: Enable
3	EN_ADC_IBAT_ DISCHG	0	RW	A/D conversion for battery discharge current 0: Disable (default) 1: Enable
2	EN_ADC_IBAT_CHG	0	RW	A/D conversion for battery charge current 0: Disable (default) 1: Enable

Bit	Bit Name	Default	Type	Description
1	EN_ADC_VSYS	0	RW	A/D conversion for SYS voltage 0: Disable (default) 1: Enable
0	EN_ADC_VBAT	0	RW	A/D conversion for battery voltage 0: Disable (default) 1: Enable

Table 32. ChargeOption4

<table>
<tr><td colspan="9">Address: 0x36
Description: Configure the operation options</td></tr>
<tr><td>Bit</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>Field</td><td colspan="3">VSYS_UVP</td><td colspan="2">DITHER_EN</td><td>VSYS_UVP_NO_HICCUP</td><td>PP_VBUS_VAP</td><td>VBUS_VAP_PP_STAT</td></tr>
<tr><td>Default</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Type</td><td colspan="3">RW</td><td colspan="2">RW</td><td>RW</td><td>RW</td><td>RWC</td></tr>
<tr><td>Bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Field</td><td colspan="2">IDCHG_DEG2</td><td colspan="3">IDCHG_TH2</td><td>PP_IDCHG2</td><td>IDCHG2_PP_STAT</td><td>Reserved</td></tr>
<tr><td>Default</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Type</td><td colspan="2">RW</td><td colspan="3">RW</td><td>RW</td><td>RWC</td><td>R</td></tr>
</table>

Bit	Bit Name	Default	Type	Description
15:13	VSYS_UVP [2:0]	001	RW	VSYS undervoltage-lockout. 000: 3.65V 001: 3.65V (default) 010: 4.0V 011: 4.8V 100: 5.6V 101: 6.4V 110: 7.2V 111: 8.0V
12:11	DITHER_EN [1:0]	00	RW	Frequency dithering configuration 00: Disable (default) 01: 2% 10: 4% 11: 6%
10	VSYS_UVP_NO_HICCUP	0	RW	Disable VSYS_UVP hiccup configuration 0: Enable (default) 1: Disable
9	PP_VBUS_VAP	0	RW	Enable VBUS PROCHOT 0: Disable (default) 1: Enable
8	VBUS_VAP_PP_STAT	0	RWC	VBUS_VAP PROCHOT status. 0: Not triggered (default) 1: Triggered
7:6	IDCHG_DEG2 [1:0]	01	RW	Battery discharge current limit 2 deglitch time 00: 100μs 01: 1.6ms (default) 10: 6ms 11: 12ms

Bit	Bit Name	Default	Type	Description
5:3	IDCHG_TH2 [2:0]	001	RW	Battery discharge current limit2 based on percentage of IDCHG_TH1. 000: 125% 001: 150% (default) 010: 175% 011: 200% 100: 250% 101: 300% 110: 350% 111: 400%
2	PP_IDCHG2	0	RW	Enable IDCHG2 PROCHOT 0: Disable (default) 1: Enable
1	IDCHG2_PP_ STAT	0	RWC	IDCHG2 PROCHOT status. 0: Not triggered (default) 1: Triggered
0	Reserved	0	R	Reserved

Table 33. VAP

<table>
<tr><td colspan="9">Address: 0x37
Description: Configure VAP (Vmin Active Protection) operation options</td></tr>
<tr><td>Bit</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>Field</td><td colspan="7">VBUS_VAP_TH</td><td>Reserved</td></tr>
<tr><td>Default</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Type</td><td colspan="7">RW</td><td>R</td></tr>
<tr><td>Bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Field</td><td colspan="6">VSYS_TH2</td><td>EN_TH2_ FOLLOW_ TH1</td><td>EN_FRS</td></tr>
<tr><td>Default</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Type</td><td colspan="6">RW</td><td>RW</td><td>RW</td></tr>
</table>

Bit	Bit Name	Default	Type	Description
15:9	VBUS_VAP_TH [6:0]	0000101	RW	VBUS PROCHOT trigger voltage threshold in 7bits with 3.2V offset: LSB = 100mV 0000101 (default) is 3.7V
8	Reserved	0	R	Reserved
7:2	VSYS_TH2 [5:0]	011011	RW	VSYS PROCHOT trigger voltage threshold in 6bits: LSB = 100mV 011011 (default) is 5.9V
1	EN_TH2_ FOLLOW_TH1	0	RW	Enable neglecting register VSYS_TH2 (Reg 0x37 [7:2]) setting 0: Disable, VSYS_TH2 set by 0x37[7:2] (default) 1: Enable, VSYS_TH2 follow to VSYS_TH1 (0x33[7:2])
0	EN_FRS	0	RW	Fast role swap enables. Do not toggle while OTG is enabled. 0: Disable (default) 1: Enable

Table 34. OTGVoltage

Address: 0x3B **Description:** Set the OTG output voltage								
Bit	15	14	13	12	11	10	9	8
Field	Reserved		VOTG_REG					
Default	0	0	0	0	1	0	0	1
Type	R		RW					
Bit	7	6	5	4	3	2	1	0
Field	VOTG_REG						Reserved	
Default	1	1	0	0	0	1	0	0
Type	RW						R	

Bit	**Bit Name**	**Default**	**Type**	**Description**
15:14	Reserved	00	R	Reserved
13:2	VOTG_REG [11:0]	00100111 0001	RW	OTG output and VAP charge voltage are in 12bits: LSB = 8mV The effective range is 3.0V (0x177) to 24.0V (0xBB8). Values written outside of this range are ignored. 0010 0111 0001 (default) is 5V.
1:0	Reserved	00	R	Reserved

Table 35. OTGCurrent

Address: 0x3C **Description:** Set the OTG current limit								
Bit	15	14	13	12	11	10	9	8
Field	Reserved	IOTG_REG						
Default	0	0	1	1	1	1	0	0
Type	R	RW						
Bit	7	6	5	4	3	2	1	0
Field	Reserved							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	**Bit Name**	**Default**	**Type**	**Description**
15	Reserved	0	R	Reserved
14:8	IOTG_REG [6:0]	0111100	RW	OTG current limit in 7 bits: LSB = 50mA (R_{SENSE_IN} = 10mΩ), 100mA (R_{SENSE_IN} = 5mΩ) 0111100 (default) is 3.0A
7:0	Reserved	00000000	R	Reserved

Table 36. MIVR

Address: 0x3D **Description:** Set the MIVR (Minimum Input Voltage Regulation) voltage								
Bit	15	14	13	12	11	10	9	8
Field	Reserved		VMIVR					
Default	0	0	0	0	0	0	0	0
Type	R		RW					
Bit	7	6	5	4	3	2	1	0
Field	VMIVR		Reserved					
Default	0	0	0	0	0	0	0	0
Type	RW		R					

Bit	Bit Name	Default	Type	Description
15:14	Reserved	00	R	Reserved
13:6	VMIVR [7:0]	00000000	RW	MIVR voltage in 8 bits with 3.2V offset: LSB = 64mV The effective range is 3.2V (0x00) to 19.52V (0xFF). Writing values outside of this range is ignored.
5:0	Reserved	000000	R	Reserved

Table 37. VsysMin

Address: 0x3E **Description:** Set the system minimum voltage								
Bit	15	14	13	12	11	10	9	8
Field	VSYS_MIN							
Default	0	0	0	0	0	0	0	0
Type	RW							
Bit	7	6	5	4	3	2	1	0
Field	Reserved							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Bit Name	Default	Type	Description
15:8	VSYS_MIN [7:0]	00000000	RW	VSYS_MIN voltage in 8 bits: LSB = 100mV The effective range is 5.0V (0x32) to 19.2V (0xC0). Writing values outside of this range is ignored.
7:0	Reserved	00000000	R	Reserved

Table 38. AICRHost

<table>
<tr><td colspan="9">Address: 0x3F
Description: Set the AICR (Average Input Current Regulation) current</td></tr>
<tr><td>Bit</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>Field</td><td>Reserved</td><td colspan="7">AICR_HOST</td></tr>
<tr><td>Default</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Type</td><td>R</td><td colspan="7">RW</td></tr>
<tr><td>Bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Field</td><td colspan="8">Reserved</td></tr>
<tr><td>Default</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Type</td><td colspan="8">R</td></tr>
</table>

Bit	Bit Name	Default	Type	Description
15	Reserved	0	R	Reserved
14:8	AICR_HOST [6:0]	1000001	RW	AICR current in 7 bits: LSB = 50mA (R_{SENSE_IN} = 10mΩ), 100mA (R_{SENSE_IN} = 5mΩ) This register value is reflected in 0x22[14:8]. 1000001 (default) is 3.25A
7:0	Reserved	00000000	R	Reserved

Table 39. AuxFunction

Address: 0x40
Description: Configure micelles operation

Bit	15	14	13	12	11	10	9	8
Field	PROCHOT_DELAY	VSYS_OVP			Reserved	PWM_LOWFREQ	SMBUS_TIMEOUT_DISABLE	SMBUS_TIMEOUT_MODE
Default	1	0	0	0	0	0	0	1
Type	RW	RW			R	RW		
Bit	7	6	5	4	3	2	1	0
Field	UNLOCK_PORT_CTRL	Reserved				ENZ_VBAT_OVP	RESET_REG_INHIBIT	
Default	0	0	0	0	0	0	0	0
Type	RW	R				RW		

Bit	Bit Name	Default	Type	Description
15	PROCHOT_DELAY	1	RW	0: 1μs 1: 10μs (default)
14:12	VSYS_OVP [2:0]	000	RW	VSYS overvoltage protection threshold. 000: Depends on cell count by CELL_BATPRES (default) 001: 15V 010: 16V 011: 20V 100: 21V 101: 22V 110: 23V 111: 24V
11	Reserved	0	R	Reserved
10	PWM_LOWFREQ	0	RW	Set PWM frequency. 0: Follow 0x12[9] setting (1200kHz or 800kHz) (default) 1: 720kHz 0x40[10] setting has higher priority. If 0x40[10] = 1, PWM frequency is set to 720kHz regardless of 0x12[9] setting.
9	SMBUS_TIMEOUT_DISABLE	0	RW	0: Enable Timeout (default) 1: Disable Timeout
8	SMBUS_TIMEOUT_MODE	1	RW	0: SCL 1: SCL and SDA (default)
7	UNLOCK_PORT_CTRL	0	RW	Activates EN_PORT_CTRL (0x32[10]). 0: EN_PORT_CTRL is disabled (default) 1: EN_PORT_CTRL is enabled
6:3	Reserved	0000	R	Reserved
2	ENZ_VBAT_OVP	0	RW	0: Enable VBAT_OVP (default) 1: Disable VBAT_OVP

Bit	Bit Name	Default	Type	Description
1:0	RESET_REG_ INHIBIT	00	RW	00: Inhibit when VBAT < VBAT_UVLO (default) 01: Inhibit when VBAT < VBAT_OTG_EN 10: Inhibit when VSYS < VSYS_MIN*0.95 11: Not Inhibit

Table 40. MfgID

Address: 0xFE **Description:** Manufacturer ID								
Bit	15	14	13	12	11	10	9	8
Field	Reserved							
Default	0	0	0	0	0	0	0	0
Type	R							
Bit	7	6	5	4	3	2	1	0
Field	MFG_ID							
Default	0	0	0	1	1	1	1	0
Type	R							

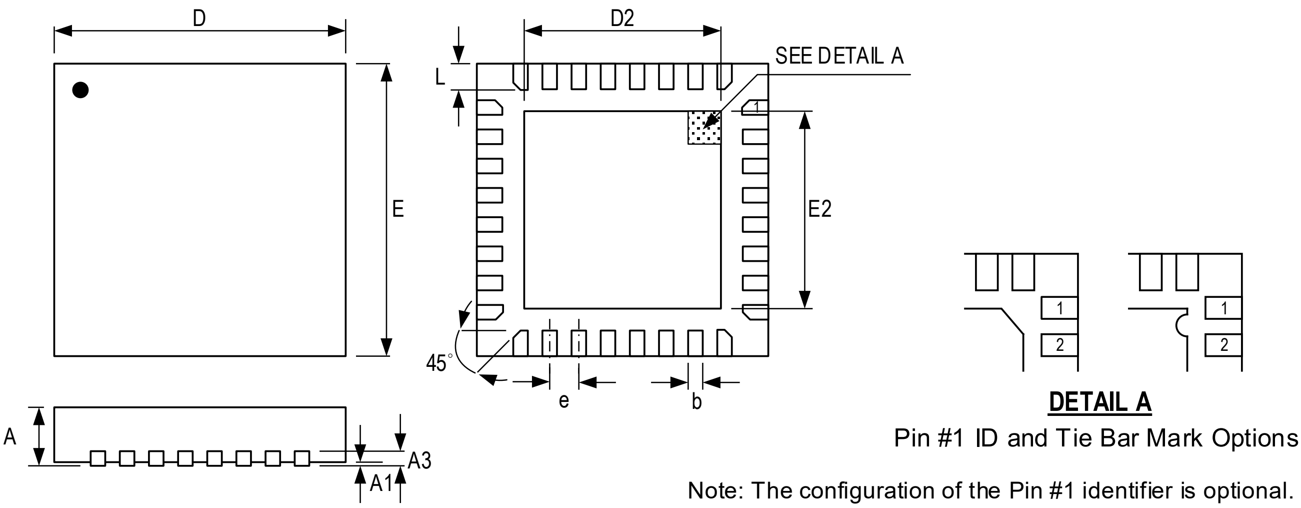
Bit	Bit Name	Default	Type	Description
15:8	Reserved	00000000	R	Reserved
7:0	MFG_ID [7:0]	00011110	R	Manufacturer ID, 0x1E

Table 41. DeviceID

Address: 0xFF **Description:** Device ID								
Bit	15	14	13	12	11	10	9	8
Field	Reserved							
Default	0	0	0	0	0	0	0	0
Type	R							
Bit	7	6	5	4	3	2	1	0
Field	DEVICE_ID							
Default	0	0	0	1	1	1	0	0
Type	R							

Bit	Bit Name	Default	Type	Description
15:8	Reserved	00000000	R	Reserved
7:0	DEVICE_ID [7:0]	00011100	R	Device ID, 0x1C

18 Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

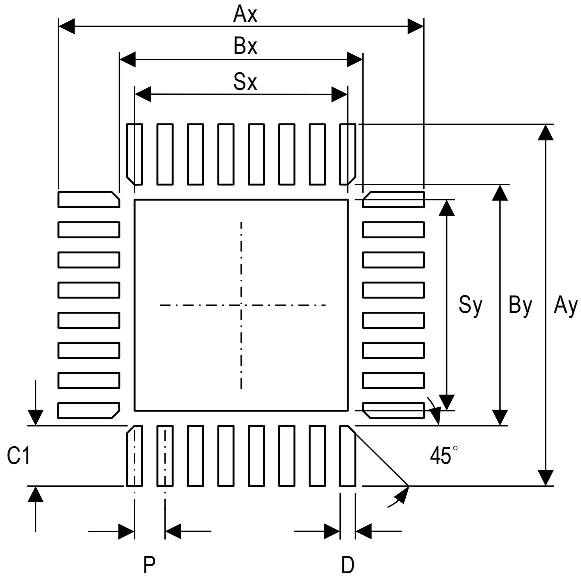
Note: The configuration of the Pin #1 identifier is optional. but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.150	0.250	0.006	0.010
D		3.900	4.100	0.154	0.161
D2	Option 1	2.650	2.750	0.104	0.108
	Option 2	2.750	2.850	0.108	0.112
E		3.900	4.100	0.154	0.161
E2	Option 1	2.650	2.750	0.104	0.108
	Option 2	2.750	2.850	0.108	0.112
e		0.400		0.016	
L		0.300	0.400	0.012	0.016

W-Type 32L QFN 4x4 Package

Note 10. The package of the RT9478 uses Option 2.

19 Footprint Information

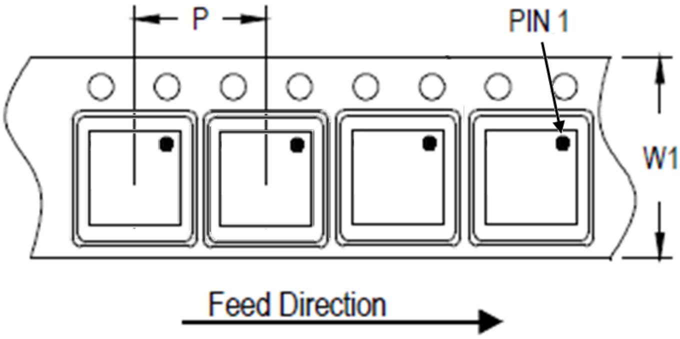


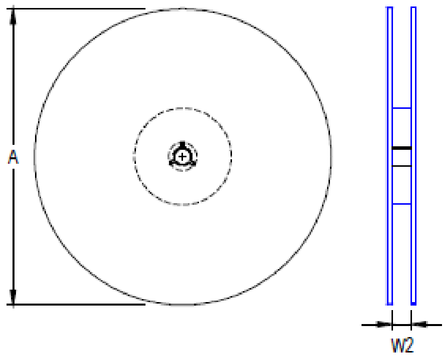
<table>
<tr><th colspan="2" rowspan="2">Package</th><th rowspan="2">Number of Pins</th><th colspan="10">Footprint Dimension (mm)</th><th rowspan="2">Tolerance</th></tr>
<tr><th>P</th><th>Ax</th><th>Ay</th><th>Bx</th><th>By</th><th>C*32</th><th>C1*8</th><th>D</th><th>Sx</th><th>Sy</th></tr>
<tr><td rowspan="2">V/W/U/XQFN4*4-32</td><td>Option1</td><td rowspan="2">32</td><td rowspan="2">0.40</td><td rowspan="2">4.80</td><td rowspan="2">4.80</td><td rowspan="2">3.20</td><td rowspan="2">3.20</td><td rowspan="2">0.80</td><td rowspan="2">0.75</td><td rowspan="2">0.20</td><td rowspan="2">2.80</td><td rowspan="2">2.80</td><td rowspan="2">±0.05</td></tr>
<tr><td>Option2</td></tr>
</table>

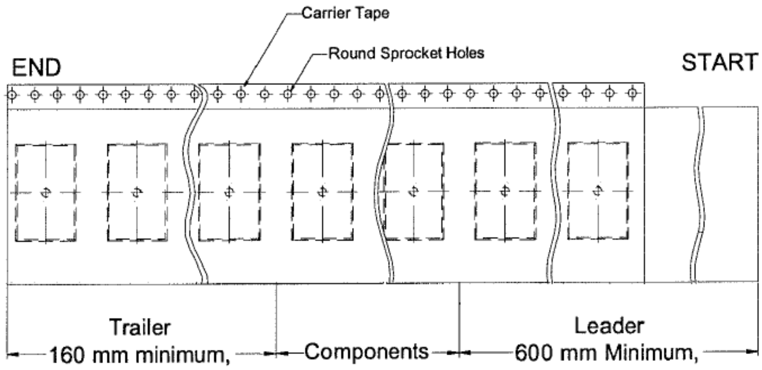
Note 11. The package of the RT9478 uses Option 2.

20 Packing Information

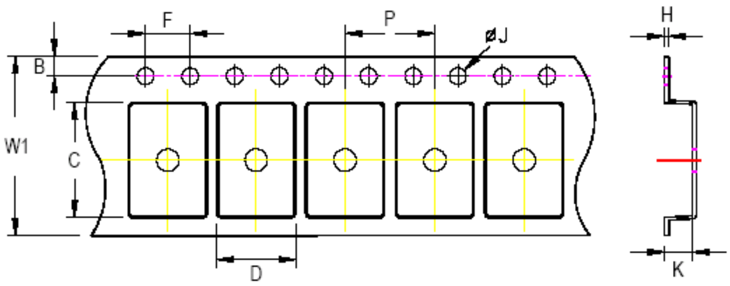
20.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 4x4	12	8	330	13	3,000	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
(V, W) QFN and DFN 4x4	13”	3,000	Box G	1	3,000	Carton A	6	18,000

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description
00	2026/1/21	First Edition