MOSFET Integrated Smart Photoflash Capacitor Charger with IGBT Driver

General Description
The RT9598 is a complete photoflash module solution for digital and film cameras. It is targeted for applications that use 2 to 4 AA batteries or 1 to 2 Lithium-Ion batteries. The RT9598 adopts Flyback topology which uses constant primary peak current and zero secondary valley current to charge photoflash capacitor quickly and efficiently. The built-in 55V MOSFET allows flexibility in transformer design and simplifies the PCB layout. The RT9598 also integrates an IGBT driver for igniting photoflash tube. Only a few external components are required, which greatly reduces the PCB space and cost. The RT9598 is available in the WDFN-8L 2x2 package.

Features
- 55V MOSFET Integrated
- Charge any Size Photoflash Capacitor
- Adjustable Input Current
- Adjustable Output Voltage
- Charge Complete Indicator
- Built-In IGBT Driver for IGBT Application
- Constant Peak Current Control
- Over-Voltage Protection
- Maximum On-Time Protection
- 8-Lead WDFN Package
- RoHS Compliant and Halogen Free

Applications
- Digital Still Camera
- Film Camera Flash Unit
- Camera Phone Flash

Marking Information

1K : Product Code
W : Date Code

Simplified Application Circuit
Ordering Information

RT9598

Package Type
QW : WDFN-8L 2x2 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note:
Richtek products are:
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Functional Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DRVOUT</td>
<td>IGBT Driver Output.</td>
</tr>
<tr>
<td>2</td>
<td>DRVIN</td>
<td>IGBT Driver Input.</td>
</tr>
<tr>
<td>3</td>
<td>CHARGE</td>
<td>Charge Enable Control Input. The charge function is executed when CHARGE pin is set from Low to High. The chip is in Shutdown mode when CHARGE pin is set to Low.</td>
</tr>
<tr>
<td>4</td>
<td>STAT</td>
<td>Charge Status Open-Drain Output. When target output voltage is reached, this pin will be pulled low. This pin needs a pull-up resistor.</td>
</tr>
<tr>
<td>5</td>
<td>FB</td>
<td>Feedback Voltage Input.</td>
</tr>
<tr>
<td>6</td>
<td>CS</td>
<td>Input Current Setting.</td>
</tr>
<tr>
<td>7</td>
<td>VDD</td>
<td>Supply Voltage Input.</td>
</tr>
<tr>
<td>8</td>
<td>SW</td>
<td>N-MOSFET Switch Node.</td>
</tr>
<tr>
<td>9 (Exposed Pad)</td>
<td>GND</td>
<td>Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.</td>
</tr>
</tbody>
</table>

Function Block Diagram
Operation

Basic Operation
The RT9598 is a photo flash charger comprised of several building blocks. The following paragraphs are described in detail.

Enable
If the output voltage is below its target voltage, the CHARGE pin pulling high enables charging cycle and pulling low stops charging. When the output voltage reaches the target voltage, the MOSFET will be turned off and the STAT pin will be pulled low to indicate that charging is completed.

Peak Current Control
The MOSFET peak current is set by an external resistor on the CS pin.

DCM
The RT9598 uses DCM operation mechanism to decide the timing to turn on MOSFET. This block senses transformer's secondary current through the SW pin. When the current drops to zero, the energy is delivered to output, and the MOSFET will turn on for next cycle.

Maximum Off-Time
During pre-charge, a 9μs maximum off-time is used to reduce the charging time.

Maximum On-Time Protection
If the on-time of the internal MOSFET is over 2ms, the maximum on-time protection will be triggered to shut down the charging system.

OVP Protection
The over-voltage protection supervises the abnormal voltage via the FB and SW pins. If OVP occurs, the internal MOSFET will turn off immediately.

IGBT Driver
The DRVOUT is used to trigger flash tube module when HV capacitor is charged ready. It also equips with false trigger protection when VDD is low or the STAT pin is not at low status.
Absolute Maximum Ratings  (Note 1)

- Supply Voltage, VDD ........................................................................................................................................... –0.3V to 6V
- Built-in N-Channel Enhancement MOSFET
  Drain-Source Voltage ................................................................................................................................. –0.3V to 55V
  CS, CHARGE, DRVIN, DRVOUT, STAT, FB ............................................................. –0.3V to 6V
  SW Pulse Current (Pulse Width 1μs) ........................................................................................................ 4A
  SW Continuous Current .............................................................................................................................. 2A
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-8L 2x2 ................................................................................................................................. 2.19W
- Package Thermal Resistance  (Note 2)
  WDFN-8L 2x2, θ JA .......................................................................................................................... 45.5°C/W
  WDFN-8L 2x2, θ JC .......................................................................................................................... 11.5°C/W
- Junction Temperature ............................................................................................................................. 150°C
- Lead Temperature (Soldering, 10 sec.) ................................................................................................. 260°C
- Storage Temperature Range ................................................................................................................ –65°C to 150°C
- ESD Susceptibility  (Note 3)
  HBM (Human Body Model) ............................................................................................................... 2kV
  MM (Machine Model) .......................................................................................................................... 200V

Recommended Operating Conditions  (Note 4)

- Supply Voltage, VDD ................................................................................................................................... 2.9V to 5.5V
- Battery Voltage ........................................................................................................................................... 1.6V to 9V
- Drain Source Voltage ................................................................................................................................. 50V
- Junction Temperature Range .................................................................................................................. –40°C to 125°C
- Ambient Temperature Range ................................................................................................................ –40°C to 85°C

Electrical Characteristics
(VDD = 3.3V, T_A = 25°C, unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switch Off Current</td>
<td>I_{VDD_SW_OFF}</td>
<td>V_{FB} = 1.1V</td>
<td>--</td>
<td>1</td>
<td>10</td>
<td>μA</td>
</tr>
<tr>
<td>Shutdown Current</td>
<td>I_{OFF}</td>
<td>CHARGE pin = 0V</td>
<td>--</td>
<td>0.1</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td>FB Voltage</td>
<td>V_{FB}</td>
<td></td>
<td>0.985</td>
<td>1</td>
<td>1.015</td>
<td>V</td>
</tr>
<tr>
<td>Line Regulation</td>
<td></td>
<td>ΔV_{FB}</td>
<td>2.9V &lt; V_{DD} &lt; 5.5V</td>
<td>--</td>
<td>--</td>
<td>10</td>
</tr>
<tr>
<td>STAT Open Drain R_{DS(ON)}</td>
<td></td>
<td></td>
<td>--</td>
<td>11</td>
<td>19</td>
<td>Ω</td>
</tr>
<tr>
<td>Charge Enable High</td>
<td>V_{CEH}</td>
<td></td>
<td>1.3</td>
<td>--</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>Charge Enable Low</td>
<td>V_{CEL}</td>
<td></td>
<td>--</td>
<td>--</td>
<td>0.4</td>
<td>V</td>
</tr>
</tbody>
</table>

Built-In N-Channel Enhancement MOSFET

<table>
<thead>
<tr>
<th>Drain-Source On-Resistance</th>
<th>R_{DS(ON)}</th>
<th>V_{DD} = 3.3V, I_D = 10mA</th>
<th>--</th>
<th>0.3</th>
<th>0.4</th>
<th>Ω</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Off-Time During Pre-Charge</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum Off-Time</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum On-time Protection</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Absolute Maximum Ratings

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. $\theta_{JA}$ is measured at $T_A = 25^\circ$C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. $\theta_{JC}$ is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

### IGBT Driver

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRVIN Trip Point</td>
<td></td>
<td>$V_{DD} = 3.3V$ to $5V$</td>
<td>0.8</td>
<td>1.05</td>
<td>1.4</td>
<td>V</td>
</tr>
<tr>
<td>DRVOUT On-Resistance to $V_{DD}$</td>
<td></td>
<td>$V_{DD} = 3.3V$</td>
<td>5</td>
<td>10</td>
<td>15</td>
<td>Ω</td>
</tr>
<tr>
<td>DRVOUT On-Resistance to GND</td>
<td></td>
<td>$V_{DD} = 3.3V$</td>
<td>10</td>
<td>16</td>
<td>22</td>
<td>Ω</td>
</tr>
<tr>
<td>Propagation Delay (Rising)</td>
<td>$T_{PD_R}$</td>
<td>$V_{DD} = 5V$</td>
<td>--</td>
<td>11</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3.3V$</td>
<td>--</td>
<td>13.5</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>Propagation Delay (Falling)</td>
<td>$T_{PD_F}$</td>
<td>$V_{DD} = 5V$</td>
<td>50</td>
<td>110</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3.3V$</td>
<td>40</td>
<td>70</td>
<td>120</td>
<td>ns</td>
</tr>
</tbody>
</table>
Typical Application Circuit
Typical Operating Characteristics

Switching

Charge Time vs. VBAT

Output Voltage vs. VBAT
Application Information

The RT9598 integrates a constant peak current controller for charging photoflash capacitor and an IGBT driver for igniting flash tube. The photoflash capacitor charger uses constant primary peak current and SW falling control to efficiently charge the photoflash capacitor.

Pulling the CHARGE pin high will initiate the charging cycle. However, the CHARGE signal must go from low to high after \( V_{DD} > 2\text{V} \) for at least 1\( \mu \text{s} \) delay time.

![Figure 1. Recommend Charge Timing Chart](image)

During MOSFET on-period, the primary current ramps up linearly according to \( V_{BAT} \) and primary inductance. A resistor connecting from the CS pin to GND determines the primary peak current.

During the MOSFET off-period, the energy stored in the Flyback transformer is boosted to the output capacitor. The secondary current decreases linearly at a rate determined by the secondary inductance and the output voltage (neglecting the voltage drop of the diode).

The SW pin monitors the secondary current. When the secondary current drops to 0A, SW voltage falls, and then the MOSFET on-period starts again. The charging cycle repeats itself and charges the output capacitor. The output voltage is sensed by a voltage divider connecting to the anode of the rectifying diode. When the output voltage reaches the desired voltage set by the resistor divider, the charging block will be disabled and charging will be stopped.

Then STAT pin will be pulled low to indicate complete charging.

The voltage sensing path will be cut off when charging is completed to minimize the output voltage decay. Both the CHARGE and STAT pins can be easily interfaced to a microprocessor in a digital system.

Charge Current Setting

The RT9598 simply adjusts peak primary current by a resistor \( R_{CS} \) connecting to the CS pin as shown in the Function Block Diagram. \( R_{CS} \) determines the peak current of the primary N-MOSFET according to the following equation:

\[
I_{PK\_PRI} = \frac{40000}{R_{CS}} \quad (A)
\]

where \( I_{PK\_PRI} \) is the primary peak current. Users could select appropriate \( R_{CS} \) according to the battery capability and required charging time. We recommend RCS should be greater than 13k\( \Omega \).

Transformer

The Flyback transformer should be appropriately designed to ensure effective and efficient operation.

1. Turns Ratio

The turns ratio of transformer (\( N \)) should be high enough so that the absolute maximum voltage rating for the internal N-MOSFET Drain to Source voltage is not exceeded. Choose the minimum turns ratio according to the following formula:

\[
N_{MIN} \geq \frac{V_{OUT}}{50 - V_{BAT}}
\]

Where:

- \( V_{OUT} \): Target Output Voltage
- \( V_{BAT} \): Battery Voltage

2. Primary Inductance

Each switching cycle, energy transferred to the output capacitor is proportional to the primary inductance for a constant primary current. The higher the primary inductance, the higher the charging efficiency. Besides, to ensure enough off-time for the output voltage sensing, the primary inductance should be high enough according to the following formula:

\[
L_{PRI} \geq \frac{400 \times 10^{-9} \times V_{OUT}}{N \times I_{PK\_PRI}}
\]

Where:

- \( V_{OUT} \): Target Output Voltage
- \( N \): Transformer turns ratio
- \( I_{PK\_PRI} \): Primary peak current
3. Leakage Inductance
The leakage inductance of the transformer results in the first spike voltage when N-MOSFET turns off. The spike voltage is proportional to the leakage inductance and inductor peak current. The spike voltage must not exceed the dynamic rating of the N-MOSFET Drain to Source voltage (50V).

4. Transformer Secondary Capacitance
Any capacitance on the secondary can severely affect the efficiency. A small secondary capacitance is multiplied by $N^2$ when reflected to the primary side, so the equivalent capacitance will become large.

This capacitance forms a resonant circuit with the primary leakage inductance of the transformer. Therefore, both the primary leakage inductance and secondary side capacitance should be minimized.

Rectifying Diode
The rectifying diode should be with short reverse recovery time (small parasitic capacitance). Large parasitic capacitance increases switching loss and lowers charging efficiency.

In addition, the peak reverse voltage and peak current of the diode should be sufficient.

The peak reverse voltage of the diode can be calculated as the following equation:

$$V_{PK-R} = V_{OUT} + (N \times V_{BAT})$$

The peak current of the diode is equal to the primary peak current divided by the transformer turn ratio as the following equation:

$$I_{PK-SEC} = \frac{I_{PK-PRI}}{N}$$

Where : $N$ is the transformer turns ratio.

Output Voltage Setting
The RT9598 senses the output voltage by a voltage divider connecting to the anode of the rectifying diode during off-time as shown in Figure 2. This eliminates power loss at voltage sensing circuit when charging is completed. $R_1$ to $R_2$ ratio determines the output voltage as shown in the typical application circuit. The feedback reference voltage is 1V.

If $V_{OUT} = 300V$, according the following equation:

$$V_{OUT} = V_{FB} \times (1 + \frac{R_1 + R_2}{R_3})$$

and $\frac{R_1 + R_2}{R_3} = 299$

It is recommended to set $R_3 = 1k\Omega$ and $R_1 = R_2 = 150k\Omega$ for reducing parasitic capacitance coupling effect of the FB pin. $R_1$ and $R_2$ MUST be larger than 0805 package size for enduring secondary HV. Another sensing method is to sense the output voltage directly as shown in Figure 3.

Over-Voltage Protection (OVP)
The RT9598 provides an Over-Voltage Protection (OVP) function. In the typical application circuit, if the FB resistor $R_1$, $R_2$ or $R_3$ is open, the FB voltage will be pulled low or floating. In this condition, when the CHARGE pin goes high, the RT9598 begins switching. When the SW voltage reaches 14V, the OVP function will be triggered.

False Triggering Prevention
The RT9598 includes a mechanism to prevent false triggering of the DRVOUT pin while the device is still in charging mode.
Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

\[ P_{D(\text{MAX})} = \frac{(T_{J(\text{MAX})} - T_A)}{\theta_{JA}} \]

Where \( T_{J(\text{MAX})} \) is the maximum operation junction temperature, \( T_A \) is the ambient temperature and the \( \theta_{JA} \) is the junction to ambient thermal resistance.

For recommended operating conditions specification, the maximum junction temperature is 125°C. The junction to ambient thermal resistance \( \theta_{JA} \) is layout dependent. For WDFN-8L 2x2 package, the thermal resistance \( \theta_{JA} \) is 45.5°C/W on the standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at \( T_A = 25°C \) can be calculated by following formula:

\[ P_{D(\text{MAX})} = \frac{(125°C - 25°C)}{(45.5°C/W)} = 2.19W \] for WDFN-8L 2x2 package

The maximum power dissipation depends on the operating ambient temperature for fixed \( T_{J(\text{MAX})} \) and thermal resistance, \( \theta_{JA} \). The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

Layout Considerations

For the best performance of the RT9598, the following PCB layout guidelines must be strictly followed:

- Both of primary and secondary power paths should be as short as possible.
- Place the current setting resistor \( R_{CS} \) to the CS pin as close as possible. The GND side of \( R_{CS} \) should be directly connected to ground plane to avoid noise coupling.
- Keep the switching node area as small as possible to reduce parasitic capacitance coupling effect.
- Place the feedback resistors as close as possible to the FB pin.
- The GND should be connected to a strong ground plane to reduce switching noise.
Outline Dimension

W-Type 8L DFN 2x2 Package

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Dimensions in Millimeters</th>
<th>Dimensions in Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>A</td>
<td>0.700</td>
<td>0.800</td>
</tr>
<tr>
<td>A1</td>
<td>0.000</td>
<td>0.050</td>
</tr>
<tr>
<td>A3</td>
<td>0.175</td>
<td>0.250</td>
</tr>
<tr>
<td>b</td>
<td>0.200</td>
<td>0.300</td>
</tr>
<tr>
<td>D</td>
<td>1.950</td>
<td>2.050</td>
</tr>
<tr>
<td>D2</td>
<td>1.000</td>
<td>1.250</td>
</tr>
<tr>
<td>E</td>
<td>1.950</td>
<td>2.050</td>
</tr>
<tr>
<td>E2</td>
<td>0.400</td>
<td>0.650</td>
</tr>
<tr>
<td>e</td>
<td>0.500</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>0.300</td>
<td>0.400</td>
</tr>
</tbody>
</table>

Note: The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

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