RICHTEK®

RT9614L

Single-Phase Synchronous Rectified Buck MOSFET Driver

1 General Description

The RT9614L is a dual N-channel MOSFET driver for synchronous-rectified buck converters. The device integrates the power switch, replacing the need for an external bootstrap diode, which reduces system cost and complexity while allowing the use of higher-performance MOSFETs.

The RT9614L is a high-performance driver capable of driving high- and low-side MOSFETs at high switching frequencies with low power dissipation. Its operating voltage is compatible with MOSFETs featuring a 30V breakdown voltage, providing greater flexibility and a wider range of application possibilities.

The RT9614L features 4.5V to 13.2V gate driver voltage supplied via the VCC pin. It offers a propagation delay of approximately 30ns for both high-side and low-side MOSFETs, and a 1.1Ω sink impedance on the low-side gate driver to prevent shoot-through power loss during high dV/dt phase node transitions. The RT9614L can efficiently switch MOSFET gates at frequencies up to 1MHz and is capable of driving gate loads up to 3nF. As a result, the RT9614L is well-suited for a variety of high-input voltage, high-current, and single-phase or multi-phase DC to DC converter applications, such as CPU core voltage and VGA power suppliers.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Features

- **Shoot Through Protection**
- **Embedded Bootstrap Diode**
- **Up to 500kHz Operating Frequency**
- **Fast Rising and Falling Time**
- **Compatible with 3.3V or 5V Middle State PWM Input**
- **Enable Control**
- **Pre-OVP Protection**
- **8-Lead WDFN Package**

3 Applications

- Desktop Systems
- VGA Cards

4 Ordering Information

RT9614L □□

Package Type(1)
QW: WDFN-8L 3x3 (W-Type)

Lead Plating System
G: Richtek Green Policy Compliant(2)

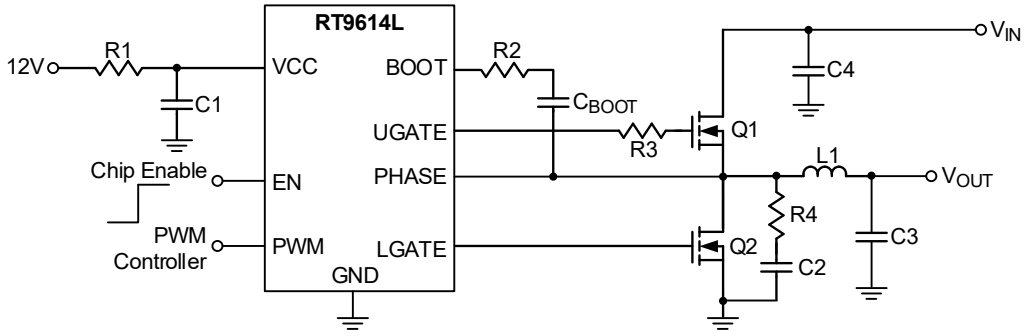
Note 1.

- Marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicates that Richtek products are Richtek Green Policy compliant.

5 Marking Information

005: Product Code
YMDAN: Date Code

6 Simplified Application Circuit



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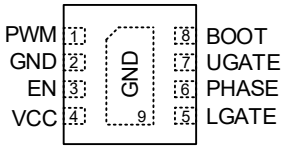
7 Pin Configuration

(TOP VIEW)

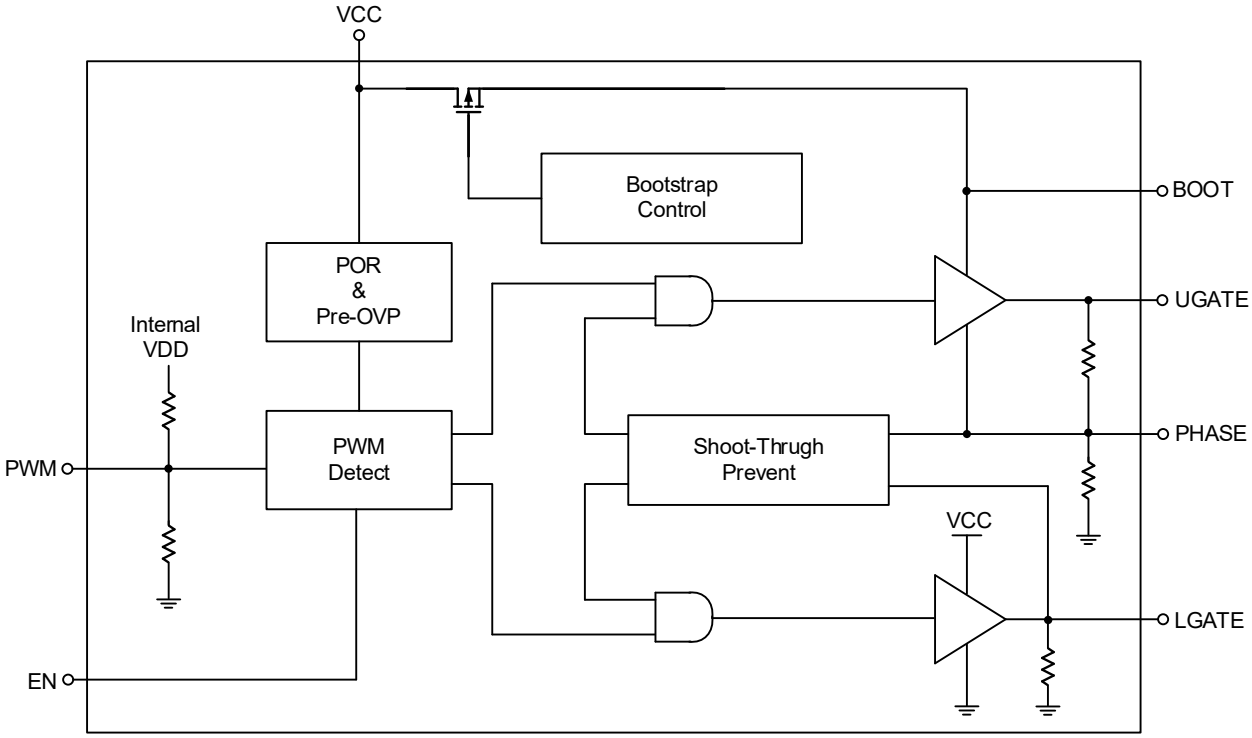


WDFN-8L 3x3

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PWM	The PWM signal input pin. The external PWM signal determines the both UGATE and LGATE signals. UGATE is complementary to LGATE. If the PWM signal is at tri-state voltage, both UGATE and LGATE are turned off.
2, 9 (Exposed Pad)	GND	Ground pin. All signals are referenced to this pin.
3	EN	Enable control input pin (Active High). When the voltage of the EN pin rises above its threshold, the RT9614L is enabled and the UGATE/LGATE is ready to be controlled. When the EN voltage falls below its falling threshold, the RT9614L is shut down. At any time, there is no need to consider accidental entry into test mode.
4	VCC	Supply voltage input pin. The VCC supplies power to the analog circuit of RT9614L and the gate drivers. Place a bypass capacitor from this pin to GND for noise immunity.
5	LGATE	Low-side gate driver output pin. Connect to the gate of low-side MOSFET. Notice, DO not connect a resistor (R_{G_EXT}) between LGATE and the gate terminal of the low-side MOSFET, as it might cause undesired shoot-through due to the LGATE voltage is monitored for shoot-through protection.
6	PHASE	Connect to the source of the high-side MOSFET and the drain of the low-side MOSFET. Provide the driving path for the high-side driver and is used for Pre-OVP and shoot-through protection.
7	UGATE	High-side gate driver output pin. Connect to the gate of the high-side MOSFET.
8	BOOT	Bootstrap capacitor output pin. The bootstrap capacitor is charged by this pin while the low-side MOSFET is turned on, providing energy to turn on the high-side MOSFET. Connect this pin through the bootstrap capacitor to the PHASE pin.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, VCC ---------- –0.3V to 15V
- BOOT to PHASE---------- –0.3V to 15V
- PHASE to GND
  - DC ---------- –0.3V to 30V
  - <100ns ---------- –10V to 35V
- LGATE to GND
  - DC ---------- –0.3V to (VCC + 0.3V)
  - <100ns ---------- –2V to (VCC + 0.3V)
- UGATE to GND
  - DC ---------- (V_{PHASE} – 0.3V) to (V_{BOOT} + 0.3V)
  - <100ns ---------- (V_{PHASE} – 2V) to (V_{BOOT} + 0.3V)
- EN, PWM to GND ---------- –0.3V to 7V
- Package Thermal Resistance
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-8L 3x3 ---------- 3.22W
- Package Thermal Resistance (Note 3)
  - WDFN-8L 3x3, θ_{JA} ---------- 31°°C/W
  - WDFN-8L 3x3, θ_{JC} ---------- 8°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ----------–65°C to 150°C
- ESD Susceptibility (Note 4)
  - HBM (Human Body Model)---------- 1.5kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Voltage, VCC ---------- 4.5V to 13.2V
- Input Voltage, (VIN + VCC) ---------- < 35V
- Ambient Temperature Range---------- –40°C to 125°C
- Junction Temperature Range---------- –40°C to 85°C

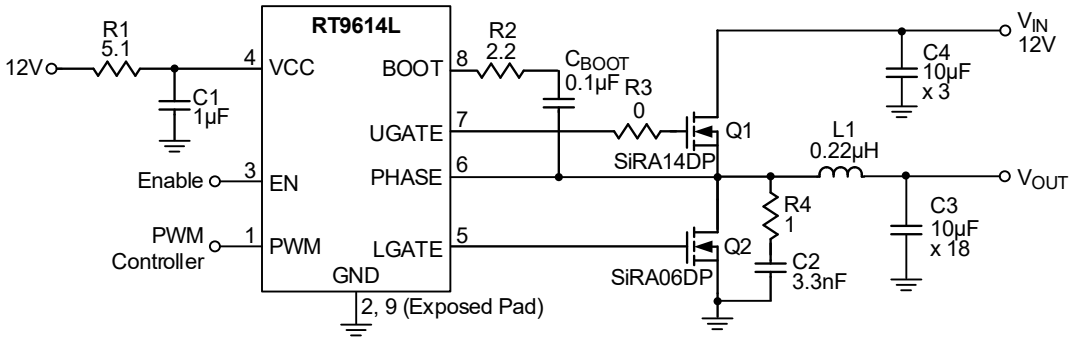
Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

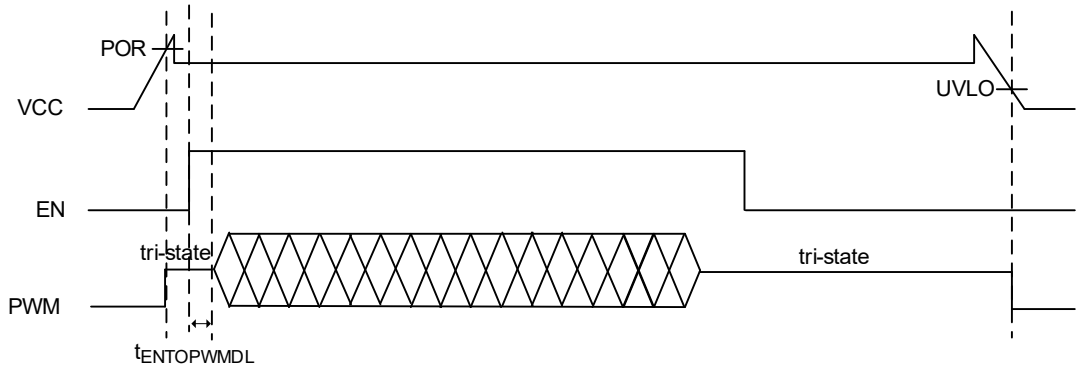
(V_{CC} = 12V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Power Supply Voltage	V_{CC}		4.5	--	13.2	V
Power Supply Current	I_{VCC}	V_{BOOT} = 12V, PWM input floating	--	120	--	μA
Power On Reset (POR)						
POR Rising Threshold	V_{POR_R}	V_{CC} rising	--	4	4.4	V
POR Falling Threshold	V_{POR_F}	V_{CC} falling	3	3.5	--	V
EN Input						
EN Input Voltage Rising Threshold	V_{EN_R}		--	1.3	1.6	V
EN Input Voltage Falling Threshold	V_{EN_F}		0.7	1	--	V
PWM Input						
Maximum Input Current	I_{PWM}	PWM = 0V or 5V	--	160	--	μA
PWM Floating Voltage	V_{PWM_FL}	PWM = open	--	1.8	--	V
PWM Logic-High	V_{PWM_H}		2.96	--	--	V
PWM Logic-Low	V_{PWM_L}		--	--	0.6	V
Timing						
UGATE Rising Time	t_{R_UGATE}	3nF load	--	25	--	ns
UGATE Falling Time	t_{F_UGATE}	3nF load	--	12	--	ns
LGATE Rising Time	t_{R_LGATE}	3nF load	--	24	--	ns
LGATE Falling Time	t_{F_LGATE}	3nF load	--	10	--	ns
UGATE Propagation Delay	$t_{DLY\_PDH\_UGATE}$	V_{BOOT} – V_{PHASE} = 12V See timing diagram	--	35	--	ns
	$t_{DLY\_PDL\_UGATE}$		--	22	--	
LGATE Propagation Delay	$t_{DLY\_PDH\_LGATE}$	See timing diagram	--	30	--	ns
	$t_{DLY\_PDL\_LGATE}$	See timing diagram	--	8	--	
EN to PWM Delay	$t_{DLY\_ENTOPWM}$		--	3	--	ns
Tri-State to High Delay	t_{UGPTST}		--	30	--	ns
High to Tri-State Delay	t_{UGSSHD}		--	20	--	ns
Tri-State to Low Delay	t_{LGPTST}		--	42	--	ns
Low to Tri-State Delay	t_{LGSSHD}		--	15	--	ns
Output						
UGATE Drive Source	R_{SRC_UGATE}	V_{BOOT} – V_{PHASE} = 12V, I_{Source} = 100mA	--	1.7	--	Ω
UGATE Drive Sink	R_{SNK_UGATE}	V_{BOOT} – V_{PHASE} = 12V, I_{Sink} = 100mA	--	1.4	--	Ω
LGATE Drive Source	R_{SRC_LGATE}	I_{Source} = 100mA	--	1.6	--	Ω
LGATE Drive Sink	R_{SNK_LGATE}	I_{Sink} = 100mA	--	1.1	--	Ω

13 Typical Application Circuit

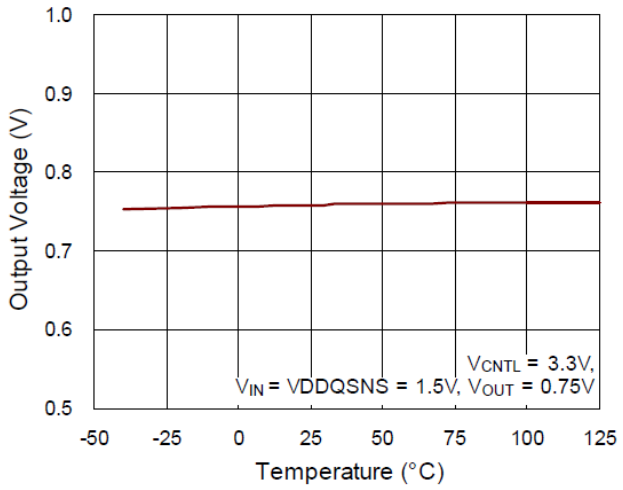


14 Timing Diagram

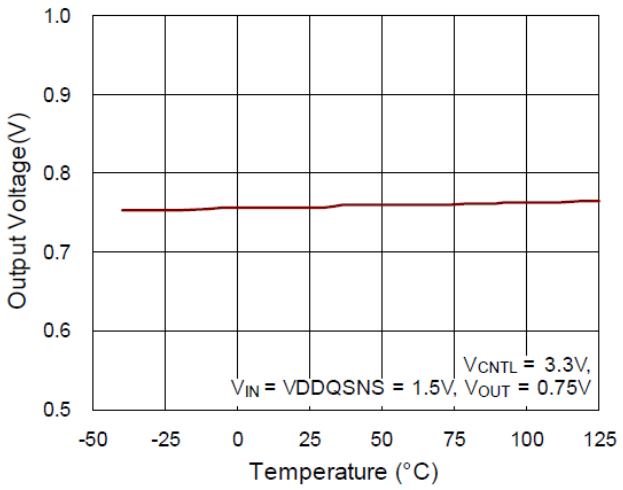


15 Typical Operating Characteristics

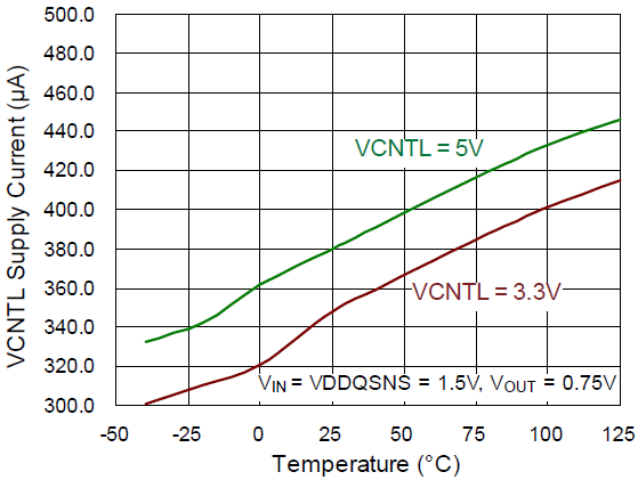
Output Voltage vs. Temperature



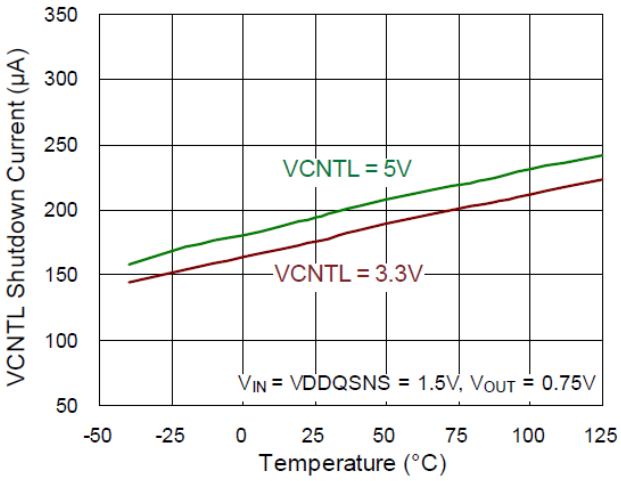
REFOUT Voltage vs. Temperature



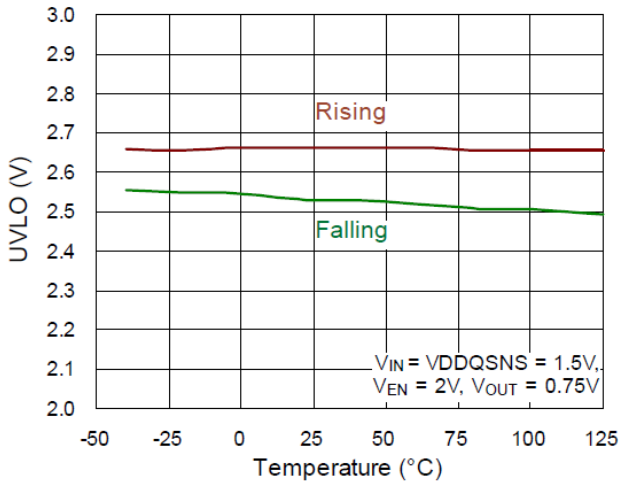
VCNTL Supply Current vs. Temperature



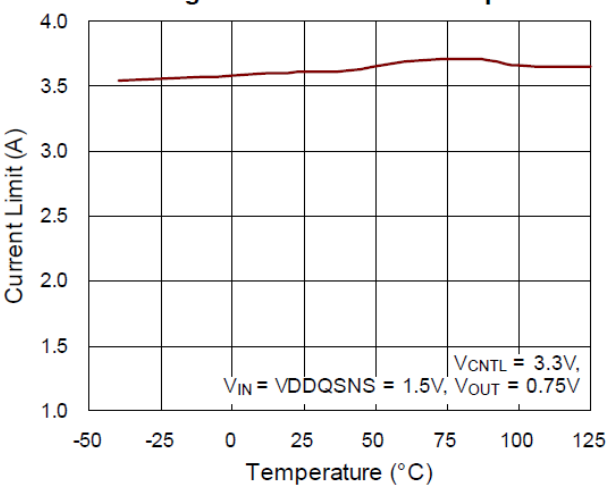
VCNTL Shutdown Current vs. Temperature



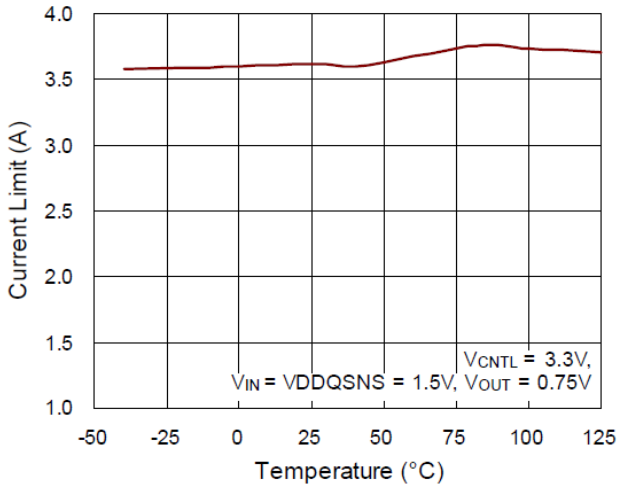
UVLO vs. Temperature



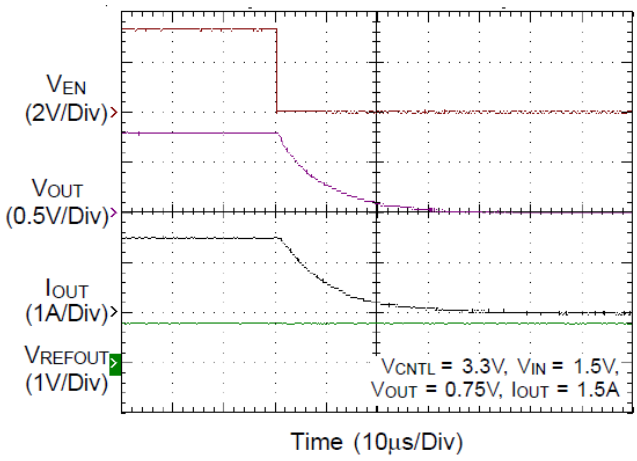
Sourcing Current Limit vs. Temperature



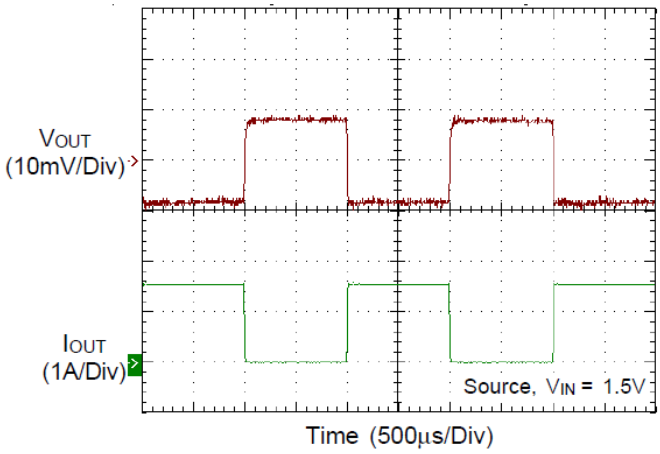
Sinking Current Limit vs. Temperature



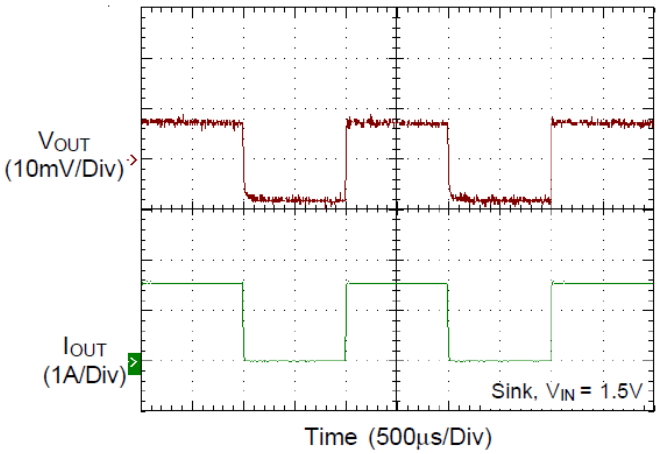
Power Off from EN



0.75V_{OUT} @ 1.5A Transient Response



0.75V_{OUT} @ 1.5A Transient Response



16 Operation

16.1 Supply Voltage

The RT9614L can operate with VCC = 5V or VCC = 12V, supporting various application fields such as NB or desktop systems. A higher VCC provides a higher driving voltage for UGATE and LGATE. In terms of efficiency, the higher driving voltage leads to higher driver loss. However, the higher VCC benefits lower conduction loss on MOSFET. Therefore, selecting VCC=12V or 5V is a tradeoff to optimize overall system efficiency.

16.2 Power-On Reset (POR)

To prevent external MOSFETs from turning on when VCC is insufficient to drive the gate drivers, the RT9614L incorporates a POR circuit. This circuit keeps the driver disabled and both high-side and low-side MOSFETs off until VCC reaches to POR rising threshold, typical 4V. As VCC exceeds the POR rising threshold and EN is high, the gate drivers are controlled by the PWM input signal. During power-down, the POR falling threshold is set to 3.5V (typical), with a 500mV hysteresis to prevent false triggering due to slow VCC slew rates.

16.3 PWM Operation Principle

As the EN pin is in high status and VCC is above the POR rising threshold, the gate drive outputs are determined by the PWM input. As shown in the PWM timing diagram (Figure 1, on the rising edge of the PWM signal, the LAGET is forced low and the non-overlap circuit monitors the LGATE voltage. Once the LGATE is lower than 1.1V, the UGATE is turned on after propagation delay. Similarly, on the falling edge of the PWM signal, the UGATE is turned off and the voltage between UGATE and PHASE is monitored. If either PHASE or UGATE-PHASE is lower than 1.1V, LGATE is turned on after a propagation delay to prevent shoot-through current events.

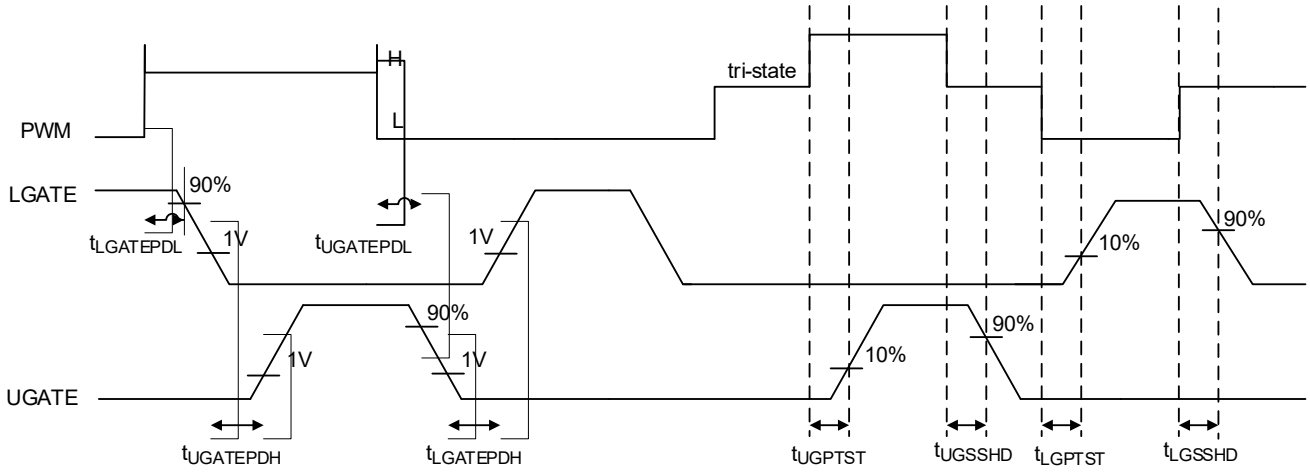


Figure 1. PWM Timing Diagram

16.4 Tri-State PWM Input

When PWM signal enters and remains within the tri-state window, the output drivers are disabled and both MOSFET gates are pulled and held low. Once the PWM signal exits the tri-state window, the output drivers resume normal operation. If the PWM signal is left floating, the pin is kept around 1.8V by the internal divider, providing the PWM controller with a recognizable level.

Table 1 lists the logic relationships among EN, PWM, LGATE, and UGATE signals.

Table 1. Logic of EN, PWM, LGATE, and UGATE Signals

EN	PWM	LGATE	UGATE
Low	High or Low	Low	Low
High	Low	High	Low
High	High	Low	High
High	Tri-state	Low	Low

16.5 Bootstrap Control

To minimize high-side conduction loss, the voltage between BOOT and PHASE should be as close as possible to the supply voltage (VCC). In the RT9614L, the conventional bootstrap diode is replaced by a FET switch with very low voltage drop, which is triggered by LGATE signal. Hence, the bootstrap capacitor is charged by VCC when the low-side MOSFET is turned on, ensuring that V_{CBOOT} is approximately equal to VCC.

16.6 Enable and Disable

The RT9614L features an EN pin for independent sequence control. When the voltage of EN pin rises above its rising threshold (typical 1.3V), both UGATE and LGATE are enabled and controlled by the PWM signal. On the contrary, when the voltage of EN pin falls below its falling threshold, the RT9614L is shut down.

16.7 Pre-Overvoltage Protection

To prevent pre-bias voltage on output or a short circuit across the high-side MOSFET before EN is high, the RT9614L applies a PREOVP function on the PHASE pin. Before EN is high, the PHASE pin voltage is monitored. If the PHASE voltage is higher than the PREOVP threshold (minimum 2.7V), LAGET is forced high to discharge the PHASE voltage. Figure 2 shows the PREOVP operation principle during the power-on period.

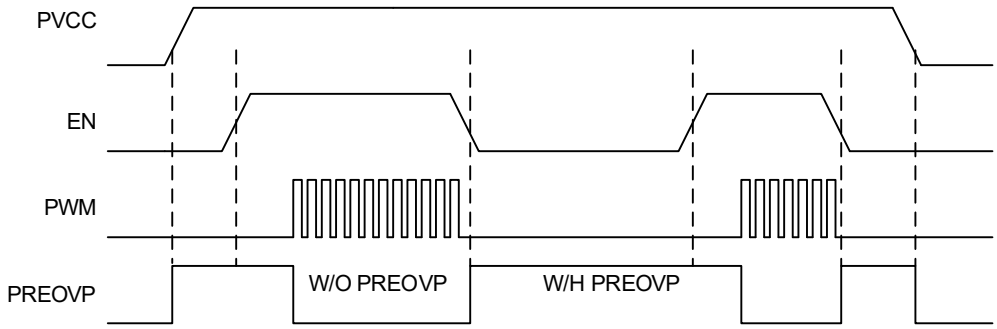


Figure 2. PREOVP Operation Principle

- PREOVP threshold

  2.7V < PREOVP threshold < 3V
- Must follow the power-on sequence

  VCC > VCC_{POR_max} is earlier than EN > EN_{rising}
- Driver should connect to Controller

The driver EN pin should be connected to the controller DRVEN signal. This configuration ensures that the PREOVP function operates correctly during both start-up and PS4.

16.8 Shoot-Through Protection

To prevent overlap between UGATE and LGATE signals which can cause additional power losses or circuit damage, the RT9614L incorporates a non-overlap protection circuit. During the falling edge of the PWM signal, UGATE begins to pull low (after a propagation delay), and the non-overlap circuit monitors the voltages at the PHASE node and the UGATE node (UGATE-PHASE). Before LGATE is pulled high, the non-overlap protection circuit ensures that these monitored voltages have dropped below 1.1V, providing shoot-through protection. Once the monitored voltage is lower than 1.1V, LGATE begins to turn high after the propagation delay time. Similarly, to avoid shoot-through during the rising edge of the PWM signal, LGATE is turned off as PWM begins to pull high. The non-overlap circuit then monitors the LGATE node voltage. If the LAGET is below 1.1V, UGATE is turned on after the propagation delay time.

17 Application Information

(Note 6)

17.1 Driving Capability

The basic requirements for a gate driver for a MOSFET include the ability to source a voltage greater than the MOSFET's gate threshold voltage ($V_{GS(th)}$) and provide sufficient driving capability to achieve the target switching frequency and performance. This section describes the gate driver requirements for an N-channel MOSFET.

The switching behavior of a MOSFET is affected by its parasitic capacitances: gate-to-source (C_{GS}), gate-to-drain (C_{GD}), and drain-to-source (C_{DS}). During the MOSFET turn-on and turn-off transitions, C_{GD} and C_{GS} are charged or discharged through the gate. Hence, the gate driver of MOSFET must consider the variations in these parasitic capacitors.

The MOSFET datasheet typically specifies these capacitances as follows:

$C_{ISS} = C_{GS} + C_{GD}$

$C_{OSS} = C_{GD} + C_{DS}$

$C_{RSS} = C_{GD}$

Figure 3 shows the equivalent circuit of the high-side MOSFET during the turn-on transition.

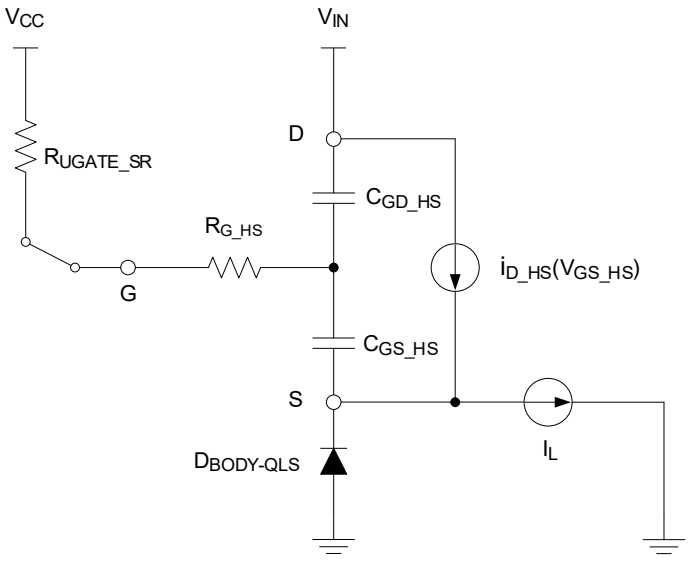


Figure 3. The Equivalent Circuit of High-Side MOSFET During Turn-On Transition

The turn-on transition of the high-side MOSFET can be divided into 5 intervals, as shown in Figure 4. During interval t_{1_HS} and t_{2_HS}, the gate-to-source voltage and the driving current can be expressed as follows:

$$V_{GS\_HS}(t) = V_{CC} \times \left(1 - e^{\frac{-t}{(R_{UGATE\_SR} + R_{G\_HS})C_{ISS\_HS}}}\right)$$

$$i_{g\_HS}(t) = \frac{V_{CC}}{\left(R_{UGATE\_SR} + R_{G\_HS}\right)} \times e^{\frac{-t}{(R_{UGATE\_SR} + R_{G\_HS})C_{ISS\_HS}}}$$

The interval t_{1_HS} and t_{2_HS} are defined as follows:

$$t_{1\_HS} = (R_{UGATE\_SR} + R_{G\_HS}) \times C_{ISS\_HS} \times \ln\left(\frac{V_{CC}}{V_{CC} - V_{TH\_HS}}\right)$$

$$t_{2\_HS} = (R_{UGATE\_SR} + R_{G\_HS}) \times C_{ISS\_HS} \times \ln\left(\frac{V_{CC} - V_{TH\_HS}}{V_{CC} - V_{GP\_HS}}\right)$$

When V_{GS_HS} reaches V_{GP_HS}, the MOSFET enters to miller plateau region. In this interval, the driving current is primarily used to discharge C_{GD}_HS, facilitating a rapid voltage change across V_{DS_HS}. The driving current during interval t_{3_HS} can be expressed as follows:

$$i_{g\_HS}(t) = \frac{V_{CC} - V_{GP\_HS}}{R_{UGATE\_SR} + R_{G\_HS}}$$

The t_{3_HS} can be calculated as:

$$t_{3\_HS} = \frac{V_{IN}}{V_{CC} - V_{GP\_HS}} \times (R_{UGATE\_SR} + R_{G\_HS}) \times C_{GD\_HS}$$

Finally, the V_{GS_HS} is continuously charged from V_{GP_HS} to approximately 0.9 x VCC, at which point the high-side MOSFET is fully turned on. The V_{GS_HS} during interval t_{4_HS} can be expressed as follows:

$$V_{GS\_HS}(t) =$$

$$(V_{GP\_HS} - V_{CC}) \times e^{\frac{-t}{(R_{UGATE\_SR}+R_{G\_HS})C_{ISS\_HS}}} + V_{CC}$$

The t_{4_HS} can be calculated as follows:

$$t_{4\_HS} = (R_{UGATE\_SR} + R_{G\_HS}) \times C_{ISS\_HS} \times \ln\left(\frac{V_{CC} - V_{GP\_HS}}{0.1V_{CC}}\right)$$

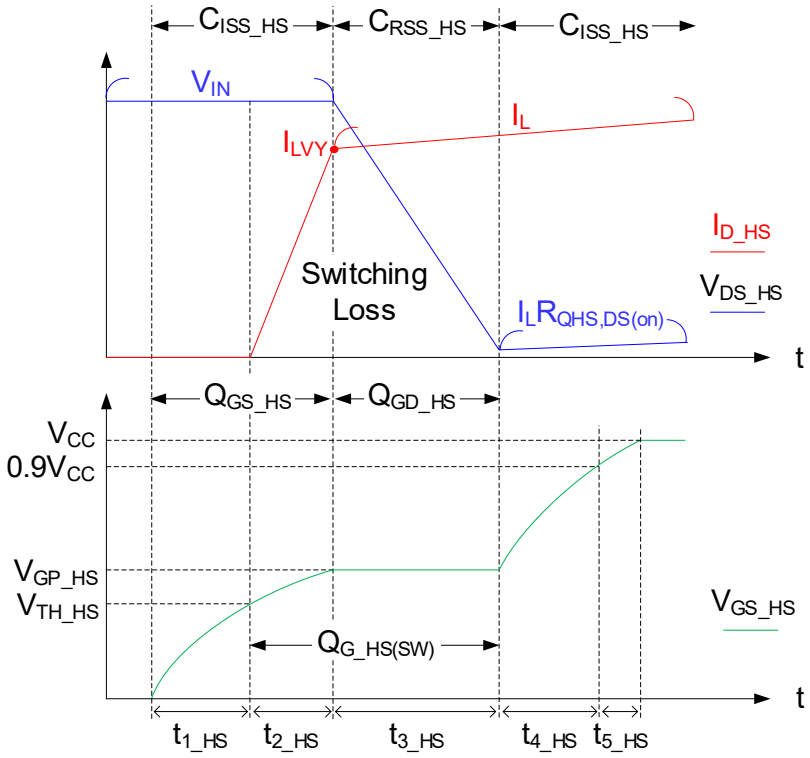


Figure 4. Timing Interval of High-Side MOSFET During Turn-On Transition

Figure 5 illustrates the equivalent circuit of the high-side MOSFET during turn-off transition.

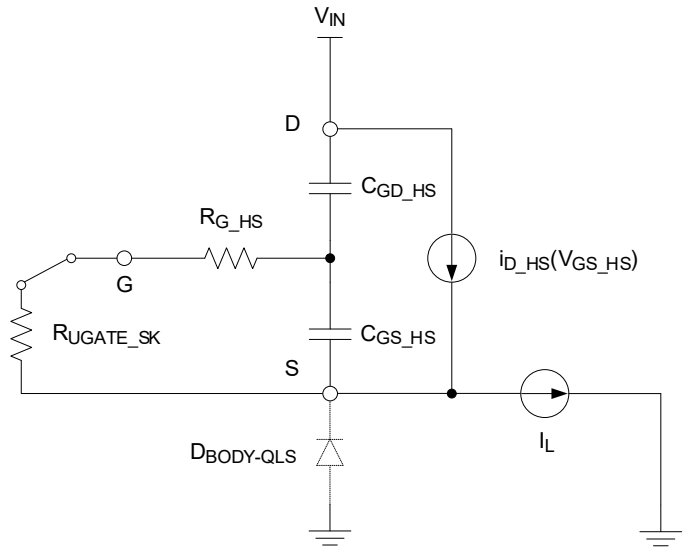


Figure 5. The Equivalent Circuit of High-Side MOSFET in Turn-off Transition

Referring to Figure 6, the turned-off transition of the high-side MOSFET can be separated into 5 regions, and the gate-to-source voltage and driving current in interval t_{6_HS} and t_{7_HS} can be derived as follows:

$$V_{GS\_HS}(t) = V_{CC} \times e^{\frac{-t}{(R_{UGATE\_SK}+R_{G\_HS})C_{ISS\_HS}}}$$

$$i_{g\_HS}(t) = \frac{-V_{GS\_HS}(t)}{R_{UGATE\_SK}+R_{G\_HS}}$$

The symbol “minus” indicates the inverse direction of the driving current. The intervals t_{6_HS} and t_{7_HS} are defined as follows:

$$t_{6\_HS} = (R_{UGATE\_SK}+R_{G\_HS}) \times C_{ISS\_HS} \times \ln\left(\frac{10}{9}\right)$$

$$t_{7\_HS} = (R_{UGATE\_SK}+R_{G\_HS}) \times C_{ISS\_HS} \times \ln\left(0.9\frac{V_{CC}}{V_{GP\_HS}}\right)$$

When V_{GS_HS} falls to V_{GP_HS}, the MOSFET enters the miller plateau region. In this interval, the driving current is primarily used to charge C_{GD_HS}. The driving current during interval t_{8_HS} can be expressed as follows:

$$i_{g\_HS}(t) = \frac{-V_{GP\_HS}}{R_{UGATE\_SK}+R_{G\_HS}}$$

The symbol “minus” indicates the inverse direction of the driving current. The interval t8_HS can be calculated as follows:

$$t_{8\_HS} = \frac{V_{IN}}{V_{GP\_HS}} \times (R_{UGATE\_SK}+R_{G\_HS}) \times C_{GD\_HS}$$

Finally, the V_{GS_HS} further decreases from V_{GP_HS} to V_{TH_HS}, and the high-side MOSFET is fully turned off. The gate-to-source voltage (V_{GS_HS}) during interval t_{9_HS} can be expressed by the following equation:

$$V_{GS\_HS}(t) = V_{GP\_HS} \times e^{\frac{-t}{(R_{UGATE\_SK}+R_{G\_HS})C_{ISS\_HS}}}$$

The interval t_{9_HS} can be calculated as follows:

$$t_{9\_HS} = \left(R_{UGATE\_SK} + R_{G\_HS}\right) \times C_{ISS\_HS} \times \ln\left(\frac{V_{GP\_HS}}{V_{TH\_HS}}\right)$$

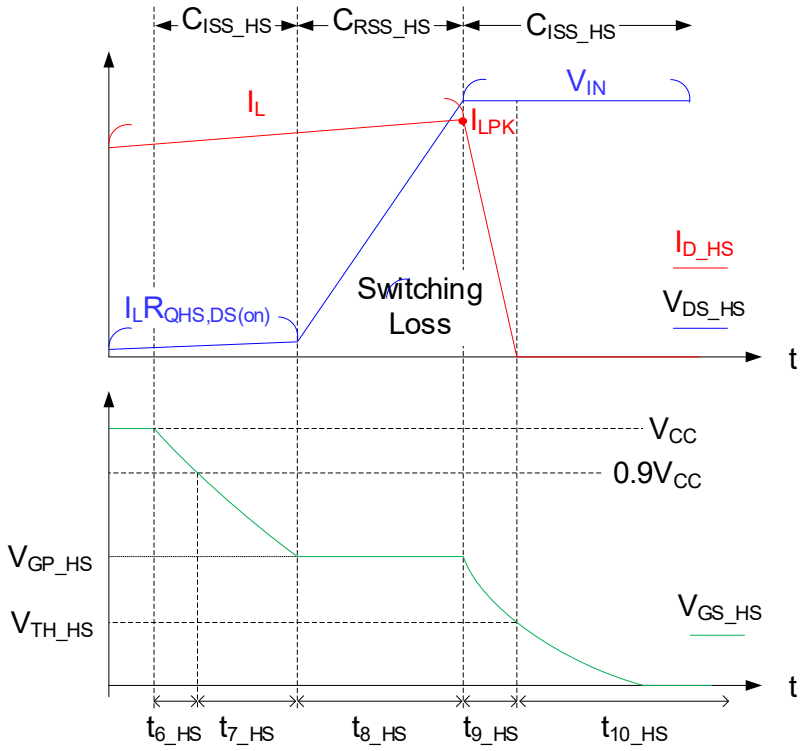


Figure 6. Timing Interval of High-Side MOSFET During Turn-off Transition.

Here is an example of a driving capability calculation for a synchronous buck converter, where both input voltage and driver voltage are 12V (V_{IN} = 12V, V_{CC} = 12V). The selected high-side MOSFET is the CSD17301Q5A, with the following parameters: C_{ISS} = 2660pF, C_{GD} = 80pF, V_{TH} = 1.1V, V_{GP} = 1.32V, and R_G = 1.3Ω.

Therefore, the maximum driving current for the CSD17301Q5A during the turn-on period can be calculated as follows:

$$I_{g\_HS\_max} = i_{g\_HS}(0)$$

$$= \frac{V_{CC}}{\left(R_{UGATE\_SR} + R_{G\_HS}\right)} \times e^{\frac{-0}{(R_{UGATE\_SR}+R_{G\_HS})C_{ISS\_HS}}}$$

$$= \frac{12}{1.7+1.3} \times e^{0} = 4A$$

Furthermore, the timing intervals of the turn-on transition can be expressed using the following equations:

$$t_{1\_HS} = \left(R_{UGATE\_SR} + R_{G\_HS}\right) \times C_{ISS\_HS} \times \ln\left(\frac{V_{CC}}{V_{CC} - V_{TH\_HS}}\right)$$

$$= (1.7+1.3) \times 2660p \times \ln\left(\frac{12}{12-1.1}\right) = 0.77ns$$

$$t_{2\_HS} = \left(R_{UGATE\_SR} + R_{G\_HS}\right) \times C_{ISS\_HS} \times \ln\left(\frac{V_{CC} - V_{TH\_HS}}{V_{CC} - V_{GP\_HS}}\right)$$

$$= (1.7+1.3) \times 2660p \times \ln\left(\frac{12-1.1}{12-1.32}\right) = 0.16ns$$

$$t_{3\_HS} = \frac{V_{IN}}{V_{CC} - V_{GP\_HS}} \times \left(R_{UGATE\_SR} + R_{G\_HS}\right) \times C_{GD\_HS}$$

$$= \frac{12}{12-1.32} \times (1.7+1.3) \times 80p = 0.27ns$$

$$t_{4\_HS} = \left(R_{UGATE\_SR} + R_{G\_HS}\right) \times C_{ISS\_HS} \times \ln\left(\frac{V_{CC} - V_{GP\_HS}}{0.1V_{CC}}\right)$$

$$= (1.7+1.3) \times 2660p \times \ln\left(\frac{12-1.32}{0.1 \times 12}\right) = 17.44ns$$

Finally, fully turning on the CSD17301Q5A requires approximately 18.64ns when using the RT9614L as the gate driver for the MOSFET.

$$t_{TOTAL\_ON} = t_{1\_HS} + t_{2\_HS} + t_{3\_HS} + t_{4\_HS}$$

$$= 0.77n+0.16n+0.27n+17.44n = 18.64ns$$

As operating in turn-off region, the maximum of driving current for CSD17301Q5A is defined.

$$i_{g\_HS\_max} = i_{g\_HS}(0)$$

$$= \frac{-v_{GS\_HS}(0)}{R_{UGATE\_SK} + R_{G\_HS}} = \frac{-12}{1.4+1.3} = -4.44A$$

Furthermore, the timing intervals of the turn-off transition can be expressed by the following equations:

$$t_{6\_HS} = \left(R_{UGATE\_SK} + R_{G\_HS}\right) \times C_{ISS\_HS} \times \ln\left(\frac{10}{9}\right)$$

$$= (1.4+1.3) \times 2660p \times \ln\left(\frac{10}{9}\right) = 0.76ns$$

$$t_{7\_HS} = \left(R_{UGATE\_SK} + R_{G\_HS}\right) \times C_{ISS\_HS} \times \ln\left(0.9\frac{V_{CC}}{V_{GP\_HS}}\right)$$

$$= (1.4+1.3) \times 2660p \times \ln\left(0.9\frac{12}{1.32}\right) = 15.1ns$$

$$t_{8\_HS} = \frac{V_{IN}}{V_{GP\_HS}} \times \left(R_{UGATE\_SK} + R_{G\_HS}\right) \times C_{GD\_HS}$$

$$= \frac{12}{1.32} \times (1.4+1.3) \times 80p = 1.96ns$$

$$t_{9\_HS} = \left(R_{UGATE\_SK} + R_{G\_HS}\right) \times C_{ISS\_HS} \times \ln\left(\frac{V_{GP\_HS}}{V_{TH\_HS}}\right)$$

$$= (1.4+1.3) \times 2660p \times \ln\left(\frac{1.32}{1.1}\right) = 1.31ns$$

The minimum turn-off time required for the CSD17301Q5A when using the RT9614L gate driver can be expressed as follows:

$$t_{TOTAL\_OFF} = t_{6\_HS} + t_{7\_HS} + t_{8\_HS} + t_{9\_HS}$$

$$= 0.76n+15.1n+1.96n+1.31n = 19.13ns$$

Selecting a proper MOSFET that is well-matched with the RT9614L gate driver can reduce the MOSFET turn-on and turn-off intervals. This improvement enhances system efficiency and enables higher switching frequencies.

17.2 Power Loss of MOSFET

The synchronous buck converter is widely used in low-voltage and high-current applications, such as CPU peripherals. Therefore, achieving high efficiency is always a key concern. To improve overall system efficiency, it is important to analyze and break down the power losses of each selected device. The section introduces the power losses on MOSFET, which can be divided into two categories: conduction loss and switching loss.

The conduction loss of the high-side MOSFET can be represented as follows:

$$P_{COND(QHS)} = I_{D(QHS,RMS)}^2 \times R_{QHS,DS(on)}$$

The conduction loss of the low-side MOSFET can be calculated using the following equation:

$$P_{COND(QLS)} = I_{D(QLS,RMS)}^2 \times R_{QLS,DS(on)}$$

$$+ V_{F\_LS} \times \left(I_{LPK} \times t_{LGATEPDH} + I_{LVY} \times t_{HGATEPDH}\right) \times f_S$$

Where:

$I_{D(QHS,RMS)}$ is the RMS current of the high-side MOSFET.

$R_{QHS,DS(ON)}$ is the on-resistance of the high-side MOSFET.

$I_{D(QLS,RMS)}$ is the RMS current of the low-side MOSFET.

$R_{QLS,DS(ON)}$ is the on-resistance of the low-side MOSFET.

V_{F_LS} is the forward voltage drop of the low-side MOSFET body diode.

I_{LPK} is the peak current of the inductor.

I_{LVY} is the valley current of the inductor. When the buck converter operates in DEM, the I_{LVY} is equal to zero.

$t_{LGATEPDH}$ and $t_{UGATEPDH}$ are the propagation delay in the gate driver of the MOSFET.

f_S is the switching frequency.

17.3 Driver Loss

The driver loss can be defined as follows:

$$P_{LOSS\_GDRV\_HS} = Q_{G\_HS} \times V_{CC} \times f_S$$

$$P_{LOSS\_GDRV\_LS} = Q_{G\_LS} \times V_{CC} \times f_S$$

Where

Q_{G_HS} is the total gate charge of the high-side MOSFET.

Q_{G_LS} is the total gate charge of the low-side MOSFET.

The switching loss of the high-side and low-side MOSFETs can be further classified into turn-on/turn-off losses, C_{OSS} loss, and reverse recovery loss caused by the MOSFET body diode.

17.4 High-Side MOSFET

Referring to the conduction loss of the high-side MOSFET and the conduction loss of the low-side MOSFET in Power Loss of MOSFET, the turn-on switching loss of the high-side MOSFET can be derived as follows:

$$P_{LOSS,HS\_ON} = \frac{1}{2} \times V_{IN} \times I_{LVY} \times \left(t_{2\_HS} + t_{3\_HS}\right) \times f_S$$

Referring to the conduction loss of the high-side MOSFET and the conduction loss of the low-side MOSFET in Power Loss of MOSFET, the turn-off switching loss of the high-side MOSFET can be derived as follows:

$$P_{LOSS,HS\_OFF} = \frac{1}{2} \times V_{IN} \times I_{LPK} \times \left(t_{8\_HS} + t_{9\_HS}\right) \times f_S$$

Additionally, since C_{OSS} is charged and discharged during every switching cycle, the C_{OSS} loss of the high-side MOSFET must be considered. The calculation of this loss is as follows:

$$P_{LOSS,HS\_COSS} = \frac{1}{2} \times C_{OSS\_HS} \times V_{IN}^2 \times f_S$$

17.5 Low-Side MOSFET

The turn-on switching loss of the low-side MOSFET can be obtained as follows:

$$P_{LOSS,LS\_ON} = \frac{1}{2} \times V_{F\_LS} \times I_{LPK} \times \left(t_{2\_LS} + t_{3\_LS}\right) \times f_S$$

where V_F is the forward voltage drop of the low-side MOSFET body diode.

The intervals t_{2_LS} and t_{3_LS} of the turn-on process for the low-side MOSFET are defined as follows:

$$t_{2\_LS} = \left(R_{LGATE\_SR} + R_{G\_LS}\right) \times C_{ISS\_LS} \times \ln\left(\frac{V_{CC} - V_{TH\_LS}}{V_{CC} - V_{GP\_LS}}\right)$$

$$t_{3\_LS} = \frac{V_{F\_LS}}{V_{CC} - V_{GP\_LS}} \times \left(R_{LGATE\_SR} + R_{G\_LS}\right) \times C_{GD\_LS}$$

The turn-off switching loss of the low-side MOSFET can be obtained as follows:

$$P_{LOSS,LS\_OFF} = \frac{1}{2} \times V_{F\_LS} \times I_{LVY} \times \left(t_{8\_LS} + t_{9\_LS}\right) \times f_S$$

The intervals t_{8_LS} and t_{9_LS} of the turn-off process for the low-side MOSFET are defined as follows:

$$t_{8\_LS} = \frac{V_{F\_LS}}{V_{GP\_LS}} \times \left(R_{LGATE\_SK} + R_{G\_LS}\right) \times C_{GD\_LS}$$

$$t_{9\_LS} = \left(R_{LGATE\_SK} + R_{G\_LS}\right) \times C_{ISS\_LS} \times \ln\left(\frac{V_{GP\_LS}}{V_{TH\_LS}}\right)$$

The C_{OSS} loss of the low-side MOSFET is typically much smaller and is generally ignored. However, for completeness in loss calculations, it can be estimated using the following equation:

$$P_{LOSS,LS\_COSS} = \frac{1}{2} \times C_{OSS\_LS} \times V_{F\_LS}^{2} \times f_S$$

Additionally, the reverse recovery loss occurs in the body diode of the low-side MOSFET when the high-side MOSFET turns on and the low-side MOSFET is in the off-state. The reverse recovery loss Can be calculated as follows:

$$P_{LOSS,LS\_RR} = Q_{RR\_LS} \times V_{IN} \times f_S$$

where Q_{RR_LS} is the reverse recovery charge of the low-side MOSFET body diode.

By understanding the power loss distribution in the MOSFETs, system efficiency can be improved and overall performance can be enhanced.

17.6 Bootstrap Capacitor Selection

To reduce power consumption, the transitional bootstrap circuit is replaced by an integrated FET sin the RT9614L, saving board space. Now, only an external capacitor (C_{BOOT}) needs to be connected between BOOT and PHASE. To effectively turn on the high-side MOSFET, the stored energy in C_{BOOT} must be greater than the total gate charge of the high-side MOSFET.

The value of the bootstrap capacitor is defined by the following equation:

$$C_{BOOT} \geq \frac{Q_g}{\Delta V_{BOOT}}$$

where

Qg: Total gate charge

$\Delta V_{BOOT} = V_{CC} - V_{TH}$

ΔV_{BOOT}: Maximum allowable voltage drop on the bootstrap capacitor

V_{CC}: Supply voltage of the gate driver

V_{TH}: Threshold voltage of the high-side MOSFET

The theoretically C_{BOOT} is illustrated in Figure 7. Additionally, when selecting C_{BOOT}, consider DC de-rating, AC de-rating, and thermal de-rating effects. It is recommended to use a ceramic capacitor for C_{BOOT} due to its low ESR and good local de-coupling characteristics.

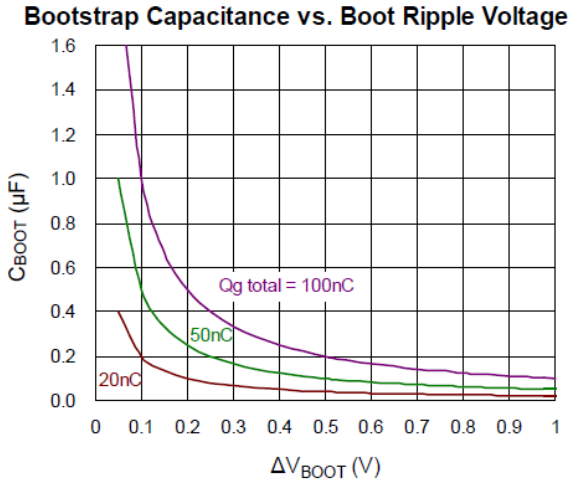


Figure 7. Bootstrap Capacitance vs. Boot Ripple Voltage

17.7 Power Dissipation

The power dissipation is directly related to the switching frequency and the total gate charge of the selected MOSFET. Accurate calculation of gate driver power dissipation is essential to ensure safe operation. In general designs, the power dissipation should not exceed the specified maximum value, and the operating junction temperature remains below 125°C.

Figure 8 shows the power dissipation test circuit, where CL and CU are the load capacitors for LGATE and UGATE, respectively. The bootstrap capacitor value is 0.1µF. Figure 9 presents the power dissipation curves, illustrating that power dissipation is proportional to both switching frequency and load capacitance. Higher operating frequencies and larger load capacitances result in increased power dissipation.

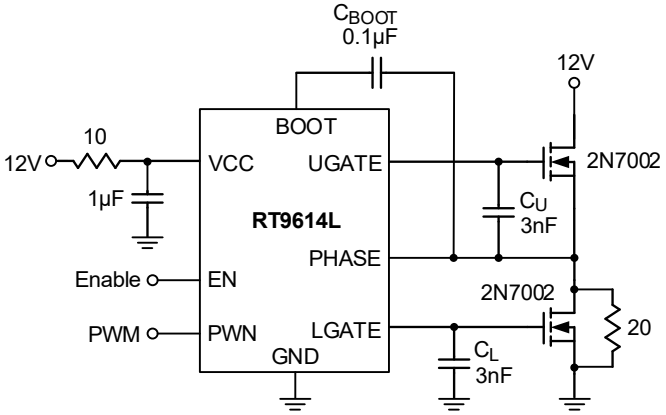


Figure 8. Power Dissipation Test Circuit

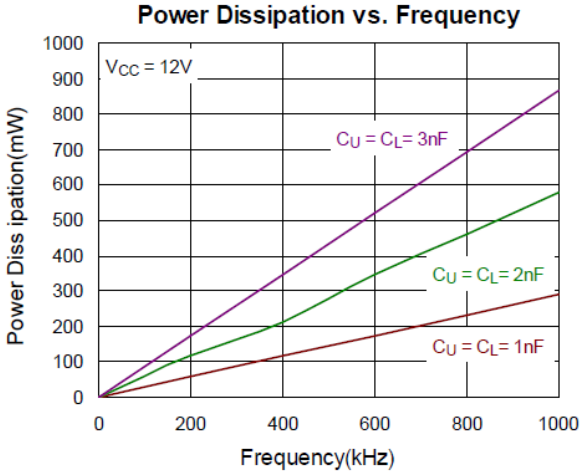


Figure 9. Power Dissipation vs. Frequency

17.8 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_J(MAX)$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-8L 3x3, the thermal resistance, θ_{JA}, is 31°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C − 25°C) / (31°C/W) = 3.22W for a WDFN-8L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 10 allows the user to see the effect of rising ambient temperature on the maximum power dissipation.

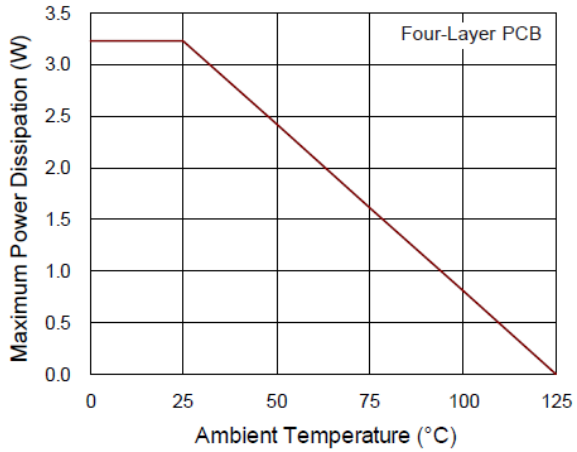


Figure 10. Derating Curve of Maximum Power Dissipation

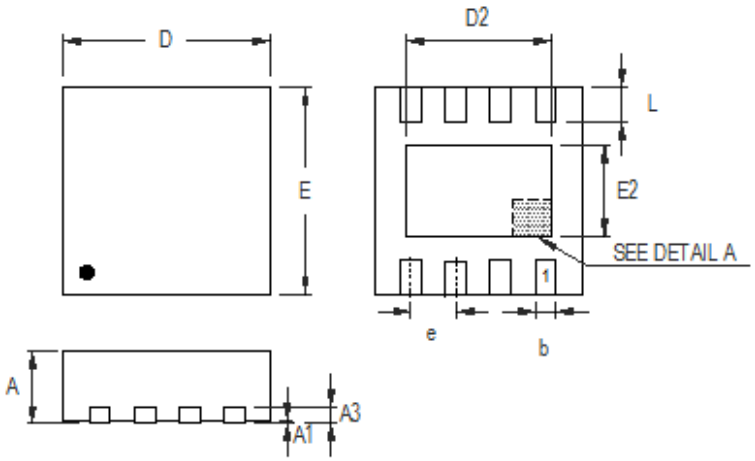
17.9 Layout Consideration

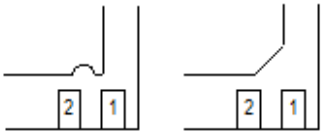
The parasitic inductance of PCB and power device can affect the switching characteristics to aggravate PHASE ringing and further decrease efficiency. To improve these drawbacks, the following layout guidelines must be considered:

- Place the RT9614L as close as possible to the MOSFETs to minimize parasitic components between devices.
- Place the VCC bypass capacitor as close as possible to the VCC pin. This helps eliminate high-frequency noise generated during high/low-side MOSFET switching.
- Place the bootstrap capacitor as close as possible to the BOOT and PHASE pins to minimize parasitic inductance and reduce the high-current trace path, including the bootstrap capacitor, GND, VCC bypass capacitor, and the drain-to-source path of the low-side MOSFET.
- Keep the gate driver paths (UGATE, PHASE, LGATE, GND) short and wide to reduce parasitic impedance. The UGATE and PHASE traces for the high-side driver should be directly connected to the gate and source terminals of the high-side MOSFET. The PHASE trace for the gate driver should be independent from the high-current path. Apply the same rule for LGATE and GND traces on the low-side driver.
- Place the source terminal of the high-side MOSFET as close as possible to the drain terminal of the low-side MOSFET. Similarly, keep the connection between the source terminal of the low-side MOSFET and GND wide and short to minimize the impedance between the high/low-side MOSFET and GND.
- If layers changes are required, use at least two vias to reduce parasitic inductance.
- Avoid routing the PWM and enable traces close to the switching node, as they may be susceptible to noise interference from high dV/dt.

Note 6. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

18 Outline Dimension





DETAIL A

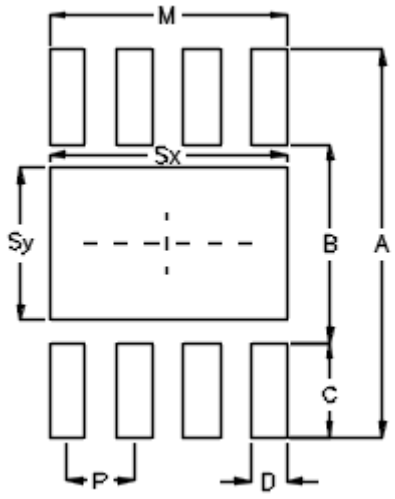
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	2.950	3.050	0.116	0.120
D2	2.100	2.350	0.083	0.093
E	2.950	3.050	0.116	0.120
E2	1.350	1.600	0.053	0.063
e	0.650		0.026	
L	0.425	0.525	0.017	0.021

W-Type 8L DFN 3x3 Package

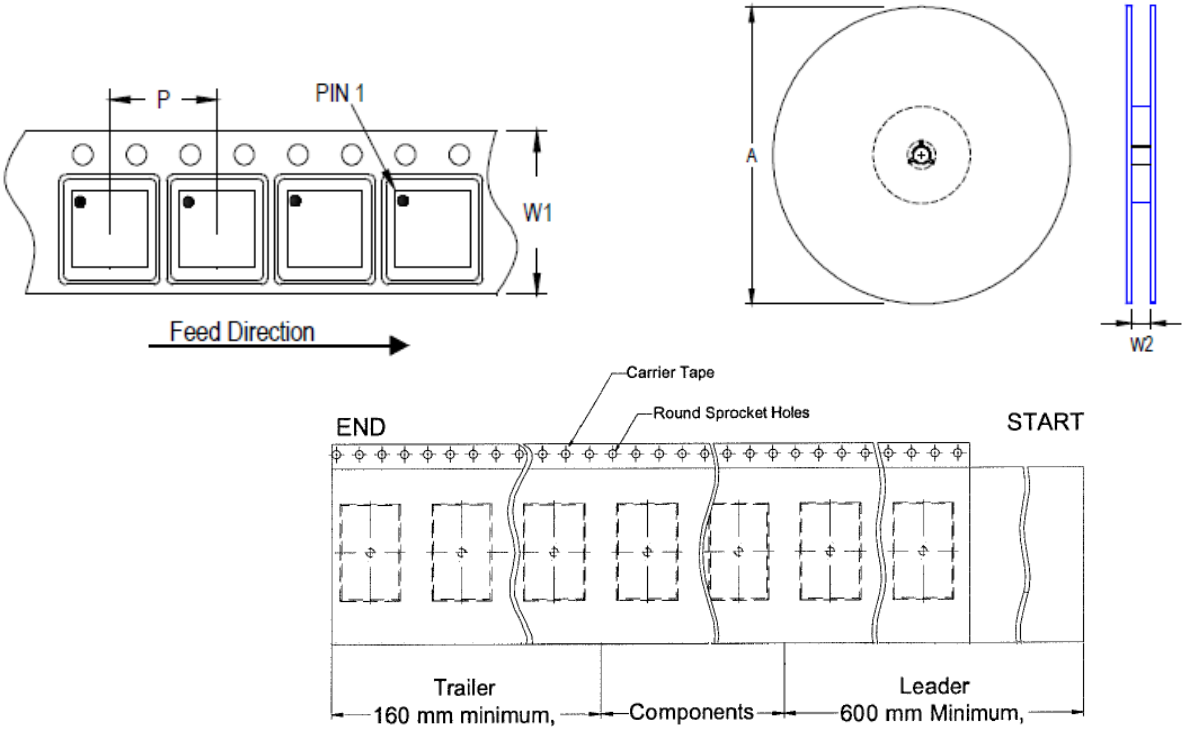
19 Footprint Information



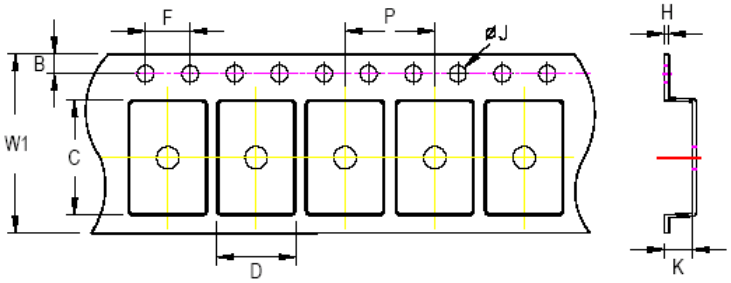
Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN3*3-8	8	0.65	3.80	1.94	0.93	0.35	2.30	1.50	2.30	±0.05

20 Packing Information

20.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 3x3	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Taiyuan 1st St., Zhubei City,
Hsinchu County 302082, Taiwan (R.O.C.)
Tel: 886-3-5526-789

21 Datasheet Revision History

Version	Date	Description
00	2026/3/19	First Edition
01	2026/8/24	Functional Pin Description