RICHTEK®

RT9624D

Single-Phase Synchronous Rectified Buck MOSFET Driver

1 General Description

The RT9624D is a high-frequency, synchronous rectified, single-phase MOSFET driver designed for both standard MOSFET driving applications and high-performance CPU VR solutions.

The RT9624D can be supplied from 4.5V to 13.2V and supports power stage VIN voltages from 5V to 24V. An internal power switch is integrated to replace external bootstrap diode.

Capable of efficiently supporting switching frequencies up to 500kHz, the RT9624D features both UGATE and LGATE driving circuits, making it ideal for synchronous rectified DC-DC converter applications. The device incorporates a robust shoot-through protection mechanism to prevent simultaneous conduction of the high-side and low-side MOSFETs. Additionally, the RT9624D offers a tri-state PWM input with a shutdown function, allowing the driver to force both UGATE and LGATE outputs low for system protection.

The RT9624D is available in a compact WDFN-8SL 2x2 package. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

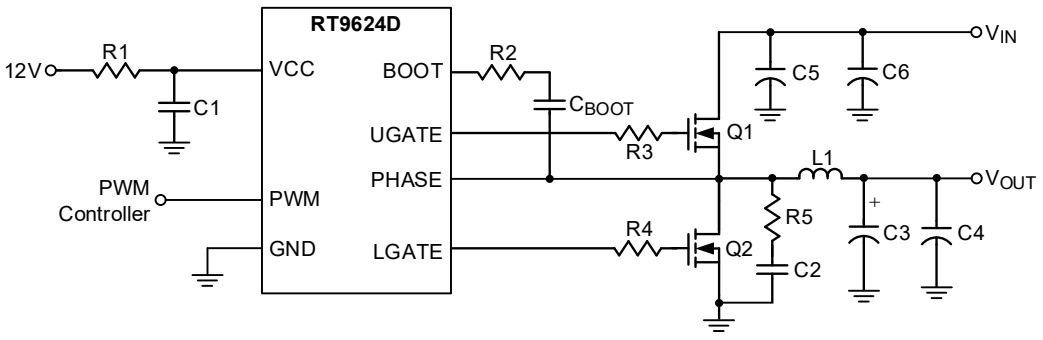
2 Features

- **Drive Two N-MOSFETs**
- **Shoot-Through Protection**
- **Embedded Bootstrap Switch**
- **Support High Switching Frequency**
- **Fast Output Rising Time**
- **Tri-State PWM Input for Output Shutdown**
- **Compact 8-Lead WDFN Package**

3 Applications

- Core Voltage Supplies for Desktop, Motherboard CPUs
- High-Frequency, Low-Profile DC-DC Converters
- High-Current, Low-Voltage DC-DC Converters
- Core Voltage Supplies for GFX Cards

4 Simplified Application Circuit



5 Ordering Information

RT9624D□□

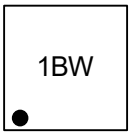
Package Type(1)
QWA: WDFN-8SL 2x2 (W-Type)
(Exposed Pad: Option 1)

Lead Plating System
G: Richtek Green Policy Compliant(2)

Note 1.

- Marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicates that Richtek products are Richtek Green Policy compliant.

6 Marking Information



1B: Product Code
W: Date Code

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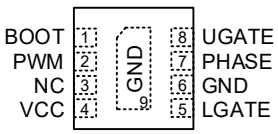
7 Pin Configuration

(TOP VIEW)

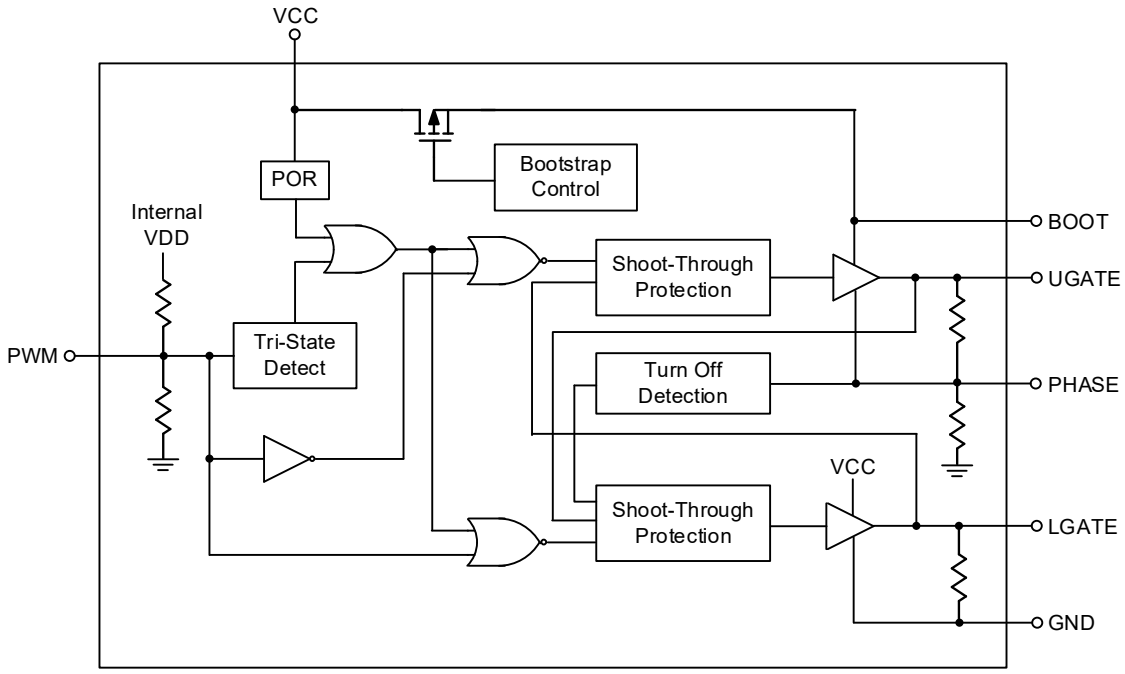


WDFN-8SL 2x2

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap supply for high-side gate driver.
2	PWM	PWM signal input. Connect this pin to the PWM output of the controller.
3	NC	No internal connection.
4	VCC	Supply voltage input.
5	LGATE	Low-side gate driver output. Connect this pin to the Gate of low-side power N-MOSFET.
6, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
7	PHASE	Connect this pin to the source of the high-side N-MOSFET and the drain of the low-side N-MOSFET.
8	UGATE	High-side gate driver output. Connect this pin to the Gate of high-side power N-MOSFET.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, VCC ---------- –0.3V to 15V
- BOOT to PHASE
  - DC ---------- –0.3V to 15V
  - < 60ns ---------- –3V to 25V
- BOOT to GND
  - DC ---------- –0.3V to 45V
  - < 60ns ---------- –20V to 46V
- PHASE to GND
  - DC ---------- –0.3V to 30V
  - < 60ns ---------- –20V to 31V
- UGATE to PHASE
  - DC ---------- –0.3V to 15V
  - < 60ns ---------- –3V to 25V
- UGATE to GND
  - DC ---------- –0.3V to 30V
  - < 60ns ---------- –20V to 31V
- LGATE to GND
  - DC ---------- –0.3V to 15V
  - < 60ns ---------- –3V to 16V
- PWM to GND ---------- –0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-8SL 2x2 ---------- 2.17W
- Package Thermal Resistance (Note 3)
  - WDFN-8SL 2x2, θ_{JA} ---------- 46°C/W
  - WDFN-8SL 2x2, θ_{JC} ---------- 11.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  - HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Voltage, VCC ---------- 4.5V to 13.2V
- Input Voltage, (V_{IN} + VCC) ---------- < 35V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

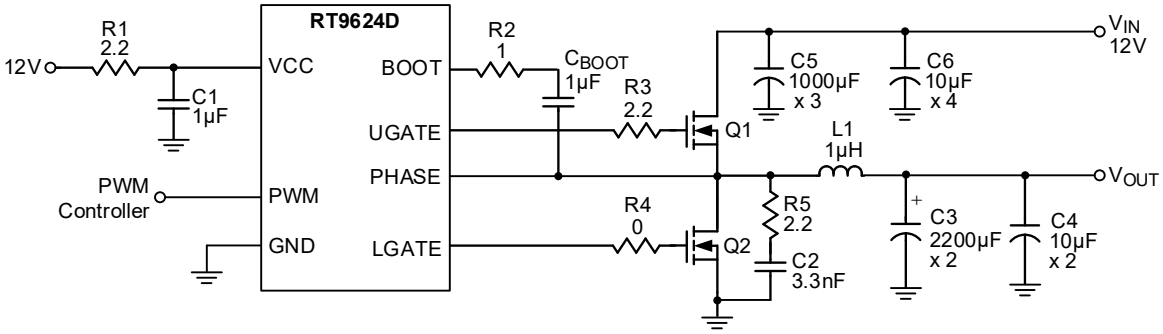
Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

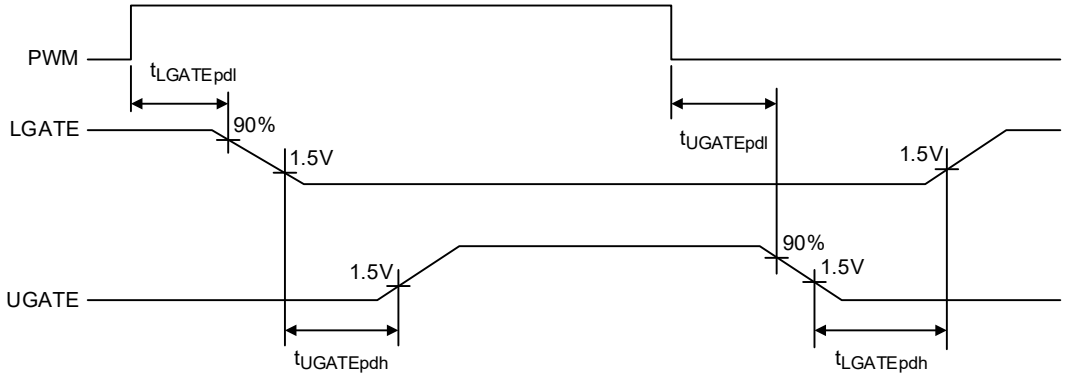
(V_{CC} = 12V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Power Supply Voltage	V_{CC}		4.5	--	13.2	V
Power Supply Current	I_{VCC}	V_{BOOT} = 12V, PWM Input Floating	--	120	--	μA
Power-On Reset (POR)						
POR Rising Threshold	V_{POR_r}	V_{CC} rising	--	4	4.4	V
POR Falling Threshold	V_{POR_f}	V_{CC} falling	3	3.5	--	V
PWM Input						
Maximum Input Current	I_{PWM}	PWM = 0V or 5V	--	160	--	μA
PWM Floating Voltage	V_{PWM_fl}	PWM = Open	--	1.8	--	V
PWM Rising Threshold	V_{PWM_rth}		2.3	2.8	3.2	V
PWM Falling Threshold	V_{PWM_fth}		0.7	1.1	1.4	V
Timing						
UGATE Rising Time	t_{UGATEr}	3nF Load	--	25	--	ns
UGATE Falling Time	t_{UGATEf}	3nF Load	--	12	--	ns
LGATE Rising Time	t_{LGATEr}	3nF Load	--	24	--	ns
LGATE Falling Time	t_{LGATEf}	3nF Load	--	10	--	ns
UGATE Propagation Delay	$t_{UGATEpdh}$	$V_{BOOT} - V_{PHASE}$ = 12V See timing diagram	--	60	--	ns
	$t_{UGATEpdl}$		--	22	--	
LGATE Propagation Delay	$t_{LGATEpdh}$	See timing diagram	--	30	--	ns
	$t_{LGATEpdl}$	See timing diagram	--	8	--	
Output						
UGATE Drive Source	$R_{UGATEsr}$	$V_{BOOT} - V_{PHASE}$ = 12V, I_{Source} = 100mA	--	1.7	--	Ω
UGATE Drive Sink	$R_{UGATEsk}$	$V_{BOOT} - V_{PHASE}$ = 12V, I_{Sink} = 100mA	--	1.4	--	Ω
LGATE Drive Source	$R_{LGATEsr}$	I_{Source} = 100mA	--	1.6	--	Ω
LGATE Drive Sink	$R_{LGATEsk}$	I_{Sink} = 100mA	--	1.1	--	Ω

13 Typical Application Circuit

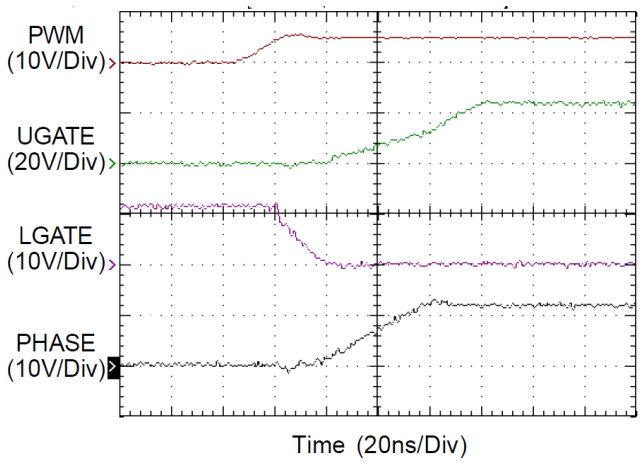


14 Timing Diagram

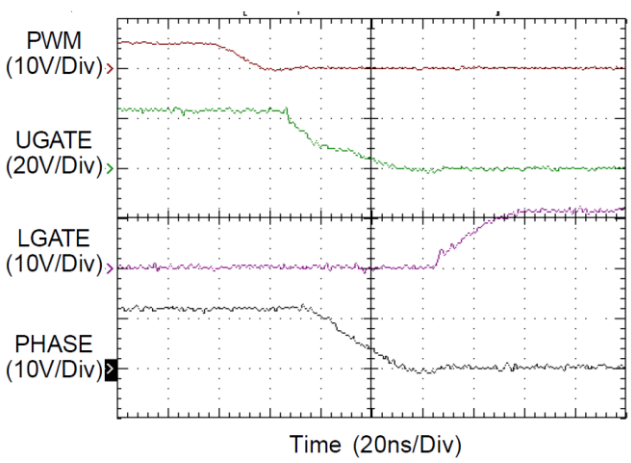


15 Typical Operating Characteristics

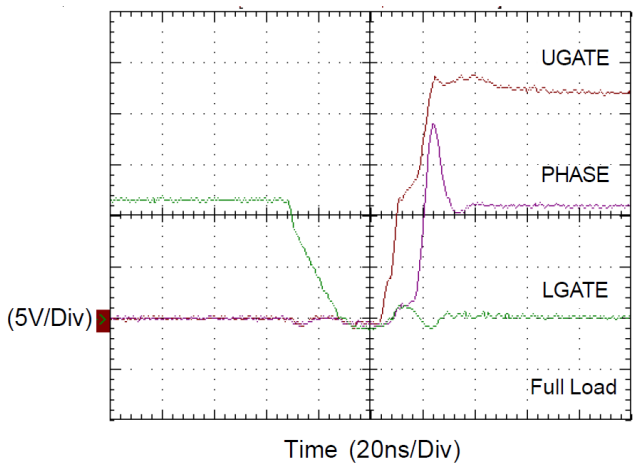
PWM Rising Edge



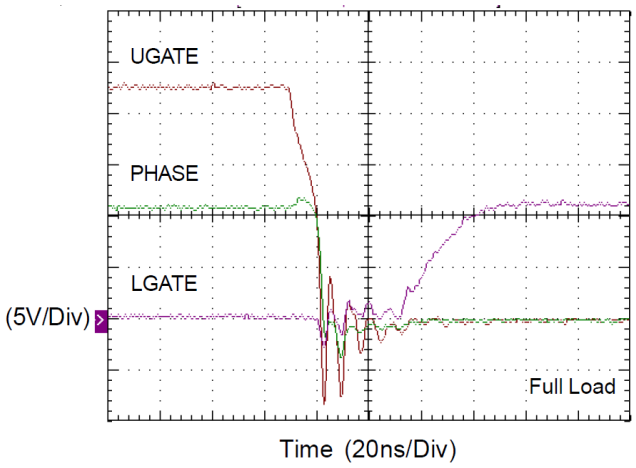
PWM Falling Edge



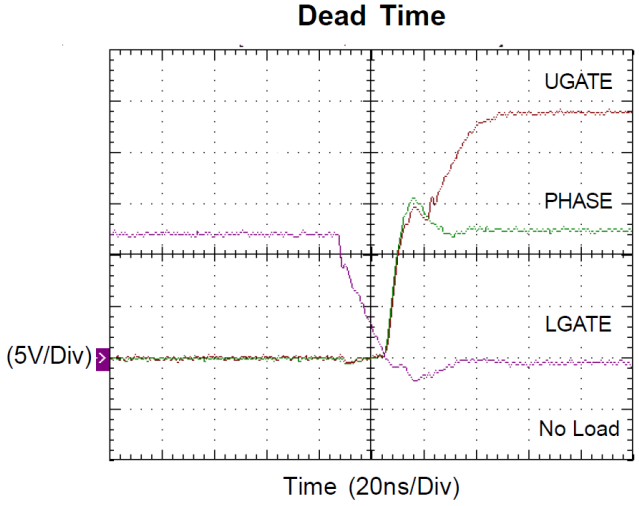
Dead Time



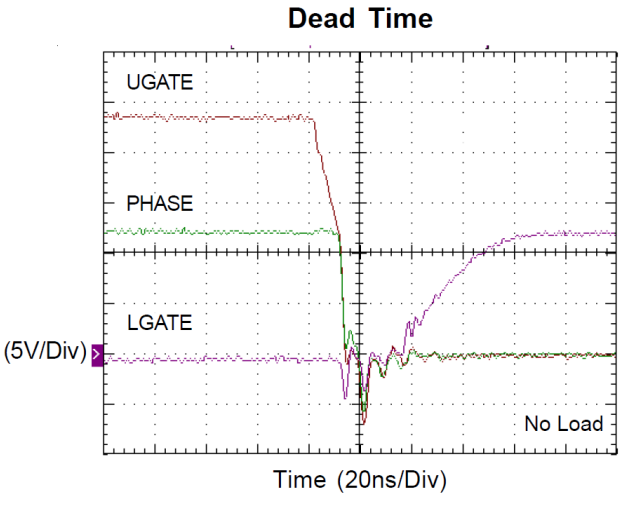
Dead Time



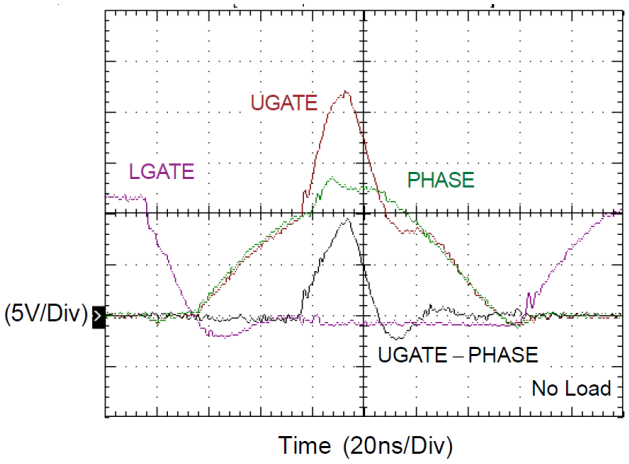
Dead Time



Dead Time



Short Pulse



16 Operation

16.1 POR (Power-On Reset)

The POR block detects the voltage at the VCC pin. When the VCC pin voltage is higher than the POR rising threshold, the POR block output is high. The POR output is low when VCC is less than the POR rising threshold. When the POR block output is high, UGATE and LGATE can be controlled by the PWM input voltage. If the POR block output is low, both UGATE and LGATE are forced low.

16.2 Tri-State Detect

When the POR output is high, UGATE and LGATE are controlled by the PWM input, which supports three modes: high, low, and shutdown. If the PWM input is within the shutdown window, both UGATE and LGATE outputs are low. When the PWM input is higher than its rising threshold, UGATE is high and LGATE is low. When the PWM input is lower than its falling threshold, UGATE is low and LGATE is high.

16.3 Bootstrap Control

The bootstrap control block controls the integrated bootstrap switch. When LGATE is high (low-side MOSFET is turned on), the bootstrap switch is turned on to charge the bootstrap capacitor at the BOOT pin. When LGATE is low (low-side MOSFET is turned off), the bootstrap switch is turned off to disconnect the VCC pin and BOOT pin.

16.4 Turn-Off Detection

The turn-off detection block detects whether high-side MOSFET is turned off by monitoring the PHASE pin voltage. To avoid shoot-through between high-side and low- side MOSFETs, low-side MOSFET can be turned on only after high-side MOSFET is effectively turned off.

16.5 Shoot-Through Protection

The shoot-through protection block implements the dead time when both high-side and low-side MOSFETs are off. This mechanism ensures that the high-side and low-side MOSFETs are never on simultaneously, effectively preventing shoot-through conditions.

17 Application Information

(Note 6)

The RT9624D is a high-frequency, synchronous rectified, single-phase dual MOSFET driver containing Richtek's advanced MOSFET driver technologies. The RT9624D is designed to adapt to a wide range of applications, from standard MOSFET driving to high-performance CPU VR solutions.

17.1 Supply Voltage and Power-On Reset

The RT9624D can be utilized under both V_{CC} = 5V or V_{CC} = 12V applications which may happen in different fields of electronics application circuits. In terms of efficiency, a higher V_{CC} provides a higher driving voltage for UGATE/LGATE, which may result in increased switching loss but reduced conduction loss in the power MOSFETs. The choice of V_{CC} = 12V or V_{CC} = 5V can be a tradeoff to optimize system efficiency.

The RT9624D is designed to drive both high-side and low-side N-MOSFET through external input PWM control signal. It has a power-on protection function which holds UGATE and LGATE low until the VCC voltage exceeds the rising threshold.

17.2 Tri-State PWM Input

After initialization, the PWM signal takes the control. The rising PWM signal first forces the LGATE signal to turn low, then UGATE signal is allowed to go high after a non-overlapping time to avoid shoot-through current. The falling of PWM signal first forces UGATE to go low. When UGATE and PHASE signal reach a predetermined low level, LGATE signal is allowed to turn high.

The PWM signal is acted as “High” when the signal is above the rising threshold and acted as “Low” when the signal is below the falling threshold. If the PWM signal enters and remains within the shutdown window, both output drivers are disabled and the MOSFET gates are held low. If the PWM pin is left floating, an internal divider maintains the pin at approximately 1.8V and provides the PWM controller with a recognizable level.

17.3 Internal Bootstrap Power Switch

The RT9624D builds in an internal bootstrap power switch, eliminating the need for an external bootstrap diode. This integration simplifies PCB design and reduces overall BOM cost.

17.4 Non-Overlap Control

To prevent the overlap of the gate drivers during the UGATE pulls low and the LGATE pulls high, the non-overlap circuit monitors the voltages at the PHASE node and high-side gate drive (UGATE-PHASE). When the PWM input signal goes low, UGATE begins to pull low (after a propagation delay). Before LGATE is pulled high, the non-overlap protection circuit ensures that the monitored voltages have dropped below 1.1V. Once this condition is met, LGATE is enabled. By waiting for the voltages of the PHASE pin and high-side gate driver to fall below 1.1V, the non-overlap protection circuit ensures that UGATE is low before LGATE pulls high.

Also, to prevent the overlap of the gate drivers during LGATE pulls low and UGATE pulls high, the non-overlap circuit monitors the LGATE voltage. When LGATE goes below 1.1V, UGATE goes high after a propagation delay.

17.5 Driving Power MOSFETs

The DC input impedance of the power MOSFET is extremely high. When V_{gs1} or V_{gs2} is at 12V or 5V, the gate draws the current only a few nano-amperes. Thus, once the gate is driven to the “ON” level, the steady-state current is negligible.

However, the gate-to-source capacitance should be considered, as it requires relatively large currents to drive the gate up and down 12V (or 5V) rapidly. It is also required to switch drain current on and off with the required speed. The required gate drive currents can be calculated as follows.

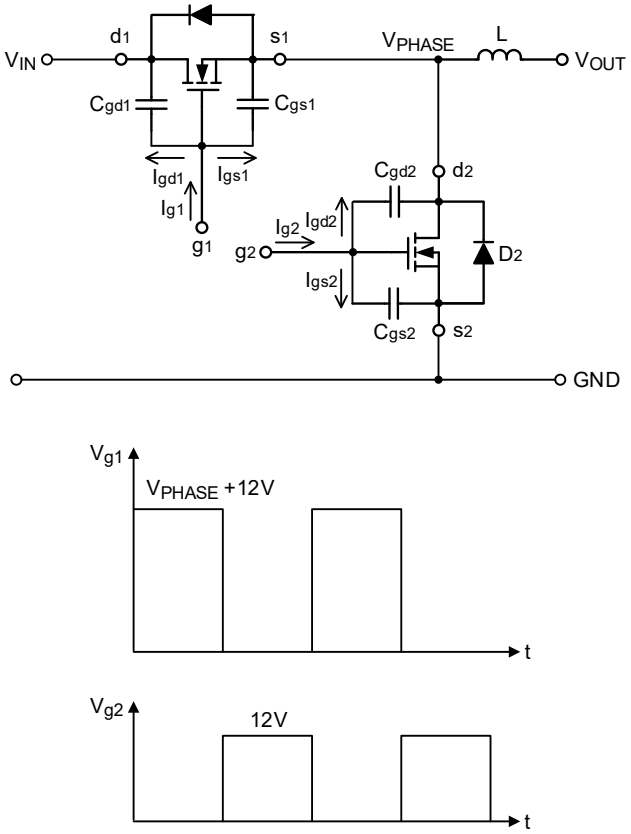


Figure 1. Equivalent Circuit and Waveforms (V_{CC} = 12V)

In Figure 1, the gate drive currents I_{g1} and I_{g2} are required to move the gate up to 12V. The operation involves charging the gate-to-source capacitances (C_{gs1} and C_{gs2}) and gate-to-source capacitances (C_{gd1} and C_{gd2}) of the high-side and low-side power MOSFETs, respectively. In typical datasheets, C_{gs1} and C_{gs2} are referred as "C_{iss}," the input capacitance, while C_{gd1} and C_{gd2} are referred as "C_{rss}," the reverse transfer capacitance. For example, if t_{r1} and t_{r2} are the rise times of the high-side and the low-side power MOSFETs, respectively, the required gate drive currents (I_{gs1} and I_{gs2}) can be calculated as follows:

$$I_{gs1} = C_{gs1} \frac{dV_{g1}}{dt} = \frac{C_{gs1} \times 12}{t_{r1}} \quad (1)$$

$$I_{gs2} = C_{gs1} \frac{dV_{g2}}{dt} = \frac{C_{gs1} \times 12}{t_{r2}} \quad (2)$$

Before the gate of the high-side MOSFET is driven up to 12V, the low-side MOSFET must be turned off. The high-side MOSFET must be turned off before the low-side is turned on. As shown in Figure 1, the body diode (D_2) will be turned on before the high-side MOSFET turns on.

$$I_{gd1} = C_{gd1} \frac{dV}{dt} = C_{gd1} \frac{12}{t_{r1}} \quad (3)$$

Before the low-side MOSFET is turned on, the C_{gd2} has been charged to V_{IN}. Therefore, as C_{gd2} reverses its polarity and the gate (g_2) is driven up to 12V, the required gate drive current is:

$$I_{gd2} = C_{gd2} \frac{dV}{dt} = C_{gd2} \frac{V_{IN} + 12}{t_{r2}} \quad (4)$$

It is useful to calculate these gate drive currents for a typical application. Consider a synchronous rectified buck converter with an input voltage V_{IN} = 12V, V_{gs1} = 12V, and V_{gs2} = 12V. The high-side MOSFET is PHB83N03LT with C_{iss} = 1660pF, C_{rss} = 380pF, and t_r = 14ns. The low-side MOSFET is PHB95N03LT with C_{iss} = 2200pF, C_{rss} = 500pF and t_r = 30ns. Using equation (1) and (2) the required gate drive currents can be calculated as follows:

$$I_{gs1} = \frac{1660 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 1.428 \quad (A) \quad (5)$$

$$I_{gs2} = \frac{2200 \times 10^{-12} \times 12}{30 \times 10^{-9}} = 0.88 \quad (A) \quad (6)$$

from equation (3) and (4)

$$I_{gd1} = \frac{380 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 0.326 \quad (A) \quad (7)$$

$$I_{gd2} = \frac{500 \times 10^{-12} \times (12+12)}{30 \times 10^{-9}} = 0.4 \quad (A) \quad (8)$$

The total current required from the gate driver can be calculated using the following equations:

$$I_{g1} = I_{gs1} + I_{gd1} = (1.428 + 0.326) = 1.754 \quad (A) \quad (9)$$

$$I_{g2} = I_{gs2} + I_{gd2} = (0.88 + 0.4) = 1.28 \quad (A) \quad (10)$$

By a similar calculation, the required sink current for turning off the MOSFET can also be determined.

17.6 Select the Bootstrap Capacitor

Figure 2 shows part of the bootstrap circuit of the RT9624D. The bootstrap voltage, V_{CB} (the voltage difference between BOOT and PHASE on the RT9624D, provides a voltage to drive the gate of the high-side power MOSFET. To ensure reliable operation, the value of the bootstrap capacitor C_{BOOT} must be selected properly. The required capacitance is determined by the following constraints.

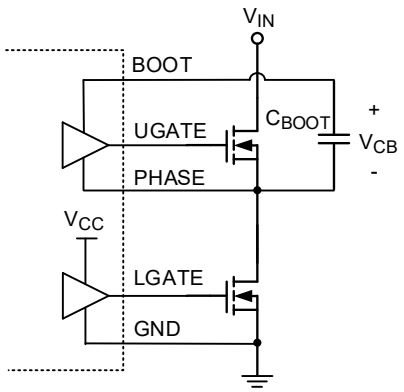


Figure 2. Part of Bootstrap Circuit of RT9624D

In practice, selecting a bootstrap capacitor (C_{BOOT}) with too low a value can result in excessive voltage overshoot, potentially damaging the IC. To minimize the risk of overcharging and to reduce ripple on V_{CB}, the bootstrap capacitor should not be smaller than 0.1μF, and the larger the better. For most designs, a 1μF capacitor provides optimal performance. At least one low-ESR capacitor should be used to ensure effective local de-coupling. It is recommended to adopt a ceramic or tantalum capacitor.

17.7 Power Dissipation

To ensure the IC operates within the maximum recommended operating junction temperature of 125°C, it is necessary to accurately calculate power dissipation. Power dissipation depends on the switching frequency and the total gate charge of the selected MOSFET. Figure 3 illustrates the power dissipation test circuit, where C_L and C_U represent the UGATE and LGATE load capacitors, respectively. The bootstrap capacitor value is set to 1μF.

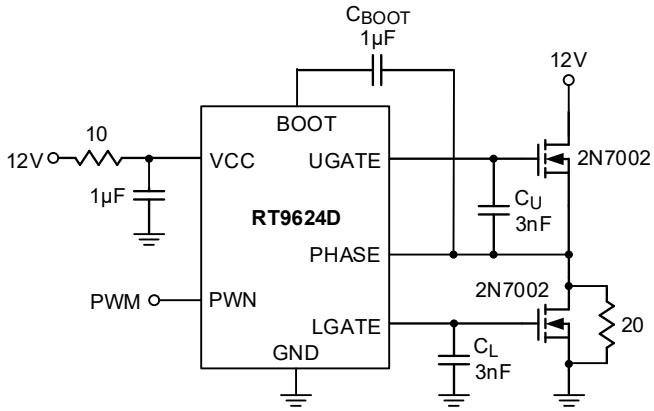


Figure 3. Power Dissipation Test Circuit

Figure 4 shows the power dissipation of the RT9624D as a function of switching frequency and load capacitance when V_{CC} = 12V. The values of C_U and C_L are the same and the switching frequency varies from 100kHz to 1MHz.

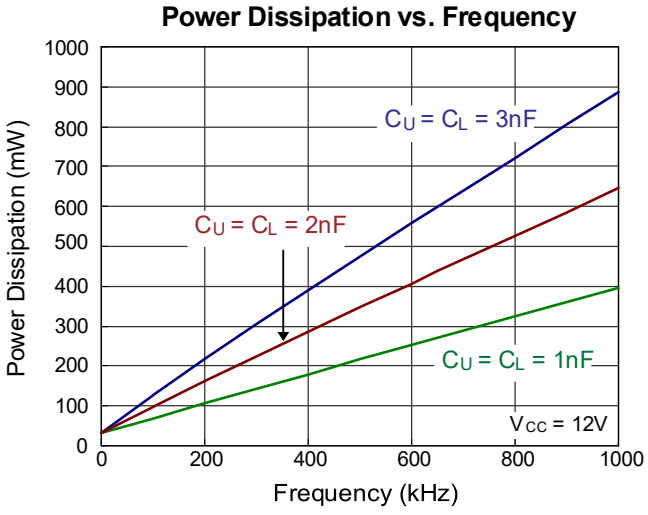


Figure 4. Power Dissipation vs. Frequency

The operating junction temperature can be calculated from the power dissipation curves (Figure 4). For example, assume V_{CC} = 12V, operating frequency is 200kHz, and C_U = C_L = 1nF, which emulate the input capacitances of the high-side and low-side power MOSFETs. From Figure 4, the power dissipation is 100mW. For the WDFN-8SL 2x2 package, the thermal resistance (θ_{JA}) is 46°C/W. The operating junction temperature (T_J) is calculated as

follows:

T_J = (46°C/W x 100mW) + 25°C = 29.6°C (11)

where the ambient temperature (T_A) is 25°C.

17.8 Thermal Consideration

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} – T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-8SL 2x2 package, the thermal resistance, θ_{JA}, is 46°C/W on a standard JEDEC 51-7 high effective-thermal conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (125°C – 25°C) / (46°C/W) = 2.17W for a WDFN-8SL 2x2 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 5 allows the user to see the effect of rising ambient temperature on the maximum power dissipation.

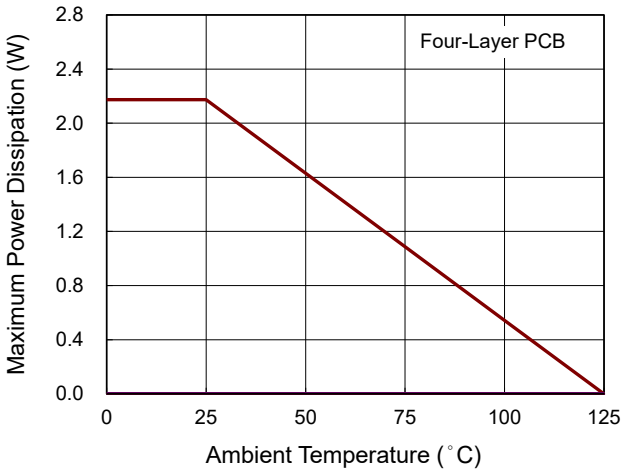


Figure 5. Derating Curve of Maximum Power Dissipation

17.9 Layout Considerations

Figure 6 shows the schematic of a synchronous buck converter to implement the RT9624D. The converter operates with an input voltage range from 5V to 12V. Careful attention must be paid to the PCB layout, as the power circuit section is the most critical area. Improper layout can result in significant EMI. To minimize EMI and ensure optimal performance, the placement of Q1, Q2, L1 should be as close as possible.

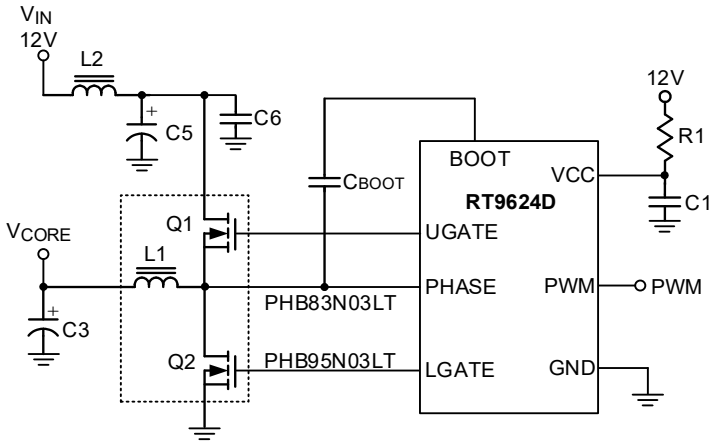
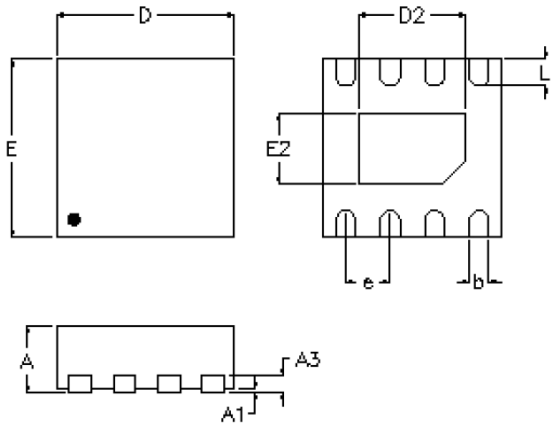
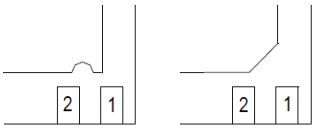


Figure 6. Synchronous Buck Converter Circuit

Note 6. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

18 Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

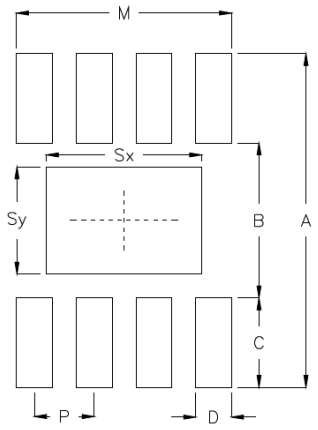
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min.	Max.	Min.	Max.
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.200	0.300	0.008	0.012
D		1.900	2.100	0.075	0.083
D2	Option1	1.150	1.250	0.045	0.049
	Option2	1.550	1.650	0.061	0.065
E		1.900	2.100	0.075	0.083
E2	Option1	0.750	0.850	0.030	0.033
	Option2	0.850	0.950	0.033	0.037
e		0.500		0.020	
L		0.250	0.350	0.010	0.014

W-Type 8SL DFN 2x2 Package

Note 7. The package of the RT9624D uses Option 1.

19 Footprint Information

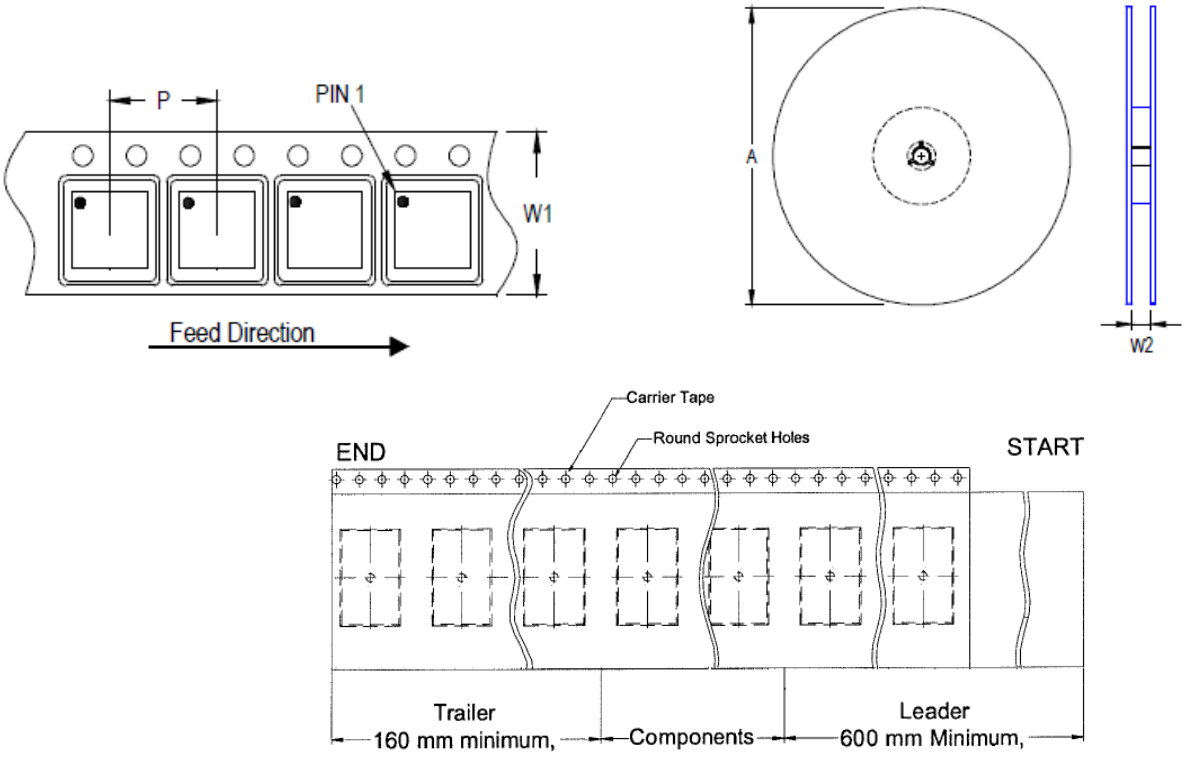


Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2*2-8S	Option 1	8	0.50	2.80	1.30	0.75	0.30	1.30	0.90	1.80	±0.05
	Option 2							1.60	0.90		

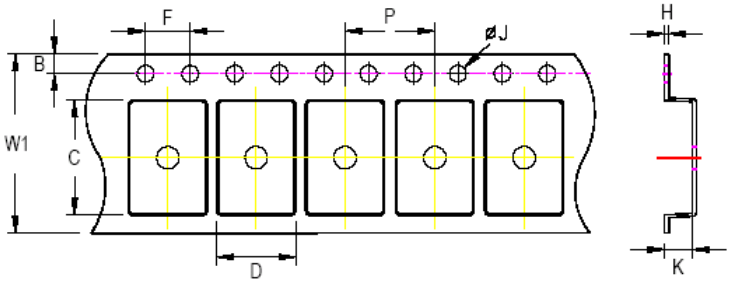
Note 8. The package of the RT9624D uses Option 1.

20 Packing Information

20.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 2x2	8	4	180	7	2,500	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 2x2	7”	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description
05	2026/3/16	Ordering Information - Updated notes Absolute Maximum Ratings - Updated Packing Information - Added