

Single Phase Synchronous Rectified Buck MOSFET Driver

1 General Description

The RT9624K/RT9624L is a high frequency, synchronous rectified, single phase MOSFET driver designed for normal MOSFET driving applications and high performance CPU VR driving capabilities.

The RT9624K/RT9624L can be supplied from 4.5V to 13.2V. The applicable power stage VIN range is from 5V to 24V. The RT9624K/RT9624L also builds in an internal power switch to replace external bootstrap diode.

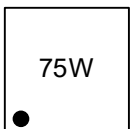
The RT9624K/RT9624L can support switching frequency efficiently up to 500kHz. The RT9624K/RT9624L has both the UGATE and LGATE driving circuits for synchronous rectified DC-DC converter applications. The shoot through protection mechanism is designed to prevent shoot through between high side and low side power MOSFETs. The RT9624K/RT9624L has tri-state PWM input with shutdown and EN input shutdown functions, which can force driver to output low UGATE and LGATE signals.

The RT9624K comes in a small footprint with WDFN-8SL 2x2 package. The RT9624L is available in a small footprint WDFN-8L 3x3 package.

The recommended junction temperature range is -40°C to 125°C, and the ambient temperature range is -40°C to 85°C.

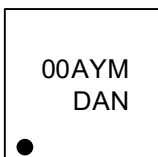
2 Marking Information

RT9624KGQWA



75: Product Code
W: Date Code

RT9624LGQW



00A: Product Code
YMDAN: Date Code

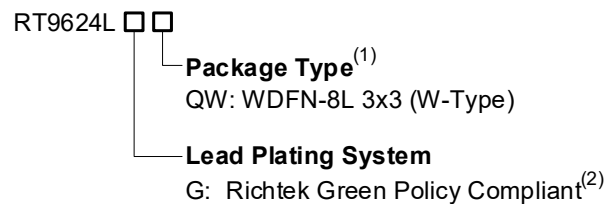
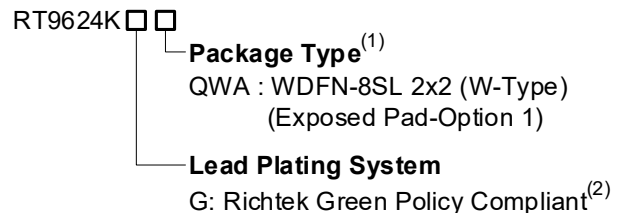
3 Features

- Drive Two N-MOSFETs
- Shoot-Through Protection
- Embedded Bootstrap Switch
- Support High Switching Frequency
- Fast Output Rising Time
- Tri-State PWM Input for Output Shutdown
- RT9624K
 - Enable Control
 - Small 8-Lead WDFN Package
- RT9624L
 - 8-Lead WDFN Package
- Compatible with 3.3V or 5V Middle State PWM Input

4 Applications

- Core Voltage Supplies for Desktop, Motherboard CPU
- High Frequency Low Profile DC-DC Converters
- High Current Low Voltage DC-DC Converters
- Core Voltage Supplies for GFX Card

5 Ordering Information



Note 1.

- Marked with ⁽¹⁾ indicates compatibility with the current requirements of IPC/JEDEC J-STD-020.
- Marked with ⁽²⁾ indicates that Richtek products are Richtek Green Policy compliant.

6 Simplified Application Circuit

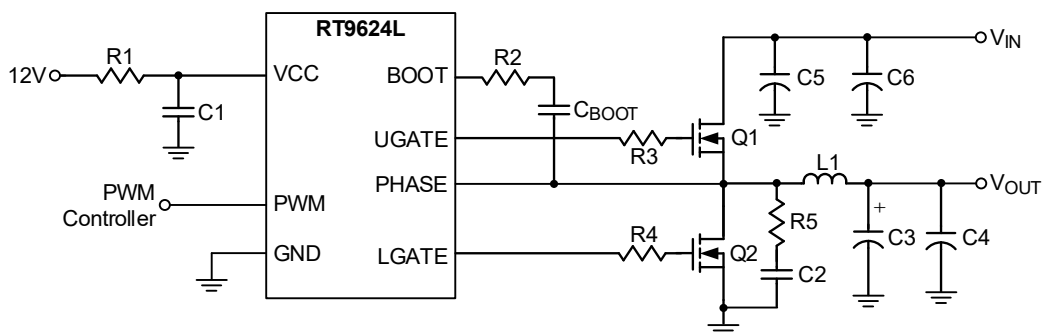
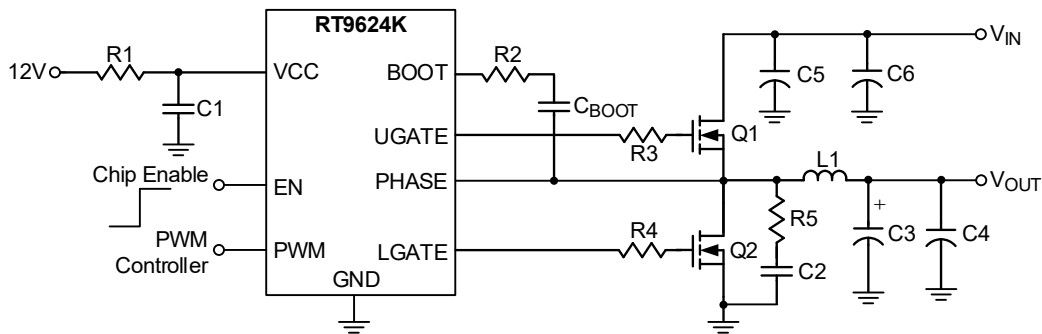
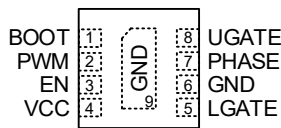


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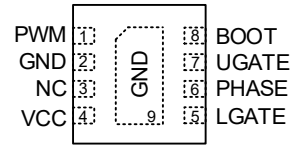
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7 Pin Configuration

(TOP VIEW)



WDFN-8SL 2x2
(RT9624K)



WDFN-8L 3x3
(RT9624L)

8 Functional Pin Description

8.1 WDFN-8SL 2x2 Package

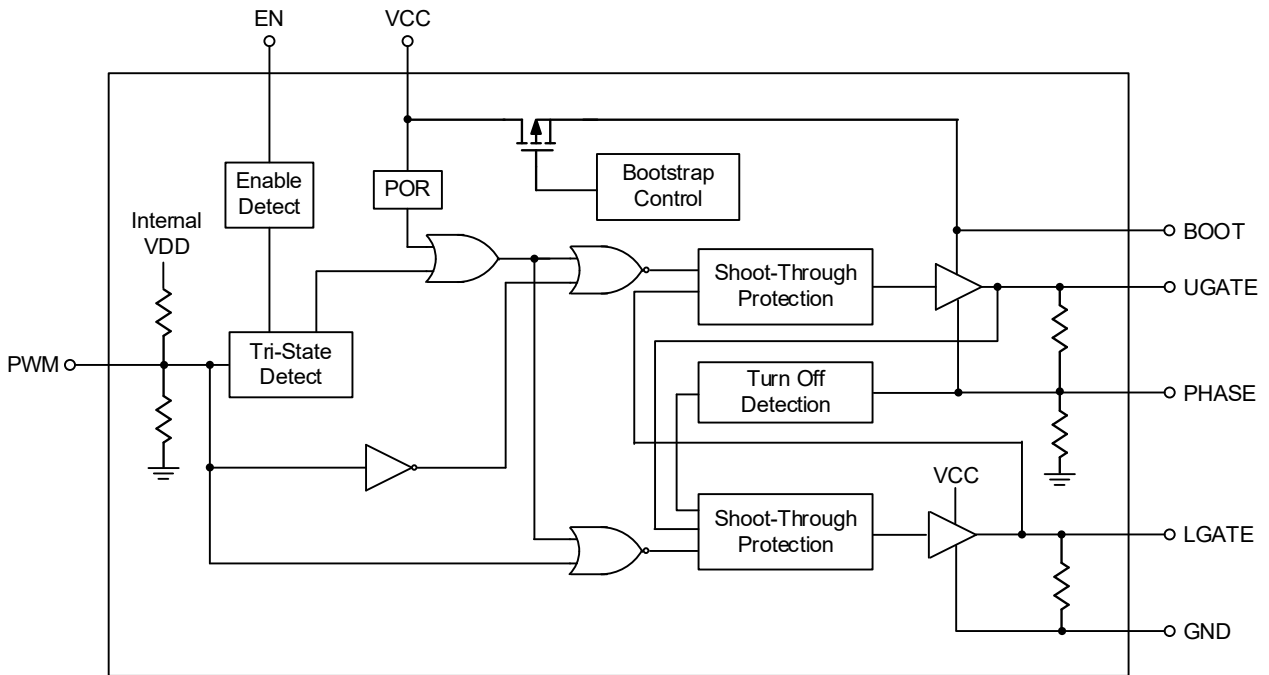
Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap Supply for High Side Gate Driver.
2	PWM	PWM Signal Input. Connect this pin to the PWM output of the controller.
3	EN	Chip Enable (Active High). When this pin is low, both UGATE and LGATE are driven to low.
4	VCC	Supply Voltage Input.
5	LGATE	Low Side Gate Driver Output. Connect this pin to the Gate of low side power N-MOSFET.
6, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
7	PHASE	Connect this pin to the Source of the high side N-MOSFET and the Drain of the low side N-MOSFET.
8	UGATE	High Side Gate Driver Output. Connect this pin to the Gate of high side power N-MOSFET.

8.2 WDFN-8L 3x3 Package

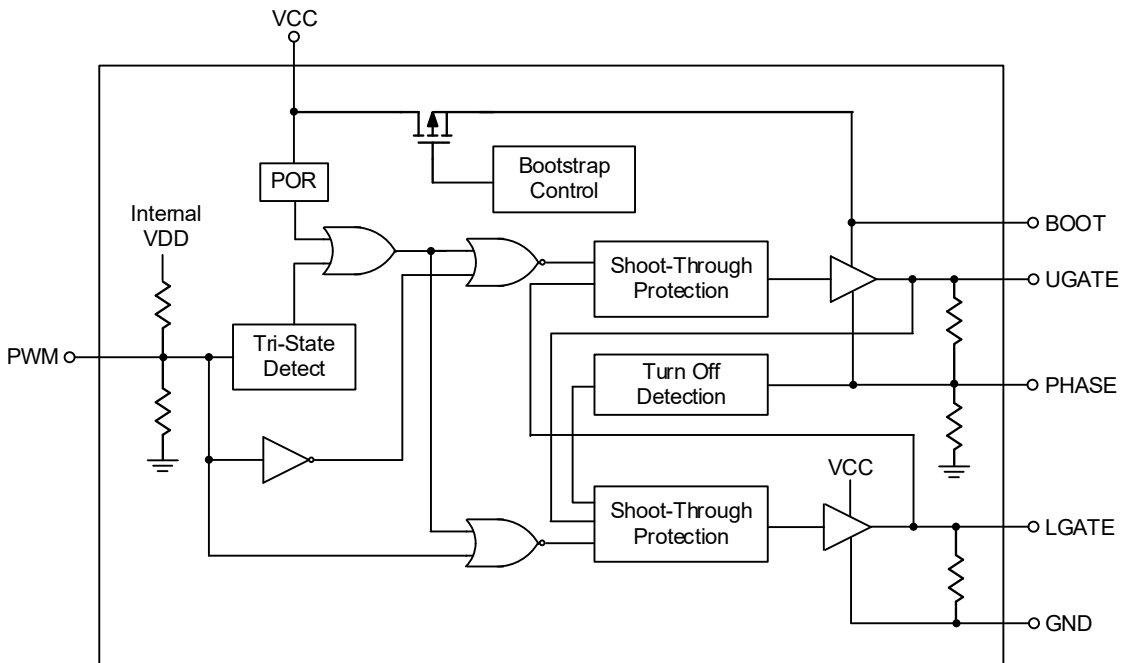
Pin No.	Pin Name	Pin Function
1	PWM	PWM Signal Input. Connect this pin to the PWM output of the controller.
2, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
3	NC	No Internal Connection.
4	VCC	Supply Voltage Input.
5	LGATE	Low-Side Gate Driver Output. Connect this pin to the Gate of low-side power N-MOSFET.
6	PHASE	Connect this pin to the Source of the high-side N-MOSFET and the Drain of the low-side N-MOSFET.
7	UGATE	High-Side Gate Drive Output. Connect this pin to the Gate of high-side power N-MOSFET.
8	BOOT	Bootstrap Supply for High-Side Gate Drive.

9 Functional Block Diagram

RT9624K



RT9624L



10 Absolute Maximum Ratings

(Note 2)

• Supply Voltage, VCC -----	-0.3V to 15V
• BOOT to PHASE	
DC -----	-0.3V to 15V
< 60ns -----	-3V to 25V
• BOOT to GND	
DC -----	-0.3V to 45V
< 60ns -----	-20V to 46V
• PHASE to GND	
DC -----	-0.3V to 30V
< 60ns -----	-20V to 31V
• UGATE to PHASE	
DC -----	-0.3V to 15V
< 60ns -----	-3V to 25V
• UGATE to GND	
DC -----	-0.3V to 30V
< 60ns -----	-20V to 31V
• LGATE to GND	
DC -----	-0.3V to 15V
< 60ns -----	-3V to 16V
• EN, PWM to GND -----	-0.3V to 7V
• Power Dissipation, Pd @ TA = 25°C	
WDFN-8SL 2x2 -----	2.17W
WDFN-8L 3x3 -----	3.22W
• Package Thermal Resistance (Note 3)	
WDFN-8SL 2x2, θ_{JA} -----	46°C/W
WDFN-8SL 2x2, θ_{JC} -----	11.5°C/W
WDFN-8L 3x3, θ_{JA} -----	31°C/W
WDFN-8L 3x3, θ_{JC} -----	8°C/W
• Lead Temperature (Soldering, 10 sec) -----	260°C
• Junction Temperature -----	-40°C to 150°C
• Storage Temperature Range -----	-65°C to 150°C
• ESD Susceptibility (Note 4)	
HBM (Human Body Model) -----	2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at $T_A = 25^\circ\text{C}$ with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Voltage, VCC ----- 4.5V to 13.2V
- Input Voltage, ($V_{IN} + V_{CC}$) ----- < 35V
- Junction Temperature Range----- -40°C to 125°C
- Ambient Temperature Range----- -40°C to 85°C

Note 5. The device is not guaranteed to function outside its operating conditions.

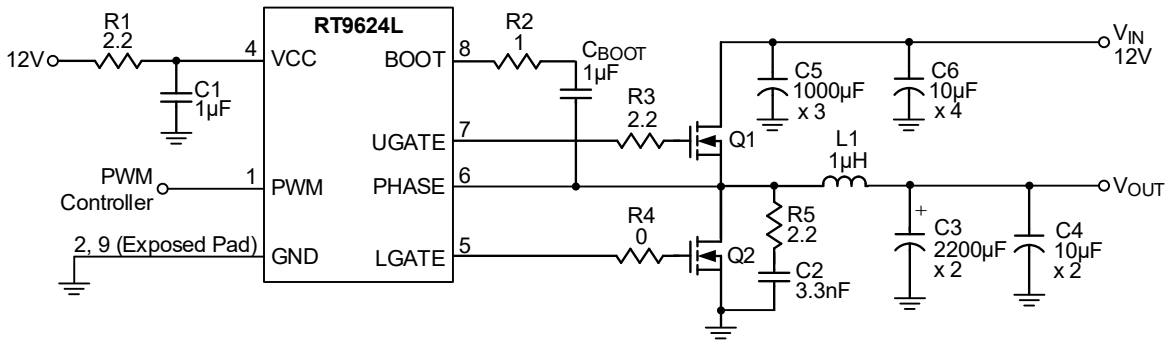
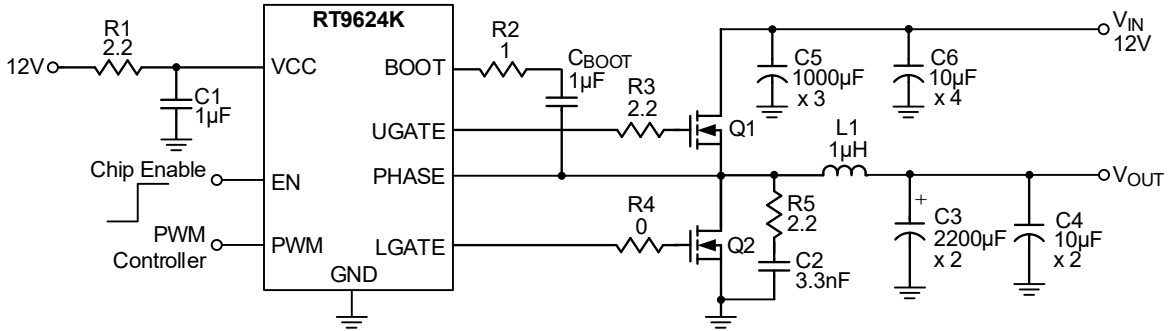
12 Electrical Characteristics

($V_{CC} = 12\text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.)

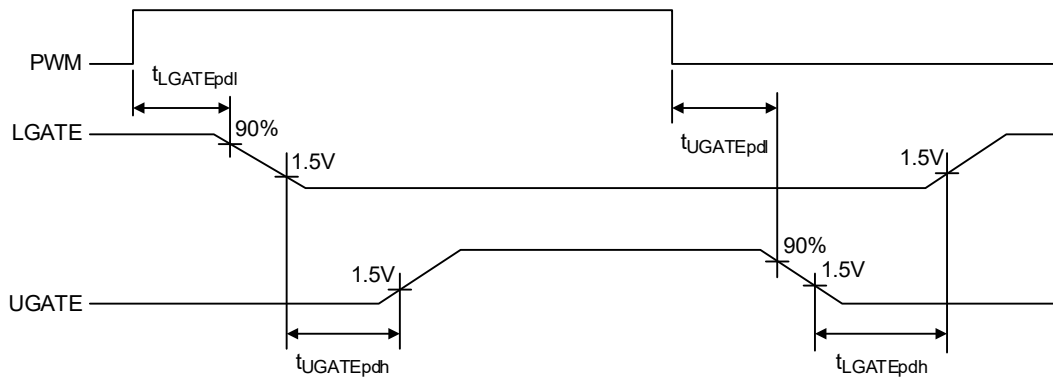
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Power Supply Voltage	VCC		4.5	--	13.2	V
Power Supply Current	I _{VCC}	V _{BOOT} = 12V, PWM input floating	--	120	--	μA
Power On Reset (POR)						
POR Rising Threshold	V _{POR_r}	VCC rising	--	4	4.4	V
POR Falling Threshold	V _{POR_f}	VCC falling	3	3.5	--	V
EN Input						
EN Rising Threshold	V _{ENH}		--	1.3	1.6	V
EN Falling Threshold	V _{ENL}		0.7	1	--	V
PWM Input						
Maximum Input Current	I _{PWM}	PWM = 0V or 5V	--	160	--	μA
PWM Floating Voltage	V _{PWM_FL}	PWM = open	--	1.8	--	V
PWM Logic-High	V _{PWM_H}		2.3	2.8	3.09	V
PWM Logic-Low	V _{PWM_L}				0.7	V
Timing						
UGATE Rising Time	t _{UGATEr}	3nF load	--	25	--	ns
UGATE Falling Time	t _{UGATEf}	3nF load	--	12	--	ns
LGATE Rising Time	t _{LGATEr}	3nF load	--	24	--	ns
LGATE Falling Time	t _{LGATEf}	3nF load	--	10	--	ns
UGATE Propagation Delay	t _{UGATEpdh}	V _{BOOT} – V _{PHASE} = 12V	--	60	--	ns
	t _{UGATEpdl}	See timing diagram	--	22	--	
LGATE Propagation Delay	t _{LGATEpdh}	See timing diagram	--	30	--	ns
	t _{LGATEpdl}	See timing diagram	--	8	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output						
UGATE Drive Source	RUGATEsr	VBOOT – VPHASE = 12V, I _{Source} = 100mA	--	1.7	--	Ω
UGATE Drive Sink	RUGATEsk	VBOOT – VPHASE = 12V, I _{Sink} = 100mA	--	1.4	--	Ω
LGATE Drive Source	RLGATEsr	I _{Source} = 100mA	--	1.6	--	Ω
LGATE Drive Sink	RLGATEsk	I _{Sink} = 100mA	--	1.1	--	Ω

13 Typical Application Circuit

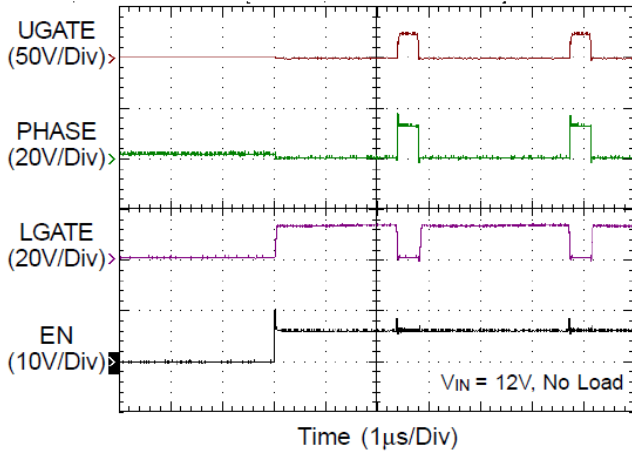


14 Timing Diagram

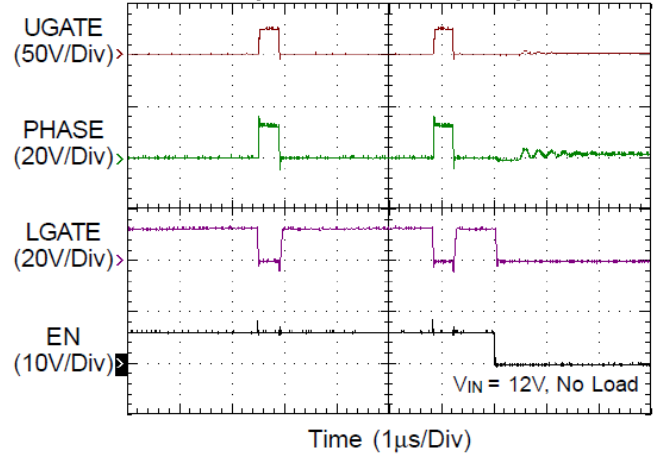


15 Typical Operating Characteristics

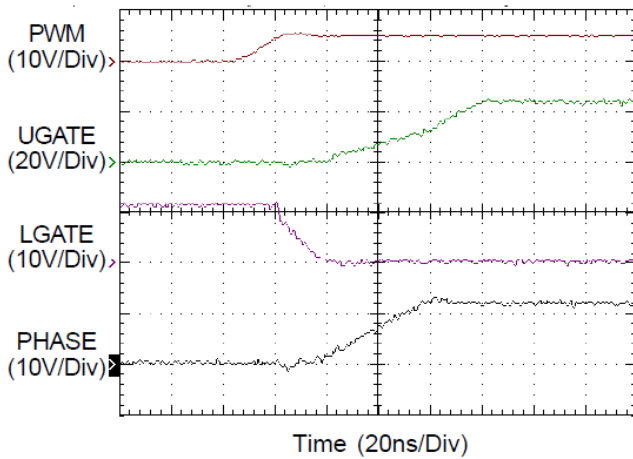
Drive Enable



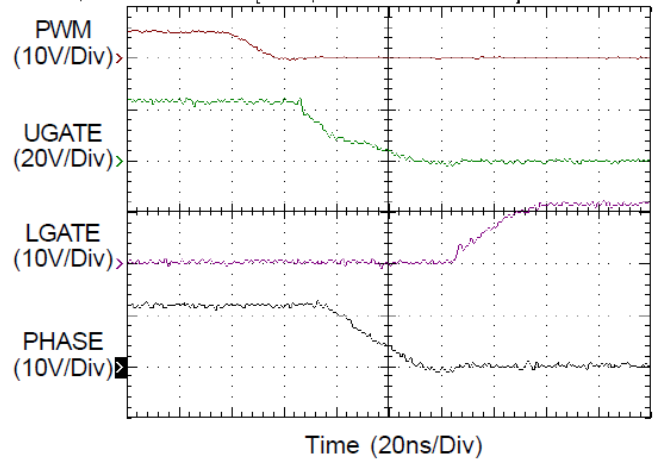
Drive Disable



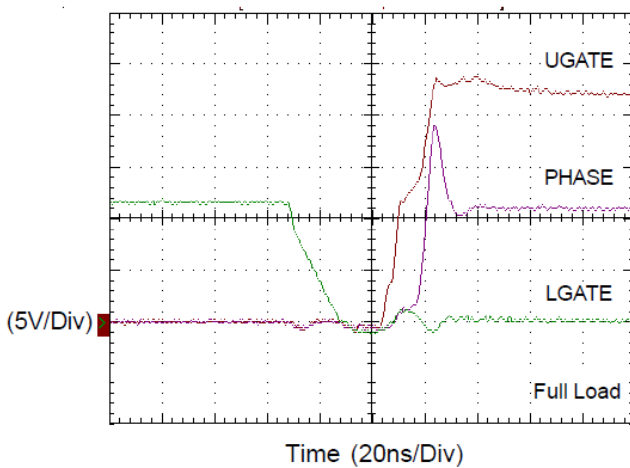
PWM Rising Edge



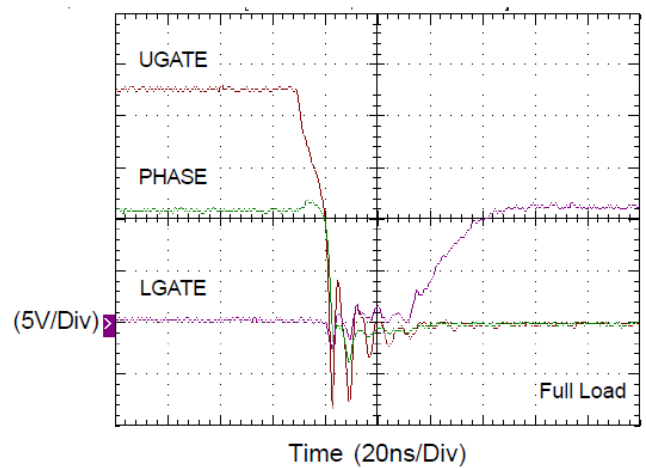
PWM Falling Edge



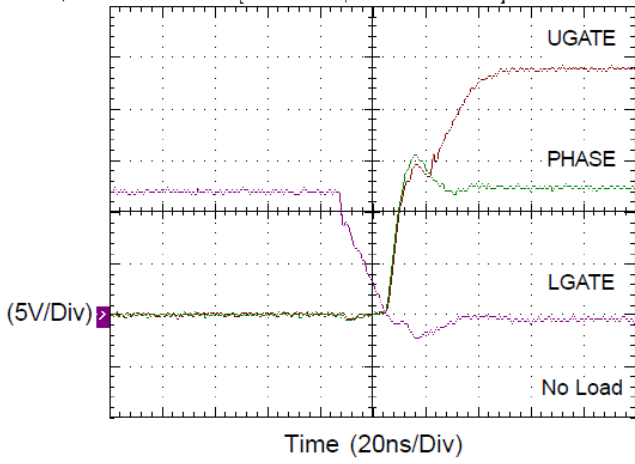
Dead Time



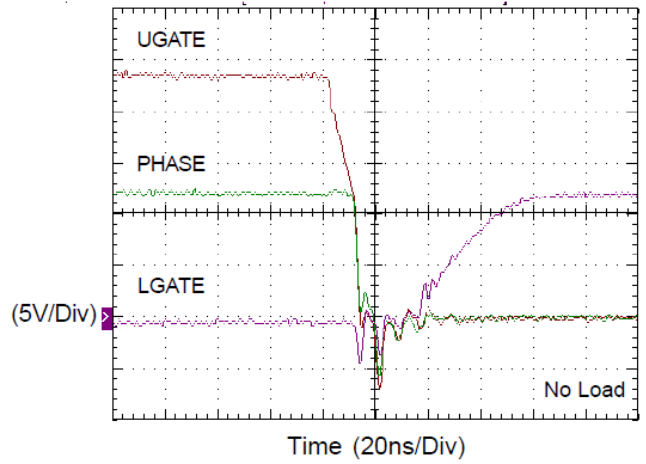
Dead Time



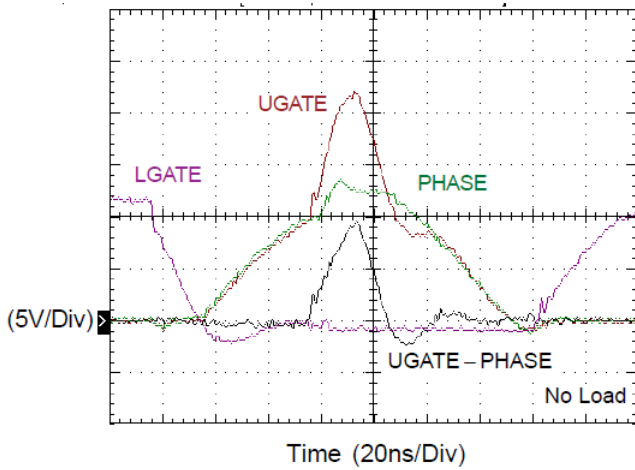
Dead Time



Dead Time



Short Pulse



16 Operation

16.1 POR (Power On Reset)

POR block detects the voltage at the VCC pin. When the VCC pin voltage is higher than POR rising threshold, POR block output is high. POR output is low when VCC is not higher than POR rising threshold. When the POR block output is high, UGATE and LGATE can be controlled by PWM input voltage. If the POR block output is low, both UGATE and LGATE will be pulled to low.

16.2 Enable Detect

When EN pin input voltage is higher than EN rising threshold, MOSFET driver is enabled. When the EN input and POR output are high, UGATE and LGATE can be controlled by PWM input voltage. When EN input is low, both UGATE and LGATE are pulled to low.

16.3 Tri-State Detect

When both POR block output and EN pin voltages are high, UGATE and LGATE can be controlled by PWM input. There are three PWM input modes, which are high, low, and shutdown state. If PWM input is within the shutdown window, both UGATE and LGATE output are low. When PWM input is higher than its rising threshold, UGATE is high and LGATE is low. When PWM input is lower than its falling threshold, UGATE is low and LGATE is high.

16.4 Bootstrap Control

Bootstrap control block controls the integrated bootstrap switch. When LGATE is high (low-side MOSFET is turned on), the bootstrap switch is turned on to charge the bootstrap capacitor connected to BOOT pin. When LGATE is low (low-side MOSFET is turned off), the bootstrap switch is turned off to disconnect VCC pin and BOOT pin.

16.5 Turn-Off Detection

Turn-off detection block detects whether high-side MOSFET is turned off by monitoring PHASE pin voltage. To avoid shoot-through between high side and low-side MOSFETs, low-side MOSFET can be turned on only after high-side MOSFET is effectively turned off.

16.6 Shoot-Through Protection

Shoot-through protection block implements the dead time when both high side and low-side MOSFETs are turned off. With shoot-through protection block, high side and low-side MOSFET are never turned on simultaneously. Thus, shoot-through between high side and low-side MOSFETs is prevented.

17 Application Information

(Note 6)

The RT9624K/RT9624L is a high frequency, synchronous rectified, single phase dual MOSFET driver containing Richtek's advanced MOSFET driver technologies. The RT9624K/RT9624L is designed to be able to adapt from normal MOSFET driving applications to high performance CPU VR driving capabilities.

17.1 Supply Voltage and Power On Reset

The RT9624K/RT9624L can be utilized under both $V_{CC} = 5V$ or V_{CC}

$= 12V$ applications which may happen in different fields of electronics application circuits. In terms of efficiency, higher V_{CC} equals higher driving voltage of UGATE/LGATE which may result in higher switching loss and lower conduction loss of power MOSFETs. The choice of $V_{CC} = 12V$ or $V_{CC} = 5V$ can be a tradeoff to optimize system efficiency.

The RT9624K/RT9624L is designed to drive both high side and low side N-MOSFET through external input PWM control signal. It has power on protection function which held UGATE and LGATE low before the VCC voltage rises to higher than rising threshold voltage.

17.2 Enable and Disable

The RT9624K includes an EN pin for sequence control. When the EN pin rises above the V_{ENH} trip point, the RT9624K begins a new initialization and follows the PWM command to control the UGATE and LGATE. When the EN pin falls below the V_{ENL} trip point, the RT9624K shuts down and keeps UGATE and LGATE low.

17.3 Tri-state PWM Input

After the initialization, the PWM signal takes the control. The rising PWM signal first forces the LGATE signal to turn low then UGATE signal is allowed to go high just after a non-overlapping time to avoid shoot through current. The falling of PWM signal first forces UGATE to go low. When UGATE and PHASE signal reach a predetermined low level, LGATE signal is allowed to turn high.

The PWM signal is acted as "High" if the signal is above the rising threshold and acted as "Low" if the signal is below the falling threshold. When PWM signal level enters and remains within the shutdown window, the output drivers are disabled and both MOSFET gates are pulled and held low. If the PWM signal is left floating, the pin will be kept around 1.8V by the internal divider and provide the PWM controller with a recognizable level.

17.4 Internal Bootstrap Power Switch

The RT9624K/RT9624L builds in an internal bootstrap power switch to replace external bootstrap diode, and this can facilitate PCB design and reduce total BOM cost of the system. Hence, no external bootstrap diode is required in real applications.

17.5 Non-overlap Control

To prevent the overlap of the gate drivers during the UGATE pull low and the LGATE pull high, the non-overlap circuit monitors the voltages at the PHASE node and high side gate drive (UGATE-PHASE). When the PWM input signal goes low, UGATE begins to pull low (after propagation delay). Before LGATE is pulled high, the non-overlap protection circuit ensures that the monitored voltages have gone below 1.1V. Once the monitored voltages fall below 1.1V, LGATE begins to turn high. By waiting for the voltages of the PHASE pin and high side gate driver to fall below 1.1V, the non-overlap protection circuit ensures that UGATE is low before LGATE pulls high.

Also to prevent the overlap of the gate drivers during LGATE pull low and UGATE pull high, the non-overlap circuit monitors the LGATE voltage. When LGATE goes below 1.1V, UGATE goes high after propagation delay.

17.6 Driving Power MOSFETs

The DC input impedance of the power MOSFET is extremely high. When V_{gs1} or V_{gs2} is at 12V or 5V, the gate draws the current only for few nano-amperes. Thus once the gate has been driven up to “ON” level, the current can be negligible.

However, the capacitance at the gate to source terminal should be considered. It requires relatively large currents to drive the gate up and down 12V (or 5V) rapidly. It is also required to switch drain current on and off with the required speed. The required gate drive currents are calculated as follows.

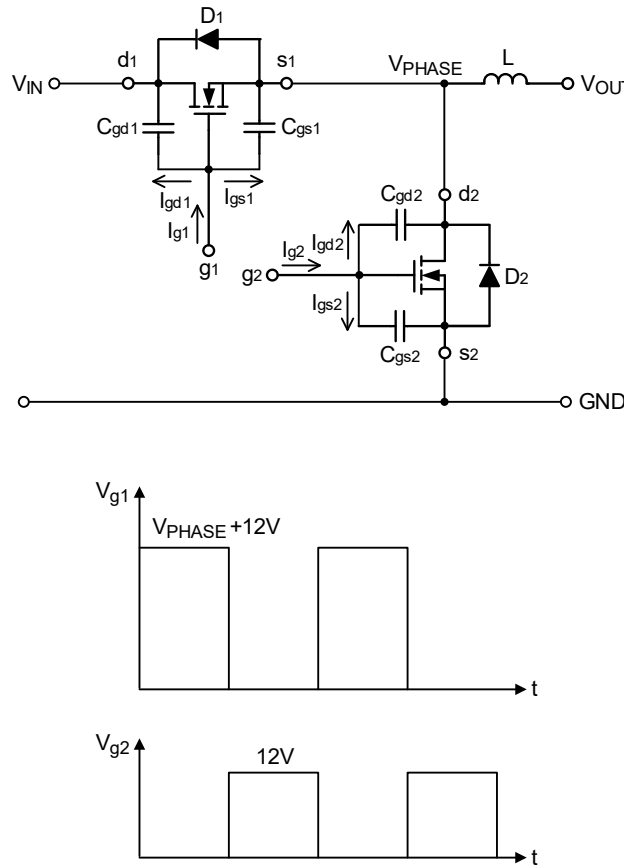


Figure 1. Equivalent Circuit and Waveforms ($V_{CC} = 12V$)

In [Figure 1](#), the current I_{g1} and I_{g2} are required to move the gate up to 12V. The operation consists of charging C_{gd1} , C_{gd2} , C_{gs1} and C_{gs2} . C_{gs1} and C_{gs2} are the capacitors from gate to source of the high-side and the low-side power MOSFETs, respectively. In general data sheets, the C_{gs1} and C_{gs2} are referred as “Ciss” which are the input capacitors. C_{gd1} and C_{gd2} are the capacitors from gate to drain of the high-side and the low-side power MOSFETs, respectively and referred to the data sheets as “Crss” the reverse transfer capacitance. For example, t_{r1} and t_{r2} are the rising time of the high-side and the low-side power MOSFETs respectively, the required current I_{gs1} and I_{gs2} , are shown as below:

$$I_{gs1} = C_{gs1} \frac{dV_{g1}}{dt} = \frac{C_{gs1} \times 12}{t_{r1}} \quad (1)$$

$$I_{gs2} = C_{gs2} \frac{dV_{g2}}{dt} = \frac{C_{gs2} \times 12}{t_{r2}} \quad (2)$$

Before driving the gate of the high-side MOSFET up to 12V, the low-side MOSFET has to be off; and the high-side MOSFET will be turned off before the low-side is turned on. From [Figure 1](#), the body diode “D2” will be turned on before high-side MOSFETs turn on.

$$I_{gd1} = C_{gd1} \frac{dV}{dt} = C_{gd1} \frac{12}{t_{r1}} \quad (3)$$

Before the low-side MOSFET is turned on, the Cgd2 have been charged to VIN. Thus, as Cgd2 reverses its polarity and g2 is charged up to 12V, the required current is

$$I_{gd2} = C_{gd2} \frac{dV}{dt} = C_{gd2} \frac{V_{IN} + 12}{t_{r2}} \quad (4)$$

It is helpful to calculate these currents in a typical case. Assume a synchronous rectified Buck converter, input voltage VIN = 12V, Vgs1 = 12V, Vgs2 = 12V. The high-side MOSFET is PHB83N03LT whose Ciss = 1660pF, Crss = 380pF, and tr = 14ns. The low-side MOSFET is PHB95N03LT whose Ciss = 2200pF, Crss = 500pF and tr = 30ns, from the equation (1) and (2) we can obtain

$$I_{gs1} = \frac{1660 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 1.428 \quad (A) \quad (5)$$

$$I_{gs2} = \frac{2200 \times 10^{-12} \times 12}{30 \times 10^{-9}} = 0.88 \quad (A) \quad (6)$$

from equation. (3) and (4)

$$I_{gd1} = \frac{380 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 0.326 \quad (A) \quad (7)$$

$$I_{gd2} = \frac{500 \times 10^{-12} \times (12+12)}{30 \times 10^{-9}} = 0.4 \quad (A) \quad (8)$$

the total current required from the gate driving source can be calculated as the following equations.

$$I_{g1} = I_{gs1} + I_{gd1} = (1.428 + 0.326) = 1.754 \quad (A) \quad (9)$$

$$I_{g2} = I_{gs2} + I_{gd2} = (0.88 + 0.4) = 1.28 \quad (A) \quad (10)$$

By a similar calculation, we can also get the sink current required from the turned off MOSFET.

17.7 Select the Bootstrap Capacitor

[Figure 2](#) shows part of the bootstrap circuit of the RT9624K/RT9624L. The VCB (the voltage difference between BOOT and PHASE on RT9624K/RT9624L) provides a voltage to the gate of the high-side power MOSFET. This supply needs to be ensured that the MOSFET can be driven. For this, the capacitance CBOOT has to be selected properly. It is determined by the following constraints.

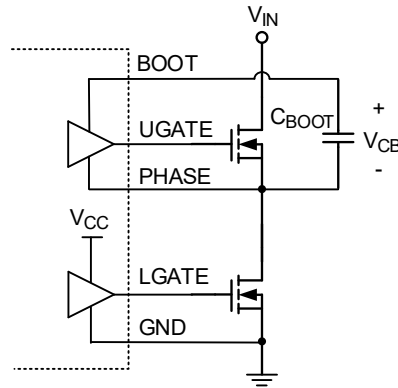


Figure 2. Part of Bootstrap Circuit of RT9624F

In practice, a low value capacitor C_{BOOT} will lead to the over charging that can damage the IC. Therefore, to minimize the risk of overcharging and to reduce the ripple on V_{CB} , the bootstrap capacitor should not be smaller than $0.1\mu\text{F}$, and the larger the better. In general design, using $1\mu\text{F}$ can provide better performance. At least one low-ESR capacitor should be used to provide good local de-coupling. It is recommended to adopt a ceramic or tantalum capacitor.

17.8 Power Dissipation

To prevent driving the IC beyond the maximum recommended operating junction temperature of 125°C , it is necessary to calculate the power dissipation appropriately. This dissipation is a function of switching frequency and total gate charge of the selected MOSFET.

Figure 3 shows the power dissipation test circuit. C_L and C_U are the UGATE and LGATE load capacitors, respectively. The bootstrap capacitor value is $1\mu\text{F}$.

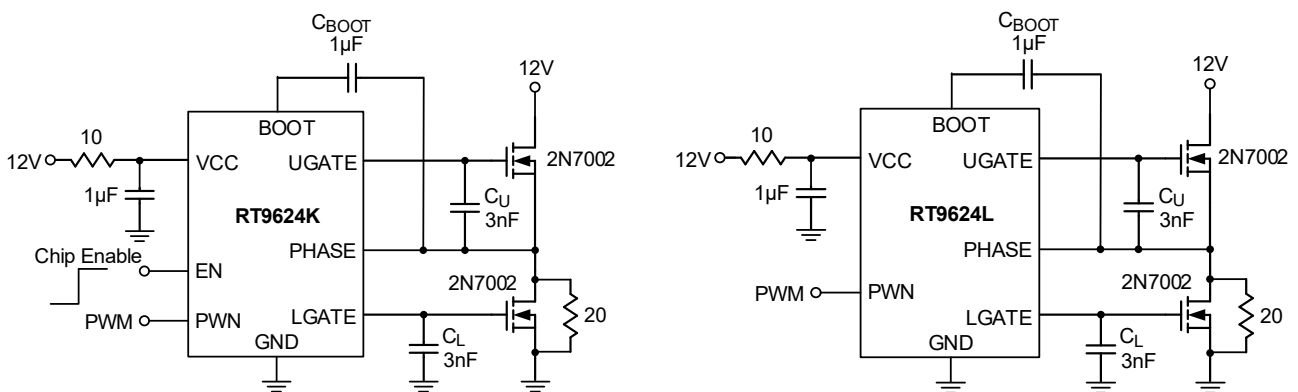


Figure 3. Power Dissipation Test Circuit

Figure 4 shows the power dissipation of the RT9624K/RT9624L as a function of frequency and load capacitance when VCC = 12V. The value of CU and CL are the same and the frequency is varied from 100kHz to 1MHz.

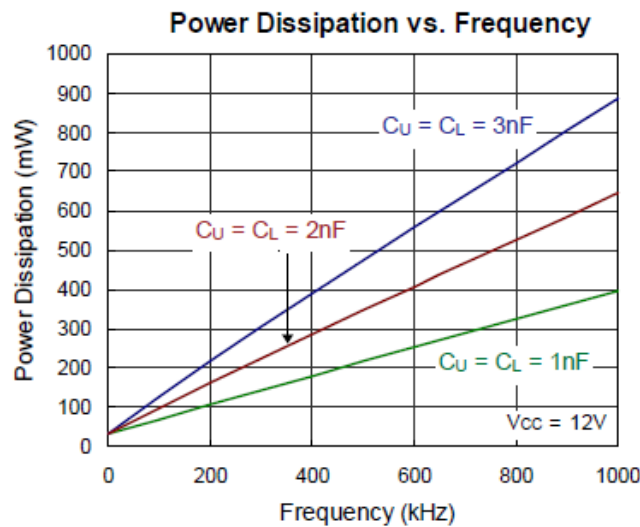


Figure 4. Power Dissipation vs. Frequency

The operating junction temperature can be calculated from the power dissipation curves (Figure 4). Assume VCC = 12V, operating frequency is 200kHz and CU = CL = 1nF which emulate the input capacitances of the high-side and low-side power MOSFETs. From Figure 4, the power dissipation is 100mW.

Thus, for example, with the WDFN-8L 3x3 package thermal resistance θ_{JA} is 120°C/W. The operating junction temperature is then calculated as:

$$T_J = (120^\circ\text{C/W} \times 100\text{mW}) + 25^\circ\text{C} = 37^\circ\text{C} \quad (11)$$

where the ambient temperature is 25°C.

Thus, for example, with the WDFN-8SL 2x2 package, the package thermal resistance θ_{JA} is 46°C/W. The operating junction temperature is then calculated as:

$$T_J = (46^\circ\text{C/W} \times 100\text{mW}) + 25^\circ\text{C} = 29.6^\circ\text{C} \quad (11)$$

where the ambient temperature is 25°C.

17.9 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(\text{MAX})}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(\text{MAX})} = (T_{J(\text{MAX})} - T_A) / \theta_{JA}$$

where $T_{J(\text{MAX})}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a WDFN-8SL 2x2 package, the thermal resistance, θ_{JA} , is 46°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a WDFN-8L 3x3 package, the thermal resistance, θ_{JA} , is 31°C/W on a

standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as below:

$$P_{D(\text{MAX})} = (125^\circ\text{C} - 25^\circ\text{C}) / (46^\circ\text{C/W}) = 2.17\text{W for a WDFN-8SL 2x2 package.}$$

$$P_{D(\text{MAX})} = (125^\circ\text{C} - 25^\circ\text{C}) / (31^\circ\text{C/W}) = 3.22\text{W for a WDFN-8L 3x3 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(\text{MAX})}$ and the thermal resistance, θ_{JA} . The derating curves in [Figure 5](#) allow the user to see the effect of rising ambient temperature on the maximum power dissipation.

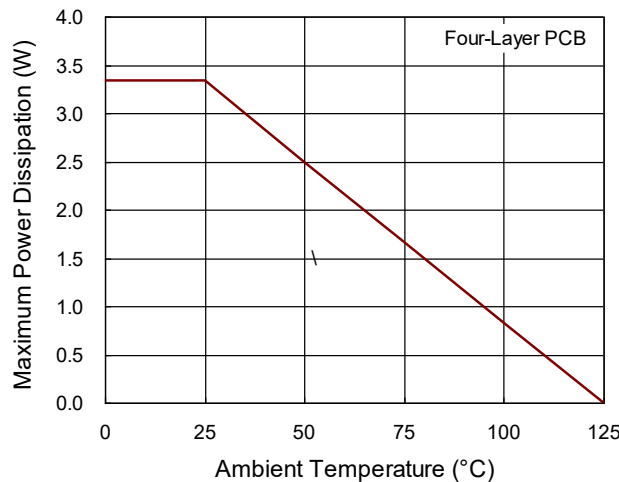
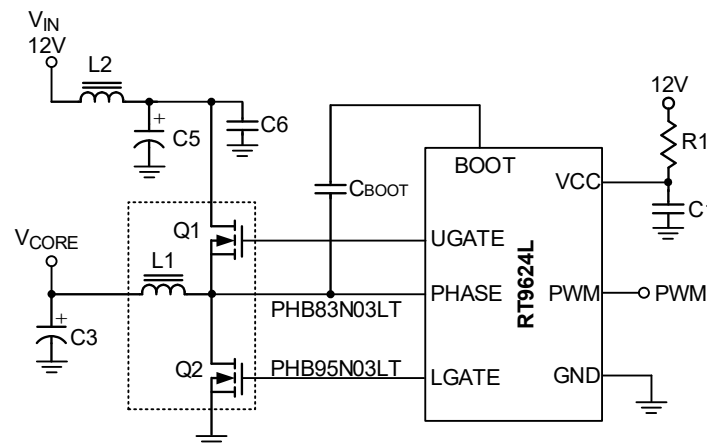


Figure 5. Derating Curve of Maximum Power Dissipation

17.10 Layout Consideration

[Figure 6](#) shows the schematic circuit of a synchronous buck converter to implement the RT9624C. The converter operates from 5V to 12V of input Voltage. For the PCB layout, it should be very careful. The power circuit section is the most critical one. If not configured properly, it will generate a large amount of EMI. The location of Q1, Q2, L1 should be very close.

Next, the trace from UGATE, and LGATE should also be short to decrease the noise of the driver output signals. PHASE signals from the junction of the power MOSFET, carrying the large gate drive current pulses, should be as heavy as the gate drive trace. The bypass capacitor C1 should be connected to GND directly. Furthermore, the bootstrap capacitors (C_{BOOT}) should always be placed as close to the pins of the IC as possible.



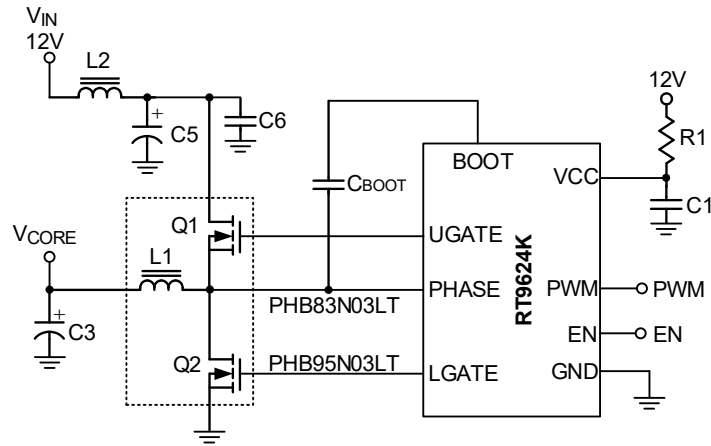
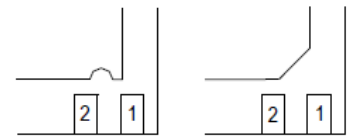
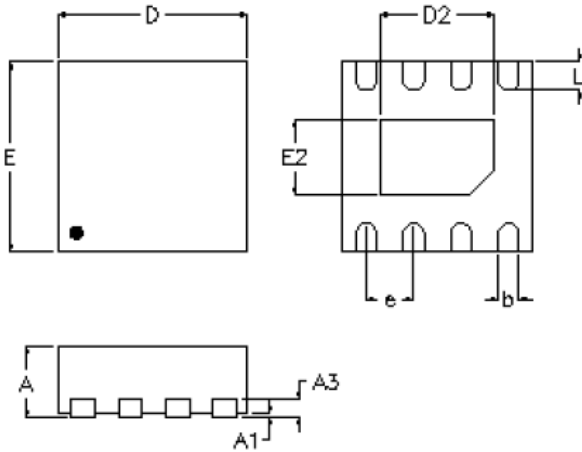


Figure 6. Synchronous Buck Converter Circuit

Note 6. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

18 Outline Dimension

18.1 WDFN-8SL 2x2 Package



DETAIL A

Pin #1 ID and Tie Bar Mark Options

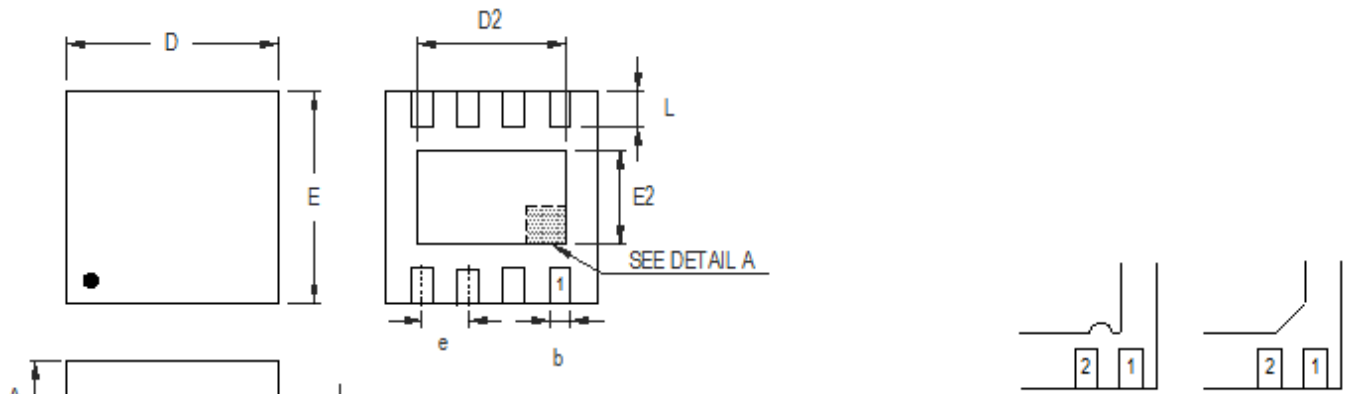
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min	Max	Min	Max	
A	0.700	0.800	0.028	0.031	
A1	0.000	0.050	0.000	0.002	
A3	0.175	0.250	0.007	0.010	
b	0.200	0.300	0.008	0.012	
D	1.900	2.100	0.075	0.083	
D2	Option1	1.150	1.250	0.045	0.049
	Option2	1.550	1.650	0.061	0.065
E	1.900	2.100	0.075	0.083	
E2	Option1	0.750	0.850	0.030	0.033
	Option2	0.850	0.950	0.033	0.037
e	0.500		0.020		
L	0.250	0.350	0.010	0.014	

W-Type 8SL DFN 2x2 Package

Note 7. The package of the RT9624K/RT9624L uses Option 1.

18.2 WDFN-8L 3x3 Package



DETAIL A

Pin #1 ID and Tie Bar Mark Options

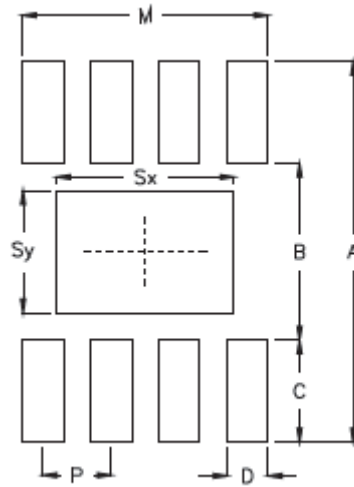
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	2.950	3.050	0.116	0.120
D2	2.100	2.350	0.083	0.093
E	2.950	3.050	0.116	0.120
E2	1.350	1.600	0.053	0.063
e	0.650		0.026	
L	0.425	0.525	0.017	0.021

W-Type 8L DFN 3x3 Package

19 Footprint Information

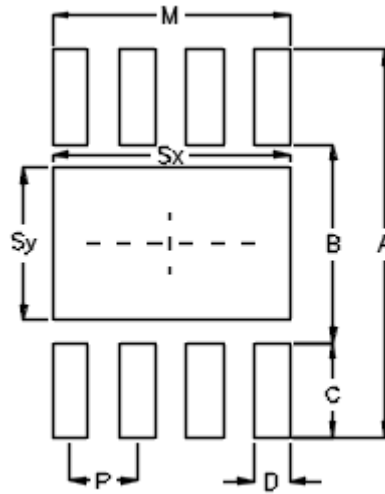
19.1 WDFN-8SL 2x2 Package



Package		Number of Pin	Footprint Dimension (mm)							Tolerance	
			P	A	B	C	D	Sx	Sy		M
V/W/U/XDFN2*2-8S	Option1	8	0.50	2.80	1.30	0.75	0.30	1.30	0.90	1.80	±0.05
	Option2							1.60	0.90		

Note 8. The package of the RT9624K/RT9624L uses Option 1.

19.2 WDFN-8L 3x3 Package

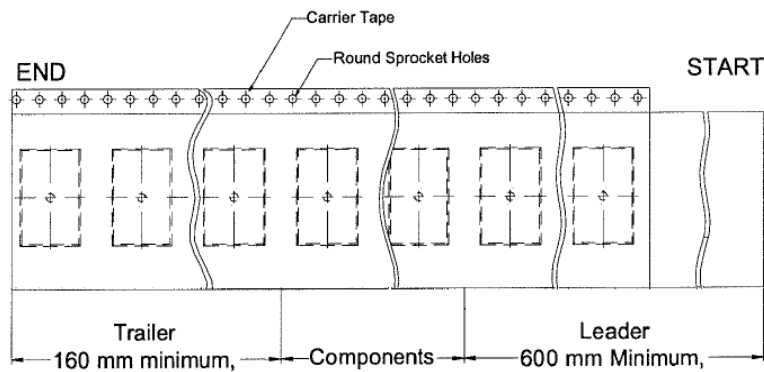
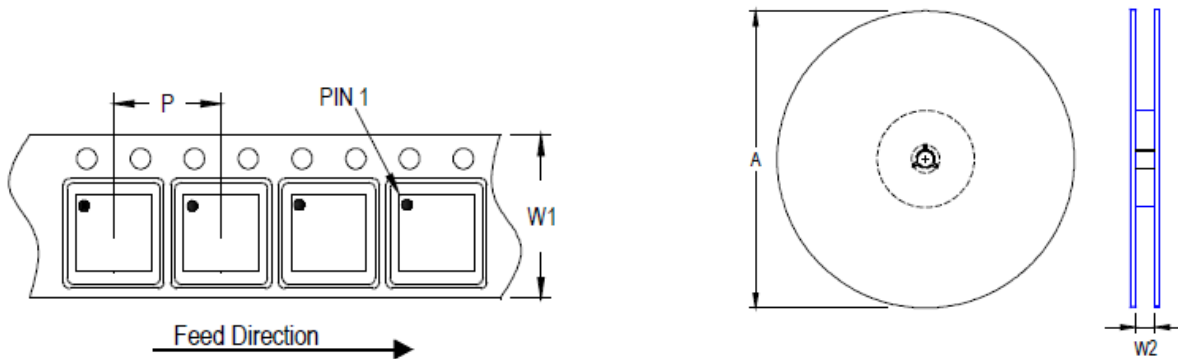


Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN3*3-8	8	0.65	3.80	1.94	0.93	0.35	2.30	1.50	2.30	±0.05

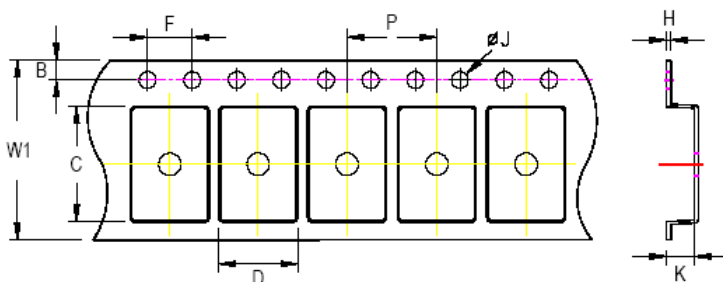
20 Packing Information

20.1 Tape and Reel Data

20.1.1 WDFN-8SL 2x2 Package



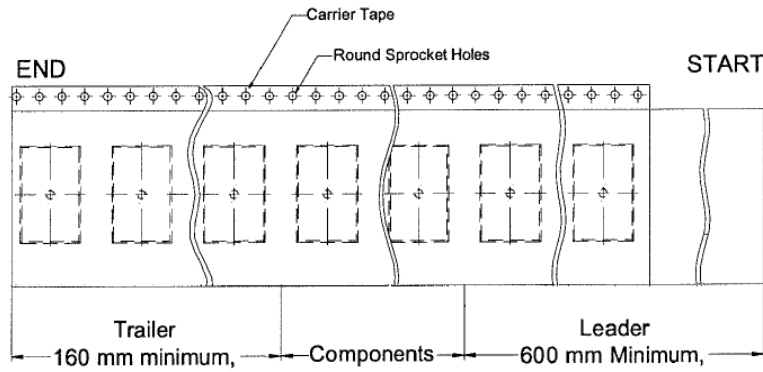
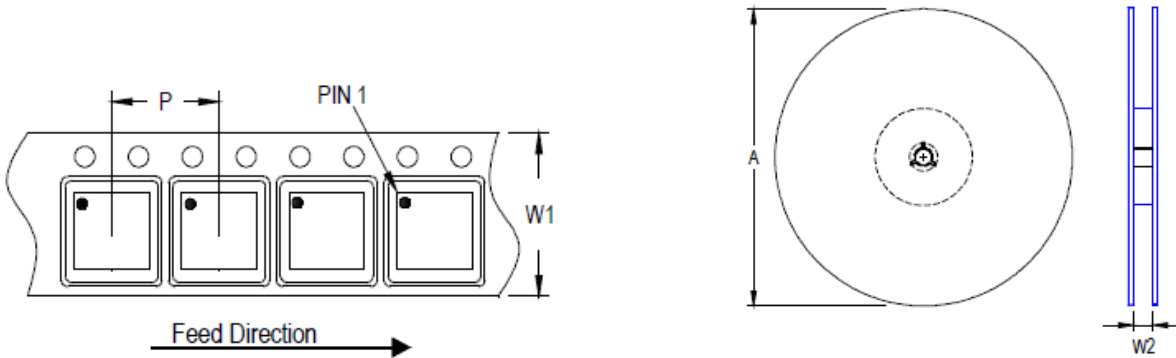
Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 2x2	8	4	180	7	2,500	160	600	8.4/9.9



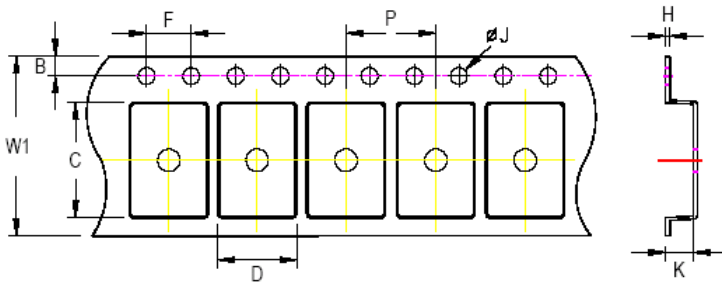
C, D, and K are determined by component size.
The clearance between the components and the cavity is as follows:
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1		P		B		F		ØJ		K		H
	Max	Min	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

20.1.2 WDFN-8L 3x3 Package



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4









C, D, and K are determined by component size.
The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm







20.2 Tape and Reel Packing

20.2.1 WDFN-8SL 2x2 Package

Step	Photo/Description	Step	Photo/Description
1	 Reel 7"	4	 3 reels per inner box Box A
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box Carton A

Container Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 2x2	7"	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

20.2.2 WDFN-8L 3x3 Package

Step	Photo/Description	Step	Photo/Description
1	 <p>Reel 7"</p>	4	 <p>3 reels per inner box Box A</p>
2	 <p>HIC & Desiccant (1 Unit) inside</p>	5	 <p>12 inner boxes per outer box</p>
3	 <p>Caution label is on backside of Al bag</p>	6	 <p>Outer box Carton A</p>

Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 3x3	7"	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}

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21 Datasheet Revision History

Version	Date	Description
00	2026/3/24	First Edition