RICHTEK® **RT9650B**

Single Phase Synchronous Rectified Buck MOSFET Driver

1 General Description

The RT9650B is a high-frequency, single-phase N-Channel MOSFET driver optimized for synchronous rectification in DC-DC converters and high-performance CPU voltage regulation.

It is engineered to minimize driver switching losses in low-voltage (5V) power systems for high-frequency applications.

The RT9650B features both UGATE and LGATE driving circuits and includes an internal bootstrap switch with low on-resistance, eliminating the need for an external bootstrap diode and reducing the system's BOM cost.

Its shoot-through protection ensures safe operation by preventing simultaneous conduction of high-side and low-side MOSFETs. For shutdown and power-saving modes, the IC supports a middle-state PWM input to drive UGATE and LGATE signals low.

The RT9650B is available in a compact WDFN-10L 2x2 package, suitable for junction temperatures from −10°C to 105°C.

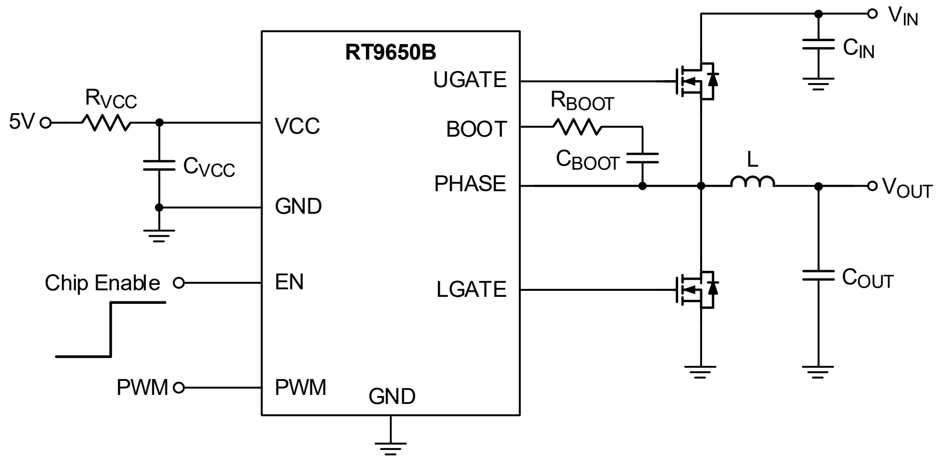
2 Features

- **Drive Two N-MOSFETs**
- **Shoot Through Protection**
- **Embedded Bootstrap Diode**
- **Support High Switching Frequency**
- **Fast Output Rising Time**
- **Compatible with 3.3V or 5V Middle State PWM Input**
- **Enable Control**
- **10-Lead WDFN Packages**

3 Applications

- Core Voltage Supplies for Desktop, Motherboard CPU
- High Frequency Low Profile DC-DC Converters
- High Current Low Voltage DC-DC Converters
- Core Voltage Supplies for GFX Card

4 Simplified Application Circuit



5 Ordering Information

RT9650B □-□

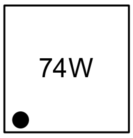
Packing
A: Standard

Package Type(1)
N: WDFN-10L 2x2 (W-Type)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information



74: Product Code
W: Date Code

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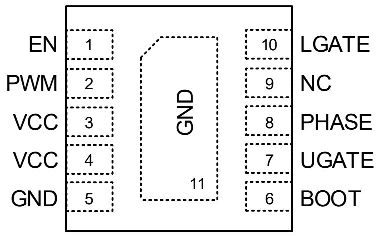
7 Pin Configuration

(TOP VIEW)

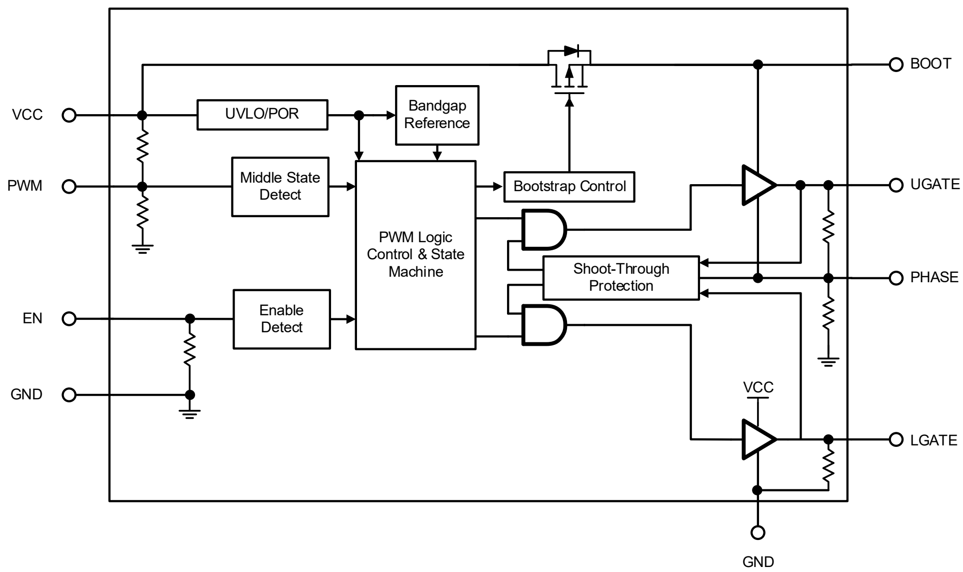


WDFN-10L 2x2

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Chip enable (Active High). When this pin is low, both UGATE and LGATE are driven to low.
2	PWM	PWM signal input. Connect this pin to the PWM output of the controller.
3, 4	VCC	5V supply voltage input. It is recommended adding RC filter (R = 1Ω, C = 1μF) for noise suppression. **Both the pins cannot be left floating.**
5, 11 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
6	BOOT	Bootstrap supply for high-side gate drive. Connect a ceramic capacitor with a value between 0.1μF to 1μF from BOOT to PHASE pins.
7	UGATE	High-side gate drive output. Connect this pin to the Gate of the high-side power N-MOSFET.
8	PHASE	Connect this pin to the source of the high-side N-MOSFET and the drain of the low-side N-MOSFET.
9	NC	No connection.
10	LGATE	Low-side gate driver output. Connect this pin to the gate of the low-side power N-MOSFET.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, VCC
  - DC ---------- –0.3V to 6V
  - < 20ns---------- –2.5V to 7.5V
- BOOT to PHASE
  - DC ---------- –0.3V to 6V
  - < 20ns---------- –5V to 7.5V
- PHASE to GND
  - DC ---------- –0.3V to 32V
  - < 20ns---------- –8V to 38V
- LGATE to GND
  - DC ---------- –0.3V to 6V
  - < 20ns---------- –2.5V to 7.5V
- UGATE to PHASE
  - DC ---------- –0.3V to 6V
  - < 20ns---------- –5V to 7.5V
- EN, PWM to GND ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-10L 2x2 ---------- 1.39W
- Package Thermal Resistance (Note 3)
  - WDFN-10L 2x2, θ_{JA} ---------- 57.45°C/W
  - WDFN-10L 2x2, θ_{JC} ---------- 6.37°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  - HBM (Human Body Model)---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VCC --- 4.5V to 5.5V
- Junction Temperature Range -- −10°C to 105°C

Note 5. The device is not guaranteed to function outside its operating conditions.

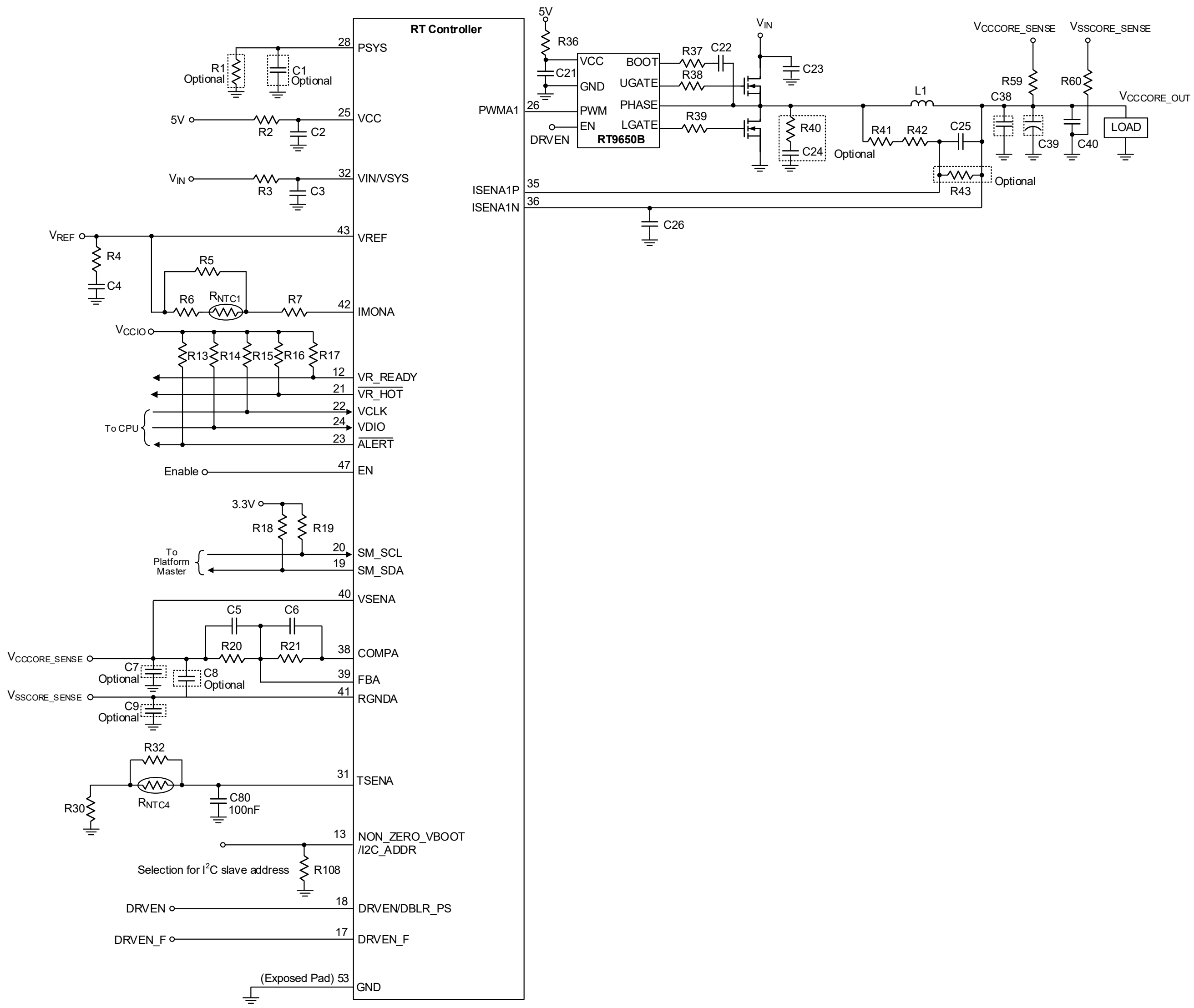
12 Electrical Characteristics

(V_{CC} = 5V, typical values are referenced to T_J = 25°C, Min and Max values are referenced to T_J from –10°C to 105°C, unless otherwise noted.)

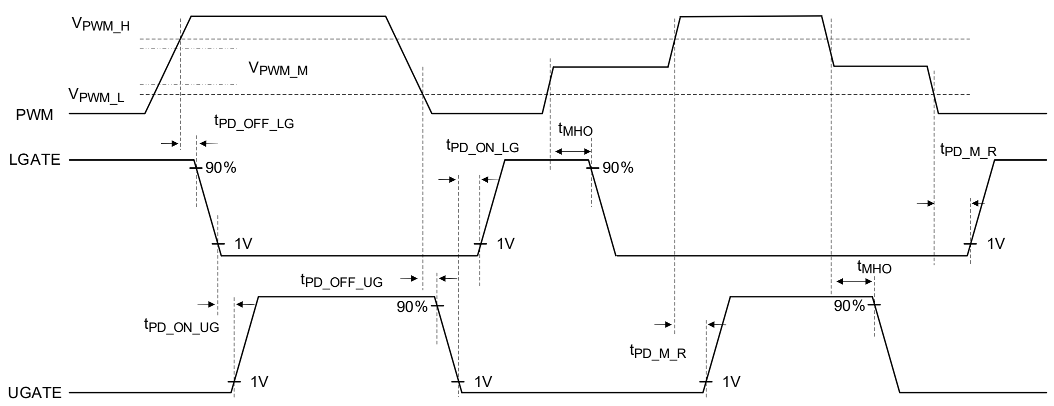
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply						
Power Supply Voltage	V_{CC}		4.5	--	5.5	V
Quiescent Current in Normal Operation	I_Q	V_{PWM} = Middle, V_{EN} = 5V	--	80	--	μ A
Quiescent Current in Standby Operation	I_{SHDN}	V_{PWM} = Middle, V_{EN} = 0V, T_J = 25°C	--	6	--	μA
Power-On Reset (POR)						
POR Rising Threshold	V_{POR_R}	V_{CC} Rising	--	4.1	4.3	V
POR Falling Threshold	V_{POR_F}	V_{CC} Falling	3.6	3.8	--	V
EN Input						
EN Input Voltage Rising Threshold	V_{EN_R}		1.35	--	--	V
EN Input Voltage Falling Threshold	V_{EN_F}		--	--	0.65	V
PWM Input						
Maximum Input Current	I_{PWM}	V_{PWM} = 0V or 5V	--	--	350	μA
PWM Input Middle State Threshold	V_{PWM_M}	V_{PWM} = Floating	1.4	--	2.2	V
PWM Input Logic-High	V_{PWM_H}		2.72	--	--	V
PWM Input Logic-Low	V_{PWM_L}		--	--	0.78	V
Timing						
Middle State to UGATE/LGATE Rising Propagation Delay	$t_{PD\_M\_R}$	No load	--	25	--	ns
Middle State Hold-Off Time	t_{MHO}	No load	--	50	--	ns
UGATE Rising Time	t_{UGR}	6nF load, UGATE rising edge 10% to 90%	--	16	--	ns
UGATE Falling Time	t_{UGF}	6nF load, UGATE falling edge 10% to 90%	--	16	--	ns
LGATE Rising Time	t_{LGR}	10nF load, LGATE rising edge 10% to 90%	--	32	--	ns
LGATE Falling Time	t_{LGF}	10nF load, LGATE falling edge 10% to 90%	--	16	--	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
UGATE Turn-On Propagation Delay	$t_{PD\_ON\_UG}$	V_{BOOT} – V_{PHASE} = 5V See timing diagram	--	30	--	ns
UGATE Turn-Off Propagation Delay	$t_{PD\_OFF\_UG}$	V_{BOOT} – V_{PHASE} = 5V See timing diagram	--	30	--	ns
LGATE Turn-On Propagation Delay	$t_{PD\_ON\_LG}$	See timing diagram	--	30	--	ns
LGATE Turn-Off Propagation Delay	$t_{PD\_OFF\_LG}$	See timing diagram	--	20	--	ns
Standby Mode Exit Delay Time	t_{STBY_EXIT}	EN = L to H	--	--	30	μs
Minimum UGATE On-Time	t_{ON_MIN}	No load	--	35	--	ns
Output						
UGATE Drive Source Resistance	R_{UG_sr}	V_{BOOT} – V_{PHASE} = 5V, I_{Source} = 100mA	--	0.8	--	Ω
UGATE Drive Sink Resistance	R_{UG_sk}	V_{BOOT} – V_{PHASE} = 5V, I_{Sink} = 100mA	--	0.6	--	Ω
LGATE Drive Source Resistance	R_{LG_sr}	I_{Source} = 100mA	--	1	--	Ω
LGATE Drive Sink Resistance	R_{LG_sk}	I_{Sink} = 100mA	--	0.4	--	Ω
Internal Bootstrap Switch						
Internal Boost Switch On-Resistance	R_{BOOT}	VCC to BOOT, 10mA	--	--	40	Ω

13 Typical Application Circuit



14 Timing Diagram



15 Operation

15.1 Power-On Reset (POR)

The POR block monitors the voltage of the VCC pin. When the VCC voltage exceeds the POR rising threshold, the POR block output becomes high, allowing UGATE and LGATE to be controlled by the PWM input voltage. Conversely, if the VCC voltage does not exceed the threshold, the POR output remains low, and both UGATE and LGATE are pulled low.

15.2 Enable Detection

The MOSFET driver is enabled when the EN pin input voltage exceeds the EN rising threshold. When both the EN input and POR output are high, UGATE and LGATE are controlled by the PWM input voltage. If the EN input is low, both UGATE and LGATE are pulled low, and the PWM input terminal is opened.

15.3 Middle-State Detection

When both the POR block output and EN pin voltage are high, UGATE and LGATE are controlled by the PWM input. The PWM input has three modes: high, low, and middle state. If the PWM input is within the middle-state window, both UGATE and LGATE outputs are low. When the PWM input exceeds its Logic-High, UGATE is high and LGATE is low. Conversely, when the PWM input is below its Logic-Low, UGATE is low and LGATE is high.

15.4 Bootstrap Control

The bootstrap control block manages the integrated bootstrap switch. When LGATE is high (indicating the low-side MOSFET is on), the bootstrap switch is activated to charge the bootstrap capacitor connected to the BOOT pin. Conversely, when LGATE is low (indicating the low-side MOSFET is off), the bootstrap switch is deactivated, disconnecting the VCC pin from the BOOT pin.

15.5 Shoot-Through Protection

The shoot-through protection block ensures safe operation by implementing dead time, during which both the high-side and low-side MOSFETs are turned off. This mechanism prevents the high-side and low-side MOSFETs from being turned on simultaneously, effectively avoiding shoot-through currents between them.

16 Application Information

(Note 6)

The RT9650B is a high-frequency, synchronous rectified, single-phase dual-MOSFET driver that incorporates Richtek's advanced MOSFET driver technologies. It is designed to support a wide range of applications, from standard MOSFET driving to high-performance CPU/GPU voltage regulation (VR) driving.

16.1 Supply Voltage and Power-On Reset

The RT9650B operates with a VCC = 5V supply and is designed to drive both high-side and low-side N-MOSFETs using an external PWM control signal. It features a power-on protection function that keeps UGATE and LGATE low until the VCC voltage exceeds the rising threshold voltage.

16.2 Enable and Disable

The RT9650B features an EN pin for sequence control. When the EN pin rises above the V_{EN_R} trip point, the RT9650B initiates a new initialization and follows the PWM command to control UGATE and LGATE. Conversely, when the EN pin falls below the V_{EN_F} trip point, the RT9650B shuts down, keeping UGATE and LGATE low and the PWM input terminal open.

16.3 Middle State PWM Input

After initialization, the PWM signal controls the operation. A rising PWM signal first forces LGATE low, then allows UGATE to go high after a non-overlapping time to prevent shoot-through current. Conversely, a falling PWM signal first forces UGATE low, and once UGATE and PHASE reach a predetermined low level, LGATE is allowed to turn high. The PWM signal is considered "High" when above the rising threshold and "Low" when below the falling threshold. When the PWM signal enters and remains within the middle state window, the output drivers are disabled, and both MOSFET gates are pulled and held low. If the PWM signal is left floating, the pin is maintained around 1.8V by the internal divider, providing the PWM controller with a recognizable level.

16.4 Internal Bootstrap Power Switch

The RT9650B incorporates an internal bootstrap power switch that eliminates the need for an external bootstrap diode. This integration simplifies PCB design and reduces the total BOM cost of the system, making an external bootstrap diode unnecessary in real applications.

16.5 Non-Overlap Control

The non-overlap circuit prevents gate driver overlap during UGATE pull-down and LGATE pull-up transitions by monitoring the PHASE node and the high-side gate drive (UGATE-PHASE). When the PWM input signal goes low, UGATE begins to pull low after a propagation delay. Before LGATE is pulled high, the non-overlap protection circuit ensures the monitored voltages drop below 1V. Once they do, LGATE turns high, ensuring UGATE is low before LGATE pulls high. Similarly, during LGATE pull-down and UGATE pull-up transitions, the circuit monitors the LGATE voltage. When LGATE falls below 1V, UGATE goes high after a propagation delay.

16.6 Driving Power MOSFETs

The DC input impedance of the power MOSFET is extremely high. When V_{gs1} or V_{gs2} is at 5V, the gate draws only a few nano-amperes of current, making the current negligible once the gate reaches the "ON" level. However, the gate-to-source capacitance must be considered, as it requires relatively large currents to rapidly drive the gate up and down by 5V. This is necessary to switch the drain current on and off at the required speed. The required gate drive currents are calculated accordingly.

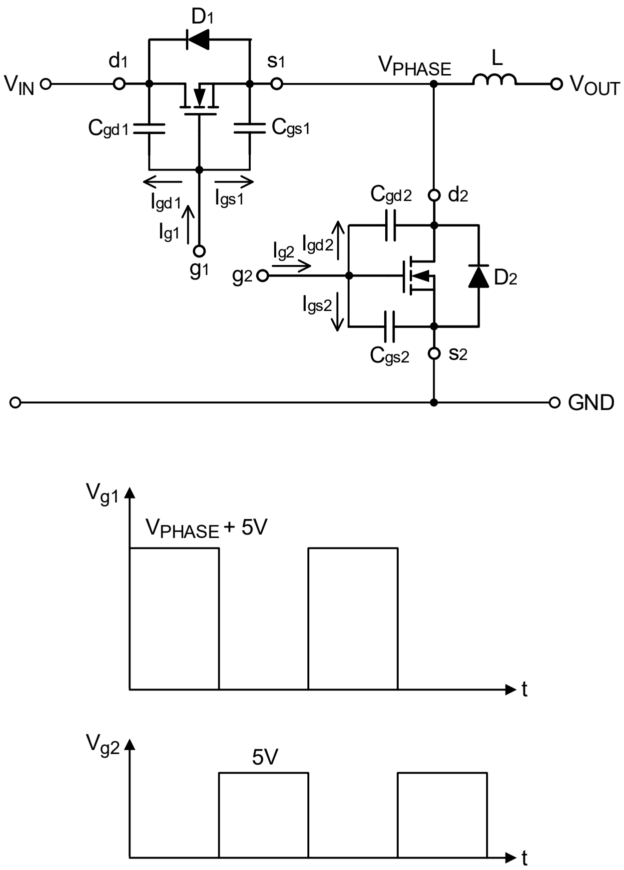


Figure 1. Equivalent Circuit and Waveforms (VCC = 5V)

In Figure 1, the current I_{g1} and I_{g2} are required to drive the gate voltage up to 5V, which involves charging the capacitors C_{gd1}, C_{gd2}, C_{gs1}, and C_{gs2}. Here, C_{gs1} and C_{gs2} represent the gate-to-source capacitances of the high-side and low-side power MOSFETs, respectively, and are commonly referred to as "C_{iss}" (input capacitance) in datasheets. Similarly, C_{gd1} and C_{gd2} are the gate-to-drain capacitances of the high-side and low-side power MOSFETs, referred to as "C_{rss}" (reverse transfer capacitance) in datasheets. For example, if t_{r1} and t_{r2} are the rising times of the high-side and low-side power MOSFETs, the required currents I_{gs1} and I_{gs2} can be calculated accordingly.

$$I_{gs1} = C_{gs1}\frac{dV_{g1}}{dt} = \frac{C_{gs1} \times 5}{t_{r1}} \quad (1)$$

$$I_{gs2} = C_{gs1}\frac{dV_{g2}}{dt} = \frac{C_{gs1} \times 5}{t_{r2}} \quad (2)$$

Before driving the gate of the high-side MOSFET up to 5V, the low-side MOSFET must be off. Similarly, the high-side MOSFET will be turned off before the low-side is turned on. As shown in Figure 1, the body diode “D2” will be turned on before the high-side MOSFET is activated.

$$I_{gd1} = C_{gd1}\frac{dV}{dt} = C_{gd1}\frac{5}{t_{r1}} \quad (3)$$

Before the low-side MOSFET is turned on, the C_{gd2} is charged to VIN. As C_{gd2} reverses polarity and g2 is charged up to 5V, the required current is:

$$I_{gd2} = C_{gd2}\frac{dV}{dt} = C_{gd2}\frac{V_{IN}+5}{t_{r2}} \quad (4)$$

To illustrate, let's calculate these currents in a typical scenario. Consider a synchronous rectified buck converter with an input voltage V_{IN} = 12V, V_{gs1} = 5V, V_{gs2} = 5V. The high-side MOSFET is SiRA14, with C_{iss} = 1450pF, C_{rss} = 38pF, and t_r = 8ns. The low-side MOSFET is SiRA06, with C_{iss} = 3595pF, C_{rss} = 79pF, and t_r = 10ns. Using equations (1) and (2), the required currents can be calculated accordingly:

$$I_{gs1} = \frac{(1450\text{-}38) \times 10^{-12} \times 5}{8 \times 10^{-9}} = 0.883 \quad (A) \quad (5)$$

$$I_{gs2} = \frac{(3595\text{-}79) \times 10^{-12} \times 5}{10 \times 10^{-9}} = 1.758 \quad (A) \quad (6)$$

From equations (3) and (4):

$$I_{gd1} = \frac{38 \times 10^{-12} \times 5}{8 \times 10^{-9}} = 0.024 \quad (A) \quad (7)$$

$$I_{gd2} = \frac{79 \times 10^{-12} \times (12+5)}{10 \times 10^{-9}} = 0.134 \quad (A) \quad (8)$$

The total current required from the gate driving source can be calculated using the following equations:

$$I_{g1} = I_{gs1} + I_{gd1} = (0.883 + 0.024) = 0.907 \quad (A) \quad (9)$$

$$I_{g2} = I_{gs2} + I_{gd2} = (1.758 + 0.134) = 1.892 \quad (A) \quad (10)$$

Through a similar calculation, we can also determine the sink current required from the turned-off MOSFET.

16.7 Bootstrap Circuit Component Selection

To reduce power consumption, the transitional bootstrap circuit is replaced by a MOSFET switch integrated into the RT9650B, allowing for more space saving. Now, only an external capacitor (C_{BOOT}) needs to be connected between BOOT and PHASE. To effectively turn on the high-side MOSFET, the energy stored in C_{BOOT} must be greater than the total gate charge of the high-side MOSFET. Figure 2 illustrates the bootstrap circuit of the RT9650B. In this figure, the gate charges of the high-side and low-side MOSFETs are defined as Q_{gH} and Q_{gL}, respectively. For charging C_{BOOT}, the internal bootstrap switch and the low-side MOSFET are turned on simultaneously, creating a charging path from V_{CC}. The sum of C_{BOOT} charging current and the low-side MOSFET driving current is defined as I_{VCC}. Consequently, the voltage V_{CBOOT} on C_{BOOT} can be represented as follows.

$$V_{CBOOT} = V_{CC} - \frac{V_{IN} f_{SW}}{V_{IN} - V_{OUT}}\left[(Q_{gH} + Q_{gL})R_{VCC} + Q_{gH}(R_{BOOT(max)} + R_{BOOT\_ext})\right]$$

where

V_{IN}: Input voltage

V_{OUT}: Output voltage

V_{CC}: Supply voltage to VCC

f_{SW}: Switching frequency

$R_{BOOT(max)}$: Internal boost switch on resistance

R_{BOOT_ext}: External bootstrap resistor

Calculating V_{CBOOT} is essential to ensure the safe operation of the MOSFET in the ohmic region. Therefore, V_{CBOOT} must be sufficiently large to prevent the high-side MOSFET from being incompletely turned on.

The value of the bootstrap capacitor is defined by the following:

$$C_{BOOT} \geq \frac{Q_{gH}}{\Delta V_{CBOOT}}$$

where

ΔV_{CBOOT}: Maximum allowable voltage drop on bootstrap capacitor.

In practice, using a low-value capacitor C_{BOOT} can lead to overcharging, potentially damaging the IC. To minimize the risk of overcharging and reduce ripple on C_{BOOT}, the bootstrap capacitor should be no smaller than 0.1μF. At least one low-ESR capacitor is recommended to ensure effective local decoupling, with ceramic or tantalum capacitors being preferred. Additionally, C_{BOOT} selection is critical, especially in applications requiring fast VID changes or fast soft-start, as these demand shorter C_{BOOT} charging times. The charging time depends on the inductor, output capacitor, and operating frequency. For assistance in selecting the appropriate C_{BOOT} value for such applications, contact our sales representative or a Richtek distributor in your area.

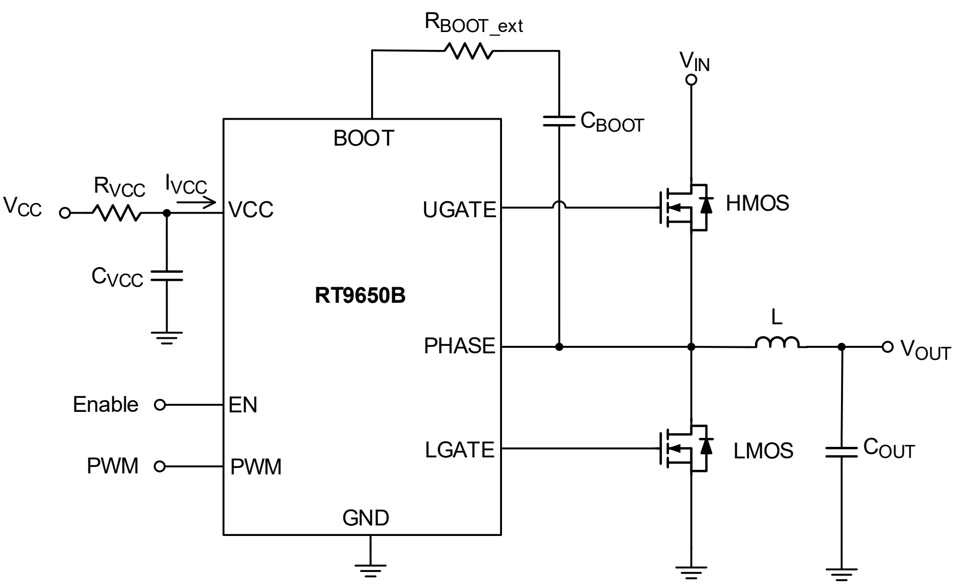


Figure 2. Partial Bootstrap Circuit

16.8 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 105°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-10L 2x2 package, the thermal resistance, θ_{JA}, is 57.45°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (105°C − 25°C) / (57.45°C/W) = 1.39W for a WDFN-10L 2x2 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 3 allow the user to see the effect of rising ambient temperature on the maximum power dissipation.

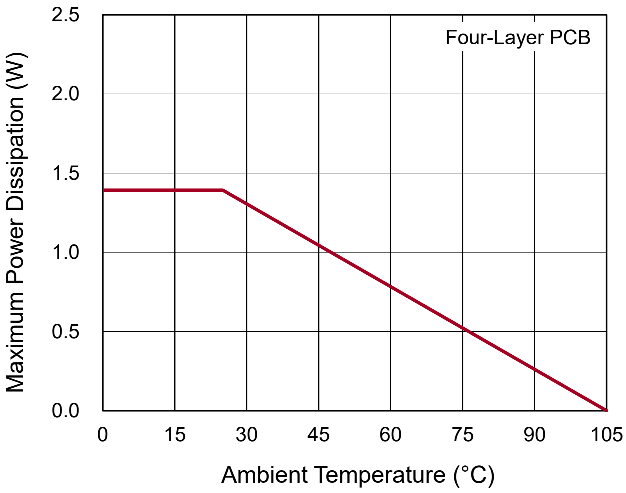


Figure 3. Derating Curve of Maximum Power Dissipation

16.9 Layout Consideration

An example of PCB layout guide is shown in Figure 4 for reference. Make sure to consider the following before starting a layout using the RT9650B.

- Make traces of the high current paths as short and wide as possible.
- Put the input capacitor as close as possible to the MOSFET.
- The PHASE node encounters high frequency voltage swings so it should be kept in a small area. Keep sensitive components away from the PHASE node to prevent noise coupling.
- The GND pin should be connected to a strong ground plane for heat sinking and noise protection.
- The ground of VCC is recommended connecting to GND layer through via, and the decoupling capacitor (C_{VCC}) should be placed near the VCC pin. No via connection is recommended.
- For PCB layout, care must be taken. The power circuit section is the most critical one. If not configured properly, it will generate a large amount of EMI. The location of the high-side MOSFET, low-side MOSFET, and inductor should be very close to each other. Next, the trace from UGATE and LGATE should also be short to minimize noise in the driver output signals. The PHASE signals from the junction of the power MOSFET carrying the large gate drive current pulses should be as heavy as the gate drive trace. The bypass capacitor C_{VCC} should be connected to GND directly. Furthermore, the bootstrap capacitor (C_{BOOT}) should always be placed as close to the pins of the IC as possible.

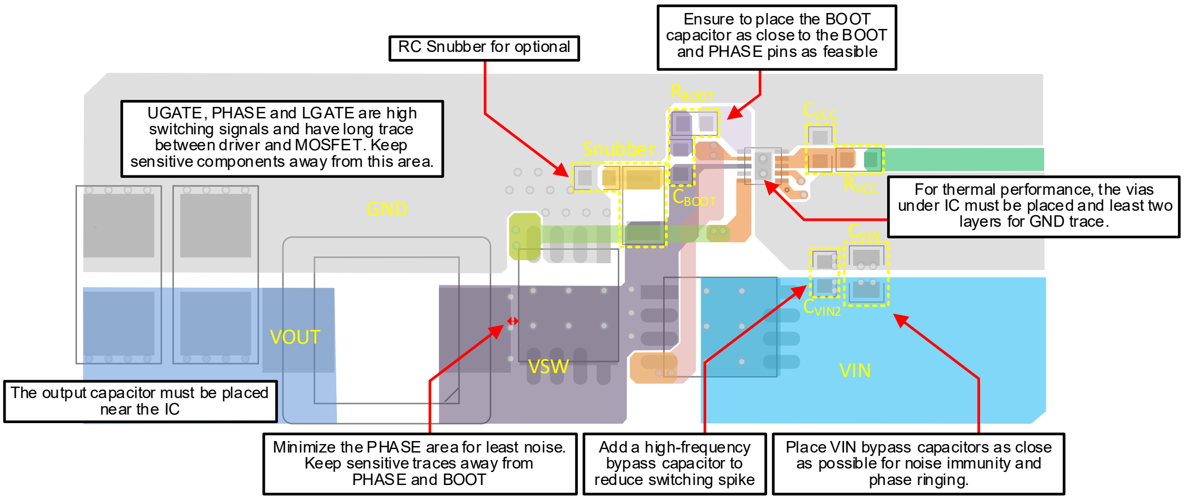
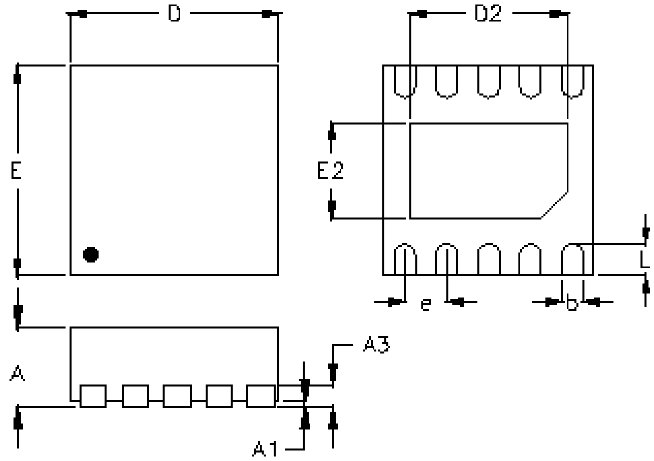
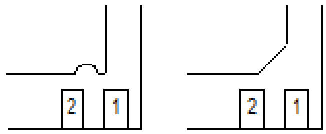


Figure 4. PCB Layout Guide

Note 6. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

17 Outline Dimension





DETAIL A

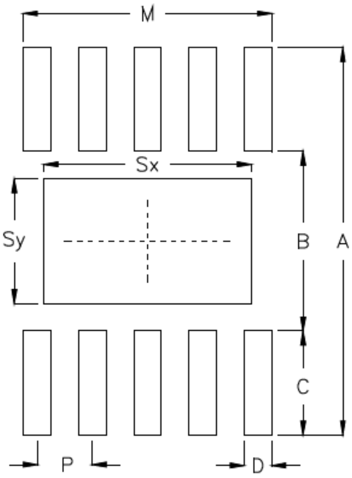
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	1.900	2.100	0.075	0.083
D2	1.450	1.550	0.057	0.061
E	1.900	2.100	0.075	0.083
E2	0.850	0.950	0.033	0.037
e	0.400		0.016	
L	0.250	0.350	0.010	0.014

W-Type 10L DFN 2x2 Package

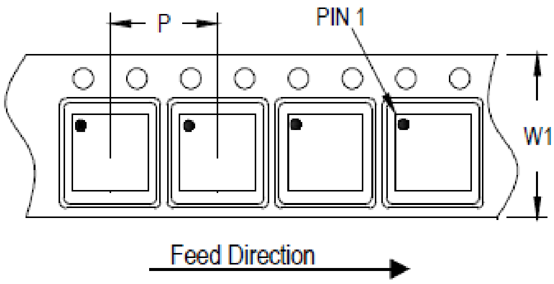
18 Footprint Information

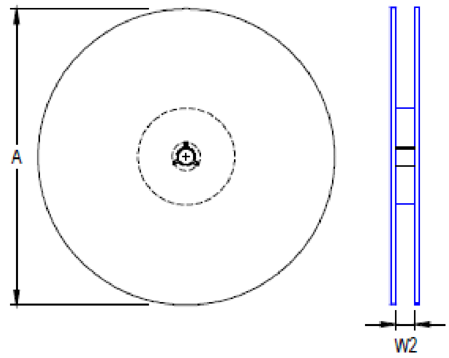


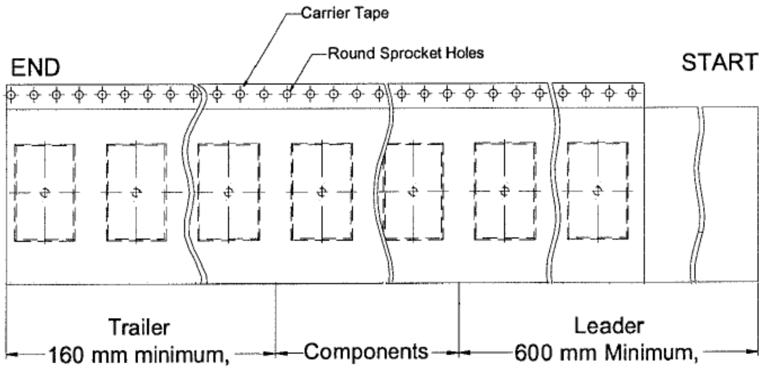
Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2x2-10	10	0.40	2.80	1.30	0.75	0.20	1.50	0.90	1.80	±0.05

19 Packing Information

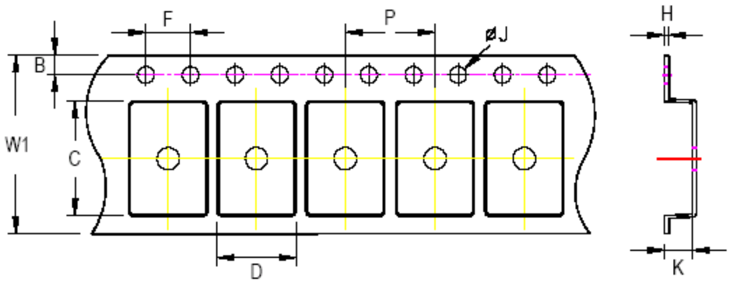
19.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 2x2	8	4	180	7	2,500	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 2x2	7”	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description
00	2025/10/23	First Edition
01	2026/4/8	General Description Absolute Maximum Ratings Operation Application Information