80mΩ, 1A Power Multiplexer

General Description

The RT9705B is a dual input single output power multiplexer specifically designed to provide seamless voltage transition between two independent power suppliers. Equipped with two low $R_{DS(ON)}$ N-Channel MOSFETs driven by internal charge pump circuitry, the RT9705B is able to deliver 1A output current with only 80mV voltage drop. Manual or auto switching mode is easily selected by two digital inputs D1 and D0. When both D0 and D1 are selected high, the RT9705B enters shutdown mode and consumes minimum power making it ideal suitable for battery powered equipments. A STAT pin with open drain output is provided to indicate the switch status. A user-programmable up to 1.25A current limit function is available for maximum safety in various applications.

The RT9705B provides comprehensive protection functions, including adjustable current limit, over temperature protection, soft start function for minimum inrush current, cross-conduction protection, and reverse conduction protection. These features greatly simplify power multiplexer design. The RT9705B is available in TSSOP-8 package requiring minimum board area and smallest components.

Ordering Information

RT9705B □□

- Package Type
  C : TSSOP-8
- Lead Plating System
  P : Pb Free
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **Adjustable Current Limiting up to 1.25A**
- **Built-In (Typically 80mΩ) N-Channel MOSFET**
- **Reverse Current Flow Blocking (no body diode) i.e. Output Can Be Forced Higher than Input (Off-State)**
- **Low Supply Current :**
  - **55μA Typical at Switch on State**
  - **Less than 0.5μA Typical at Switch Off State**
- **Guaranteed 1A Continuous Load Current**
- **Wide Input Voltage Ranges : 2.8V to 5.5V**
- **Open-Drain STAT Output**
- **Hot Plug-In Application (Soft-Start)**
- **Thermal Shutdown Protection**
- **Smallest TSSOP-8 Package Minimizes Board Space**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

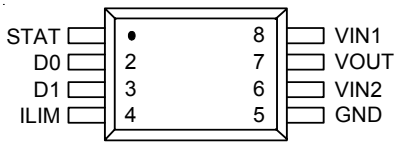
- LCD Monitor, LCD-TV
- Information Appliance and Set-Top Box
- Battery-Powered Equipment
- ACPI Power Distribution
- Motherboard & Notebook PCs
- Mini PCI & PCI-Express Cards
- PCMCIA & New Cards

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

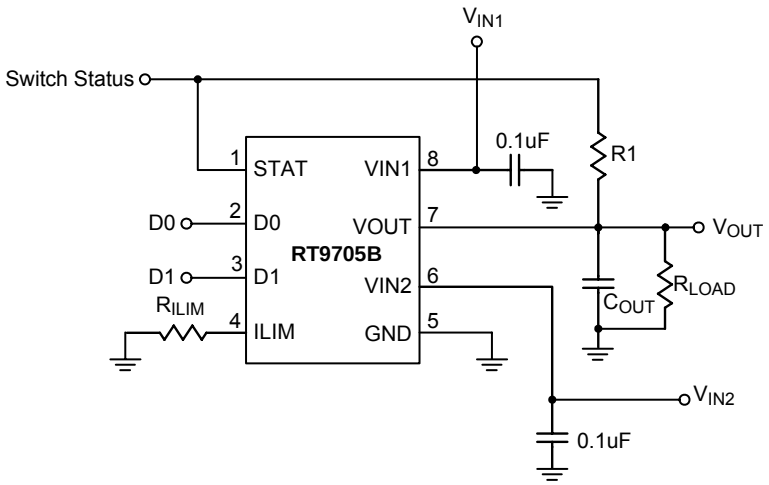
Pin Configurations

(TOP VIEW)



TSSOP-8

Typical Application Circuit



Functional Pin Description

Pin Name	Pin Function
VIN1	Power Input1 Voltage
VIN2	Power Input2 Voltage
VOUT	Output Voltage
GND	Ground
STAT	STAT is an open-drain output that is Hi-Z if the VIN2 switch is ON.
D0, D1	The truth table shown below illustrates the functionality of D0 and D1.
ILIM	A resistor R_{ILIM} from ILIM to GND sets the current limit I_{LIM} to (500/R_{ILIM}).

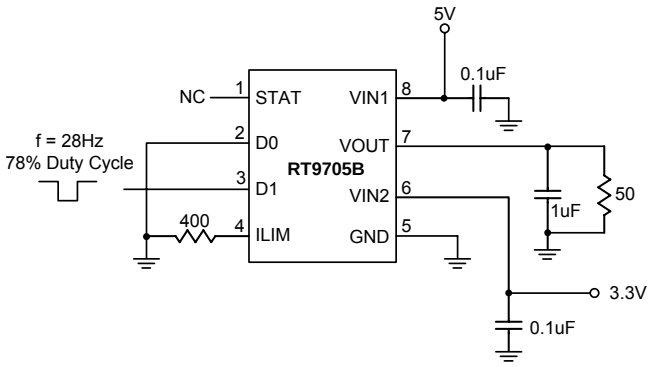
Table 1. Truth Table

D1	D0	V_{IN2}>V_{IN1}	STAT	V_{OUT}
0	0	X	Hi-Z	V_{IN2}
0	1	No	0	V_{IN1}
0	1	Yes	Hi-Z	V_{IN2}
1	0	X	0	V_{IN1}
1	1	X	0	0

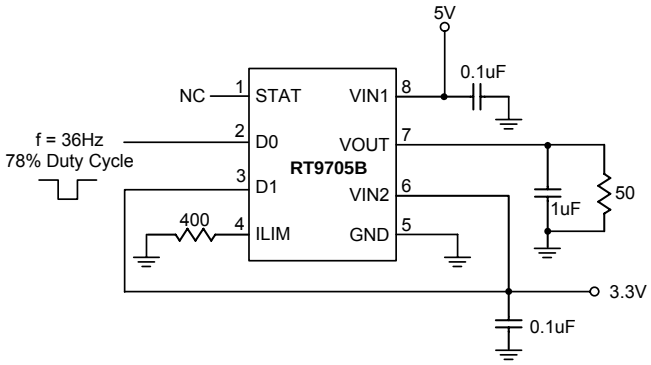
Notes for Table 1.

1. X : Don’ t care
2. Hi-Z: High impedance node
3. D0 and D1 cannot be floating which will lead to an unknown state.
4. An internal MOSFET with 2kΩ $R_{DS(ON)}$ turns on and softly discharges the output voltage when D0 = D1 = 1.

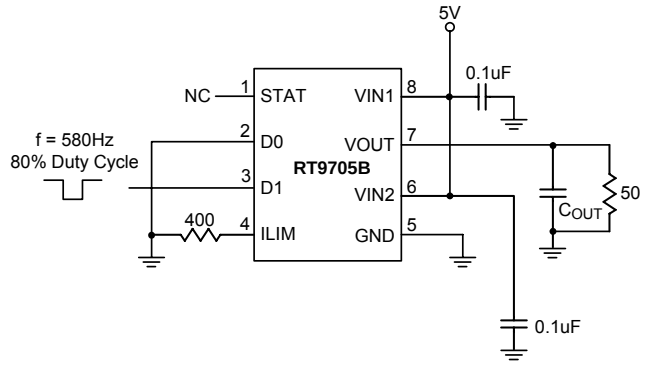
Test Circuits



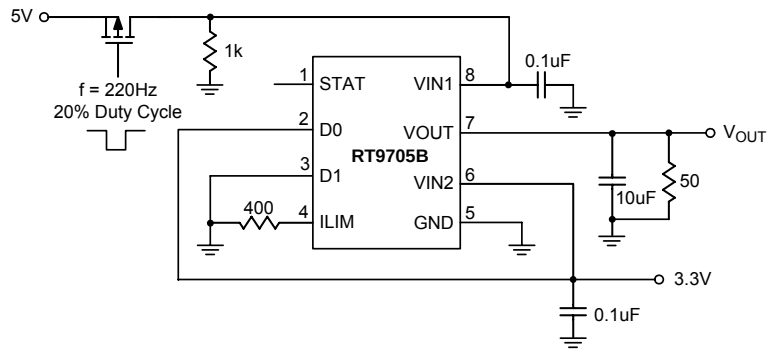
Test Circuit 1



Test Circuit 2

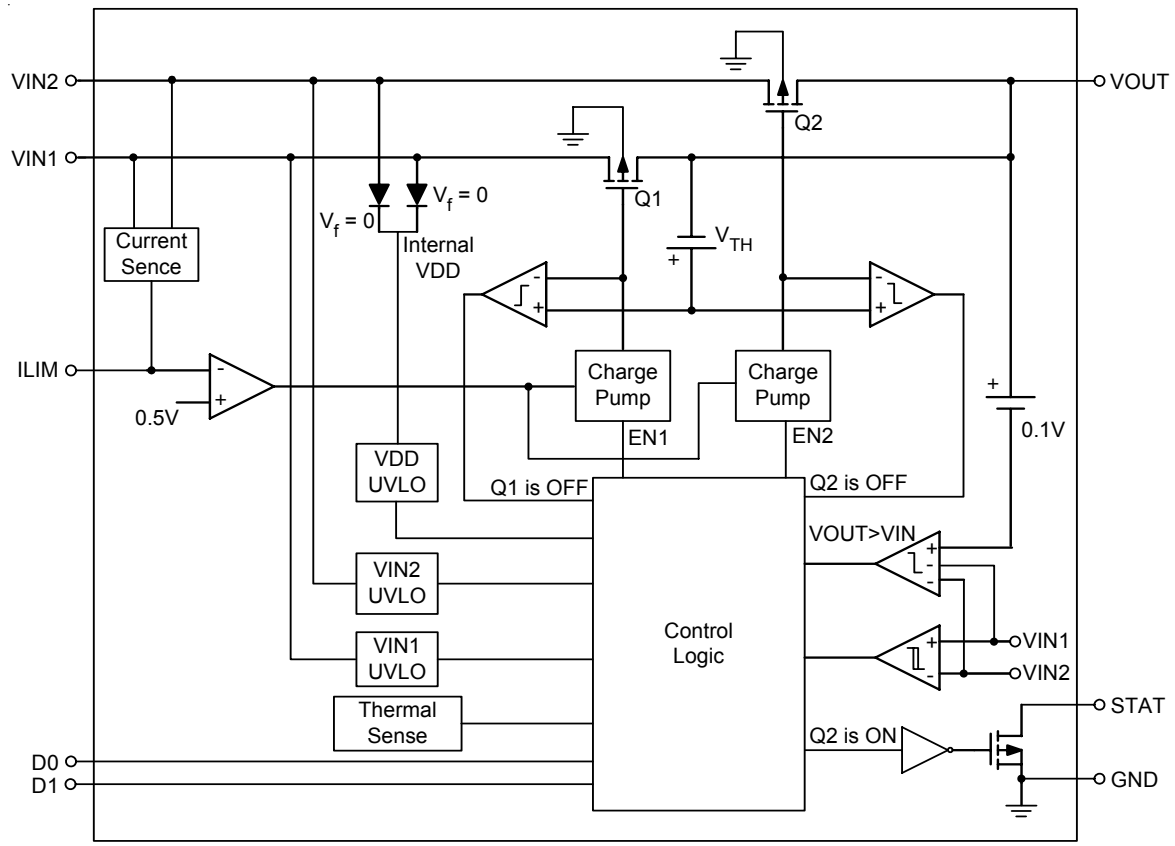


Test Circuit 3

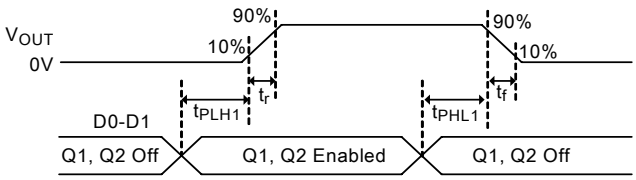


Test Circuit 4

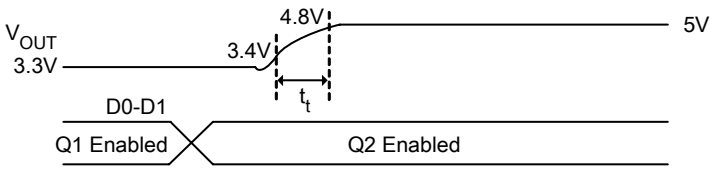
Function Block Diagram



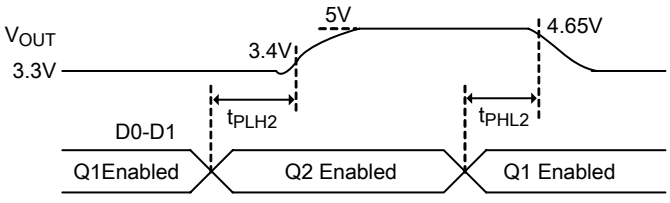
Timing Diagram



(a)



(b)



(c)

Absolute Maximum Ratings (Note 1)

- Input Voltage, VIN1 & VIN2 ---------- –0.3V to 6.0V
- Logic Inputs Voltage, D0 &D1 ---------- –0.3V to 6.0V
- Output Voltage, VOUT, STAT & ILIM ---------- –0.3V to 6.0V
- Power Dissipation, P_D @ T_A = 25°C
  TSSOP-8 ---------- 0.43W
- Package Thermal Resistance (Note 2)
  TSSOP-8, θ_{JA} ---------- 230°C/W
- Junction Temperature ---------- 125°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Input Voltage
  V_{IN1} (if V_{IN2} ≥2.8V) ---------- 2.3V to 5.5V
  V_{IN1} (if V_{IN2} < 2.8V) ---------- 2.8V to 5.5V
  V_{IN2} (if V_{IN1} ≥2.8V) ---------- 2.3V to 5.5V
  V_{IN2} (if V_{IN1} < 2.8V) ---------- 2.8V to 5.5V
- Logic Inputs Voltage (D0 &D1) ---------- 0V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN1} = V_{IN2} = 3.6V, C_{IN} = C_{OUT} = 1μF, R_{ILIM} = 400Ω, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Switch						
Switch On Resistance	$R_{DS(ON)}$	V_{IN1} = V_{IN2} = 3.6V, I_{OUT} = 1A	--	80	95	mΩ
		V_{IN1} = V_{IN2} = 3.6V, I_{OUT} = 1A –5°C ≤ T_A ≤ 85°C (Note 5)	--	--	120	
Logic Inputs (D0 and D1)						
Logic Low to High Threshold Voltage	V_{TH_LH}		1.5	--	2.1	V
Threshold Hysteresis	V_{TH_HYS}		--	500	--	mV
Input Current at D0 or D1	I_{IL}	D0 or D1 = High, Sink Current	--	--	1	μA
	I_{IH}	D0 or D1 = Low, Source Current	--	--	1	

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply and Leakage Currents						
Quiescent Current From (VIN1 + VIN2) (Operating)	I_{S1}	D1 = High, D0 = Low (VIN1 Active), V_{IN1} = 3.6V, V_{IN2}= 3.3V, I_{OUT} = 0A	--	55	200	μA
	I_{S2}	D0 = D1 = Low (VIN2 Active), V_{IN1} = 3.3V, V_{IN2}= 3.6V, I_{OUT} = 0A	--	55	200	
Shut Down Current From (VIN1 + VIN2) (Standby)	I_{SHDN}	D0 = D1 = High (Inactive), V_{IN1} = V_{IN2} = 3.6V, I_{OUT} = 0A	--	0.5	3	μA
Forward Leakage Current From VIN1 (Measured from VOUT to GND)	I_{FLKG_VIN1}	D0 = D1 = High (inactive), V_{IN1} = 3.6V, V_{IN2} Open, V_{OUT} = 0V (Shorted)	--	0.1	5	μA
Forward Leakage Current From VIN2 (Measured from VOUT to GND)	I_{FLKG_VIN2}	D0 = D1 = High (inactive), V_{IN2} = 3.6V, V_{IN1} Open, V_{OUT} = 0V (Shorted)	--	0.1	5	μA
Reverse Leakage Current to VINx (Measured from VINx to GND)	I_{RLKG_VINx}	D0 = D1 = High (inactive), V_{INX} = 0V, V_{OUT} = 3.6V	--	0.3	5	μA
Current Limit circuit						
Current Limit Accuracy	I_{LIM_400}	R_{ILIM} = 400Ω, V_{IN1} = V_{IN2} = 3.6V	0.95	1.25	1.56	A
	I_{LIM_700}	R_{ILIM} = 700Ω, V_{IN1} = V_{IN2} = 3.6V	0.47	0.71	0.99	
Output Current at ILIM	I_{LIM}	V_{ILIM} = 0V, I_{OUT} = 0A	0	--	150	μA
UVLO						
VIN1 and VIN2 UVLO	V_{UVLO_FAL}	Falling Edge	1.2	1.28	--	V
	V_{UVLO_RSE}	Rising Edge	--	1.34	1.6	
Internal VDD UVLO (the higher of VIN1 and VIN2)	V_{UVLO_FAL}	Falling Edge	2.2	2.4	--	V
	V_{UVLO_RSE}	Rising Edge		2.5	2.8	
UVLO Deglitch for VIN1 and VIN2		Rising Edge (Note 6) (Note7)	--	100	--	μs
VIN2 to VIN1 Comparators						
Hysteresis of VIN2 to VIN1 comparator			0.1	--	0.25	V
Deglitch of VIN2 to VIN1 comparator (both Rising & Falling)		(Note 6)	--	75	--	μs
Reverse Conduction Blocking						
$\Delta V_{O\ (I\_Block)}$ Minimum Output-to-Input Voltage Difference to Block Switching	D0 = D1 = High, V_{INX} = 3.3V. Connect V_{OUT} to a 5V supply through a series 100Ω resistor. Let D0 = Low. Slowly decrease the supply voltage until V_{OUT} connects to V_{IN1}.		--	130	--	mV
STAT Output						
Leakage Current	$I_{LEAKAGE}$	$V_{O(STAT)}$ = 5.5V	--	0.01	1	μA
Saturation Voltage	V_{SAT}	$I_{I(STAT)}$ = 2mA, V_{IN1} Switch is On	--	--	0.4	V
Deglitch Time (falling edge only)		(Note 6)	--	150	--	μs
Thermal Shutdown						
Thermal Shutdown Protection	T_{SD}		--	135	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	10	--	°C

To be continued

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Power Switch Timing (Note 6)							
Output Rise Time from an enable	t_r	V_{IN1} = V_{IN2} = 3.3V, I_{OUT} = 500mA See Timing Diagram (a)		1	1.72	3	ms
Output Fall Time from a disable	t_f	V_{IN1} = V_{IN2} = 3.3V, I_{OUT} = 500mA See Timing Diagram (a)		0.1	0.26	1.5	ms
Transition Time	t_t	V_{IN1} to V_{IN2} transition, V_{IN1} = 3.3V, V_{IN2} = 5V	I_{OUT} = 500mA, (Measure transition time as 10 to 90% rise time or from 3.4V to 4.8V on V_{OUT}) See Timing Diagram (b)	--	20	60	µs
		V_{IN2} to V_{IN1} transition, V_{IN1} = 5V, V_{IN2} = 3.3V		--	20	60	
Turn-on Propagation Delay from Enable	t_{PLH1}	V_{IN1} = V_{IN2} = 3.3V, Measure from enable to 10% of V_{OUT}, I_{OUT} = 500mA See Timing Diagram (a)		--	1	--	ms
Turn-off Propagation Delay from Disable	t_{PHL1}	V_{IN1} = V_{IN2} = 3.3V, Measure from disable to 90% of V_{OUT}, I_{OUT} = 500mA See Timing Diagram (a)		--	1	--	ms
Switch-over Rising Propagation Delay	t_{PLH2}	Logic 1 to Logic 0 transition on D1, Measure from D1 to 10% of V_{OUT}	V_{IN1} = 3.3V, V_{IN2} = 5V, V_{D0} = 0V, I_{OUT} = 500mA See Timing Diagram (c)	--	20	100	µs
Switch-over Falling Propagation Delay	t_{PHL2}	Logic 0 to Logic 1 transition on D1, Measure from D1 to 90% of V_{OUT}		2	3.8	10	ms

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

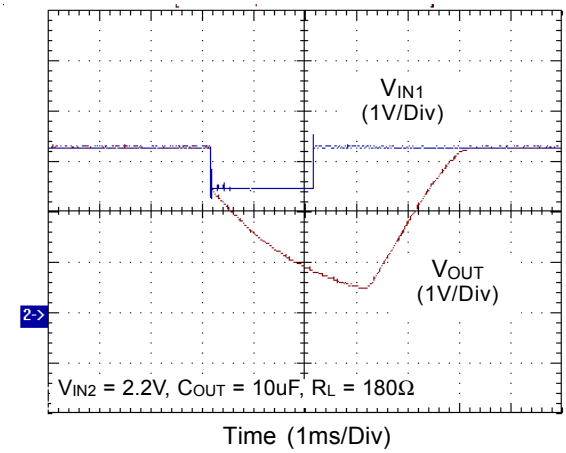
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Performance at −5°C ≤ T_A ≤ 85°C is assured by design.

Note 6. Not tested for production.

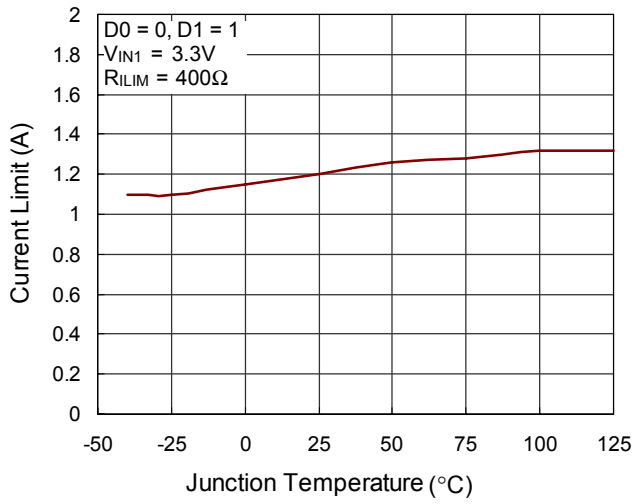
Note 7. The UVLO is without latch. In V_{IN} falling dege, the output voltage will depend on I_{OUT} and C_{OUT}. Please see below curve as reference.

V_{OUT} Response vs. UVLO

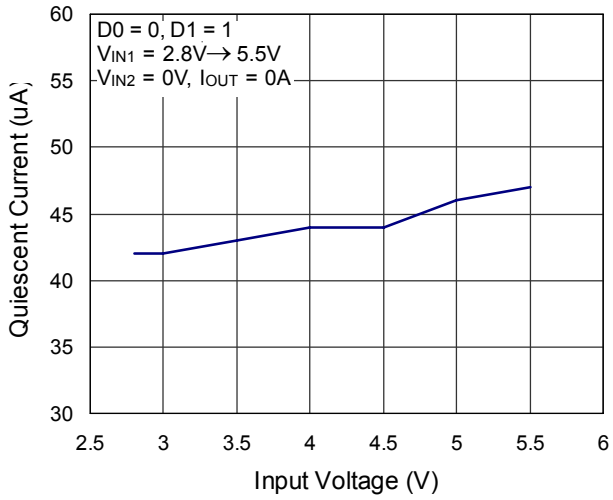


Typical Operating Characteristics

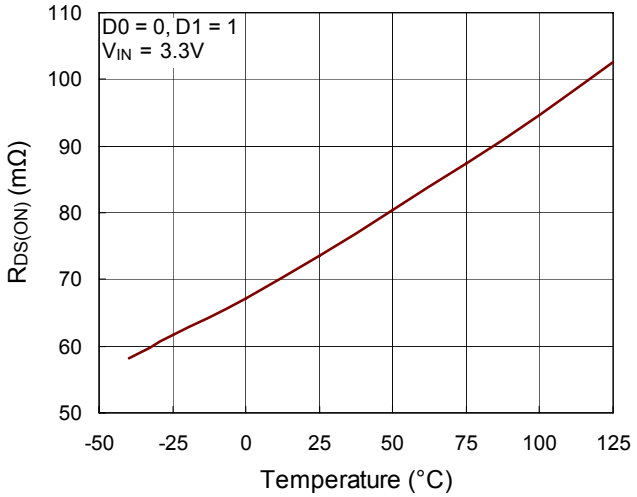
Current Limit vs. Junction Temperature



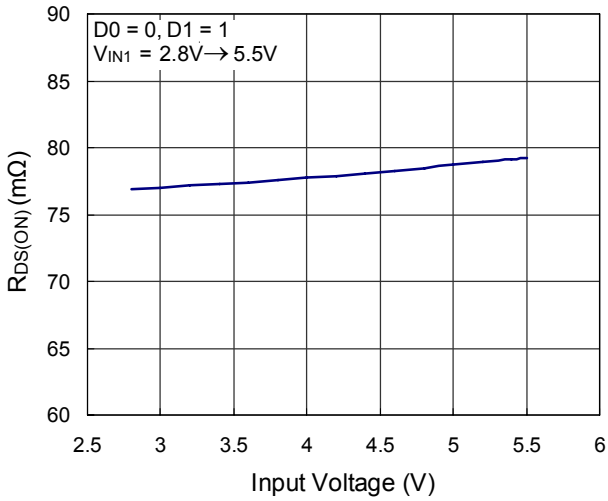
Quiescent Current vs. Input Voltage



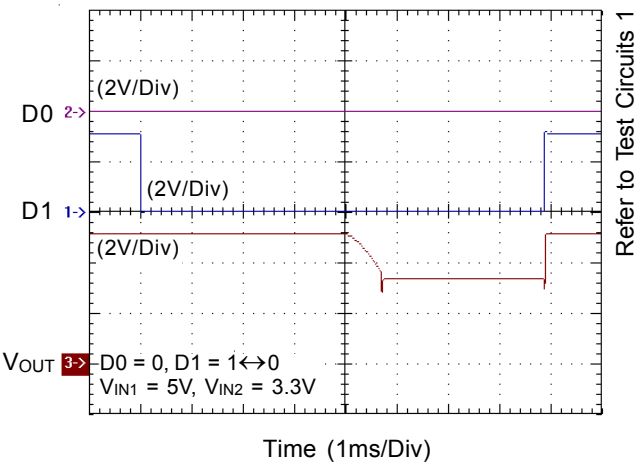
$R_{DS(ON)}$ vs. Temperature



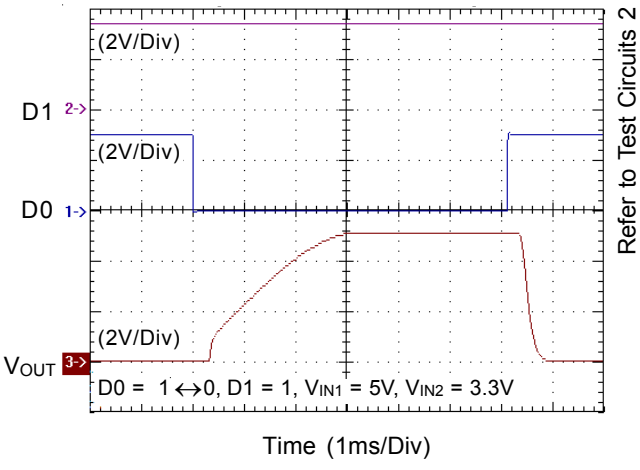
$R_{DS(ON)}$ vs. Input Voltage



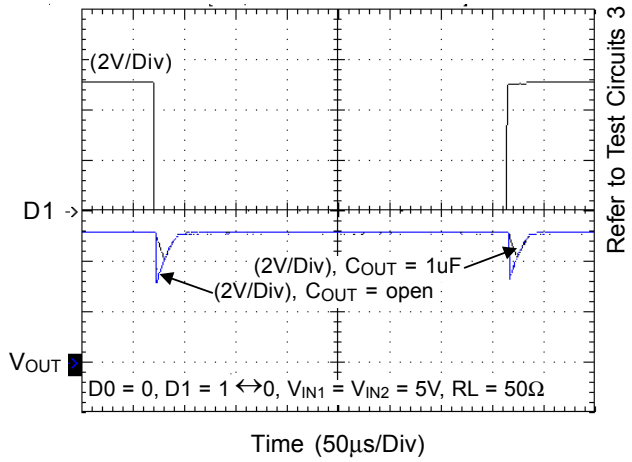
Output Switchover Response



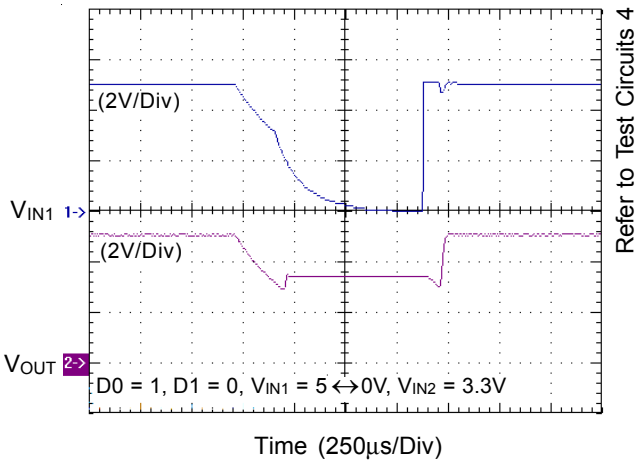
Output Turn-On Response



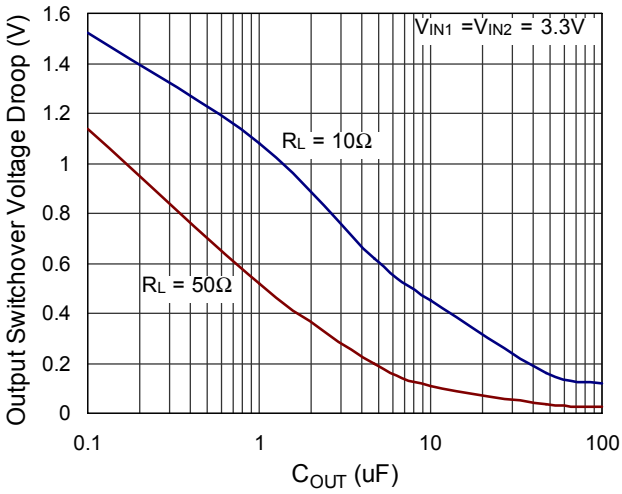
Output Switchover Voltage Droop



Auto Switchover Voltage Droop



Output Switchover Voltage Droop vs. C_{OUT}



Application Information

The RT9705B is dual input single output power multiplexer specifically designed to provide seamless voltage transition between two independent power suppliers. Equipped with two low $R_{DS(ON)}$ N-Channel MOSFETs driven by internal charge pump circuitry, the RT9705B is able to deliver 1A output current with only 80mV voltage drop. The RT9705B provides comprehensive protection functions, including adjustable current limit, over temperature protection, soft start function for minimum inrush current, cross-conduction protection, and reverse conduction protection. These features greatly simplify power multiplexer design.

Manual Switching Mode

The RT9705B provides two logic input D0 and D1 for switch selection as shown in Table 1. The RT9705B selects the manual-switching mode when the D0 is pulled low. In this mode V_{OUT} connects to V_{IN1} if D1 pulled high, otherwise V_{OUT} connects to V_{IN2}.

Auto Switching Mode

RT9705B selects the auto-switching mode when the D0 is pulled high and D1 is pulled low. In this mode V_{OUT} connects to the higher of V_{IN1} and V_{IN2}.

Shutdown Mode

When both D0 and D1 are selected high, the RT9705B enters shutdown mode and consumes minimum power. An internal MOSFET with 2kΩ $R_{DS(ON)}$ turns on and softly discharges the output voltage in the shutdown mode. Since no body diode exists between V_{INX} and V_{OUT}, output voltage is allowed to be high than the input voltages in the shutdown mode.

Switch Status Indication

A STAT pin with open drain output is provided to indicate the switch status. STAT pin outputs high impedance if V_{IN2} is active, otherwise STAT pin outputs low.

Current Limiting

The current limit circuitry prevents damage to the MOSFET switch and external load. A resistor R_{ILIM} from ILIM to GND sets the current limit to 500/R ILIM and the adjustable current limiting up to 1.25 A. A setting resistor R_{ILIM} equal to zero is not recommended as that disables current limiting.

Thermal Considerations

Thermal protection limits power dissipation in RT9705B. When the operation junction temperature exceeds 135°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turn on again after the junction temperature cools by 10°C.

For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is :

$$P_D = (V_{IN}-V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT9705B, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA} is layout dependent) for TSSOP-8 package is 230°C/W on standard JEDEC 51-3 thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$$P_{D(MAX)} = (125°C - 25°C) / 230°C/W = 430 \text{ mW (TSSOP-8)}$$

Layout Consideration

In order to meet the voltage drop, droop, and EMI requirements, careful PCB layout is necessary. The following guidelines must be considered :

- Keep all main current traces as short and wide as possible.
- Place a ground plane under all circuitry to lower both resistance and inductance and improve DC and transient performance (Use a separate ground and power plans if possible).
- Locate the ceramic input capacitors as close as possible to the VIN and GND pins of the device.

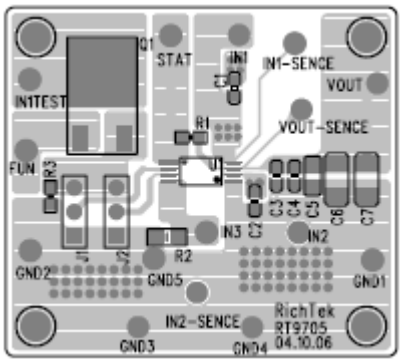


Figure 1. Top Layer

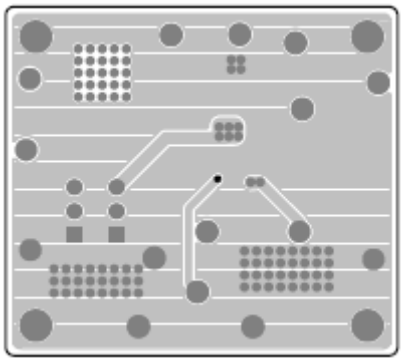
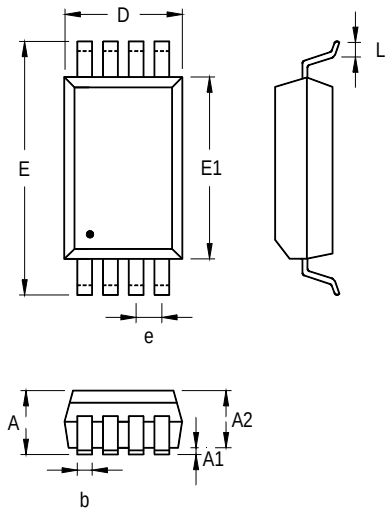


Figure 2. Bottom Layer

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.200	0.039	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
D	2.900	3.100	0.114	0.122
e	0.650		0.026	
E	6.300	6.500	0.248	0.256
E1	4.300	4.500	0.169	0.177
L	0.450	0.750	0.018	0.030

8-Lead TSSOP Plastic Package

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