6-A Smart Load Switch Battery Charger

General Description

The RT9748 is a 6-A smart load switch battery charger that integrates an internal load switch with charge pump control and 4-path constant current/constant voltage regulation, a 5-way hardware protection, and a 10-channel 12-bit analog-to-digital converter. The RT9748 provides accurate analog-to-digital converter for voltage/current measurement through I^2C serial interface to report the battery charging parameters and 3-way software protection and flags.

Applications

- Handheld Products
- Portable Media Players

Ordering Information

RT9748 □

Package Type
WSC: WL-CSP-42B 2.75x3.05 (BSC)

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

Features

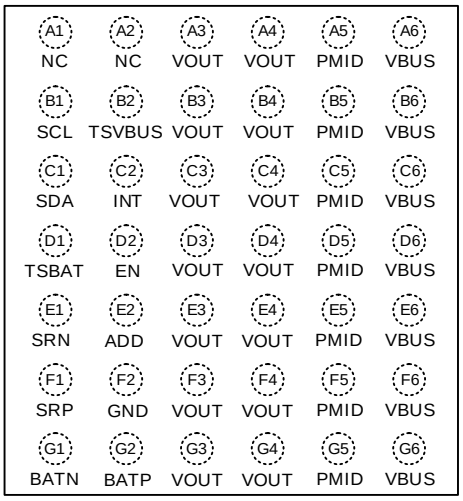
- **Internal Load Switch with Charge Pump Control**
  - **Dual NFETs in a Back to Back Configuration**
  - **Internal Charge Pump Control**
- **4-Path CC/CV Regulation**
  - **Input Current Regulation (ICR)**
  - **Output Voltage Regulation (OVR)**
  - **Battery Voltage Regulation (BVR)**
  - **Battery Current Regulation (BCR)**
- **5-Way Hardware Protection**
  - **VBUS Overvoltage Protection (VBUS_OVP)**
  - **Drop-Out Overvoltage Protection (VDR_OVP)**
  - **Reverse Overcurrent Protection (RE_OCP)**
  - **Junction Over-Temperature Protection (TJ_OTP)**
  - **Input Overcurrent Protection (IOC_OCP)**
- **10-Channel 12-bit ADC**
  - **High Accuracy of 12-bit Resolution**
  - **10-Channel for Voltage/Current Measurement**
  - **High Speed Data Rate for 8/16 Times Average Per Channel**
- **3-Way Software Protection**
  - **Drop-Out Overvoltage Protection Alarm (VDR_ALM)**
  - **TS of the VBUS Over-Temperature Protection (TBUS_OTP)**
  - **TS of the BAT Over-Temperature Protection (TBAT_OTP)**

Marking Information

0S: Product Code
YMDNN: Date Code

Pin Configuration

(TOP VIEW)



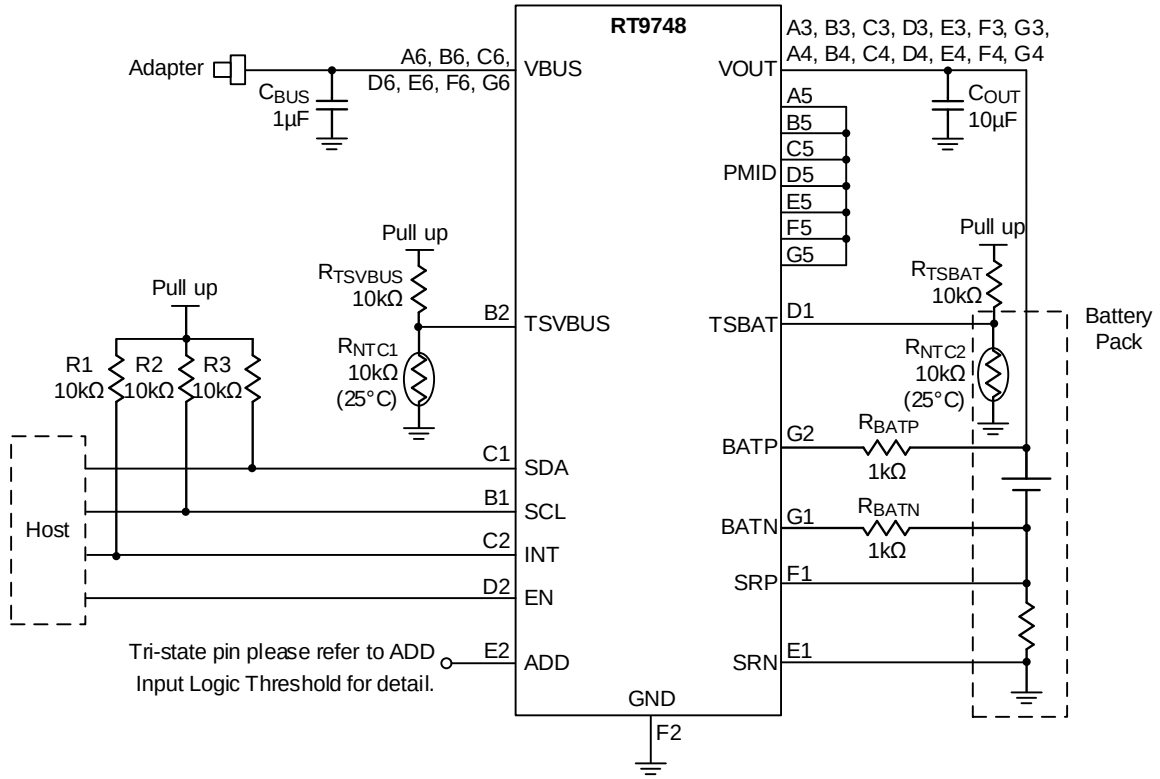
WL-CSP-42B 2.75x3.05 (BSC)

Functional Pin Description

Pin No.	Pin Name	I/O	Pin Function
A1, A2	NC	NC	No internal connection.
A6, B6, C6, D6, E6, F6, G6	VBUS	P	DC input power supply.
A5, B5, C5, D5, E5, F5, G5	PMID	NC	Connect these pins together and do not connect to power input or ground.
A3, B3, C3, D3, E3, F3, G3, A4, B4, C4, D4, E4, F4, G4	VOUT	P	Battery connection point to positive terminal of the battery pack.
F2	GND	P	Ground.
E1	SRN	AI	Negative input for battery current sensing.
F1	SRP	AI	Positive input for battery current sensing.
G1	BATN	AI	Negative input for battery current sensing by 1kΩ. Connect to negative terminal of battery pack.
G2	BATP	AI	Positive input for battery voltage sensing by 1kΩ. Connect to positive terminal of battery pack.
B2	TSVBUS	AI	VBUS temperature qualification voltage input. An external resistor divider and a voltage reference are required.
D1	TSBAT	AI	Battery temperature qualification voltage input. An external resistor divider and a voltage reference are required.
C1	SDA	DI	I^2C interface data. Connect to pull-up voltage via 10kΩ pull-up resistor.
B1	SCL	DIO	I^2C interface clock. Connect to pull-up voltage via 10kΩ pull-up resistor.
E2	ADD	DI	I^2C address configurable. Tri-state driver should be used to interface this pin.
D2	EN	DI	Device enable control pin. Pull low to disable device. I^2C is not available when the device is disabled.

Pin No.	Pin Name	I/O	Pin Function
C2	INT	DO	Open drain interrupt output. Connect to pull-up voltage via 10kΩ pull-up resistor. Normally high, the INT pin sends an active low.

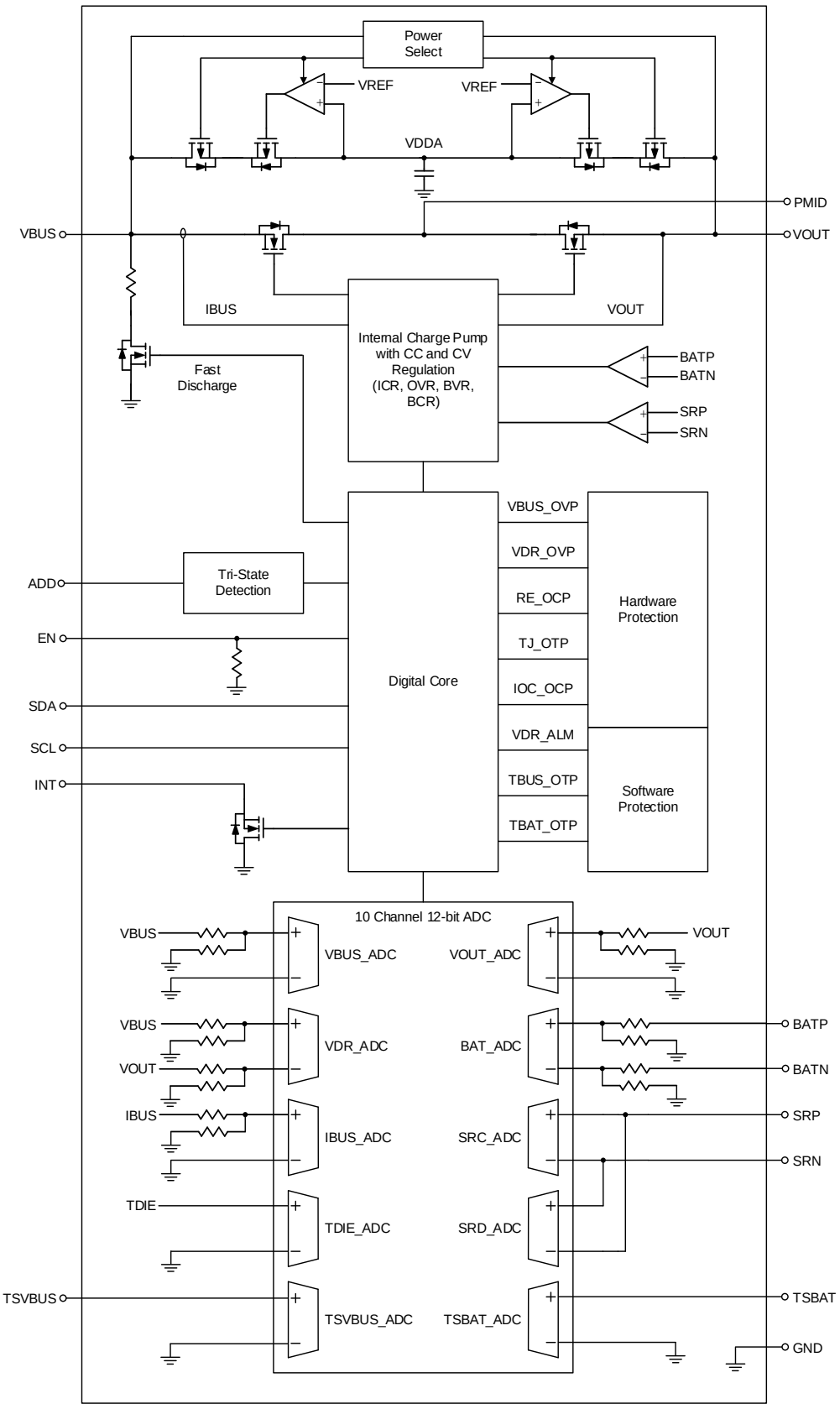
Typical Application Circuit



Below are recommended capacitor and inductor information

Pin	Description	Part Number	Package	Manufacturer
VBUS	1µF/25V/X5R	GRM185R61E105KA12	0603	muRata
VOUT	10µF/25V/X5R	GRM188R61E106MA73	0603	muRata
SRP/SRN	10mΩ/±1%	WMCS0805R010FSTA	0805	Wellcomp
BATP BATN	1kΩ/±1%	WR04X1001FTL	0402	WALSIN

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Pin Voltage, VBUS ---------- –0.3V to 22V
- Supply Pin Voltage, VOUT ---------- –0.3V to 22V
- Other Pin Voltage ---------- 0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  WL-CSP-42B 2.75x3.05 (BSC) ---------- 3.54W
- Package Thermal Resistance (Note 2)

  WL-CSP-42B 2.75x3.05 (BSC), θ_{JA} ---------- 28.2°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model), per ANSI/ESDA/JEDEC JS-001 ---------- ±2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage Range, VBUS ---------- 3V to 6V
- Supply Input Voltage Range, VOUT ---------- 3V to 6V
- Analog Sense Voltage Range, SRP, SRN, BATP, BATN ---------- 0V to 5V
- Temperature Sense Voltage Range, TSVBUS, TSBAT ---------- 0V to 3V
- Output Sink Current, INT ---------- 1mA
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Source						
VDDA UVLO Threshold	$V_{DDA\_VBUS\_UVLO}$	V_{DDA} rising, V_{BUS} > V_{OUT}, V_{DDA} = V_{BUS}	2.7	2.8	2.9	V
	$V_{DDA\_VOUT\_UVLO}$	V_{DDA} rising, V_{BUS} < V_{OUT}, V_{DDA} = V_{OUT}				
VDDA UVLO Hysteresis	$V_{DDA\_VBUS\_HYS}$	V_{DDA} falling, V_{BUS} > V_{OUT}, V_{DDA} = V_{BUS}	50	150	250	mV
	$V_{DDA\_VOUT\_HYS}$	V_{DDA} falling, V_{BUS} < V_{OUT}, V_{DDA} = V_{OUT}				
VBUS Quiescent Current	I_{BUS_IQ}	V_{BUS} = 4.2V > V_{OUT}, charge mode, LDSW enable	3	4	6	mA
VOUT Quiescent Current	I_{OUT_IQ}	V_{OUT} = 4.2V > V_{BUS}, battery mode, ADC enable	2	3	5	mA
VOUT Leakage Current	I_{OUT_LEAK}	V_{OUT} = 4.2V > V_{BUS}, EN disable	0.5	1	1.5	μA
VBAT Insert	V_{BAT_INSERT}	V_{BAT} = BATP-BATN	1.9	2	2.1	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Load Switch RON and Regulation						
Load Switch RON	R_{LDSW}		--	10	12	mΩ
IBUS REG Threshold Range	I_{BUS_REG}	I²C programmable	0.4	--	6.35	A
IBUS REG Threshold Step		7-bit DAC	25	50	75	mA
VOUT REG Threshold Range	V_{OUT_REG}	I²C programmable	4.2	--	5	V
VOUT REG Threshold Step		7-bit DAC	5	10	15	mV
VBAT REG Threshold Range	V_{BAT_REG}	I²C programmable	4.2	--	5	V
VBAT REG Threshold Step		7-bit DAC	5	10	15	mV
IBAT REG Threshold Range	I_{BAT_REG}	I²C programmable	0.4	--	6.35	A
IBAT REG Threshold Step		7-bit DAC	25	50	75	mA
Hardware Protection						
VBUS OVP Threshold Range	V_{BUS_OVP}	I²C programmable	4.2	--	6.5	V
VBUS OVP Threshold Step		7-bit DAC	12.5	25	37.5	mV
Drop-Out OVP Threshold	V_{DROP_OVP}	I²C programmable	0	--	1000	mV
Drop-Out OVP Step		7-bit DAC	5	10	15	mV
Reverse OCP Threshold	I_{RE_OCP}	Default, load switch R_{ON} = 10mΩ	0.5	1.5	2.5	A
Junction OTP Threshold	T_{DIE_OTP}	1-value	115	125	140	°C
Input OCP Threshold	I_{OC_OCP}	I²C programmable	0	--	6.5	A
Input OCP Step		4-bit DAC	250	500	750	mA
Software Protection						
Drop-Out ALM Threshold	V_{DROP_ALM}	I²C programmable	0	--	1000	mV
Drop-Out ALM Step		7-bit DAC	5	10	15	mV
TSVBUS OTP Threshold	V_{TSVBUS_OTP}	I²C programmable	0	--	2.4	V
TSVBUS OTP Step		7-bit DAC	10	20	30	mV
TSBAT OTP Threshold	V_{TSBAT_OTP}	I²C programmable	0	--	2.4	V
TSBAT OTP Step		7-bit DAC	10	20	30	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ADC Specification						
ADC Sample Rate	f_{SAMPLE_ADC}	(Note 5)	--	2.25	--	MHz
ADC Data Rate	f_{DATA_ADC}	(Note 5), 16 averages	--	10	--	kHz
VBUS ADC Range	$V_{BUS\_ADC\_RAN}$	VDDA > 3V, 16 averages	1.5	--	6.5	V
VBUS ADC Accuracy	$V_{BUS\_ADC\_ACC}$		–10	--	10	mV
IBUS ADC Range	$I_{BUS\_ADC\_RAN}$	VDDA > 3V, 16 averages	0	--	7	A
IBUS ADC Accuracy	$I_{BUS\_ADC\_ACC}$		–150	--	150	mA
VOUT ADC Range	$V_{OUT\_ADC\_RAN}$	VDDA > 3V, 16 averages	1.5	--	6.5	V
VOUT ADC Accuracy	$V_{OUT\_ADC\_ACC}$		–10	--	10	mV
VDROP ADC Range	$V_{DROP\_ADC\_RAN}$	VDDA > 3V, 16 averages	0	--	1000	mV
VDROP ADC Accuracy	$V_{DROP\_ADC\_ACC}$		–10	--	10	mV
VBAT ADC Range	$V_{BAT\_ADC\_RAN}$	VDDA > 3V, 16 averages	2.5	--	5	V
VBAT ADC Accuracy	$V_{BAT\_ADC\_ACC}$		–10	--	10	mV
IBAT ADC Range	$I_{BAT\_ADC\_RAN}$	VDDA > 3V, 16 averages	–7	--	7	A
IBAT ADC Accuracy	$I_{BAT\_ADC\_ACC}$		–100	--	100	mA
TSVBUS ADC Range	$V_{TSVBUS\_ADC\_RAN}$	VDDA > 3V, 16 averages	0	--	2.4	V
TSVBUS ADC Accuracy	$V_{TSVBUS\_ADC\_ACC}$		–10	--	10	mV
TSBAT ADC Range	$V_{TSBAT\_ADC\_RAN}$	VDDA > 3V, 16 averages	0	--	2.4	V
TSBAT ADC Accuracy	$V_{TSBAT\_ADC\_ACC}$		–10	--	10	mV
TDIE ADC Range	$T_{DIE\_ADC\_RAN}$	VDDA > 3V, 16 averages	0	--	125	°C
TDIE ADC Accuracy	$T_{DIE\_ADC\_ACC}$		–3	--	3	°C
I²C Interface						
Serial-Clock Frequency	$f_{SCL\_I^2C}$	(Note 5)	10	--	1000	kHz
I²C Input Logic Threshold	$V_{IH\_I^2C}$	Logic high	1.5	--	--	V
	$V_{IL\_I^2C}$	Logic low	--	--	0.4	
EN Input						
EN Input Logic Threshold	V_{IH_EN}	Logic high	1	--	--	V
	V_{IL_EN}	Logic low	--	--	0.4	
EN Pull-Down Resistor	R_{PD_EN}	On chip	--	500	--	kΩ
Device turn-on delay time after EN pull-high			--	--	500	μs
ADD Tri-State Input						
ADD Input Logic Threshold	V_{IH_ADD}	Logic high	1.2	--	--	V
	$V_{IFLOATING\_ADD}$	Input floating	0.5	--	1.1	
	V_{IL_ADD}	Logic low	--	--	0.4	
ADD Pull Down Resistor	R_{PD_ADD}	On chip	--	500	--	kΩ

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

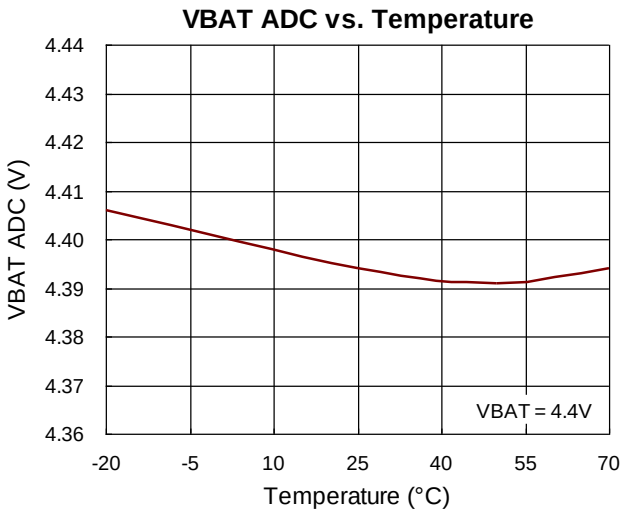
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

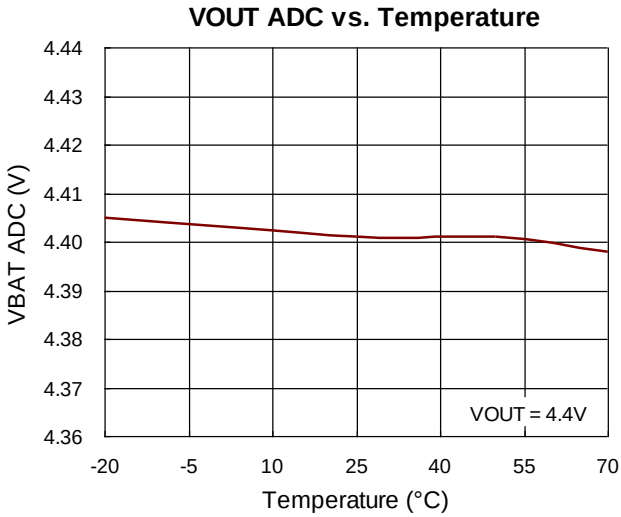
Note 3. Devices are ESD sensitive. Handling precautions are recommended.

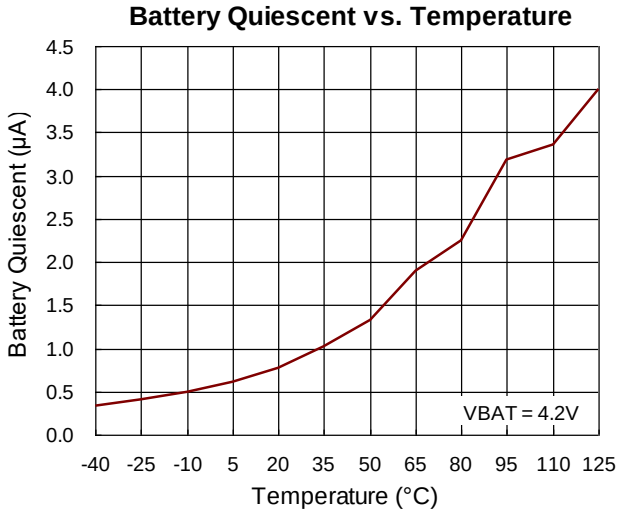
Note 4. The device is not guaranteed to function outside its operating conditions.

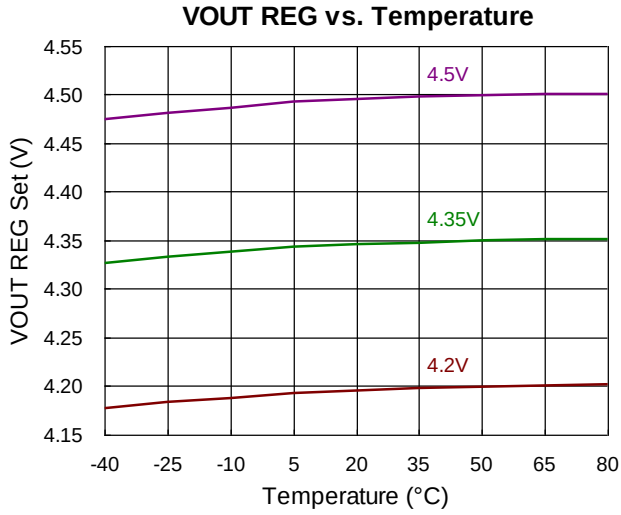
Note 5. Specification is guaranteed by design and/or correlation with statistical process control.

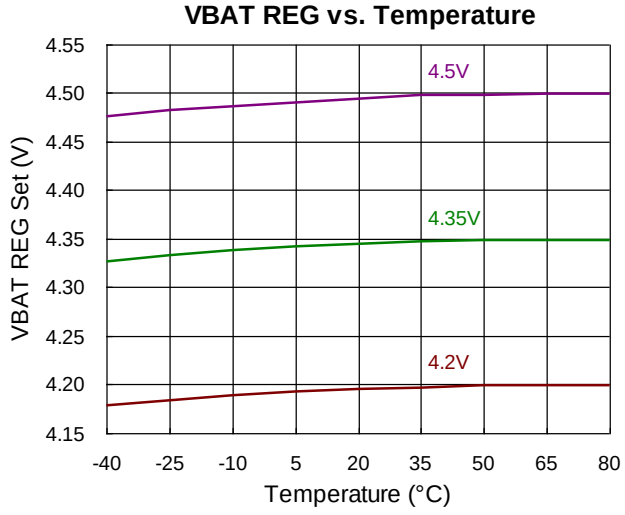
Typical Operating Characteristics

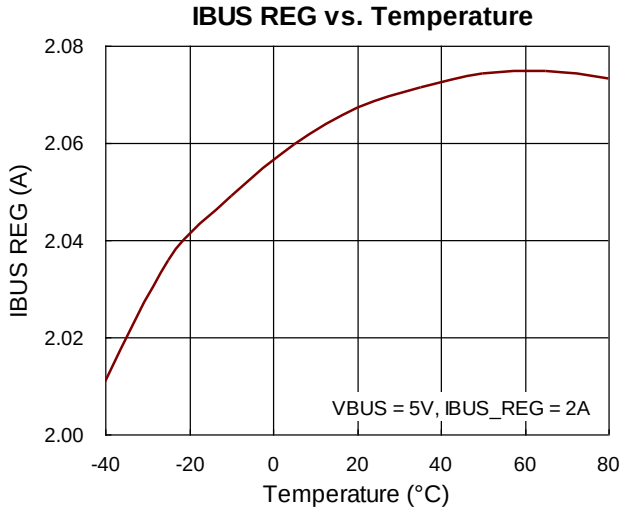


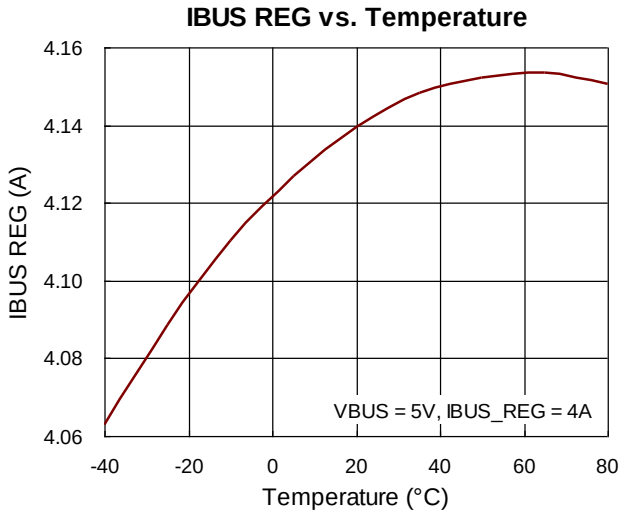












Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

Device Power-On

The internal bias circuit (VDDA) is powered from the higher of two voltages between VBUS and VOUT. The device will be powered-on when the VDDA is higher than VDDA UVLO threshold and EN pin is higher than VIH_EN. When VBUS > VDDA UVLO and EN pin goes from low logic to high logic, the device need maximum 500μs turn on delay time after EN pin set to high logic.

Smart Load Switch

The RT9748 is a smart load switch battery charger with 8mΩ RON and loading up to 6A. The load switch can be controlled by the host via I^2C. The load switch can be turned on by setting CHG_EN bit to '1' (0x06 bit4) if no protection event happens (Please check 0x03 and 0x04). The load switch can be turned off by setting CHG_EN bit to '0' or pulling EN pin to low. If a protection event happens, the load switch will be turned off automatically and sets the CHG_EN bit to '0'. The smart load switch also implements soft-on and soft-off function to minimize the inrush current and voltage spike.

8-Channel 12-bit Analog to Digital Converter

The device integrates 8-Cannel 12bit ADC function, users can monitor voltage of VBUS, VOUT, VDROP (voltage different between VBUS and VOUT), and VBAT. The user also can monitor the internal junction temperature, battery temperature (by external resistor divider and NTC thermistor), and VBUS temperature (by external resistor divider and NTC thermistor). The ADC function also provides IBUS information for users to monitor.

Users can set ADC_EN (0x07 bit3) bit to enable or disable ADC conversion. Users can also enable or disable ADC channels respectively by using register 0x07 and 0x08. The ADC has two conversion rates: 1-shot mode and continuous mode. Users can select the mode by ADC_RATE bit (0X07 bit2).

- **1-shot Mode**

  In this mode, users need to set ADC_EN bit to 1 to start ADC conversion. The ADC_EN bit will change to 0 automatically after ADC starts conversion. After the ADC conversion is complete, the ADC_DONE bit (0x04 bit6) will change to 1 and INT pin will pull low if the ADC_DONE_MASK bit is no masked. The typical conversion time of one channel is 100μs (16 averages).

- **Continuous Mode**

  In continuous mode, ADC conversion continues if users set ADC_EN bit to 1. The ADC stops conversion if users set ADC_EN bit to 0.

  Users can set the ADC_AVG_EN bit to enable or disable ADC measurement averaging function in both 1-shot mode and continuous mode. If ADC_AVG_EN = 0, the ADC performs instantaneous measurement. If ADC_AVG_EN = 1, the ADC performs averaging measurement and users can set the number of samples by ADC_SAMPLES bit.

Linear Regulation Mode (LDO)

The load switch implements LDO mode to regulate VOUT voltage, battery voltage and input current. In the event that the VOUT_REG, VBAT_REG, or IBUS_REG threshold is exceeded, the load switch will function as an LDO and regulate the voltage or current accordingly. The specific regulation threshold can be selected through the I2C interface, depending on which parameter is exceeded (VOUT, VBAT, or IBUS).

Protection Features

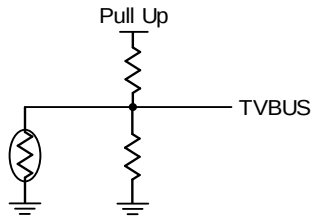
The load switch implements 5-way hardware protection and 2 temperature protections as described below. Each of these protection functions is equipped with an IRQ and can be activated using the INT pin, which alerts the host to monitor the active protection.

- **VBUS Over-Voltage Protection (VBUS_OVP)**

  When VBUS_OVP event happens, the device will turn off load switch and the CHG_EN bit will be set to 0. Users can enable or disable this protection function by I^{2}C 0x05 bit 7. The protection threshold and deglitch time can also be selected by I^{2}C (Protection threshold is 0x0A, deglitch time is 0x09 bit0).

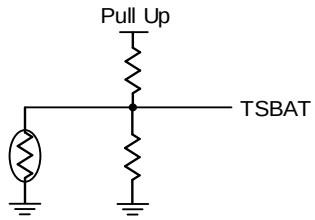
- **VBUS Over-Temperature Protection (TSVBUS_OTP)**

  As shown in the figure below, users need to place an external NTC voltage divider circuit at TSBUS pin. When the voltage of TSVBUS pin is over the threshold, the device will turn off load switch and set CHG_EN bit to 0. Users can enable or disable this protection function by I^{2}C (0x05 bit2). Users can also set the threshold by I^{2}C (0x11).



- **VBAT Over-Temperature Protection (TSBAT_OTP)**

  As shown in the figure below, users need to place an external NTC voltage divider circuit at TSBAT pin. When the voltage of TSBAT pin is over the threshold, the device will turn off load switch and set CHG_EN bit to 0. Users can enable or disable this protection function by I^{2}C (0x05 bit1). User can also set the threshold by I^{2}C (0x12).



- **IBUS Reverse Current Protection (IBUS_ IREV)**

  The device implements a reverse current protection function to turn off load switch when the reverse current is detected (current flow from VOUT to VBUS). The device sets CHG_EN to “0” when this event is detected. The user can set the protection level and deglitch time by I^{2}C (0x26 set level, 0x27 set deglitch).

- **Dropout Voltage Protection (VDROP_OVP)**

  VDROP is the voltage difference between VBUS and VOUT. The device implements two VDROP thresholds for users to set by I^{2}C: One is VDROP_LAM and the other on is VDROP_OVP. Users can use these thresholds to monitor the load switch. When the VDROP_ALM threshold is triggered, the device asserts the INT pin low to alert the host. If VDROP_OVP threshold is triggered, the device will turn off the load switch and set CHG_EN bit to ‘0’.

  Since the VDROP_ALM is an alarm signal, users should set VDROP_OVP threshold higher than VDROP_ALM.

- **Junction Thermal Shutdown (TSHUT_FLT)**

  The device will turn off load switch and set CHG_EN bit to ‘0’ if the threshold of junction temperature shutdown is triggered. If the junction thermal shutdown is triggered, the device asserts INT low to alert the host (no mask for TSHUT_FLT), and also sets the TSHUT_FLT bit to ‘1’.

- **IBUS Overcurrent Protection (IOC_FLT)**

  The device monitors the current flow from VBUS to VOUT. If the current is over the threshold, the device has two protection options for users to select by I^{2}C. If users set OCP_RES bit to ‘0’ (blanking mode), the device will turn off load switch and set CHG_EN to ‘0’ when IBUS current is over IOC threshold. If users set OCP_RES bit to ‘1’ (hiccup mode), load switch is disabled instantaneously, and the device will attempt to turn on the load switch and wait for 250μs to check OCP and turns off every 100ms, up to 7 times before latching off.

Communication Interface

The device uses I²C compatible interface by 2-wire line (SCL and SDA) to communicate with the host. The SCL and SDA pins are open drain, which needs to connect to supply voltage by pull-up resistors. The device acts as an I²C slave with a 7-bit address of either 65H, 66H, or 67H, depending on the ADD setting. It can support up to 1MHz conditionally. To start an I²C communication, begin with START (S) condition, and then the host sends slave address. This address is 7-bit long followed by an eighth bit which is a data direction bit (RW). The second byte is register address. The third byte contains data to the selected register. End with STOP (P) condition.

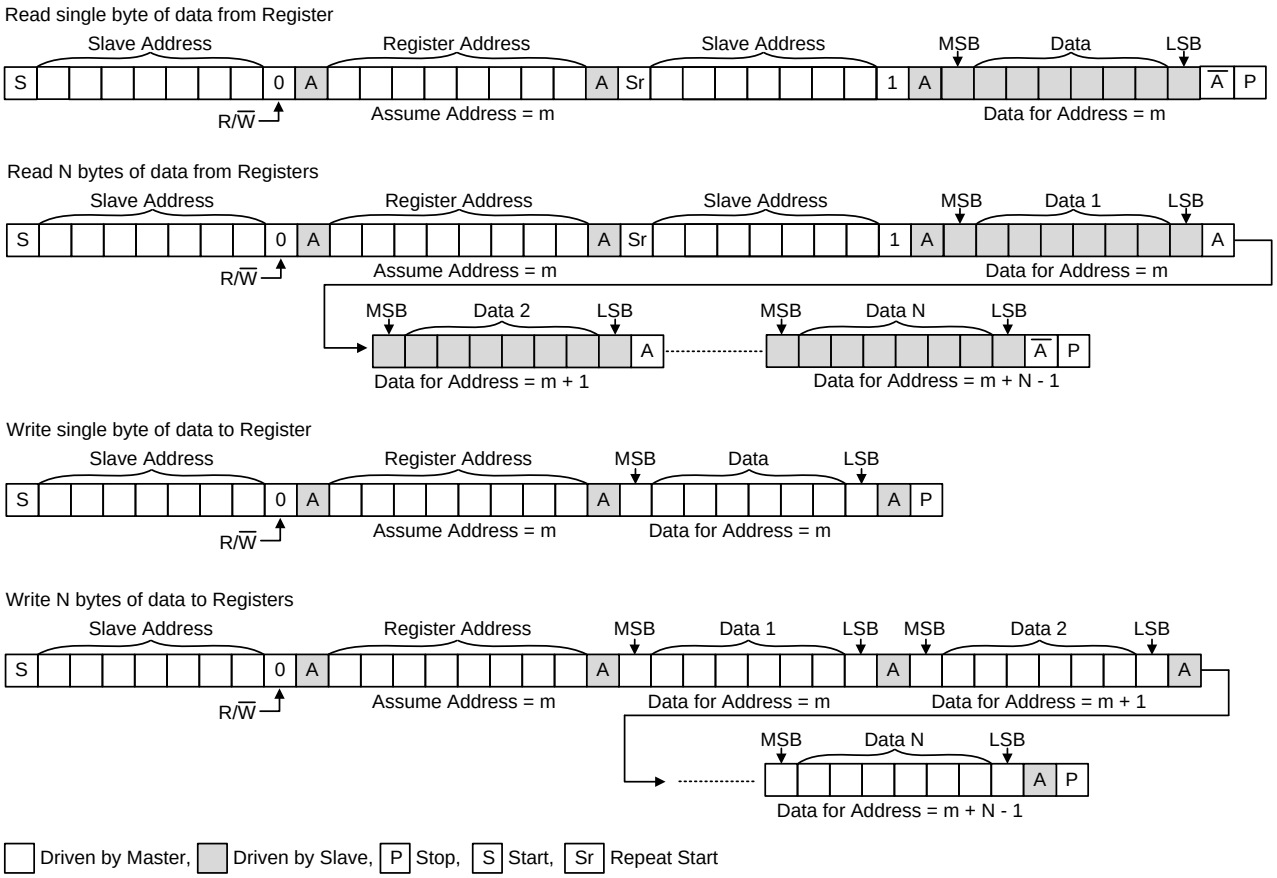


Figure 8. Read and Write Function

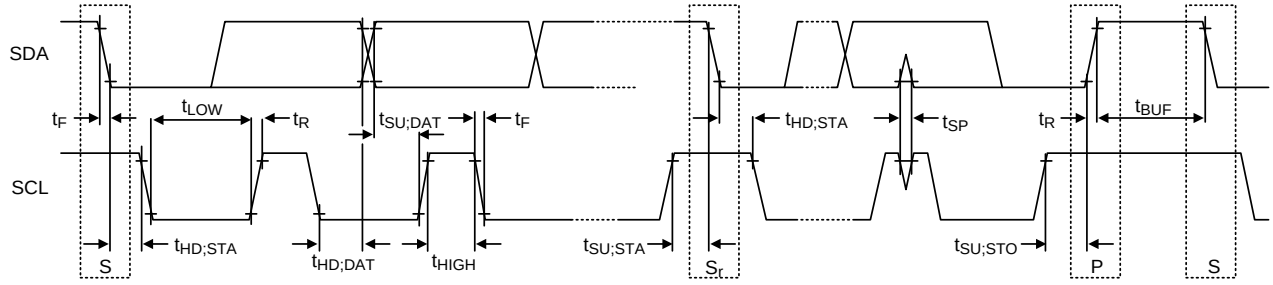


Figure 9. I²C Waveform Information

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is normally 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-42B 2.75x3.05 (BSC) package, the thermal resistance, θ_{JA}, is 28.2°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (28.2°C/W) = 3.54W for a WL-CSP-42B 2.75x3.05 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to inspect the effect of rising ambient temperature on the maximum power dissipation.

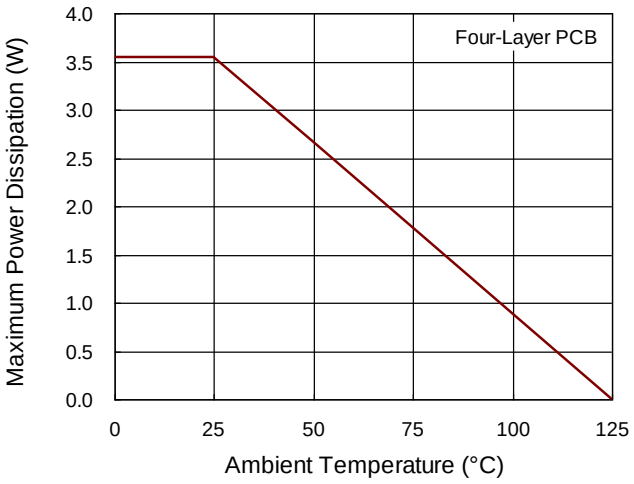


Figure 1. Derating Curve of Maximum Power Dissipation

Functional Register Description

I²C Slave Address

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ADD Input Logic Threshold	V_{IH_ADD}	Logic High, Slave Address is **1100101 (65H)**	1.2	--	--	V
	$V_{IFLOATING\_ADD}$	Input Middle, Slave Address is **1100110 (66H)**	0.5	--	1.1	
	V_{IL_ADD}	Logic Low, Slave Address is **1100111 (67H)**	--	--	0.4	

Register Map

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Type
0x00	DEVICE_INFO	Reserved		DEVICE_RE			DEVICE_ID			0x00	R
0x01	EVENT_1_MASK	VBUS_OVP_MASK	IBUS_REG_MASK	VBAT_REG_MASK	IBAT_REG_MASK	VOUT_REG_MASK	TBUS_OTP_MASK	TBAT_OTP_MASK	IBUS_IREV_MASK	0x00	RW
0x02	EVENT_2_MASK	LOWCHG_ALM_MASK	ADC_DONE_MASK	VDROP_ALM_MASK	VDROP_OVP_MASK	VBUS_INSERT_MASK	BAT_INSERT_MASK	TSHUT_FLT_MASK	IOC_FLT_MASK	0x00	RW
0x03	EVENT_1	VBUS_OVP_FLT	IBUS_REG_LDO	VBAT_REG_LDO	IBAT_REG_LDO	VOUT_REG_LDO	TBUS_OTP_FLT	TBAT_OTP_FLT	IBUS_IREV_FLT	0x00	RC
0x04	EVENT_2	LOWCHG_ALM_FLT	ADC_DONE	VDROP_ALM_FLT	VDROP_OVP_FLT	VBUS_INSERT	BAT_INSERT	TSHUT_FLT	IOC_FLT 0	0x00	RC
0x05	EVENT_1_EN	VBUS_OVP_EN	IBUS_REG_EN	VBAT_REG_EN	IBAT_REG_EN	VOUT_REG_EN	TBUS_OTP_EN	TBAT_OTP_EN	VBUS_PD_EN	0xFE	RW
0x06	CONTROL 1	VDROP_OVP_EN	VDROP_ALM_EN	SENSE_R	CHG_EN	WATCHDOG<1:0>		IREV_EN	REG_RST	0x2A	RW
0x07	ADC_CTRL	TDIE_ADC_EN	Reserved			ADC_EN	ADC_RATE	ADC_AVG_EN	ADC_SAMPLES	0x8F	RW
0x08	SAMPLE_EN	VBUS_ADC_EN	IBUS_ADC_EN	VOUT_ADC_EN	VDROP_ADC_EN	VBAT_ADC_EN	IBAT_ADC_EN	TBUS_ADC_EN	TBAT_ADC_EN	0xFF	RW
0x09	PROT_DLY&OCP	IOC_OCP<3:0>				LOWCHG_ALM_EN	LOWCHG_ALM	OCP_RES	VBUS_OVP_DLY	0xA0	RW
0x0A	VBUS_OVP	Reserved	VBUS_OVP<6:0>							0x34	RW
0x0B	VOUT_REG	Reserved	VOUT_REG <6:0>							0x14	RW
0x0C	VDROP_OVP	Reserved	VDROP_OVP<6:0>							0x1E	RW

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Type
0x0D	VDROP_ALM	Reserved	VDROP_ALM<6:0>							0x0A	RW
0x0E	VBAT_REG	Reserved	VBAT_REG<6:0>							0x0A	RW
0x0F	IBAT_OCP	Reserved	IBAT_OCP<6:0>							0x28	RW
0x10	IBUS_OCP	Reserved	IBUS_OCP<6:0>							0x64	RW
0x11	TBUS_OTP	Reserved	TBUS_OTP<6:0>							0x1E	RW
0x12	TBAT_OTP	Reserved	TBAT_OTP<6:0>							0x23	RW
0x13	VBUS_ADC2	VBUS_POL	Reserved		VBUS_ADC2<4:0>					0x00	R
0x14	VBUS_ADC1	VBUS_ADC1<7:0>								0x00	R
0x15	IBUS_ADC2	IBUS_POL	Reserved		IBUS_ADC2<4:0>					0x00	R
0x16	IBUS_ADC1	IBUS_ADC1<7:0>								0x00	R
0x17	VOUT_ADC2	VOUT_POL	Reserved		VOUT_ADC2<4:0>					0x00	R
0x18	VOUT_ADC1	VOUT_ADC1<7:0>								0x00	R
0x19	VDROP_ADC2	VDROP_POL	Reserved					VDROP_ADC2<1:0>		0x00	R
0x1A	VDROP_ADC1	VDROP_ADC1<7:0>								0x00	R
0x1B	VBAT_ADC2	VBAT_POL	Reserved		VBAT_ADC2<4:0>					0x00	R
0x1C	VBAT_ADC1	VBAT_ADC1<7:0>								0x00	R
0x1D	IBAT_ADC2	IBAT_POL	Reserved		IBAT_ADC2<4:0>					0x00	R
0x1E	IBAT_ADC1	IBAT_ADC1<7:0>								0x00	R
0x1F	TBUS_ADC2	TBUS_POL	Reserved			TBUS_ADC2<3:0>				0x03	R
0x20	TBUS_ADC1	TBUS_ADC1<7:0>								0x84	R
0x21	TBAT_ADC2	TBAT_POL	Reserved			TBAT_ADC2<3:0>				0x03	R
0x22	TBAT_ADC1	TBAT_ADC1<7:0>								0x84	R

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Type
0x23	TDIE_ ADC1	TDIE_ADC1<7:0>								0x00	R
0x24	EVENT_ STATUS_ 1	VBUS_ OVP_ STATUS	IBUS_ REG_ STATUS	VBAT_ REG_ STATUS	IBAT_ REG_ STATUS	VOUT_ REG_ STATUS	TBUS_ OTP_ STATUS	TBAT_ OTP_ STATUS	IBUS_ IREV_ STATUS	0x00	R
0x25	EVENT_ STATUS_ 2	LOWCHG _ALM_ STATUS	ADC_ DONE_ STATUS	VDROP _ALM_ STATUS	VDROP _OVP_ STATUS	VBUS_ INSERT_ STATUS	BAT_ INSERT_ STATUS	TSHUT_ STATUS	IOC_ STATUS	0x00	R
0x26	CONTROL 2	Reserved				IREV_OCP<3:0>				0x01	RW

Table 1. DEVICE_INFO

Address: 0x00
Description: DEVICE_INFO

Bit	7	6	5	4	3	2	1	0
Field	Reserved		DEVICE_RE			DEVICE_ID		
Default	0	0	0	0	0	0	0	0
Type	R		R			R		

Bit	Name	Description
7:6	Reserved	Reserved
5:3	DEVICE_RE	Device revision
2:0	DEVICE_ID	Device ID

Table 2. EVENT_1_MASK

Address: 0x01 **Description:** EVENT_1_MASK								
Bit	7	6	5	4	3	2	1	0
Field	VBUS_OVP_MASK	IBUS_REG_MASK	VBAT_REG_MASK	IBAT_REG_MASK	VOUT_REG_MASK	TBUS_OTP_MASK	TBAT_OTP_MASK	IBUS_IREV_MASK
Default	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Description
7	VBUS_OVP_MASK	VBUS overvoltage fault mask. 0: No mask. INT will toggle when VBUS_OVP_FLT bit is set. (default) 1: VBUS_OVP_FLT is masked. INT will not toggle when VBUS_OVP_FLT bit is set.
6	IBUS_REG_MASK	IBUS overcurrent fault mask. 0: No mask. INT will toggle when IBUS_REG_FLT bit is set. (default) 1: IBUS_REG_FLT is masked. INT will not toggle when IBUS_REG_FLT bit is set.
5	VBAT_REG_MASK	VBAT overvoltage fault mask. 0: No mask. INT will toggle when VBAT_REG_LDO bit is set. (default) 1: VBAT_REG_LDO is masked. INT will not toggle when VBAT_REG_LDO bit is set.
4	IBAT_REG_MASK	IBAT overcurrent fault mask. 0: No mask. INT will toggle when IBAT_REG_LDO bit is set. (default) 1: IBAT_REG_LDO is masked. INT will not toggle when IBAT_REG_LDO bit is set.
3	VOUT_REG_MASK	VOUT overvoltage fault mask. 0: No mask. INT will toggle when VOUT_REG_LDO bit is set. (default) 1: VOUT_REG_LDO is masked. INT will not toggle when VOUT_REG_LDO bit is set.
2	TBUS_OTP_MASK	VBUS over-temperature fault mask. 0: No mask. INT will toggle when TBUS_OTP_FLT bit is set. (default) 1: TBUS_OTP_FLT is masked. INT will not toggle when TBUS_OTP_FLT bit is set.
1	TBAT_OTP_MASK	BAT over-temperature fault mask. 0: No mask. INT will toggle when TBAT_OTP_FLT bit is set. (default) 1: TBAT_OTP_FLT is masked. INT will not toggle when TBAT_OTP_FLT bit is set.
0	IBUS_IREV_MASK	IBUS reverse current fault mask. 0: No mask. INT will toggle when IBUS_REV_FLT bit is set. (default) 1: IBUS_REV_FLT is masked. INT will not toggle when IBUS_REV_FLT bit is set.

Table 3. EVENT_2_MASK

Address: 0x02 **Description:** EVENT_2_MASK								
Bit	7	6	5	4	3	2	1	0
Field	LOWCHG_ALM_MASK	ADC_DONE_MASK	VDROP_ALM_MASK	VDROP_OVP_MASK	VBUS_INSERT_MASK	BAT_INSERT_MASK	TSHUT_FLT_MASK	IOC_FLT_MASK
Default	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Description
7	LOWCHG_ALM_MASK	LOWCHG_ALM event mask. 0: No mask. INT will toggle when LOWCHG_ALM bit is set. (default) 1: LOWCHG_ALM is masked. INT will not toggle when LOWCHG_ALM bit is set.
6	ADC_DONE_MASK	ADC_DONE event mask. After all required CHs complete, set ADC_DONE 0: No mask. INT will toggle no mask when ADC_DONE bit is set. (default). 1: ADC_DONE bit is masked. INT will not toggle when ADC_DONE bit is set.
5	VDROP_ALM_MASK	VDROP_ALM_FLT mask. 0: No mask. INT will toggle when VDROP_ALM_FLT bit is set. (default) 1: VDROP_ALM_FLT is masked. INT will not toggle when VDROP_ALM_FLT bit is set.
4	VDROP_OVP_MASK	VDROP_OVP_FLT mask. 0: No mask. INT will toggle when VDROP_OVP_FLT bit is set. (default) 1: VDROP_OVP_FLT is masked. INT will not toggle when VDROP_OVP_FLT bit is set.
3	VBUS_INSERT_MASK	VBUS_INSERT mask. 0: No mask. INT will toggle when VBUS_INSERT bit is set. (default) 1: VBUS_INSERT is masked. INT will not toggle when VBUS_INSERT bit is set.
2	BAT_INSERT_MASK	BAT_INSERT mask. 0: No mask. INT will toggle when BAT_INSERT bit is set. (default) 1: VBUS_INSERT is masked. INT will not toggle when BAT_INSERT bit is set.
1	TSHUT_FLT_MASK	TSHUT_FLT mask. 0: No mask. INT will toggle when TSHUT_FLT bit is set. (default) 1: TSHUT_FLT is masked. INT will not toggle when TSHUT_FLT bit is set.
0	IOC_FLT_MASK	IOC_FLT mask. 0: No mask. INT will toggle when IOC_FLT bit is set. (default) 1: IOC_FLT is masked. INT will not toggle when IOC_FLT bit is set.

Table 4. EVENT_1

Address: 0x03 **Description:** EVENT_1								
Bit	7	6	5	4	3	2	1	0
Field	VBUS_OVP_FLT	IBUS_REG_LDO	VBAT_REG_LDO	IBAT_REG_LDO	VOUT_REG_LDO	TBUS_OTP_FLT	TBAT_OTP_FLT	IBUS_IREV_FLT
Default	0	0	0	0	0	0	0	0
Type	RC	RC	RC	RC	RC	RC	RC	RC

Bit	Name	Description
7	VBUS_OVP_FLT	VBUS overvoltage fault. This bit is set when the VBUS voltage exceeds the limit set in VBUS_OVP register. 0: No fault (default) 1: VBUS OVP fault
6	IBUS_REG_LDO	Indicates if in LDO mode due to IBUS regulation threshold. 0: No fault (default) 1: IBUS in regulation
5	VBAT_REG_LDO	Indicates if in LDO mode due to VBAT regulation threshold. 0: Not in regulation (default) 1: VBAT in regulation
4	IBAT_REG_LDO	Indicates if in LDO mode due to IBAT regulation threshold. 0: Not in regulation (default) 1: IBAT in regulation
3	VOUT_REG_LDO	Indicates if in LDO mode due to VOUT regulation threshold. 0: Not in regulation (default) 1: VOUT in regulation
2	TBUS_OTP_FLT	VBUS over-temperature fault. This bit is set when the TS_BUS voltage exceeds the limit set in TBUS_OTP register. 0: No fault (default) 1: VBUS over-temperature fault
1	TBAT_OTP_FLT	BAT over-temperature fault. This bit is set when the TS_BAT voltage exceeds the limit set in TBAT_OTP register. 0: No fault (default) 1: BAT over-temperature fault
0	IBUS_IREV_FLT	IBUS reverse current fault. This bit is set when current from BAT to VBUS is detected. The battery switch will be disabled when reverse current is detected. 0: No fault (default) 1: IBUS reverse current fault

Table 5. EVENT_2

Address: 0x04 **Description:** EVENT_2								
Bit	7	6	5	4	3	2	1	0
Field	LOWCHG_ALM_FLT	ADC_DONE	VDROP_ALM_FLT	VDROP_OVP_FLT	VBUS_INSERT	BAT_INSERT	TSHUT_FLT	IOC_FLT 0
Default	0	0	0	0	0	0	0	0
Type	RC	RC	RC	RC	RC	RC	RC	RC

Bit	Name	Description
7	LOWCHG_ALM_FLT	Indicates if LOWCHG_ALM threshold is reached. 0: No LOWCHG_ALM (default) 1: LOWCHG_ALM when CHG_EN and IBUS < threshold
6	ADC_DONE	Indicates if the ADC conversion is complete for the requested parameters in 1-shot mode only (set from 0x07). 0: Conversion not complete (default) 1: Conversion complete
5	VDROP_ALM_FLT	Indicates if VDROP_ALM threshold is reached. 0: No fault (default) 1: VDROP_ALM fault
4	VDROP_OVP_FLT	Indicates if VDROP_OVP threshold is reached. 0: No fault (default) 1: VDROP_OVP fault
3	VBUS_INSERT	Indicates if VBUS is detected 0: No VBUS (default) 1: VBUS inserted (VBUS > 2.8V)
2	BAT_INSERT	Indicates if battery is detected (sensed between BATP and BATN). 0: No BAT (default) 1: BAT inserted (VBAT > 2.0V)
1	TSHUT_FLT	IC thermal shutdown fault indicator. (TDIE > 125°C) 0: Normal operation (default) 1: Thermal shutdown
0	IOC_FLT	Indicates if high current from VBUS to VOUT has hit the internal threshold. 0: No fault (default) 1: High current fault

Table 6. EVENT_1_EN

Address: 0x05 **Description:** EVENT_1_EN								
Bit	7	6	5	4	3	2	1	0
Field	VBUS_OVP_EN	IBUS_REG_EN	VBAT_REG_EN	IBAT_REG_EN	VOUT_REG_EN	TBUS_OTP_EN	TBAT_OTP_EN	VBUS_PD_EN
Default	1	1	1	1	1	1	1	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Description
7	VBUS_OVP_EN	Enables VBUS_OVP protection 0: Disable VBUS OVP protection 1: Enable VBUS OVP protection (default)
6	IBUS_REG_EN	Enables IBUS regulation for LDO mode 0: Disable IBUS OCP protection 1: Enable IBUS OCP protection (default)
5	VBAT_REG_EN	Enables VBAT regulation for LDO mode 0: Disable VBAT regulation 1: Enable VBAT regulation (default)
4	IBAT_REG_EN	Enables IBAT regulation for LDO mode 0: Disable IBAT regulation 1: Enable IBAT regulation (default)
3	VOUT_REG_EN	Enables VOUT regulation in LDO mode 0: Disable VOUT regulation 1: Enable VOUT regulation (default)
2	TBUS_OTP_EN	Enables TS_VBUS pin protection 0: Disable TBUS_OTP 1: Enable TBUS_OTP (default)
1	TBAT_OTP_EN	Enables TS_BAT pin protection 0: Disable TBAT_OTP 1: Enable TBAT_OTP (default)
0	VBUS_PD_EN	Enables the VBUS pull-down resistor 0: Disable RVBUS_PD (default) 1: Enable RVBUS_PD

Table 7. CONTROL1

Address: 0x06 **Description:** CONTROL1								
Bit	7	6	5	4	3	2	1	0
Field	VDROP_OVP_EN	VDROP_ALM_EN	SENSE_R	CHG_EN	WATCHDOG<1:0>		IREV_EN	REG_RST
Default	0	0	1	0	1	0	1	0
Type	RW	RW	RW	RW	RW		RW	RW

Bit	Name	Description
7	VDROP_OVP_EN	Enables VDROP_OVP protection 0: Disable VDROP_OVP (default) 1: Enable VDROP_OVP
6	VDROP_ALM_EN	Enables VDROP_ALM alarm 0: Disable VDROP_ALM (default) 1: Enable VDROP_ALM
5	SENSE_R	Selects the sense resistor value between SRP and SRN 0: 5mΩ 1: 10mΩ (default)
4	CHG_EN	Software bit for charge enable. This enables the Load Switch. This bit will be set to '0' if reset or any action of FET turned off (STATUS register). 0: Charge disabled (default) 1: Charge enabled
3:2	WATCHDOG<1:0>	Watchdog timer setting. RW any register will clear the watchdog timer. FET must turn off after watchdog timer out. 00: Disable watchdog timer 01: 0.5sec 10: 1.0sec (default) 11: 2.0sec
1	IREV_EN	Reverse current protection (RCP) comparator control. 0: RCP disable 1: RCP enable (default)
0	REG_RST	Register reset 0: No reset (default) 1: Reset all registers to their default values

Table 8. ADC_CTRL

Address: 0x07 **Description:** ADC_CTRL								
Bit	7	6	5	4	3	2	1	0
Field	TDIE_ ADC_EN	Reserved			ADC_EN	ADC_ RATE	ADC_ AVG_EN	ADC_ SAMPLES
Default	1	0	0	0	1	1	1	1
Type	RW	RW			RW	RW	RW	RW

Bit	Name	Description
7	TDIE_ADC_EN	Enable/disable TDIE_ADC sampling 0: Disable sampling 1: Enable sampling (default)
6:4	Reserved	Reserved
3	ADC_EN	Enable/disable ADC 0: Disable ADC 1: Enable ADC (default)
2	ADC_RATE	Sets ADC conversion rate 0: 1-shot conversion 1: Continuous conversion (default)
1	ADC_AVG_EN	Enable/disable ADC measurement averaging 0: Disable averaging (instantaneous measurement) 1: Enable averaging (default)
0	ADC_SAMPLES	Sets the number of samples to be taken for an ADC conversion 0: 8 samples taken for averaging 1: 16 samples taken for averaging (default)

Table 9. SAMPLE_EN

Address: 0x08 **Description:** SAMPLE_EN								
Bit	7	6	5	4	3	2	1	0
Field	VBUS_ ADC_EN	IBUS_ ADC_EN	VOUT_ ADC_EN	VDROP _ADC_ EN	VBAT_ ADC_EN	IBAT_ ADC_EN	TBUS_ ADC_EN	TBAT_ ADC_EN
Default	1	1	1	1	1	1	1	1
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Description
7	VBUS_ADC_EN	Enable/disable VBUS_ADC sampling. 0: Disable sampling 1: Enable sampling (default)
6	IBUS_ADC_EN	Enable/disable IBUS_ADC sampling. 0: Disable sampling 1: Enable sampling (default)
5	VOUT_ADC_EN	Enable/disable VOUT_ADC sampling. 0: Disable sampling 1: Enable sampling (default)
4	VDROP_ADC_EN	Enable/disable VDROP_ADC sampling. 0: Disable sampling 1: Enable sampling (default)
3	VBAT_ADC_EN	Enable/disable VBAT_ADC sampling. 0: Disable sampling 1: Enable sampling (default)
2	IBAT_ADC_EN	Enable/disable IBAT_ADC sampling. 0: Disable sampling 1: Enable sampling (default)
1	TBUS_ADC_EN	Enable/disable TBUS_ADC sampling. 0: Disable sampling 1: Enable sampling (default)
0	TBAT_ADC_EN	Enable/disable TBAT_ADC sampling. 0: Disable sampling 1: Enable sampling (default)

Table 10. PROT_DLY&OCP

Address: 0x09 **Description:** PROT_DLY&OCP								
Bit	7	6	5	4	3	2	1	0
Field	IOC_OCP<3:0>				LOWCHG_ALM_EN	LOWCHG_ALM	OCP_RES	VBUS_OVP_DLY
Default	1	0	1	0	0	0	0	0
Type	RW				RW	RW	RW	RW

Bit	Name	Description
7:4	IOC_OCP<3:0>	IOC_OCP (Input Overcurrent Protection) Offset: 0A LSB<3:0>: 4A, 2A, 1A, 0.5A Range Min.: 0A (0000) Range Max.: 6.5A (1101) Default: 5A (1010)
3	LOWCHG_ALM_EN	Enables LOWCHG_ALM in CHG mode 0: Disable LOWCHG_ALM (default) 1: Enable LOWCHG_ALM
2	LOWCHG_ALM	LOWCHG_ALM 0: 100mA (default) (0x15<4:0> = 00000, 0x16<7:0> = 00110010) 1: 200mA (0x15<4:0> = 00000, 0x16<7:0> = 01100100)
1	OCP_RES	Controls the response of the OCP event for IBUS. 0: Blanking mode; the device will wait 50μs before the battery switch is disabled and latched off (default) 1: Hiccup mode; battery switch is disabled instantaneously, and the device will attempt to turn on the battery switch wait 250μs to check OCP and turn off every 100ms, up to 7 times before latching off.
0	VBUS_OVP_DLY	Sets VBUS fault deglitch time 0: 4μs deglitch time (default) 1: 20μs deglitch time

Table 11. VBUS_OVP

Address: 0x0A **Description:** VBUS_OVP								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	VBUS_OVP<6:0>						
Default	0	0	1	1	0	1	0	0
Type	RW	RW						

Bit	Name	Description
7	Reserved	Reserved
6:0	VBUS_OVP<6:0>	VBUS_OVP Offset: 4.2V LSB<6:0>: 1600mV, 800mV, 400mV, 200mV, 100mV, 50mV, 25mV Range Min.: 4.2V (0000000) Range Max.: 6.5V (1011100) Default: 5.5V (0110100)

Table 12. VOUT_REG

Address: 0x0B **Description:** VOUT_REG								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	VOUT_REG <6:0>						
Default	0	0	0	1	0	1	0	0
Type	RW	RW						

Bit	Name	Description
7	Reserved	Reserved
6:0	VOUT_REG <6:0>	VOUT_Regulation (BAT – GND) Offset: 4.2V LSB<6:0>: 640mV, 320mV, 160mV, 80mV, 40mV, 20mV, 10mV Range Min.: 4.2V (0000000) Range Max.: 5.0V (1010000) Default: 4.4V (0010100)

Table 13. VDROP_OVP

Address: 0x0C **Description:** VDROP_OVP								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	VDROP_OVP<6:0>						
Default	0	0	0	1	1	1	1	0
Type	RW	RW						

Bit	Name	Description
7	Reserved	Reserved
6:0	VDROP_OVP<6:0>	VDROP_OVP Offset: 0V LSB<6:0>: 640mV, 320mV, 160mV, 80mV, 40mV, 20mV, 10mV Range Min.: 0mV (0000000) Range Max.: 1000mV (1100100) Default: 300mV (0011110)

Table 14. VDROP_ALM

Address: 0x0D **Description:** VDROP_ALM								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	VDROP_ALM<6:0>						
Default	0	0	0	0	1	0	1	0
Type	RW	RW						

Bit	Name	Description
7	Reserved	Reserved
6:0	VDROP_ALM<6:0>	VDROP_ALM Offset: 0V LSB<6:0>: 640mV, 320mV, 160mV, 80mV, 40mV, 20mV, 10mV Range Min.: 0mV (0000000) Range Max.: 1000mV (1100100) Default: 100mV (0001010)

Table 15. VBAT_REG

Address: 0x0E **Description:** VBAT_REG								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	VBAT_REG<6:0>						
Default	0	0	0	0	1	0	1	0
Type	RW	RW						

Bit	Name	Description
7	Reserved	Reserved
[6:0]	VBAT_REG<6:0>	VBAT_Regulation (BATP – BATN) Offset: 4.2V LSB<6:0>: 640mV, 320mV, 160mV, 80mV, 40mV, 20mV, 10mV Range Min.: 4.2V (0000000) Range Max.: 5.0V (1010000) Default: 4.3V (0001010)

Table 16. IBAT_OCP

Address: 0x0F **Description:** IBAT_OCP								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	IBAT_OCP<6:0>						
Default	0	0	1	0	1	0	0	0
Type	RW	RW						

Bit	Name	Description
7	Reserved	Reserved
6:0	IBAT_OCP<6:0>	IBAT_OCP Offset: 0A LSB<6:0>: 3200mA, 1600mA, 800mA, 400mA, 200mA, 100mA, 50mA Range Min.: 0.40A (0001000) Range Max.: 6.35A (1111111) Default: 2A (0101000)

Table 17. IBUS_OCP

Address: 0x10 **Description:** IBUS_OCP								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	IBUS_OCP<6:0>						
Default	0	1	1	0	0	1	0	0
Type	RW	RW						

Bit	Name	Description
7	Reserved	Reserved
6:0	IBUS_OCP<6:0>	IBUS_OCP (Input Current Regulation) Offset: 0A LSB<6:0>: 3200mA, 1600mA, 800mA, 400mA, 200mA, 100mA, 50mA Range Min.: 0.40A (0001000) Range Max.: 6.35A (1111111) Default: 5A (1100100)

Table 18. TBUS_OTP

Address: 0x11 **Description:** TBUS_OTP								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	TBUS_OTP<6:0>						
Default	0	0	0	1	1	1	1	0
Type	RW	RW						

Bit	Name	Description
7	Reserved	Reserved
6:0	TBUS_OTP<6:0>	TBUS_OTP Offset: 0V LSB<6:0>: 1280mV, 640mV, 320mV, 160mV, 80mV, 40mV, 20mV Range Min.: 0V (0000000) Range Max.: 2.4V (1111000) Default: 0.6V (0011110) External VREF = 1.8V, 10k/10k Divide

Table 19. TBAT_OTP

Address: 0x12 **Description:** TBAT_OTP								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	TBAT_OTP<6:0>						
Default	0	0	1	0	0	0	1	1
Type	RW	RW						

Bit	Name	Description
7	Reserved	Reserved
6:0	TBAT_OTP<6:0>	TBAT_OTP Offset: 0V LSB<6:0>: 1280mV, 640mV, 320mV, 160mV, 80mV, 40mV, 20mV Range Min.: 0V (0000000) Range Max.: 2.4V (1111000) Default:0.7V (0100011) External VREF = 1.8V, 10k/10k Divide

Table 20. VBUS_ADC2

Address: 0x13 **Description:** VBUS_ADC2								
Bit	7	6	5	4	3	2	1	0
Field	VBUS_POL	Reserved		VBUS_ADC2<4:0>				
Default	0	0	0	0	0	0	0	0
Type	R	R		R				

Bit	Name	Description
7	VBUS_POL	Indicates polarity of VBUS 0: Positive voltage(default) 1: Negative voltage
6:5	Reserved	Reserved
4:0	VBUS_ADC2<4:0>	VBUS_ADC2 LSB: 1mV LSB<4:0>: 4096, 2048, 1024, 512, 256

Table 21. VBUS_ADC1

Address: 0x14 **Description:** VBUS_ADC1								
Bit	7	6	5	4	3	2	1	0
Field	VBUS_ADC1<7:0>							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	VBUS_ADC1<7:0>	VBUS_ADC1 LSB: 1mV LSB<7:0>: 128, 64, 32, 16, 8, 4, 2, 1

Table 22. IBUS_ADC2

Address: 0x15 **Description:** IBUS_ADC2								
Bit	7	6	5	4	3	2	1	0
Field	IBUS_POL	Reserved		IBUS_ADC2<4:0>				
Default	0	0	0	0	0	0	0	0
Type	R	R		R				

Bit	Name	Description
7	IBUS_POL	Indicates polarity of IBUS 0: Positive current(default) 1: Negative current
6:5	Reserved	Reserved
4:0	IBUS_ADC2<4:0>	IBUS_ADC2 LSB: 1mA LSB<4:0>: 4096, 2048, 1024, 512, 256

Table 23. IBUS_ADC1

Address: 0x16 **Description:** IBUS_ADC1								
Bit	7	6	5	4	3	2	1	0
Field	IBUS_ADC1<7:0>							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	IBUS_ADC1<7:0>	IBUS_ADC1 LSB: 1mA LSB<7:0>: 128, 64, 32, 16, 8, 4, 2, 1

Table 24. VOUT_ADC2

Address: 0x17 **Description:** VOUT_ADC2								
Bit	7	6	5	4	3	2	1	0
Field	VOUT_POL	Reserved		VOUT_ADC2<4:0>				
Default	0	0	0	0	0	0	0	0
Type	R	R		R				

Bit	Name	Description
7	VOUT_POL	Indicates polarity of VOUT 0: Positive voltage(default) 1: Negative voltage
6:5	Reserved	Reserved
4:0	VOUT_ADC2<4:0>	VOUT_ADC2 LSB: 1mV LSB<4:0>: 4096, 2048, 1024, 512, 256

Table 25. VOUT_ADC1

Address: 0x18 **Description:** VOUT_ADC1								
Bit	7	6	5	4	3	2	1	0
Field	VOUT_ADC1<7:0>							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	VOUT_ADC1<7:0>	VOUT_ADC1 LSB: 1mV LSB<7:0>: 128, 64, 32, 16, 8, 4, 2, 1

Table 26. VDROP_ADC2

Address: 0x19 **Description:** VDROP_ADC2								
Bit	7	6	5	4	3	2	1	0
Field	VDROP_POL	Reserved					VDROP_ADC2<1:0>	
Default	0	0	0	0	0	0	0	0
Type	R	R		R				

Bit	Name	Description
7	VDROP_POL	Indicates polarity of VDROP 0: Positive voltage(default) 1: Negative voltage
6:2	Reserved	Reserved
1:0	VDROP_ADC2<1:0>	VDROP_ADC2 LSB: 1mV LSB<1:0>: 512, 256

Table 27. VDROP_ADC1

Address: 0x1A **Description:** VDROP_ADC1								
Bit	7	6	5	4	3	2	1	0
Field	VDROP_ADC1<7:0>							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	VDROP_ADC1<7:0>	VDROP_ADC1 LSB: 1mV LSB<7:0>: 128, 64, 32, 16, 8, 4, 2, 1

Table 28. VBAT_ADC2

Address: 0x1B **Description:** VBAT_ADC2								
Bit	7	6	5	4	3	2	1	0
Field	VBAT_POL	Reserved		VBAT_ADC2<4:0>				
Default	0	0	0	0	0	0	0	0
Type	R	R		R				

Bit	Name	Description
7	VBAT_POL	Indicates polarity of VBAT 0: Positive voltage(default) 1: Negative voltage
6:5	Reserved	Reserved
4:0	VBAT_ADC2<4:0>	VBAT_ADC2 LSB: 1mV LSB<4:0>: 4096, 2048, 1024, 512, 256

Table 29. VBAT_ADC1

Address: 0x1C **Description:** VBAT_ADC1								
Bit	7	6	5	4	3	2	1	0
Field	VBAT_ADC1<7:0>							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	VBAT_ADC1<7:0>	VBAT_ADC1 LSB: 1mV LSB<7:0>: 128, 64, 32, 16, 8, 4, 2, 1

Table 30. IBAT_ADC2

Address: 0x1D **Description:** IBAT_ADC2								
Bit	7	6	5	4	3	2	1	0
Field	IBAT_POL	Reserved		IBAT_ADC2<4:0>				
Default	0	0	0	0	0	0	0	0
Type	R	R		R				

Bit	Name	Description
7	IBAT_POL	Indicates polarity of IBAT 0: Positive current(default) 1: Negative current
6:5	Reserved	Reserved
4:0	IBAT_ADC2<4:0>	IBAT_ADC2 LSB: 1mA LSB<4:0>: 4096, 2048, 1024, 512, 256

Table 31. IBAT_ADC1

Address: 0x1E **Description:** IBAT_ADC1								
Bit	7	6	5	4	3	2	1	0
Field	IBAT_ADC1<7:0>							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	IBAT_ADC1<7:0>	IBAT_ADC1 LSB: 1mA LSB<7:0>: 128, 64, 32, 16, 8, 4, 2, 1

Table 32. TBUS_ADC2

Address: 0x1F **Description:** TBUS_ADC2								
Bit	7	6	5	4	3	2	1	0
Field	TBUS_POL	Reserved			TBUS_ADC2<3:0>			
Default	0	0	0	0	0	0	1	1
Type	R	R			R			

Bit	Name	Description
7	TBUS_POL	Indicates polarity of TBUS 0: Positive voltage(default) 1: Negative voltage
6:4	Reserved	Reserved
3:0	TBUS_ADC2<3:0>	TBUS_ADC2 LSB: 1mV LSB<3:0>: 2048, 1024, 512, 256

Table 33. TBUS_ADC1

Address: 0x20 **Description:** TBUS_ADC1								
Bit	7	6	5	4	3	2	1	0
Field	TBUS_ADC1<7:0>							
Default	1	0	0	0	0	1	0	0
Type	R							

Bit	Name	Description
7:0	TBUS_ADC1<7:0>	TBUS_ADC1 LSB: 1mV LSB<7:0>: 128, 64, 32, 16, 8, 4, 2, 1

Table 34. TBAT_ADC2

Address: 0x21 **Description:** TBAT_ADC2								
Bit	7	6	5	4	3	2	1	0
Field	TBAT_POL	Reserved			TBAT_ADC2<3:0>			
Default	0	0	0	0	0	0	1	1
Type	R	R			R			

Bit	Name	Description
7	TBAT_POL	Indicates polarity of TBAT 0: Positive voltage(default) 1: Negative voltage
6:4	Reserved	Reserved
3:0	TBAT_ADC2<3:0>	TBAT_ADC2 LSB: 1mV LSB<3:0>: 2048, 1024, 512, 256

Table 35. TBAT_ADC1

Address: 0x22 **Description:** TBAT_ADC1								
Bit	7	6	5	4	3	2	1	0
Field	TBAT_ADC1<7:0>							
Default	1	0	0	0	0	1	0	0
Type	R							

Bit	Name	Description
7:0	TBAT_ADC1<7:0>	TBAT_ADC1 LSB: 1mV LSB<7:0>: 128, 64, 32, 16, 8, 4, 2, 1

Table 36. TDIE_ADC1

Address: 0x23 **Description:** TDIE_ADC1								
Bit	7	6	5	4	3	2	1	0
Field	TDIE_ADC1<7:0>							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	TDIE_ADC1<7:0>	TDIE_ADC1 LSB: 1°C LSB<7:0>: 128, 64, 32, 16, 8, 4, 2, 1

Table 37. EVENT_STATUS_1

Address: 0x24 **Description:** EVENT_STATUS_1								
Bit	7	6	5	4	3	2	1	0
Field	VBUS_OVP_STATUS	IBUS_REG_STATUS	VBAT_REG_STATUS	IBAT_REG_STATUS	VOUT_REG_STATUS	TBUS_OTP_STATUS	TBAT_OTP_STATUS	IBUS_IREV_STATUS
Default	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R

Bit	Name	Description
7	VBUS_OVP_STATUS	VBUS overvoltage fault. This bit is set when the VBUS voltage exceeds the limit set in VBUS_OVP register. 0: No fault (default) 1: VBUS OVP fault
6	IBUS_REG_STATUS	Indicates if in LDO mode due to IBUS regulation threshold. 0: No fault (default) 1: IBUS in regulation
5	VBAT_REG_STATUS	Indicates if in LDO mode due to VBAT regulation threshold. 0: No in regulation (default) 1: VBAT in regulation
4	IBAT_REG_STATUS	Indicates if in LDO mode due to IBAT regulation threshold. 0: Not in regulation (default) 1: IBAT in regulation
3	VOUT_REG_STATUS	Indicates if in LDO mode due to VOUT regulation threshold. 0: Not in regulation (default) 1: VOUT in regulation
2	TBUS_OTP_STATUS	VBUS over-temperature fault. This bit is set when the TS_BUS voltage exceeds the limit set in TBUS_OTP register. 0: No fault (default) 1: VBUS over-temperature fault
1	TBAT_OTP_STATUS	BAT over-temperature fault. This bit is set when the TS_BAT voltage exceeds the limit set in TBAT_OTP register. 0: No fault (default) 1: BAT over-temperature fault
0	IBUS_IREV_STATUS	IBUS reverse current fault. This bit is set when current from BAT to VBUS is detected. The battery switch will be disabled when reverse current is detected. 0: No fault (default) 1: IBUS reverse current fault

Table 38. EVENT_STATUS_2

Address: 0x25 **Description:** EVENT_STATUS_2								
Bit	7	6	5	4	3	2	1	0
Field	LOWCHG_ALM_STATUS	ADC_DONE_STATUS	VDROP_ALM_STATUS	VDROP_OVP_STATUS	VBUS_INSERT_STATUS	BAT_INSERT_STATUS	TSHUT_STATUS	IOC_STATUS
Default	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R

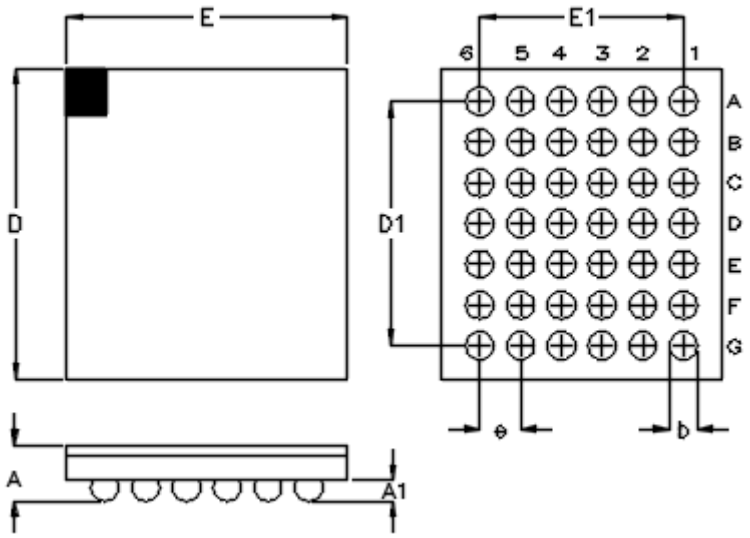
Bit	Name	Description
7	LOWCHG_ALM_STATUS	Indicates if LOWCHG_ALM threshold is reached. 0: No LOWCHG_ALM (default) 1: LOWCHG_ALM when CHG_EN and IBUS < threshold
6	ADC_DONE_STATUS	Indicates if the ADC conversion is complete for the requested parameters in 1-shot mode only (set from 0x07). 0: Conversion not complete (default) 1: Conversion complete
5	VDROP_ALM_STATUS	Indicates if VDROP_ALM threshold is reached. 0: No fault (default) 1: VDROP_ALM fault
4	VDROP_OVP_STATUS	Indicates if VDROP_OVP threshold is reached. 0: No fault (default) 1: VDROP_OVP fault
3	VBUS_INSERT_STATUS	Indicates if VBUS is detected 0: No VBUS (default) 1: VBUS inserted (VBUS > 2.8V)
2	BAT_INSERT_STATUS	Indicates if battery is detected (sensed between BATP and BATN). 0: No BAT (default) 1: BAT inserted (VBAT > 2.0V)
1	TSHUT_STATUS	IC thermal shutdown fault indicator. (TDIE > 125°C) 0: Normal operation (default) 1: Thermal shutdown
0	IOC_STATUS	Indicates if high current from VBUS to VOUT has hit the internal threshold. 0: No fault (default) 1: High current fault

Table 39. CONTROL2

Address: 0x26 **Description:** CONTROL2								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				IREV_OCP<3:0>			
Default	0	0	0	0	0	0	0	1
Type	RW				RW			

Bit `	Name	Description
7:4	Reserved	Reserved
3:0	IREV_OCP<3:0>	IREV_OCP (R_{ON} = 10mΩ) Offset: 0A LSB<3:0>: 4A (40mV), 2A (20mV), 1A(10mV), 0.5A (5mV) Range Min.: 0A (0000) Range Max.: 4A (1000) Default: 500mA (0001)

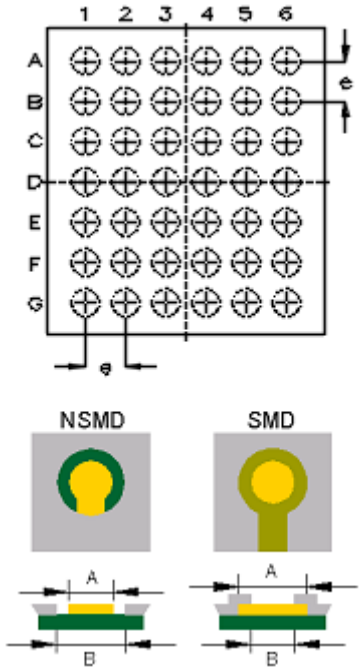
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	3.010	3.090	0.119	0.122
D1	2.400		0.094	
E	2.710	2.790	0.107	0.110
E1	2.000		0.079	
e	0.400		0.016	

42B WL-CSP 2.75x3.05 Package (BSC)

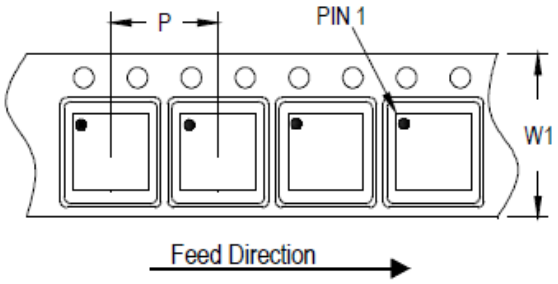
Footprint Information

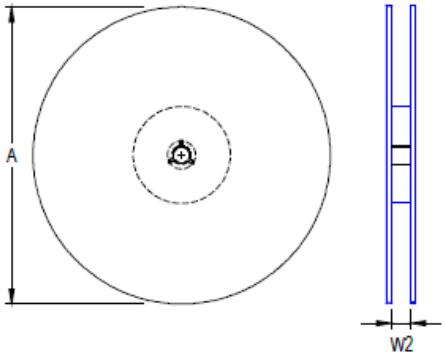


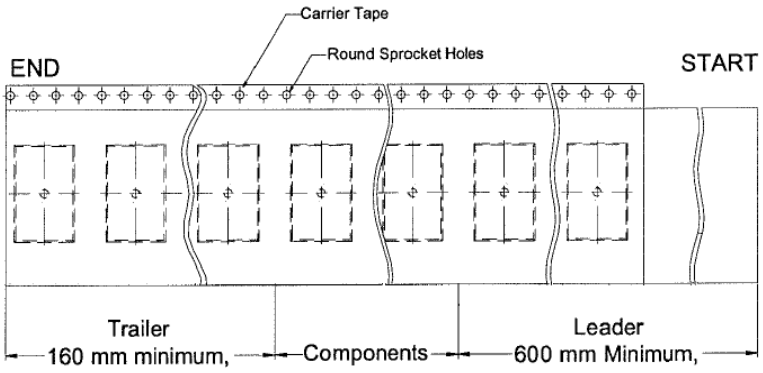
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP2.75*3.05-42(BSC)	42	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

Packing Information

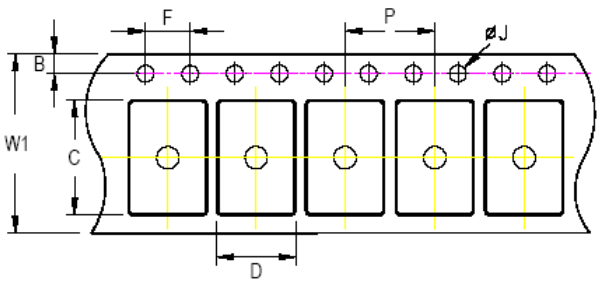
Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 2.75x3.05	12	8	180	7	1,500	160	600	12.4/14.4



C, D and K are determined by component size.

The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
WL-CSP 2.75x3.05	7”	1,500	Box A	18.3*18.3*8.0	3	4,500	Carton A	38.3*27.2*38.3	12	54,000
			Box E	18.6*18.6*3.5	1	1,500	For Combined or Partial Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

Datasheet Revision History

Version	Date	Description	Item
00	2023/6/15	Final	Ordering Information on P1