Smart Multi-Voltage Detector

General Description
The RT9824C is an integrated smart multi-voltage detector supervising three power supply voltage levels including 5V, 5.4V and additional 3.3V, 12V or other voltage which can be determined by external divided resistors.

The RT9824C performs supervisory function by sending out RESET and CTR signals whenever the monitored voltages fall below 80% of voltage levels. The RESET and CTR signals will last the whole period before VCC recovering. Once the supervising voltages are recovered to higher than 80% of the voltage levels, the RESET and CTR signal will be released after 60ms delay time.

MR (Manual Reset) controls CTR signal during three monitored power supply voltages at normal voltage levels. When MR signal is in logic high, the CTR signal will be pulled low immediately. However the RESET will not be interfered and will be kept at high level.

The RT9824C is available in the TSOT-23-8 package.

Features
- Capable of Monitoring Three Inputs Precisely
- Detection Threshold Voltages
  - VCC Connect to 5V or 3.3V Standby Power
  - V5 : 5V x 80%
  - V54 : 5.4V x 80%
  - VADJ : 1V (Using Resistor Divider)
- Accuracy : ±2%
- RESET (Open Drain Output Active Low)
- Built-in Recovery Delay 60ms
- CTR (Open Drain Output Active Low)
- Manual Reset (MR) Function
- TSOT-23-8 Package
- RoHS Compliant and Halogen Free

Applications
- LCD TV or Monitors
- Consumer Electronic Products
- System Voltage Detector

Pin Configurations

Ordering Information

Marking Information

0K=DNN
0K= : Product Code
DNN : Date Code
## Functional Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CTR</td>
<td>Control Output (Open Drain, Active-Low). Only when VCC is &gt; POR, V5 is &gt; 80%, V54 is &gt; 80%, and VADJ is &gt; 1V, the CTR will delay 60ms and become high. Once V5 or V54 or VADJ is &lt; 80%, the signal will become low. When MR is high, CTR will become low.</td>
</tr>
<tr>
<td>2</td>
<td>RESET</td>
<td>RESET Output (Open Drain, Active-Low). Only when VCC is &gt; POR, V5 is &gt; 80%, V54 is &gt; 80%, and VADJ is &gt; 1V, the RESET will delay 60ms and become high. Once V5 or V54 or VADJ is &lt; 80%, the signal will become low.</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Ground.</td>
</tr>
<tr>
<td>4</td>
<td>MR</td>
<td>Manual Reset Input. Manual reset with internal pull high resistor (1MΩ), H : CTR = Low; L : CTR signal is dependent on voltage detector output.</td>
</tr>
<tr>
<td>5</td>
<td>VADJ</td>
<td>Voltage Detection Input. Connect 12V or other power with external resister divider to this pin. The VADJ logic-high threshold voltage is 1V.</td>
</tr>
<tr>
<td>6</td>
<td>V5</td>
<td>5V Voltage Detection Input. The detection threshold is 5V x 80%.</td>
</tr>
<tr>
<td>7</td>
<td>V54</td>
<td>54V Voltage Detection Input. The detection threshold is 5.4V x 80%.</td>
</tr>
<tr>
<td>8</td>
<td>VCC</td>
<td>Connect this Pin to Standby Power from system.</td>
</tr>
</tbody>
</table>

## Function Block Diagram

![Function Block Diagram](image)

- **VCC**: Standby Power
- **VREF**: Reference Voltage
- **Voltage Regulator**: Regulates the input voltage to the desired level
- **POR**: Power On Reset
- **Voltage Detector (VTH = 1V)**: Monitors VADJ
- **Voltage Detector (VTH = 5V x 80%)**: Monitors V5 and V54
- **Delay 60ms**: Provides a delay before the output becomes active
- **CTR**: Control Output
- **RESET**: Reset Output
- **GND**: Ground
- **MR**: Manual Reset Input
Operation

The RT9824 smart voltage detector monitors three voltage levels at the same time to ensure the micro-processor is operated within the recommended input voltage range. In conventional reset IC application, to monitor one power rail needs one reset IC. The RT9824 can monitor three power rails simultaneously, by using just one reset IC. The RT9824 also provides a Manual Reset (MR) function for application easily. Glitch-rejection is implemented in the RT9824 to prevent it from false operation and to eliminate the additional de-bouncing circuitry.

POR Protection

To protect the chip from operating at insufficient supply voltage, the POR is needed. When the input voltage of VIN is lower than the POR falling threshold voltage, the device will be lockout.
Absolute Maximum Ratings  (Note 1)

- VCC, CTR, MR, RESET, V5, V54, VADJ  
  -0.3V to 6.5V
- Power Dissipation, PD @ TA = 25°C  
  TSOT-23-8  - 0.435W
- Package Thermal Resistance  (Note 2)  
  TSOT-23-8, θJA  - 230°C/W
- Junction Temperature  
  -150°C
- Lead Temperature (Soldering, 10 sec.)  
  -260°C
- Storage Temperature Range  
  -65°C to 150°C
- ESD Susceptibility  (Note 3)  
  HBM (Human Body Model)  - 2kV  
  MM (Machine Model)  - 200V

Recommended Operating Conditions  (Note 4)

- Junction Temperature Range  -40°C to 125°C

Electrical Characteristics  
(VCC = 5V, TA = 25°C, unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC Supply Current</td>
<td>IVCCE</td>
<td>Without load</td>
<td>--</td>
<td>--</td>
<td>200</td>
<td>μA</td>
</tr>
<tr>
<td>VCC Operating Voltage</td>
<td>VCC</td>
<td></td>
<td>2.97</td>
<td>5</td>
<td>5.94</td>
<td>V</td>
</tr>
<tr>
<td>VCC POR Rising</td>
<td>VPOR</td>
<td></td>
<td>--</td>
<td>2.8</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>VCC POR Hysteresis</td>
<td>VPOR_Hys</td>
<td></td>
<td>--</td>
<td>0.15</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>Voltage Detector &amp; MUTE Threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V5 High Threshold Voltage</td>
<td>V5TH</td>
<td></td>
<td>3.92</td>
<td>4</td>
<td>4.08</td>
<td>V</td>
</tr>
<tr>
<td>V54 High Threshold Voltage</td>
<td>V54TH</td>
<td></td>
<td>4.23</td>
<td>4.32</td>
<td>4.41</td>
<td>V</td>
</tr>
<tr>
<td>VADJ High Threshold Voltage</td>
<td>VADJTH</td>
<td></td>
<td>0.98</td>
<td>1</td>
<td>1.02</td>
<td>V</td>
</tr>
<tr>
<td>Manual Reset High Voltage</td>
<td>VH</td>
<td></td>
<td>2</td>
<td>--</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>Manual Reset Low Voltage</td>
<td>VL</td>
<td></td>
<td>--</td>
<td>--</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>Voltage Detector Deglitch and Delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage Detectors Delay Time</td>
<td>T_DELAY</td>
<td></td>
<td>45</td>
<td>60</td>
<td>80</td>
<td>ms</td>
</tr>
<tr>
<td>Voltage Detectors Deglitch Time</td>
<td>T_DEGLITCH</td>
<td></td>
<td>--</td>
<td>20</td>
<td>--</td>
<td>μs</td>
</tr>
<tr>
<td>Output : Open Drain</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RESET Output Low Voltage</td>
<td>VOL_RESET</td>
<td>VCC = 3.3V, 5mA sinking current at RESET output</td>
<td>--</td>
<td>--</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>CTR Output Low Voltage</td>
<td>VOL_CTR</td>
<td>VCC = 3.3V, 5mA sinking current at CTR output</td>
<td>--</td>
<td>--</td>
<td>0.3</td>
<td>V</td>
</tr>
</tbody>
</table>
Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. $\theta_{JA}$ is measured at $T_A = 25^\circ$C on a low effective thermal conductivity single-layer test board per JEDEC 51-3.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.
Typical Operating Characteristics

**V5 Detector Delay Time vs. Temperature**

![Graph](image1)

**V5 Detector Deglitch Time vs. Temperature**

![Graph](image2)

**V54 Detector Delay Time vs. Temperature**

![Graph](image3)

**V54 Detector Deglitch Time vs. Temperature**

![Graph](image4)

**VADJ Detector Delay Time vs. Temperature**

![Graph](image5)

**VADJ Detector Deglitch Time vs. Temperature**

![Graph](image6)
Supply Current vs. Temperature

- **VCC = 5V**
- **VCC = 3.3V**

Power On from MR

- **MR (5V/Div)**
- **CTR (2V/Div)**
- **RESET (2V/Div)**

Time (25ms/Div)

Power Off from MR

- **MR (1V/Div)**
- **CTR (2V/Div)**
- **RESET (2V/Div)**

Time (25ms/Div)
Application Information

The RT9824C smart voltage detector monitors three voltage levels at the same time to ensure the microprocessor is operated within the recommended input voltage range. In conventional reset IC application, to monitor one power rail needs one reset IC. The RT9824C can monitor three power rails simultaneously, by using just one reset IC. The RT9824C also provides a Manual Reset (MR) function for application easily. Glitch-rejection is implemented in the RT9824C to prevent it from false operation and to eliminate the additional de-bouncing circuitry.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

\[ P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}} \]

Where \( T_{J(MAX)} \) is the maximum operation junction temperature, \( T_A \) is the ambient temperature and the \( \theta_{JA} \) is the junction to ambient thermal resistance.

For recommended operating conditions specification, the maximum junction temperature is 125°C. The junction to ambient thermal resistance \( \theta_{JA} \) is layout dependent. For TSOT-23-8 package, the thermal resistance \( \theta_{JA} \) is 250°C/W on the standard JEDEC 51-3 single layer thermal test board. The maximum power dissipation at \( T_A = 25°C \) can be calculated by following formula:

\[ P_{D(MAX)} = \frac{(125°C - 25°C)}{(230°C/W)} = 0.435W \] for TSOT-23-8 package

The maximum power dissipation depends on operating ambient temperature for fixed \( T_{J(MAX)} \) and thermal resistance \( \theta_{JA} \). The Figure 1 of derating curve allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

Figure 1. Derating Curve of Maximum Power Dissipation
Outline Dimension

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Dimensions In Millimeters</th>
<th>Dimensions In Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>A</td>
<td>0.700</td>
<td>1.000</td>
</tr>
<tr>
<td>A1</td>
<td>0.000</td>
<td>0.100</td>
</tr>
<tr>
<td>B</td>
<td>1.397</td>
<td>1.803</td>
</tr>
<tr>
<td>b</td>
<td>0.220</td>
<td>0.380</td>
</tr>
<tr>
<td>C</td>
<td>2.591</td>
<td>3.000</td>
</tr>
<tr>
<td>D</td>
<td>2.692</td>
<td>3.099</td>
</tr>
<tr>
<td>e</td>
<td>0.585</td>
<td>0.715</td>
</tr>
<tr>
<td>H</td>
<td>0.080</td>
<td>0.254</td>
</tr>
<tr>
<td>L</td>
<td>0.300</td>
<td>0.610</td>
</tr>
</tbody>
</table>

TSOT-23-8 Surface Mount Package