Integrated Multi-Channel DC/DC Converter for TFT LCD Panels

General Description

The RT9921 includes a high-performance boost regulator, a low dropout linear regulator (LDO), a gate pulse modulator (GPM), a voltage detector, a VCOM buffer (unity-gain OPA), and a VGH charge pump controller for active-matrix thin-film transistor (TFT) liquid-crystal displays (LCDs).

The boost converter provides the regulated supply voltage for the panel source driver ICs. The converter is a high switching frequency (640kHz or 1.2MHz) current-mode regulator with an integrated 16V N-Channel 0.2Ω MOSFET that allows the use of ultra-small inductors and ceramic capacitors. It provides fast transient response to pulsed loading while achieving efficiency over 90%. The device can produce output voltage as high as 15V from an input as low as 2.5V. Soft-Start is programmed by external capacitor, which sets the input-current ramp-rate.

The low-dropout (LDO) linear regulator can supply up to 350mA current while input voltage is 3.3V. It uses an internal P-MOSFET as the pass device. It is suitable for the supply voltage of the timing controller.

The GPM is controlled by frame signals from timing controller to modulate the Gate-On voltage, VGHM, which acts a flicker compensation circuit to reduce the coupling effect between gate lines and pixels. It also can delay the Gate-On voltage while power-on for achieving a corrected power-on sequence for gate driver ICs. Both of power-on delay time and the falling time of the Gate-On voltage are programmable by external capacitor and resistor.

The voltage detector monitors the supply voltage to issue a reset signal while the detected voltage is too low. The detecting level is decided by an external resistor divider and the delay time is programmable by an external capacitor.

The VCOM buffer can drive the LCD VCOM voltage that features high short-circuit current (140mA), fast slew rate (12V/μs), wide bandwidth (12MHz) and rail-to-rail inputs and outputs.

The VGH charge pump controller provides regulated TFT Gate-On voltage. The regulation of the positive charge pump is generated by the internal comparator that senses the output voltage and compares it with an internal reference.

Features

- **2.5V to 5.5V Input Supply Voltage**
- **640kHz/1.2MHz Current-Mode Boost Regulator**
  - **Fast Transient Response to Pulsed Load**
  - **Adjustable Output Voltage (±1%)**
  - **Built-In 16V, 2A, 0.2Ω N-MOSFET**
  - **High Efficiency Up to 90%**
  - **Programmable Soft-Start**
  - **Over-Current Protection**
  - **Output Under-Voltage Protection**
- **Low Dropout Voltage Linear Regulator**
  - **Adjustable Output Voltage : 1.5V to V_{IN} – 0.5V (±1.5%)**
  - **Maximum Output Current : 350mA**
- **On-Chip GPM Controller with Adjustable**
  - **Falling Time and Power-On Delay**
  - **Flicker Compensator**
  - **Power-On Sequence Control**
- **Low Voltage Detector**
  - **Programmable Detecting Voltage (±2%) and Delay Time**
- **Unity-Gain Operation Amplifier for VCOM Buffer**
- **Charge Pump for VGH regulation**
- **Over-Temperature Protection**
- **Thin 24 Lead VQFN Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

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Ordering Information

RT9921 □ □

- Package Type
  - QV : VQFN-24L 4x4 (V-Type)
  - (Exposed Pad-Option 2)
- Lead Plating System
  - P : Pb Free
  - G : Green (Halogen Free and Pb Free)

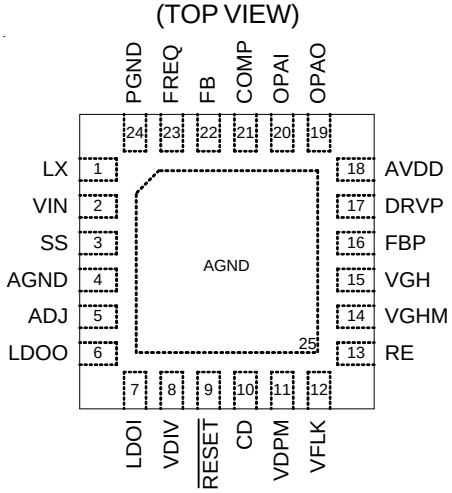
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

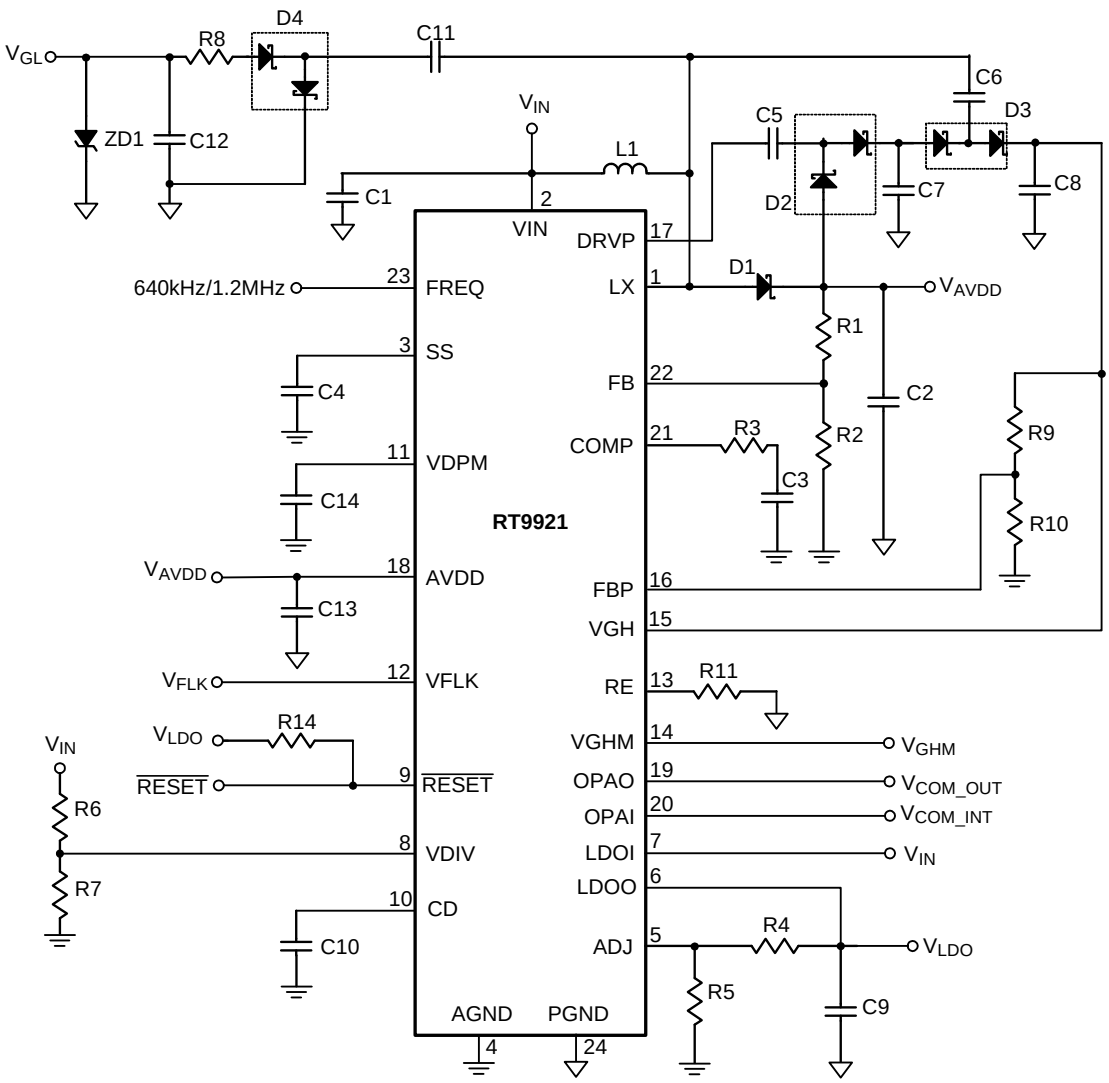
Pin Configurations

(TOP VIEW)



VQFN-24L 4x4

Typical Application Circuit



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Functional Pin Description

Pin No.	Pin Name	Pin Function
1	LX	Switching Pin. Drain of the internal power N-MOSFET for the main step-up regulator.
2	VIN	Supply Input. The supply voltage powers all the control circuits including the boost converter, negative linear-regulator and gate pulse regulator and voltage detector.
3	SS	Soft-Start Control Pin. Connect a soft-start capacitor (C_{SS}) to this pin. The soft-start capacitor is charged with a constant current 4μA.
4, 25 (Exposed Pad)	AGND	Analog Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5	ADJ	Low Dropout Linear Regulator (LDO) Feedback Input. ADJ regulates to 1.24V nominal. Connect ADJ to the center of a resistive voltage divider between the LDO output voltage LDOO and the analog ground (AGND) the LDO output voltage. Place the resistive voltage divider close to the pin.
6	LDOO	Voltage Output of the LDO.
7	LDOI	Voltage Input for the LDO.
8	VDIV	Voltage Detector Divider Input. Connect VDIV to the center of a resistive voltage-divider between the detected voltage input (VDI) and analog ground (AGND).
9	$\overline{\text{RESET}}$	Voltage Detector Output for Reset. Active Low.
10	CD	Pin for external capacitor setting the delay time for voltage detector reset delay time. The delay time t_D = 120k x C_D sec, where C_D is the capacitance value.
11	VDPM	High-Voltage Switch Delay Input. Connect a capacitor from VDPM to GND to set the delay time. A 20μA current source charges C_{DPM}. Power on delay time = 62k x C_{DPM}.
12	VFLK	VFLK is produced by timing controller for charging or discharging VGHM.
13	RE	Switch Input for Discharge VGHM.
14	VGHM	VGHM is the Supply Voltage for the Gate Driver ICs.
15	VGH	Switch Input for Charge VGHM.
16	FBP	Voltage Feedback to Determine Gate-High Regulator's Output Voltage. Connect FBP to the center of a resistive voltage-divider between the output voltage VGH and GND. Place the resistive voltage-divider close to the pin.
17	DRVP	Voltage Driver Output of Gate-High Regulator.
18	AVDD	VDD for Source Driver Power. This also supplies the GPM/OPA block.
19	OPAO	Unity-Gain OPA output pin.
20	OPAI	Unity-Gain OPA input Pin.
21	COMP	Compensation Pin for Error Amplifier. Connect a compensation network to ground.
22	FB	Main Boost Regulator Feedback Input. FB regulates to 1.24V nominal. Connect FB to the center of a resistive voltage-divider between the main output AVDD and the analog ground (AGND) the boost regulator output voltage. Place the resistive voltage divider close to the pin.
23	FREQ	Boost Converter Frequency Select Input. When FREQ is low, the oscillator frequency is set to 640kHz. When FREQ is high, the frequency is 1.2MHz. This input has a 5μA pull-down current.
24	PGND	Power Ground. PGND is the source of the power N-MOSFET. Connect PGND to the analog ground (AGND) at the device's pins.

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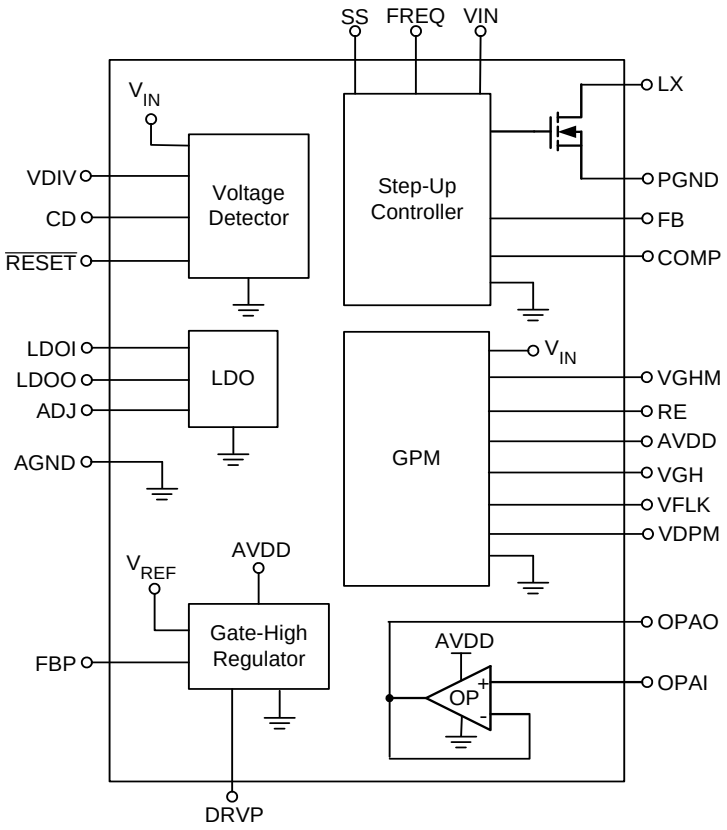
Function Block Diagram



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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- –0.3 to 6.5V
- LX ---------- –0.3 to 16V
- VGH, VGHM, RE ---------- –0.3 to 30V
- AVDD ---------- –0.3 to 16V
- VGH – AVDD, VGHM – AVDD ---------- –0.3 to 20V
- OPAI, OPAO, DRVP ---------- –0.3 to (V_{AVDD} + 0.3V)
- VDPM, VFLK, CD, $\overline{\text{RESET}}$, VDIV, SS, COMP, FB, FBP ---------- –0.3 to (V_{IN} + 0.3V)
- LDOI ---------- –0.3 to 6.5V
- ADJ, LDOO ---------- –0.3 to (LDOI+0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-24L 4x4 ---------- 1.786W
- Package Thermal Resistance (Note 2)
  VQFN-24L 4x4, θ_{JA} ---------- 56°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Maximum Output Voltage Setting, AVDD and VOUT ---------- 15V
- Maximum (VGH – AVDD) ---------- 18V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.3V, V_{OUT} = 8.5V, T_A = 25°C, unless otherwise specification)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
System Supply						
Input Supply Voltage	V_{IN}		2.5	--	5.5	V
V_{IN} Under Voltage Lockout Threshold	V_{UVLO}	V_{IN} Rising	1.8	2	2.2	V
		Hysteresis	--	0.1	--	
V_{IN} Quiescent Current	I_Q	V_{FB} = 1.3V, LX no Switching	--	0.5	1	mA
		V_{FB} = 1.1V, LX Switching	--	2	4	mA
Shutdown Current	I_{SHDN}	V_{IN} = 3.3V	--	1	5	μA
Main Boost Regulator						
Operation Frequency	f_{OSC}	FREQ = 0	--	640	--	kHz
		FREQ = V_{IN}	1	1.2	1.5	MHz
Maximum Duty Cycle			86	90	--	%

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FREQ Input Low Voltage			--	--	0.3 x V_{IN}	V
FREQ Input High Voltage			0.7 x V_{IN}	--	--	V
FREQ Pull-down Current		V_{FREQ} = 1.0V	--	4	--	μA
Feedback Voltage	V_{FB}	No Load	1.228	1.240	1.252	V
FB Input Bias Current		V_{FB} = 1.5V	−40	--	+40	nA
Transconductance of Error Amplifier	Gm	I_{COMP} = 5μA	--	160	--	μA/V
Voltage Gain of Error Amplifier	AV		--	700	--	V/V
Feedback Voltage Line Regulation		V_{IN} = 2.5 to 5.5V	--	−0.1	--	%/V
LX ON-Resistance	$R_{LX(ON)}$		--	200	500	mΩ
LX Current Limit	I_{LIM}		--	2.0	--	A
Current Sense Transresistance			--	0.5	--	A/V
Soft-Start Charge Current	I_{SS}		--	4	--	μA
Thermal Shutdown Temperature	T_{SD}		--	170	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	°C
FB Fault Trip Level (UVP Level)		V_{FB} Falling	--	1.05	--	V
FB Fault Delay (UVP Delay)			--	160	--	ms
Low Dropout Linear Regulator (LDO)						
Input Voltage	V_{LDOI}		2.5	--	5.5	V
Dropout Voltage	V_{DROP}	V_{IN} = 3.3V, I_{OUT} = 350mA	--	450	500	mV
Feedback Voltage	V_{ADJ}		1.224	1.240	1.256	V
Current Limit	I_{LIM}		350	500	--	mA
Quiescent Current	I_{LDO}		--	90	--	μA
Line Regulation		V_{IN} = 2.8 to 5.5V, I_{OUT} = 100mA, V_{LDO} = 2.5V	--	0.1	0.3	%/V
Load Regulation		I_{OUT} = 1mA to 300mA	--	0.2	0.5	%
Gate Pulse Modulator						
VFLK Input High Voltage	V_{IH_FLK}		1.5	--	--	V
VFLK Input Low Voltage	$V_{IL\ FLK}$		--	--	0.6	V
Charge Current of VDPM Pin	I_1		18	20	22	μA
VGH Switch On-Resistance	RP1		--	30	--	Ω
RE Switch On-Resistance	RN2		--	25	--	Ω
Voltage Detector						
Minimum Operating Voltage			1.6	--	--	V
Detecting Voltage Adjustment	VDIV		--	1.1	--	V
Detecting Voltage Accuracy			−2%	--	2%	%
Adjustable Delay Time-Constant	k	t_D = k(Ω) x C_D(F)	--	120k	--	Ω

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Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
VCOM Buffer							
Supply Voltage Range				AVDD	--	15	V
Supply Current	I_{OP}			--	0.8	1.5	mA
Input Offset Voltage	V_{OS}	V_{COM} = AVDD/2, T_A = 25°C		–17	--	17	mV
Input Bias Current	I_{BIAS}			--	1	50	nA
Output Voltage Swing High	V_{OH}	I_{OUT} = 100μA		AVDD –20	AVDD –5	--	mV
		I_{OUT} = 75mA		--	AVDD –1.5	--	V
Output Voltage Swing Low	V_{OL}	I_{OUT} = –100μA		--	5	20	mV
		I_{OUT} = –75mA		--	1.5	--	V
Short-Circuit Current		To AVDD/2	Source	100	180	230	mA
			Sink	100	180	230	mA
-3dB Bandwidth	F_{3dB}			--	12	--	MHz
Gain Bandwidth Product	GBW			--	8	--	MHz
Slew Rate	SR			--	12	--	V/μs
Gate-High Regulator							
Feedback Reference Voltage	V_{FBP}	No Load		1.216	1.240	1.264	V
DRVP Switch On-Resistance	R_{ON_P}	V_{AVDD} = 12V		--	20	--	Ω
	R_{ON_N}	V_{AVDD} = 12V		--	20	--	Ω
Switching Frequency	f_{SW}			0.5 x f_{OSC}			MHz

Note 1. Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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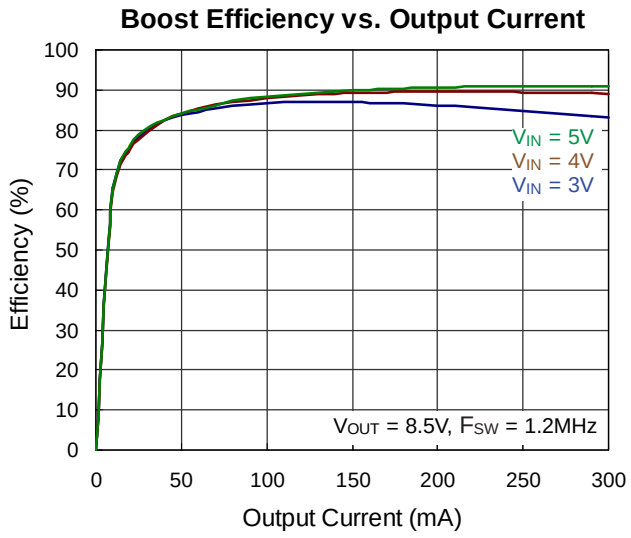
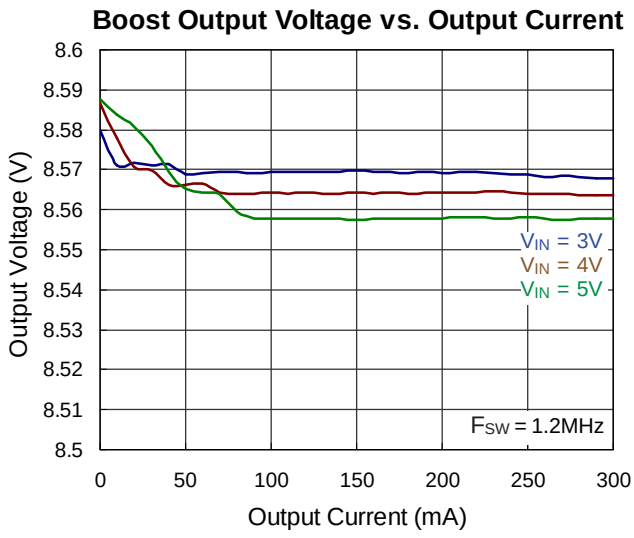
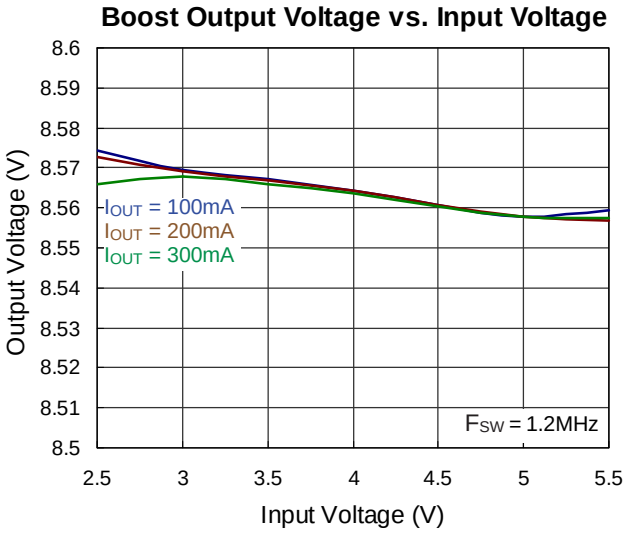
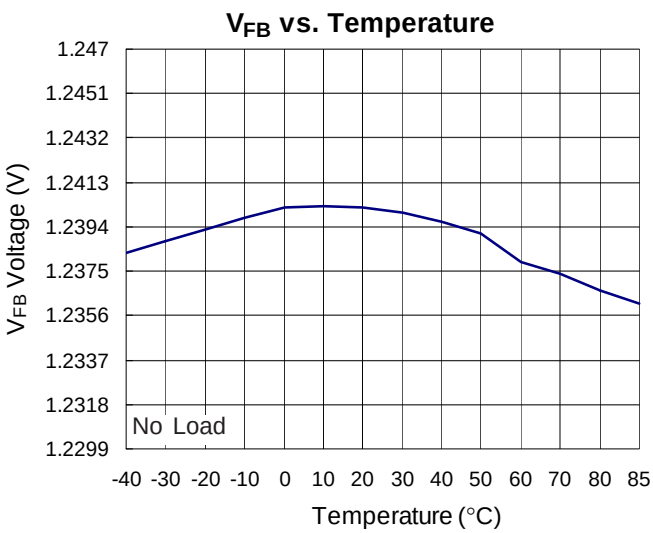
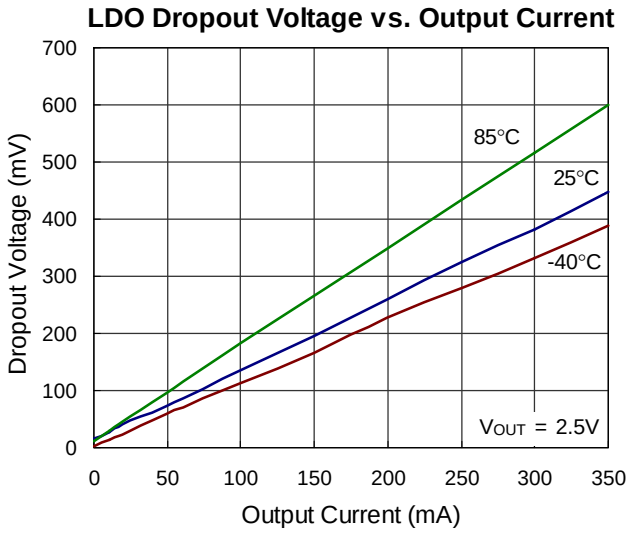
Typical Operating Characteristics

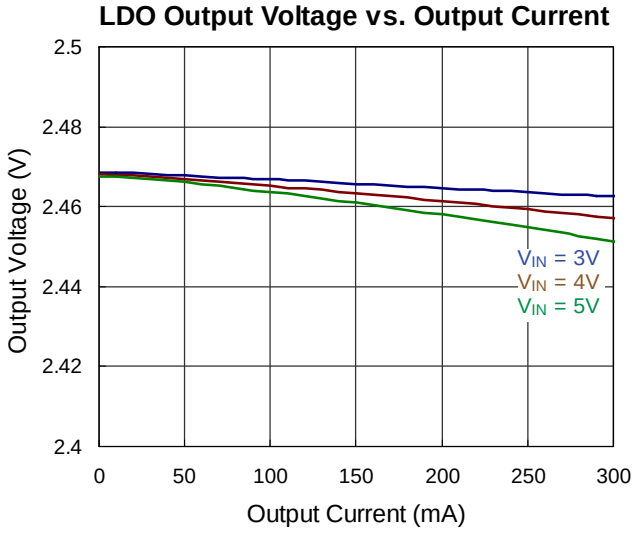












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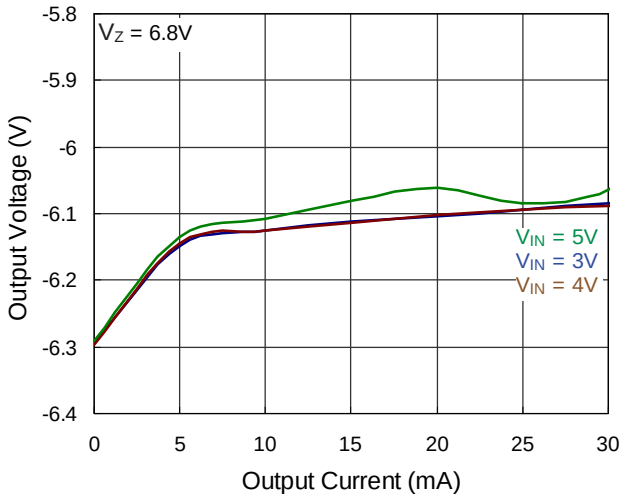
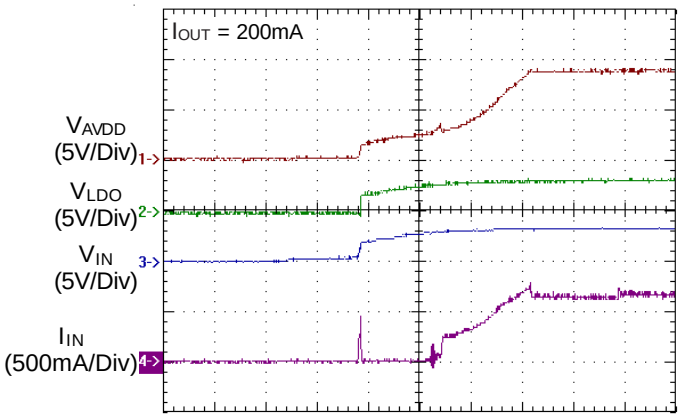
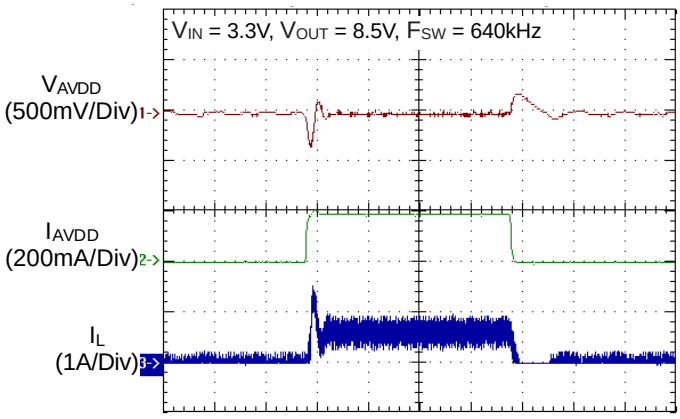
VGL Output Voltage vs. Output Current



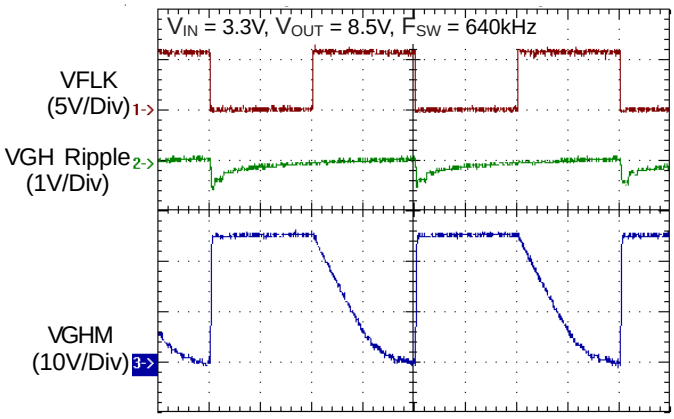
Boost Start Up



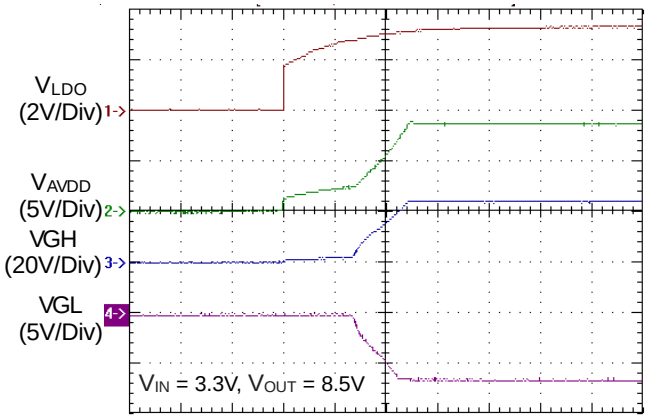
Boost Load Transient Response



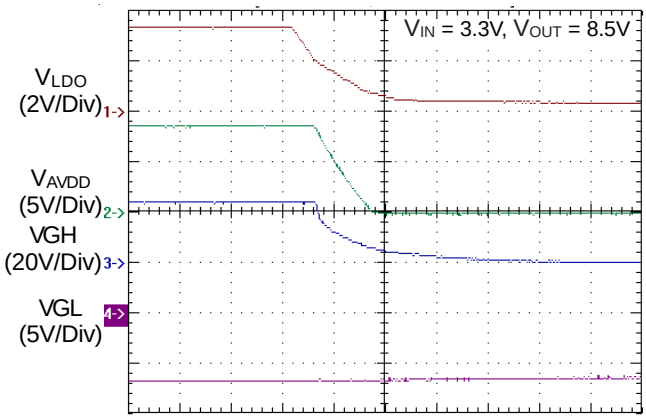
GPM with VFLK



Power On Sequence with VGL



Power Off Sequence with VGL



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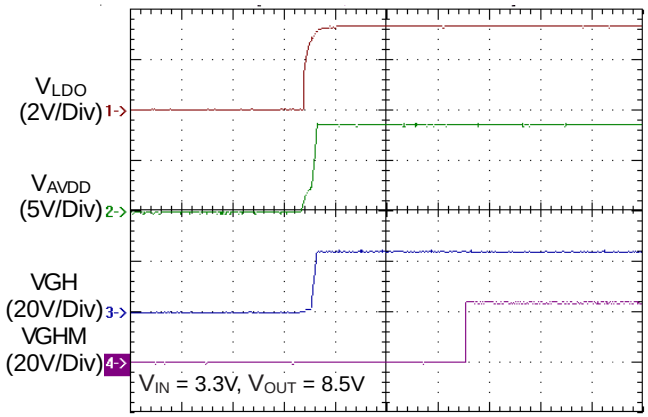
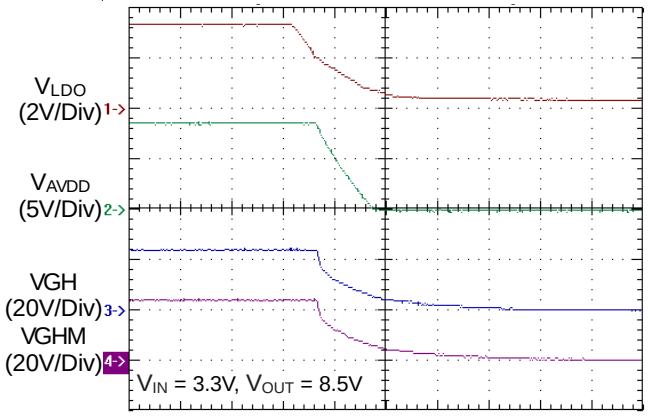
Power On Sequence with VGHM



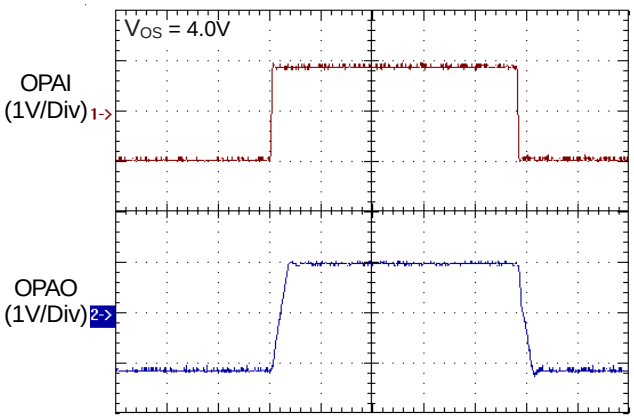
Time (25ms/Div)

Power Off Sequence with VGHM



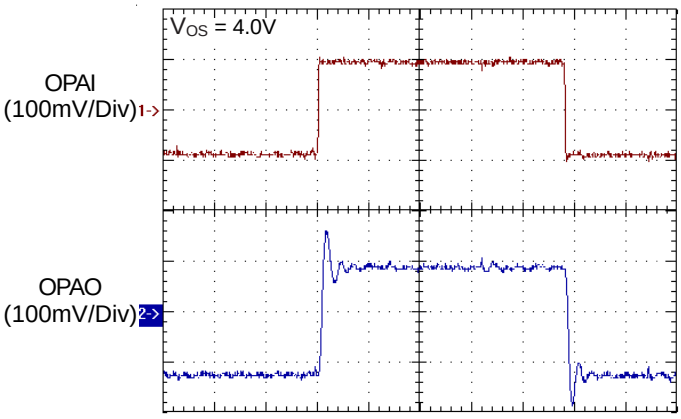
Time (10ms/Div)

OPA Large Signal Step Response



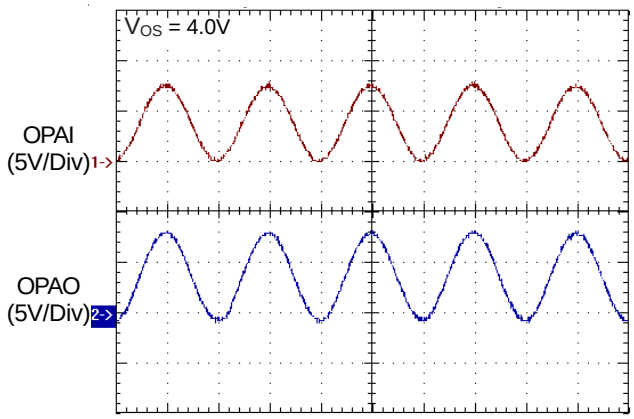
Time (500ns/Div)

OPA Small Signal Step Response



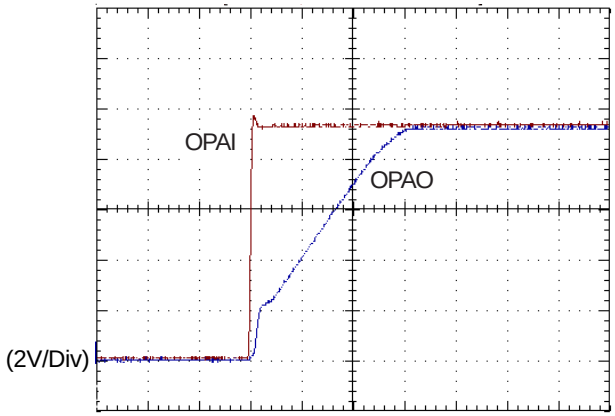
Time (500ns/Div)

OPA Rail to Rail Input/Output



Time (2.5µs/Div)

OPA Slew Rate



Time (250ns/Div)

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Application Information

The RT9921 contains a high performance boost regulator to generate voltage for output voltage, gate-on driver and gate-off driver. It also includes of a high-current rail-to rail operation amplifier, a gate pulse modulator (GPM), a programmable timing control voltage detector, and a low dropout linear regulator. The following content contains the detailed description and the information of the component selection.

Boost Regulator

The boost regulator is a high efficiency current-mode PWM architecture with 640k / 1.2MHz operation frequency. It performs fast transient responses to generate source driver supplies for TFT LCD display. The high operation frequency allows smaller components to minimize the thickness of LCD panel. To regulate the output voltage is to set resistive voltage-divider sensing at FB pin. The error amplifier varies the COMP voltage by sensing the FB pin to regulate the output voltage. For better stability, the slope compensation signal that combined with the current-sense signal will be compared with the COMP voltage to determine the current trip point and duty cycle.

Soft-Start

The RT9921 provides soft-start function to minimize the inrush current. When power on, an internal constant current charges an external capacitor. The rising voltage rate on COMP pin will be limited during the charging period and the inductor peak current will also be limited at the same time. In the meanwhile, the frequency increases slowly at the beginning. When power off, the external capacitor will be discharged for next soft start time.

The soft-start function is implemented by the external capacitor with a 4uA constant current charging to the softstart capacitor. Therefore, the capacitor should be large enough for output voltage regulation. Typical value for softstart capacitor range is 27nF. The available soft start capacitor range is from 10nF to 100nF.

Output Voltage

The regulated output voltage is calculated by the following formula :

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$, where V_{FB} = 1.24V (typ.)

The recommended value for R2 should be up to 100kΩ without some sacrificing. To place the resistor-divider as close as possible to the chip can reduce noise sensitivity.

Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisted of R3, C3 (As Figure 1). Choosing R3 to set high frequency integrator gain for fast transient response and C3 to set the integrator zero to maintain loop stability. For typical application V_{IN} = 3.3V , V_{OUT} = 8.5V , C_{OUT} = 4.7uF x 3 , L = 4.7uH, the recommened value for compensation is as below : R3 = 56kΩ, C3 = 1nF.

Over Current Protection

The RT9921 main boost converter has the function of over-current from protection to limit peak inductor current. It prevents large current damaging the inductor and diode. During the ON-time, once the inductor current exceeds the current limit, the internal LX switch turns off immediately and shortens the duty cycle. Therefore, the output voltage drops if the over-current condition occurs. Actual current limit is always larger than the nominal value because of the internal circuit delay. Current limit is also affected by the input voltage, duty cycle, and inductor value.

Over Temperature Protection

The RT9921 main boost converter has thermal protection function to prevent the excessive power dissipation from overheating. When the junction temperature exceeds 170°C, it will shut down the device. Once the device cools down by approximately 20°C, it will start to operate normally. For continuous operation, do not operate over the maximum junction temperature rating around 150°C.

Under Voltage Protection

If the boost regulator feedback voltage is under 90% of the nominal value, the RT9921 activates an internal timer. If the fault condition continues for 160ms, the PWM will latch off and won't restart until VIN power is cycled. The under-voltage protection is disabled during the soft-start time.

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Inductor Selection

The minimum inductance value, peak current rating and series resistance are factors to be considered in the inductor selecting process. These factors will affect the converter efficiency, maximum output load capability, transient response time and output voltage ripple. Physical size and cost are also important factors to be considered.

The maximum output current, input voltage, output voltage and switching frequency will determine the inductor value. Very high inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and I^2R losses in the inductor. Low inductance values decrease the physical size but increase the current ripple and the peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size and cost.

Choosing an available inductor value from an appropriate inductor family. Calculating the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$ using the following equation.

$$I_{IN(DC,MAX)} = \frac{I_{AVDD(MAX)} \times V_{AVDD}}{V_{IN(MIN)} \times \eta(MIN)}$$

The expected efficiency at that operating point (ηMIN) can be taken from an appropriate curve in the Typical Operating Characteristics. Calculating the ripple current at that operating point and the peak current required for the inductor :

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times (V_{AVDD} - V_{IN(MIN)})}{L \times V_{AVDD} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the LX over current protection (I_{OCP}) should exceed I_{PEAK} and the inductor DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choosing an inductor with less than 0.1Ω series resistance is suggested.

Diode Selection

To achieve high efficiency, Schottky diode is the recommended diode for lower forward drop voltage and faster switching time. The output diode rating should be large enough for maximum output voltage, average power dissipation and the pulsating diode peak current.

Output Capacitor Selection

For lower output voltage ripple, the low-ESR ceramic capacitor is recommended. The output voltage ripple consists of two components: one is the pulsating output ripple current flowing through the ESR, and the other is the capacitive ripple caused by charging and discharging.

$$V_{RIPPLE} = V_{RIPPLE_ESR} + V_{RIPPLE_C}$$

$$\cong I_{PEAK} \times R_{ESR} + \frac{I_{PEAK}}{C_{OUT}} \left(\frac{V_{AVDD} - V_{IN}}{V_{AVDD} \times f} \right)$$

Input Capacitor Selection

For better input bypassing, low-ESR ceramic capacitor is recommended for better performance. A 10μF input capacitor is sufficient and it is flexible to reduce the value for a lower output power requirement.

Gate-High Regulator

The gate-high regulator is to provide the TFT-LCD gate on voltage. The charge pump can provide a programmable output voltage. To regulate the output voltage must set the resistive voltage-divider sensing at FBP pin. The error amplifier varies the difference voltage by sensing FBP pin to regulate the output voltage as the following equation :

$V_{GH} = V_{FBP}$ (1+R9/R10), where V_{FBP} = 1.24V (typ.)

Besides, the Schottky diodes with a current rating should equal to or greater than two times of the average charge-pump input current. Note that the voltage difference between VGH (VGHM) and AVDD should not exceed 18V.

Zener Diode for the Negative Regulator

Bypassing a zener diode(ZD1) after the charge-pump satge can also stablize the negative voltage.

$V_{GL} = -V_Z$

V_D : Zener diode voltage

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GPM

The GPM is controlled by the frame signals from timing controller to modulate the Gate-On voltage, VGHM, which acts a flicker compensation circuit to reduce the coupling effect between gate lines and pixels. It also can delay the Gate-On voltage while power-on for achieving a correct power-on sequence for gate driver ICs. Both of the power-on delay time and the falling time of the Gate-On voltage are programmable by external capacitor and resistor.

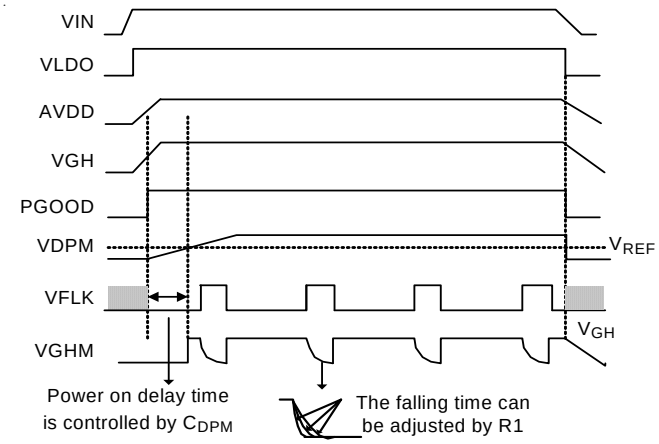

Figure 1

Operational Amplifier

The function of the operational amplifier is to drive the LCD backplane V_{COM}. The operational amplifier features +/- 140mA output short circuit current, 12V/μs slew rate, and 12MHz bandwidth. An internal short-circuit protection circuit is implemented to protect the device from output short circuit. The operational amplifier limits the short circuit current while the output is directly shorted.

LDO

The low-dropout linear regulator (LDO) can supply up to 350mA current while the input voltage is 3.3V. It uses an internal PMOS as the pass device. The output current limitation is 500mA and It is suitable for the supply voltage to be the T-CON ASIC.

Voltage Detector

The voltage detector monitors the VDIV voltage to generate a reset signal while VDIV is lower than the detecting level and the detecting level is decided by an external resistor divider.

$V_{DET} = V_{DIV} (1+R6/R7) = 1.1V \times (1+R6/R7)$

$V_{HYS} = 50mV (1+R6/R7)$

The delay time is programmable by an external capacitor (C10) as equation. For example, setting C10 = 100nF can generate a 12ms delay for reset signal.

$t_D = 120k \times C10$

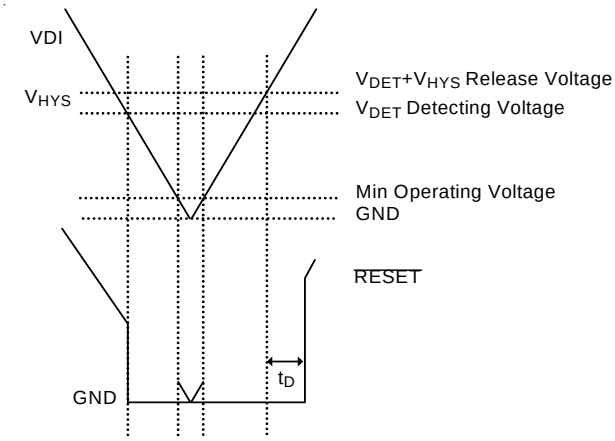

Figure 2

Layout Guideline

For high frequency switching power supplies, the PCB layout is important to get good regulation, high efficiency and stability. The following descriptions are the guidelines for better PCB layout.

- For good regulation, placing the power components as close as possible. The traces should be wide and short enough especially for the high-current output loop.
- The feedback voltage-divider resistors must near the feedback pin. The divider center trace must be shorter and avoid the trace near any switching nodes.
- The compensation circuit should be kept away from the power loops and should be shielded with a ground trace to prevent any noise coupling.
- Minimize the size of the Lx node and keep it wide and shorter. Keep the Lx node away from the FB and analog ground.
- The power ground (PGND) consists of input and output capacitor grounds, the components's ground of charge pump and GPM. The PGND should be wide and short enough to connect to a ground plane.

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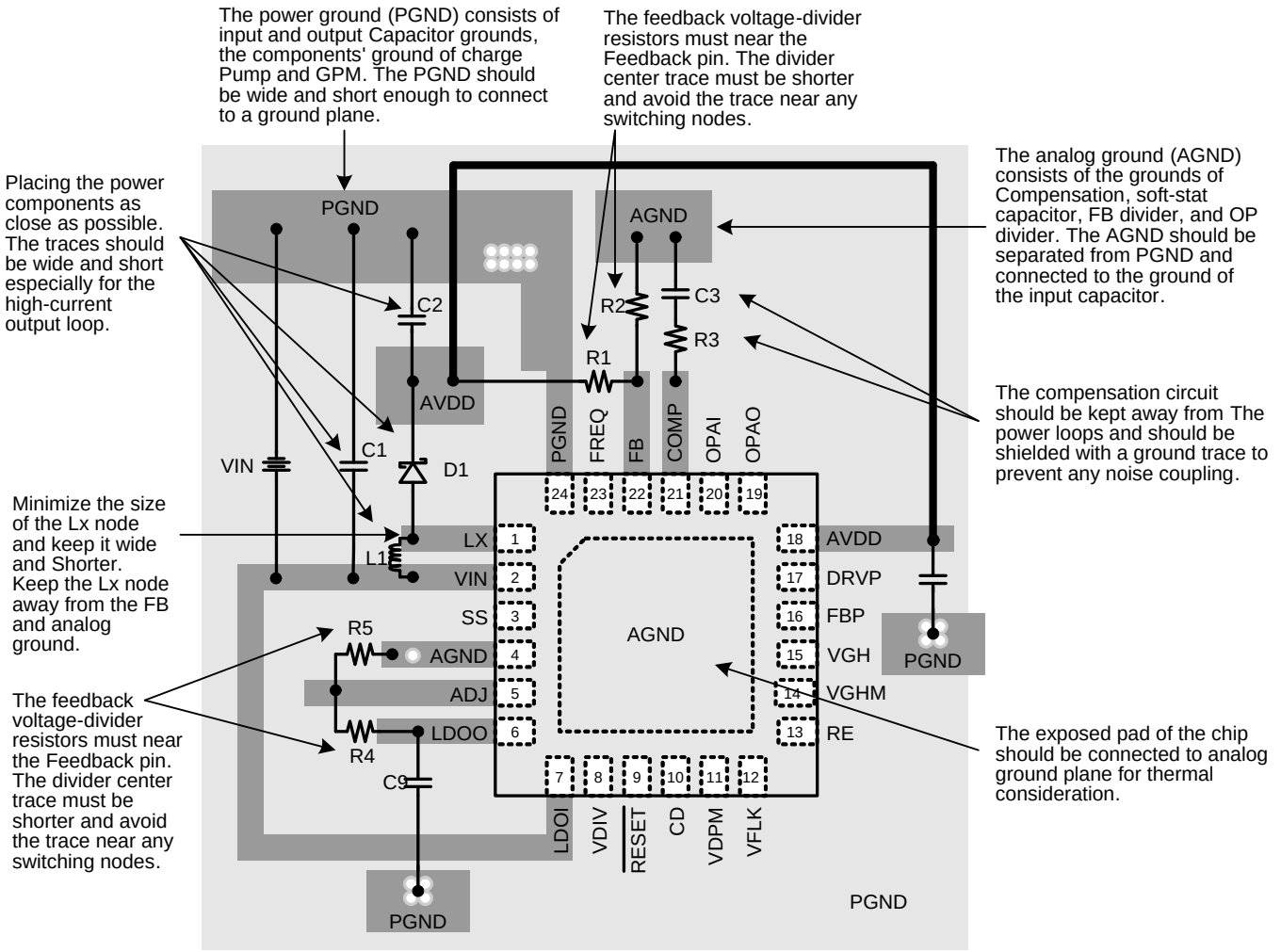
- The analog ground (AGND) consists of the grounds of compensation, soft-stat capacitor, FB divider, and OP divider. The AGND should be separated from PGND and connected to the ground of the input capacitor.
- The exposed pad of the chip should be connected to analog ground plane for thermal consideration.



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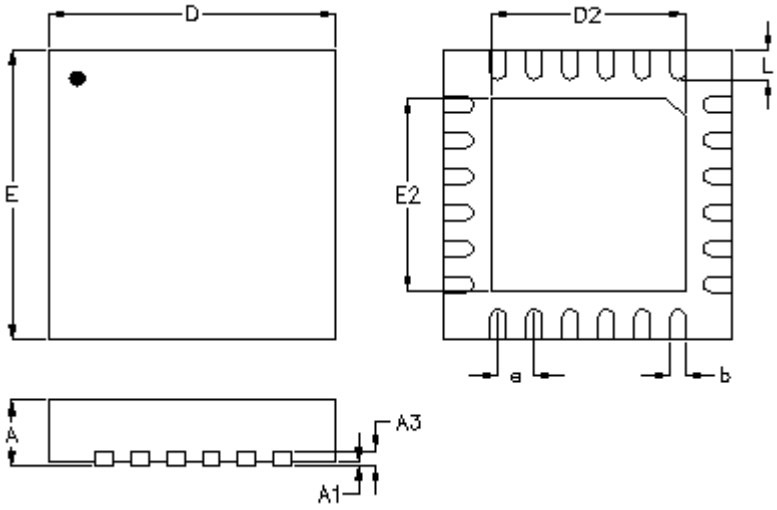
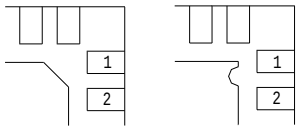
Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min.	Max.	Min.	Max.
A		0.800	1.000	0.031	0.039
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.180	0.300	0.007	0.012
D		3.950	4.050	0.156	0.159
D2	Option 1	2.400	2.500	0.094	0.098
	Option 2	2.650	2.750	0.104	0.108
E		3.950	4.050	0.156	0.159
E2	Option 1	2.400	2.500	0.094	0.098
	Option 2	2.650	2.750	0.104	0.108
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

V-Type 24L QFN 4x4 Package

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