7+2 Channel DC/DC Converters with RTC and I²C Interface

General Description

The RT9999A/B is a highly integrated power management IC that contains 7-CH switching DC/DC converters, one generic LDO, one Keep Alive low quiescent LDO, a switch with reverse leakage prevention from backup battery, and a Real-Time Clock (RTC) that includes a time counter and a 32768Hz oscillator for DSC applications.

The DC/DC converters include one low voltage step-up operated in either asynchronous PFM or synchronous PWM, one current mode synchronous step-up/down (buck boost), two synchronous step-downs, one high voltage synchronous step-up for CCD+ with load disconnect, one asynchronous inverter for CCD–, and one WLED driver operated in either synchronous step-up mode or constant current source mode. All power MOSFETs are integrated and compensation networks are built in.

The RT9999A/B uses I²C interface to set power on timing, output voltage, and WLED current and dimming level. The I²C is also used to access RTC time counters and oscillator fine tuning.

The RT9999A/B provides comprehensive protection functions, including over current, under voltage, over voltage, over temperature, and over load.

The RT9999A/B is available in a WQFN-40L 5x5 package.

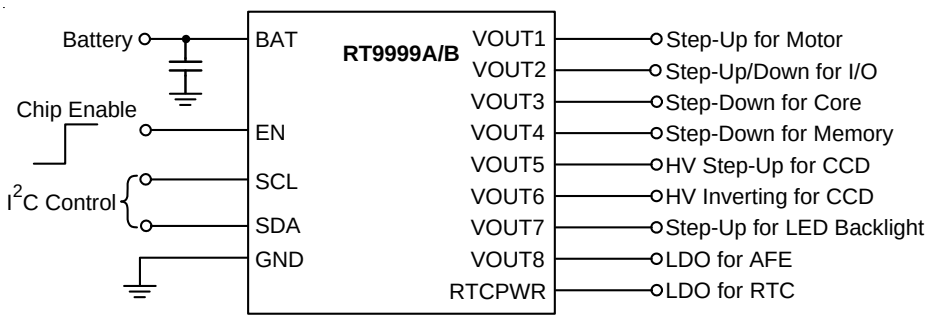
Features

- **CH1 Sync Step-Up in PWM mode or Async Step-Up in Pulse Frequency Mode**
- **CH2 LV Sync Step-Up/Down**
- **CH3/4 LV Sync Step-Down with 100% Maximum Duty Cycle**
- **CH5 HV Sync Step-Up for CCD+ Power with Load Disconnect Function**
- **CH6 HV Async Inverter for CCD- Power**
- **CH7 WLED Driver in Sync Step-Up Mode or Constant Current Source Mode**
  - **Open LED Protection**
  - **32 Dimming Levels**
- **CH8 Generic Low Voltage LDO for Multiple Purpose Power Supply**
- **CH9 Keep Alive Low Quiescent LDO**
- **I²C Interface to Program :**
  - **Enable, Power On Delay Time, Output Regulated Voltage, WLED Dimming Current**
- **RTC Timer and Oscillator**
- **CH3/4 Fixed 2MHz Frequency**
- **CH1/2/5/6/7 Fixed 1MHz Frequency**
- **CH1/3/4/7/8 Support Dynamic Voltage Scaling (DVS)**
- **High Efficiency Up to 95%**
- **RoHS Compliant and Halogen Free**

Applications

- Digital Cameras
- Portable Instruments

Simplified Application Circuit



Ordering Information

RT9999A/B□□

- Package Type
  QW : WQFN-40L 5x5 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- Battery Type
  A : Li-ion
  B : 2AA Alkaline

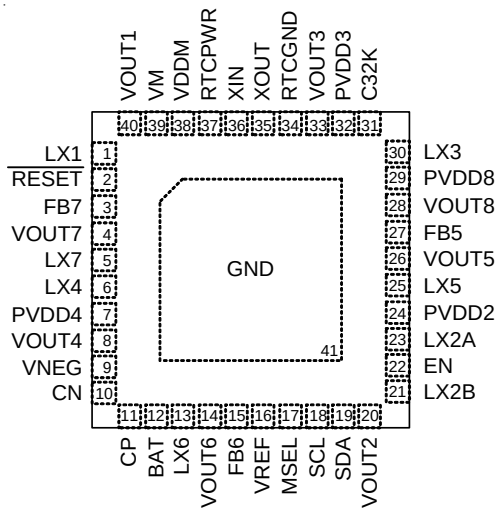
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)



WQFN-40L 5x5

Marking Information

RT9999AGQW

RT9999AGQW : Product Number

YMDNN : Date Code

RT9999BGQW

RT9999BGQW : Product Number

YMDNN : Date Code

Part Status

Part No	Status	Package Type
RT9999AGQW	Lifebuy	WQFN-40L 5x5
RT9999BGQW	Lifebuy	WQFN-40L 5x5

The part status values are defined as below :

Active : Device is in production and is recommended for new designs.

Lifebuy : The device will be discontinued, and a lifetime-buy period is in effect.

NRND : Not recommended for new designs.

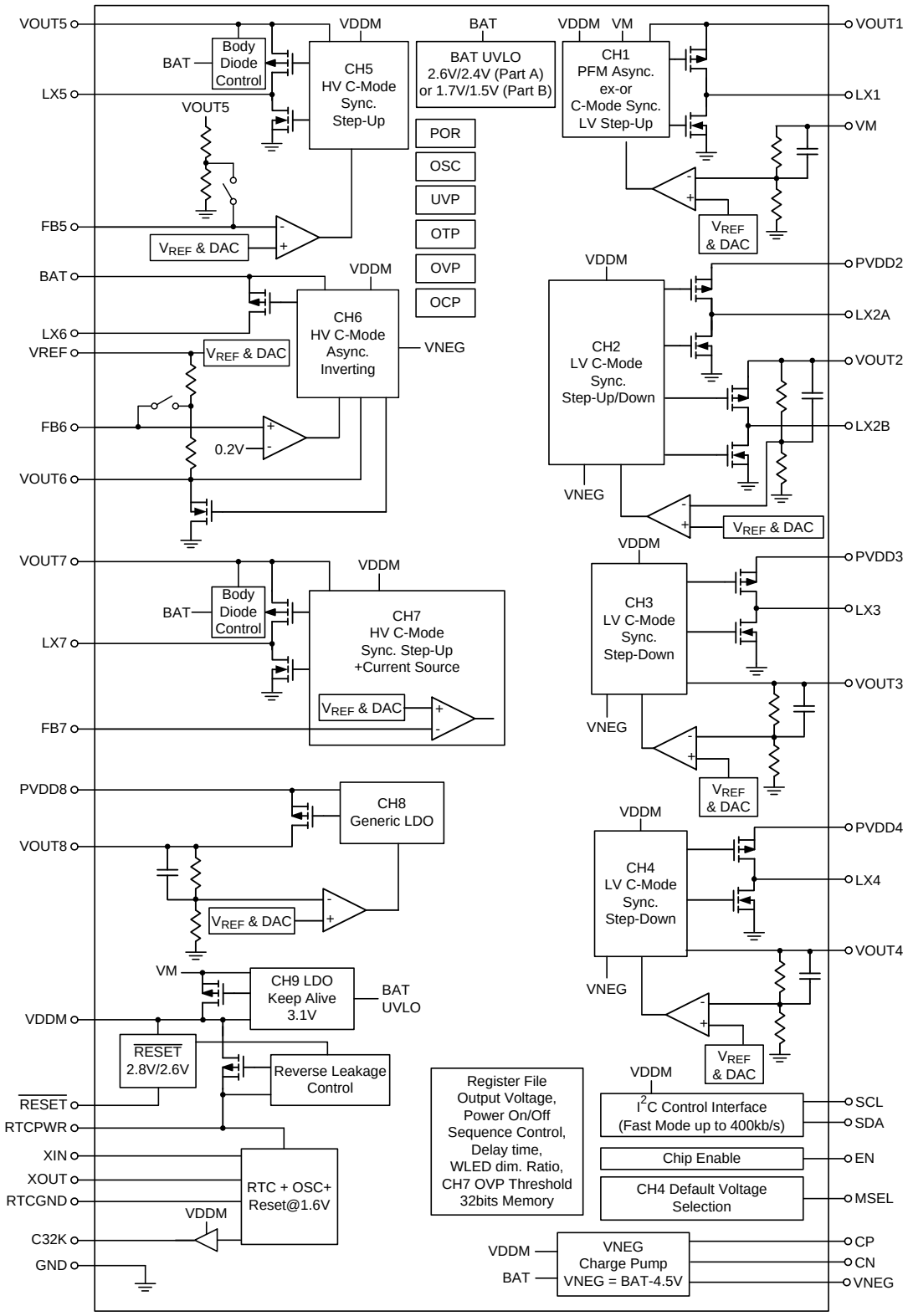
Preview : Device has been announced but is not in production.

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	LX1	Switch Node of CH1. This pin is in high impedance during shutdown.
2	$\overline{\text{RESET}}$	Push Pull Output. This pin asserts the status of monitored VDDM voltage.
3	FB7	Feedback Input for CH7. This pin is in high impedance during shutdown.
4	VOUT7	Power Output of CH7 in Step-Up Mode and Power Input of CH7 in Current Source Mode. When turning off in step-up mode, the RT9999A/B discharges CH7 output capacitors internally. This pin is in high impedance during shutdown. In current source mode, it is recommended to connect VOUT7 to CH1 output node, VOUT1.
5	LX7	Switch Node of CH7 in Step-Up Mode. This pin is in high impedance during shutdown. Connect this pin to the LED anode terminal when CH7 works in current source mode.
6	LX4	Switch Node of CH4. This pin is in high impedance during shutdown.
7	PVDD4	Power Input of CH4. This pin is in high impedance during shutdown.
8	VOUT4	Sense Pin for CH4 Output Voltage. The RT9999A/B can choose whether CH4 would discharge output capacitors internally when turning off. If RT9999A/B is set to discharge CH4 output capacitors internally, the RT9999A/B would not start to turn off CH3 till VOUT4 < 0.1V. This pin is high impedance in shut down.
9	VNEG	Output of Negative Charge Pump to Enhance CH2 (PVDD2 – LX2A), CH3, CH4, CH6 P-MOSFET Driving. The regulated voltage is the higher one between (BAT – 4.5V) and (–BAT). When the negative charge pump is off, VNEG is internally connected to GND. Connect this pin to an external 1μF capacitor.
10	CN	Negative Switch Node of Charge Pump. A fly capacitor is needed between pins CP and CN.
11	CP	Positive Switch Node of Charge Pump.
12	BAT	Power Input of CH6, Battery Power Input, and Sense Pin. It is recommended to place input bypass capacitors as close to the IC as possible. The RT9999A/B senses the voltage of this pin for UVLO and body diode direction control of CH5 and CH7 P-MOSFET switches. This pin is also the input power for the negative charge pump circuit.
13	LX6	Switch Node of CH6. This pin is in high impedance during shutdown.
14	VOUT6	Sense Pin for CH6 Output Voltage. When turning off, the RT9999A/B internally discharges CH6 output capacitors to ground.
15	FB6	Feedback Input of CH6. This pin is in high impedance during shutdown.
16	VREF	Reference Voltage Buffer Output for CH6. This pin is in high impedance during shutdown.
17	MSEL	Selection Input for CH4 Default Output Voltage. This pin is sensed at the moment when $\overline{\text{RESET}}$ goes high to determine the CH4 default output voltage. MSEL = High means CH4 default = 1.8V; MSEL = Low means CH4 default = 1.5V.
18	SCL	Clock Input for I^2C Serial Port.
19	SDA	Data Input and Output for I^2C Serial Port.
20	VOUT2	Power Output for CH2 Output Voltage. When turning off, the RT9999A/B discharges CH2 output capacitors internally until VOUT2 < 0.1V. CH3 can only start turning off after VOUT2 < 0.1V. This pin is in high impedance during shutdown. I^2C interface power level must be equal to CH2 output voltage.
21	LX2B	Switch Node B of CH2. This pin is in high impedance during shutdown.

Pin No.	Pin Name	Pin Function
22	EN	Enable Input. This pin is used to activate/deactivate the RT9999A/B. An internal pull low is included.
23	LX2A	Switch Node A of CH2. This pin is in high impedance during shutdown.
24	PVDD2	Power Input of CH2. It must be connected to the same node as BAT. This pin is in high impedance during shutdown.
25	LX5	Switch Node of CH5. This pin is in high impedance during shutdown.
26	VOUT5	Power Output and Sense Pin of CH5. When turning off, the RT9999A/B discharges CH5 output capacitors internally until VOUT5 < 0.1V. It is recommended to place output capacitors as close to the chip as possible. This pin is in high impedance during shutdown.
27	FB5	Feedback Input of CH5. This pin is in high impedance during shutdown.
28	VOUT8	Regulated Output Node of CH8 Generic LDO. When turning off, the RT9999A/B discharges CH8 output capacitors internally until VOUT8 < 0.1V. This pin is in high impedance during shutdown.
29	PVDD8	Power Input of CH8 Generic LDO. This pin is in high impedance during shutdown.
30	LX3	Switch Node of CH3. This pin is in high impedance during shutdown.
31	C32K	RTC 32768Hz Clock Output. Its rails are VDDM and GND. When $\overline{\text{RESET}}$ goes low, C32K outputs low.
32	PVDD3	Power Input of CH3. It must be connected to the same node as BAT. This pin is in high impedance during shutdown.
33	VOUT3	Sense Pin for CH3 Output Voltage. When turning off, the RT9999A/B discharges CH3 output capacitors internally until VOUT3 < 0.1V. This pin is in high impedance during shutdown.
34	RTCGND	Ground for RTC Timer Counter and Oscillator.
35	XOUT	Crystal Output. This pin's parasitic capacitance should be kept as low as possible. Noise interference should also be avoided.
36	XIN	Crystal Input. This pin's parasitic capacitance should be kept as low as possible. Noise interference should also be avoided.
37	RTCPWR	RTCLDO Power Output Pin. Connect this pin to a backup battery.
38	VDDM	Regulation Voltage Output of CH9. This pin also provides power for all IC control circuit. When VDDM is lower than $\overline{\text{RESET}}$ threshold, the RT9999A/B asserts $\overline{\text{RESET}}$ = 0V. When BAT UVLO occurs, the RT9999A/B discharges CH9 output capacitors internally.
39	VM	Output Sense Pin of CH1 and Power Input of CH9.
40	VOUT1	Power Output and Sense Pin for CH1 Output Voltage. This pin is in high impedance during shutdown. It is recommended to place the output capacitors as close to the IC as possible.
41 (Exposed Pad)	GND	Power Ground and Control Circuit Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation.

Functional Block Diagram



Operation

The RT9999A/B is a highly integrated power management IC that contains 7-CH switching DC/DC converters, one generic LDO, one Keep Alive low quiescent LDO, a switch with reverse leakage prevention from backup battery, and a Real-Time Clock (RTC) that includes a time counter and 32768Hz oscillator.

CH1 : Step-Up DC/DC Converter

CH1 is a step-up converter for motor driver power in DSC system. The converter operates at asynchronous PFM or fixed frequency PWM current mode which can be set by I^2C.

CH2 : Synchronous Step-Up / Down DC/DC Converter

CH2 is a synchronous step-up / down converter for system I/O power. The converter operates at fixed frequency PWM Current Mode.

CH3 : Synchronous Step-Down DC/DC Converter

CH3 is suitable for core power in DSC system. The converter operates in fixed frequency PWM mode with integrated internal MOSFETs, FB resistors and compensation network.

CH4 : Synchronous Step-Down DC/DC Converter

CH4 is suitable for memory power in DSC system. The converter operates in fixed frequency PWM mode with integrated internal MOSFETs, FB resistors and compensation network.

CH5 : Synchronous Step-Up DC/DC Converter

CH5 is a high voltage synchronous step-up converter for CCD positive power. The converter operates at fixed frequency PWM mode, and CCM with integrated internal MOSFETs, compensation network and load disconnect function.

CH6 : INV DC/DC Converter

This converter integrates an internal P-MOSFET with internal compensation and needs an external Schottky diode to provide CCD negative power supply.

CH7 : WLED Driver

CH7 is a WLED driver that can operate in either current source mode or synchronous step-up mode, as determined by I^2C interface.

CH8 : Generic LDO

CH8 is a generic low voltage LDO for multiple purpose power.

CH9 : Keep Alive LDO and RTC Related Function Block

The RT9999A/B provides a 3.1V output LDO for all IC control circuits and real time clock.

VNEG Charge Pump

The Charge pump is to increase the Vgs driving of big PMOSFET in Ch2/3/4/6. When BAT < 3.6V and one of Ch2/3/4/6 turns on, VNEG charge pump will turn on and start to pump. As long as BAT doesn't trigger UVLO, CH1 remains active without EN pin = H. However, when A7.PWM1 = 1, EN pin = H and no VDDM_UVLO, CH1 will switch from PFM mode to PWM mode. Otherwise, it works in PFM mode. CH2 and CH3 are both enabled by the EN pin and have turn-on delay time as defined in I^2C register A5. ENDLY2/3. To enable CH4 and CH8, the bits A7.EN4 and A7.EN8 must be set to "1" and EN pin must be high. When the enable bits are set to "1", CH8 will turn on immediately, and CH4 will turn on after a delay time defined by ENDLY4.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, BAT, VM, PVDD2, PVDD3, PVDD4, PVDD8 ---------- –0.3V to 6V
- LX1, LX2A, LX2B, LX3, LX4, CP ---------- –0.3V to 6V
- LX5, LX7, VOUT5, VOUT7 ---------- –0.3V to 24V
- LX6 ---------- (BAT – 16V) to (BAT + 0.3V)
- VOUT1, VOUT2, VOUT3, VOUT4, VOUT8, RTCPWR, VDDM ---------- –0.3V to 6V
- CN ---------- (BAT – 6V) to (BAT + 0.3V)
- VNEG ---------- (BAT – 6V) to 0.3V
- VOUT6 ---------- (BAT – 16V) to 0.3V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-40L 5x5 ---------- 2.778W
- Package Thermal Resistance (Note 2)
  WQFN-40L 5x5, θ_{JA} ---------- 36°C/W
  WQFN-40L 5x5, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 125°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, BAT ---------- 1.8V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DDM} = 3.1V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VM UVLO Threshold Voltage		VM Rising to turn on CH9	--	BAT –1.1	--	V
VDDM Over Voltage Protection			5.8	6	6.2	V
VDDM Over Voltage Protection Hysteresis			--	–0.25	--	V
BAT UVLO Threshold Voltage		RT9999A, BAT Rising Edge	--	2.6	2.678	V
		RT9999B, BAT Rising Edge	--	1.7	1.8	
BAT UVLO Hysteresis		RT9999A	--	0.2	--	V
		RT9999B	--	0.2	--	
Supply Current						
Shutdown Supply Current into VM (including CH9 Keep Alive LDO and RTC)	$I_{OFF,VM}$	V_{EN} = 0V, CH1 No Switching and V_M = V_{OUT1} = 4.2V, V_{BAT} = 3.3V	--	50	75	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Supply Current into BAT	$I_{OFF,BAT}$	V_{EN} = 0V, CH1 no switching and V_M = V_{OUT1} = 4.2V, V_{BAT} = 3.3V	--	8	15	μA
CH1 (Async Step-Up PFM) Supply Current into VOUT1	I_{Q1}	V_{EN} = 0V, CH1 No Switching and V_M = V_{OUT1} = 4.2V, V_{BAT} = 3.3V	--	--	10	μA
CH2 (Sync Step-Up/Down) + CH3 (Syn Step-Down) Supply Current into VDDM	I_{Q23}	No Switching, V_{EN} = 3.3V	--	--	1200	μA
CH1 (Sync Step-Up PWM) + CH2 (Sync Step-Up/Down) + CH3 (Sync Step-Down) + CH4 (Sync Step-Down) Supply Current into VDDM	I_{Q1234}	No Switching, V_{EN} = 3.3V	--	--	1600	μA
CH2 (Sync Step-Up/Down) + CH3 (Sync Step-Down) + CH4 (Sync Step-Down) Supply Current into VDDM	I_{Q234}	No Switching, V_{EN} =3.3V	--	--	1600	μA
CH5 (sync Step-Up) Supply Current into VDDM	I_{Q5}	No Switching, V_{EN} = 3.3V	--	--	400	μA
CH6 (Inverting) Supply Current into VDDM	I_{Q6}	No Switching, V_{EN} = 3.3V	--	--	400	μA
CH7 (WLED) in Current Source Mode Supply Current into VDDM	I_{Q7cs}	V_{EN} = 3.3V	--	--	200	μA
CH7 (WLED) in Sync Step-Up Mode Supply Current into VDDM	I_{Q7bo}	No Switching, V_{EN} = 3.3V	--	--	400	μA
CH8 (LDO) Supply Current into VDDM	I_{Q8}	No Load, V_{EN} = 3.3V	--	--	100	μA
Oscillator						
CH3, 4 Operation Frequency	f_{OSC}		1800	2000	2200	kHz
CH1, 2, 5, 6, 7 Operation Frequency		CH1 in PWM mode	900	1000	1100	kHz
CH1 Maximum Duty Cycle (Step-Up)			91	93	97	%
CH2 Maximum Duty Cycle at LX2B		V_{BAT} = 4.2V	--	55	--	%
CH2 Maximum Duty Cycle at LX2A			--	--	100	%
CH3 Maximum Duty Cycle (Step-Down)			--	--	100	%
CH4 Maximum Duty Cycle (Step-Down)			--	--	100	%
CH5 Maximum Duty Cycle (Step-Up)			91	93	97	%
CH6 Maximum Duty Cycle (Inverting)			91	93	97	%
CH7 Maximum Duty Cycle (WLED)		Step-up mode	91	93	97	%
Feedback and Output Regulation Voltage						
VOUT2, 3, 5, 6 Accuracy		VOUTx typical values are listed next.	–1.5	--	1.5	%
VOUT8 Accuracy		A3.VOUT8 = 0 to 3	–1.5	--	1.5	%
		A3.VOUT8 = 4 to 7	–2	--	2	
VOUT4 Accuracy		A1.VOUT4 = 0 to 3 (near 1.8V)	–1.5	--	1.5	%
		A1.VOUT4 = 4 to 7 (near 1.5V)	–2	--	2	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VOUT1 Accuracy			A0.VOUT1 = 0 to 7	–1.5	--	1.5	%
			A0.VOUT1 = 8 to 15	–2	--	2	
Feedback Regulation Voltage @ FB6				170	200	230	mV
(VREF – VFB6) Regulation Voltage			A2.VOUT6 = 0x7 (for CH6 external feedback)	1.222	1.24	1.258	V
VREF Load Regulation			VREF = –200μA	--	--	–10	mV
Feedback Regulation Voltage @ FB5			A2.VOUT5 = 0x7 (for CH5 external feedback)	1.232	1.25	1.268	V
Feedback Regulation Voltage @ FB7				0.237	0.25	0.263	V
VDDM Voltage (CH9 Output Regulation)				3.01	3.1	3.19	V
Power Switch R_{ON} and Current Limit							
CH1 On Resistance of MOSFET		$R_{DS(ON)}$	P-MOSFET, V_{OUT1} = 3.3V	--	200	250	mΩ
			N-MOSFET, V_{OUT1} = 3.3V	--	150	200	
CH1 Current Limitation (Step-Up)				2.5	3	3.5	A
CH2 On Resistance of MOSFET		$R_{DS(ON)}$	P-MOSFET(PVDD2 – LX2A), V_{PVDD2} = V_{OUT2} = 3.3V	--	150	200	mΩ
			N-MOSFET(LX2A – GND), V_{PVDD2} = V_{OUT2} = 3.3V	--	250	350	
CH2 On Resistance of MOSFET		$R_{DS(ON)}$	P-MOSFET (LX2B – VOUT2), V_{PVDD2} = V_{OUT2} = 3.3V	--	200	280	mΩ
			N-MOSFET (LX2B – GND), V_{PVDD2} = V_{OUT2} = 3.3V	--	150	200	
CH2 Current Limitation			Both P-MOSFET (PVDD2 – LX2A) and N-MOSFET (LX2B – GND)	1.5	2	2.5	A
CH3 On Resistance of MOSFET		$R_{DS(ON)}$	P-MOSFET, V_{PVDD3} = 3.3V	--	200	300	mΩ
			N-MOSFET, V_{PVDD3} = 3.3V	--	150	220	
CH3 Current Limitation (Step-Down)				1.5	2	2.5	A
CH4 On Resistance of MOSFET		$R_{DS(ON)}$	P-MOSFET, V_{PVDD4} = 3.3V		350	400	mΩ
			N-MOSFET, V_{PVDD4} = 3.3V		350	400	
CH4 Current Limitation (Step-Down)				1	1.5	2	A
CH5 On Resistance of MOSFET			P-MOSFET, V_{OUT5} = 3.3V	--	1.2	1.5	Ω
			N-MOSFET, V_{DDM} = 3.1V	--	0.6	0.8	
CH5 Current Limitation			N-MOSFET	0.9	1.2	1.5	A
CH6 On Resistance of MOSFET			P-MOSFET, V_{BAT} = 3.3V	--	0.6	0.8	Ω
CH6 Current Limitation			P-MOSFET, V_{BAT} = 3.3V	1	1.5	2	A
CH7 On Resistance of MOSFET			N-MOSFET	--	0.9	1.1	Ω
			P-MOSFET	--	2.0	3.0	
CH7 Current Limitation			N-MOSFET	0.6	0.8	1	A
Control							
MSEL Input Threshold Voltage	Logic-High			1.3	--	--	V
	Logic-Low			--	--	0.4	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
MSEL Sink Current			EN = High	--	1	3	μA
			EN = Low	--	--	0.5	
EN Input Threshold Voltage	Logic-High			1.3	--	--	V
	Logic-Low			--	--	0.4	
EN Sink Current				--	1	3	μA
Thermal Protection							
Thermal Shutdown		T_{SD}		125	160	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	20	--	°C
VNEG Charge Pump							
Charge Pump Low Threshold to Start		NV_{ST}	Monitor BAT Falling	3.4	3.6	3.8	V
Charge Pump Hysteresis Gap to Stop (BAT−VNEG) Clamp Level		ΔNV_{ST}		0.1	0.2	0.3	V
				4.1	4.5	4.9	
CH8 LDO							
Supply Voltage of CH8		V_{PVDD8}		2.7	--	5.5	V
PSRR+ of CH8			1kHz, I_{OUT} = 10mA, V_{PVDD8} = 3.6V, V_{OUT8} = 3.4V	--	−40	--	dB
CH8 Dropout Voltage			V_{OUT8} = 3.4V, I_{OUT} = 100mA	--	40	60	mV
CH8 Current Limitation			V_{OUT8} = 3.4V	220	300	380	mA
CH9 Keep Alive LDO							
Supply Voltage of CH9 at VM Pin				2.4	--	5.5	V
PSRR+ of CH9			1kHz, I_{OUT} = 1mA, V_M = 3.6V, V_{DDM} = 3.1V	--	−40	--	dB
CH9 Dropout Voltage			V_{DDM} = 3.1V, I_{OUT} = 20mA	--	170	200	mV
Current Limit of CH9			V_{DDM} = 3.1V	50	100	--	mA
$\overline{\text{RESET}}$ Hysteresis Low			$\overline{\text{RESET}}$ Falling	2.55	2.6	--	V
$\overline{\text{RESET}}$ Hysteresis High			$\overline{\text{RESET}}$ Rising	--	2.8	2.86	V
$\overline{\text{RESET}}$ Rising Delay Time				--	--	0.5	s
CH9 Quiescent Current			Excluding RTC Quiescent Current	--	4	8	μA
RTC							
RTC Operation Voltage				1.6	--	3.3	V
RTC Quiescent Current			Including RTC_UVLO, RTC_OSC, and Time Counter	--	--	2	μA
RTC Off Quiescent Current			When RTC RESET (UVLO) occurred	--	--	0.2	μA
RTC Clock				--	32.768	--	kHz
RTC Clock Accuracy			V_{RTCPWR} = 1.6V to 3.3V	−10	--	10	ppm
RTC Clock Output High			C32K pin source out 0.1mA	V_{DDM} − 0.3	--	--	V
RTC Clock Output Low			C32K pin sink 0.1mA	--	--	0.3	V
RTC RESET (UVLO)		V_{RTC_F}	RTCPWR Falling	1.5	1.6	1.7	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
RTC RESET POR		V_{RTC_R}	RTCPWR Rising	V_{RTC_F} + 20m	1.9	2	V
RTC Osc Startup Time				--	--	1	s
Switch On Resistance from VDDM to RTCPWR			P-MOSFET, V_{DDM} = 3.1V	--	30	--	Ω
Under Voltage and Over Voltage Protection							
CH1 OVP Threshold @ VOUT1				5.8	6	6.2	V
CH2 OVP Threshold @ VOUT2				5.8	6	6.2	V
CH5 OVP Threshold @ VOUT5				20	21	22	V
CH6 OVP Threshold @ VOUT6				--	–13	--	V
CH7 OVP Threshold Accuracy @ VOUT7			Target voltage is the one chosen in A4.OVP7	Target –1	Target	Target +1	V
CH1 UVP Threshold @ VOUT1			For PWM Mode	1.95	2.25	2.55	V
CH2 UVP Threshold @ VOUT2				1.4	1.6	1.8	V
CH3 UVP Threshold @ VOUT3				0.525	0.6	0.675	V
CH4 UVP Threshold @ VOUT4				0.7	0.8	0.9	V
CH5 UVP Threshold @ FB5				0.5	0.6	0.7	V
CH6 UVP Threshold @ FB6				0.4	0.5	0.6	V
CH8 UVP Threshold @ VOUT8			Target voltage is the one chosen in A3.VOUT8	--	0.5 x Target	--	V
CH1 Over Load P Threshold (OLP) @ VOUT1			Target voltage is the one chosen in A0.VOUT1	--	Target – 0.6	--	V
CH2 OLP Threshold @ VOUT2			Target voltage is the one chosen in A0.VOUT2	--	Target – 0.4	--	V
CH3 OLP Threshold @ VOUT3			Target voltage is the one chosen in A1.VOUT3	--	Target – 0.15	--	V
CH4 OLP Threshold @ VOUT4			Target voltage is the one chosen in A1.VOUT4	--	Target – 0.2	--	V
CH5 OLP Threshold @ VOUT5			Target voltage is the one chosen in A2.VOUT5	--	Target – 1.8	--	V
CH6 OLP Threshold @ FB6			A2.VOUT6 = 0x7	0.3	0.35	0.4	V
Protection Delay Time			For OCP and OLP, except OCP of CH2	--	100	--	ms
I^2C Interface							
SDA, SCLK Input Threshold Voltage	Logic-High		V_{OUT2} = 3.3V	0.7 x V_{OUT2}	--	--	V
	Logic-Low		V_{OUT2} = 3.3V	--	--	0.3 x V_{OUT2}	
SCLK Clock Rate		f_{SCL}	V_{OUT2} = 3.3V	--	--	400	kHz
Hold Time for Repeated START Condition (After this period, the first clock pulse is generated)		$t_{HD;STA}$	V_{OUT2} = 3.3V	0.6	--	--	µs
LOW Period of SCL Clock		t_{LOW}	V_{OUT2} = 3.3V	1.3	--	--	µs
HIGH Period of SCL Clock		t_{HIGH}	V_{OUT2} = 3.3V	0.6	--	--	µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Set-up Time for Repeated START Condition	$t_{SU;STA}$	V_{OUT2} = 3.3V	0.6	--	--	μs
Data Hold Time	$t_{HD;DAT}$	V_{OUT2} = 3.3V	0	--	0.9	μs
Data Set-up Time	$t_{SU;DAT}$	V_{OUT2} = 3.3V	100	--	--	ns
Set-up Time for STOP Condition	$t_{SU;STO}$	V_{OUT2} = 3.3V	0.6	--	--	μs
Bus Free Time between a STOP and START Condition	t_{BUF}	V_{OUT2} = 3.3V	1.3	--	--	μs
Rise Time of Both SDA and SCL Signals	t_R	V_{OUT2} = 3.3V	20	--	300	ns
Fall Time of Both SDA and SCL Signals	t_F	V_{OUT2} = 3.3V	20	--	300	ns
SDA and SCL Output Low Sink Current	I_{OL}	SDA or SCL voltage = 0.4V, V_{OUT2} = 3.3V	2	--	--	mA
Output Voltage Ramp Rate						
VOUT1 Ramp Rate		V_{OUT1} = 3.6V to 5.3V	--	1.24	--	V/ms
VOUT2 Ramp Rate		V_{OUT2} = 0V to 3.25V	--	0.82	--	V/ms
VOUT3 Ramp Rate		V_{OUT3} = 0V to 1.1V	--	0.33	--	V/ms
VOUT4 Ramp Rate		V_{OUT4} = 0V to 1.8V	--	0.44	--	V/ms
VOUT5 Ramp Rate		V_{OUT5} = 0V to 13V, A2.VOUT5 [2:0] is not 0x7.	--	1.6	--	V/ms
FB5 Reference Ramp Rate (CH5 external feedback)		V_{FB5} = 0V to 1.25V, A2.VOUT5 [2:0] = 0x7	--	0.133	--	V/ms
VOUT6 Ramp Rate		V_{OUT6} = 0V to –7.5V, A2.VOUT6 [2:0] is not 0x7.	--	0.8	--	V/ms
VREF Ramp Rate (CH6 external feedback)		V_{REF} = 0V to 1.24V, A2.VOUT6 [2:0] = 0x7	--	0.125	--	V/ms
VOUT8 Ramp Rate		V_{OUT8} = 0V to 3.4V	--	0.84	--	V/ms
Ramp Rate Accuracy		(For all ramp rates listed above)	–40	--	40	%
Enabling Delay Time						
Delay Time Step Resolution		For ENDLY2, 3, 4 at A5, A6	--	2	--	ms
Off Discharge						
VOUT2, 3, 4, 5, 7 Discharge Equivalent Resistance		V_{OUTx} = 1V	50	--	--	Ω
VOUT6 Discharge Equivalent Resistance		V_{OUT6} = –1V	100	--	--	Ω
VOUT8 Discharge Equivalent Resistance		V_{OUT8} = 1V	200	--	--	Ω
VDDM Discharge Equivalent Resistance		V_M = 4.2V and V_{DDM} = 1V	200	--	--	Ω
CH2 Discharge Finish Threshold for CH3 Starting to Turn Off			0.05	0.1	0.15	V
CH4 Discharge Finish Threshold for CH3 Starting to Turn Off		CH3 will wait for CH4 to discharge only when A1.DIS4 = 1	0.05	0.1	0.15	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CH1 Asynchronous PFM						
N-MOSFET On-Time		V_M = 3.6V	--	0.5	--	μs
Minimum Off-Time		V_M = 3.6V	--	0.5	--	μs
N-MOSFET Current Limit		V_M = 3.6V	--	0.8	--	A
N-MOSFET On Resistance		V_M = 3.6V, (the same as PWM mode)	--	150	200	mΩ
VOUT1 Regulation Voltage		V_M = 3.6V	3.5	3.6	3.7	V

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

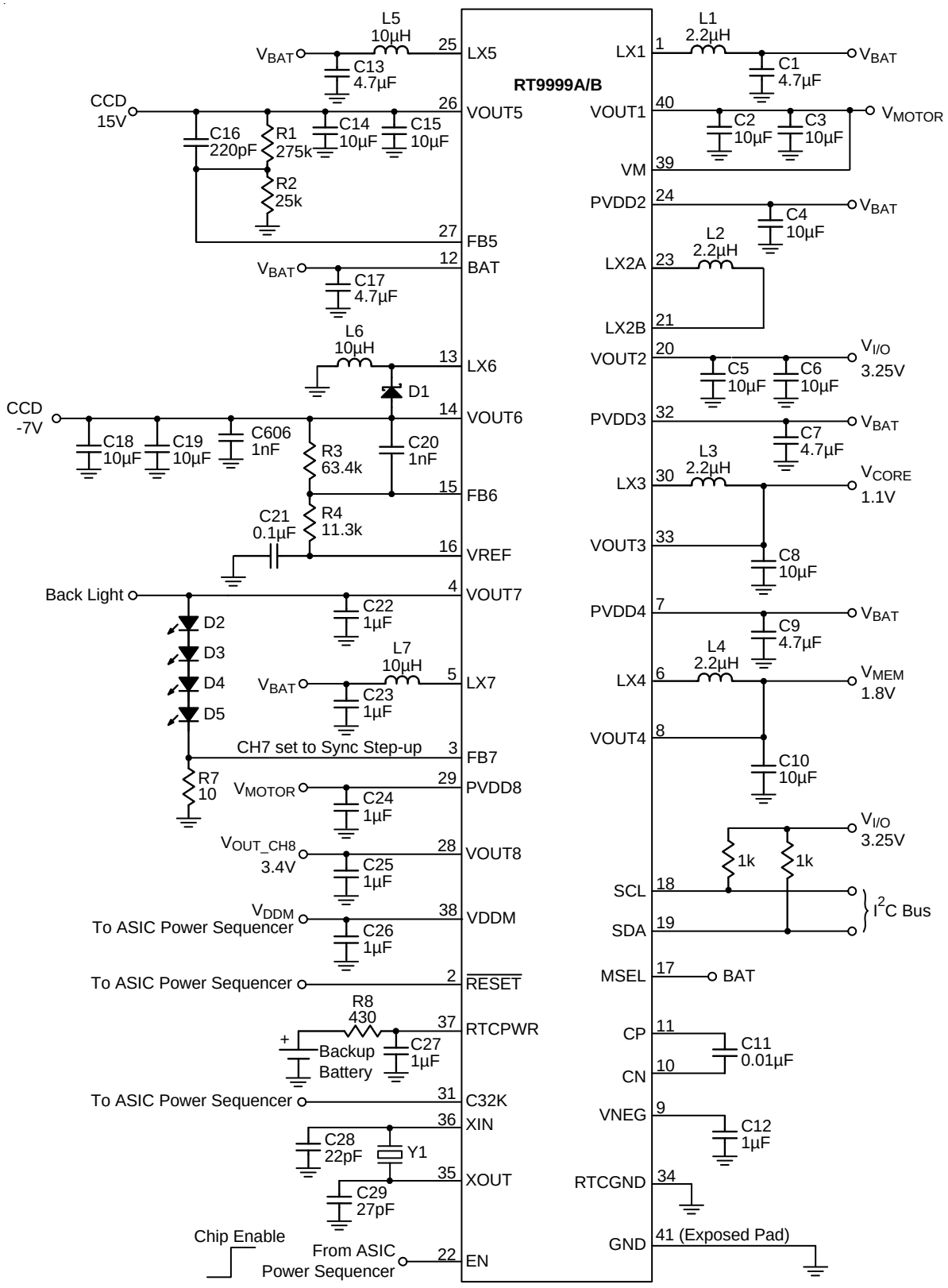


Figure 1. Application for V_{MEM} = 1.8V

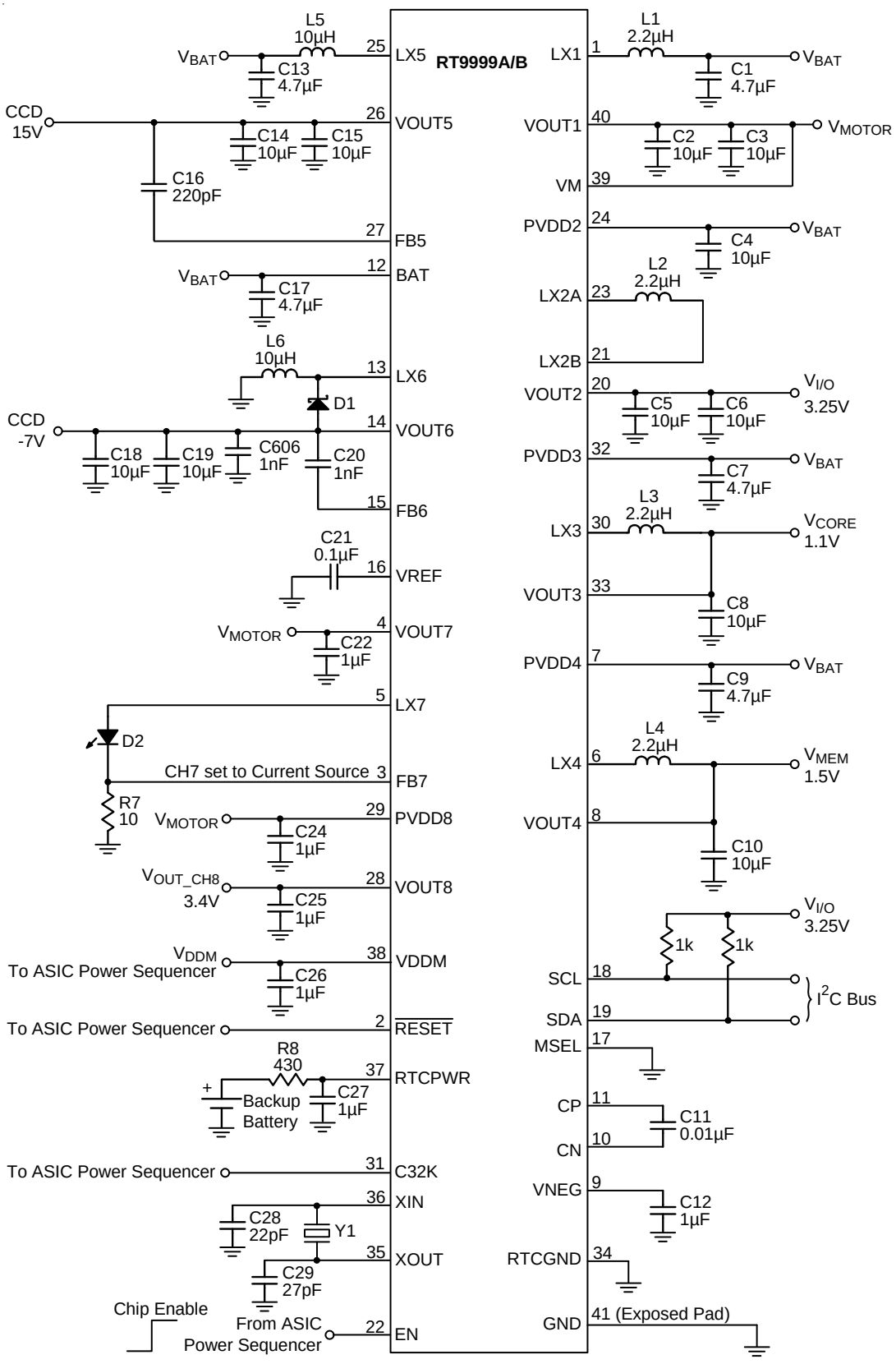
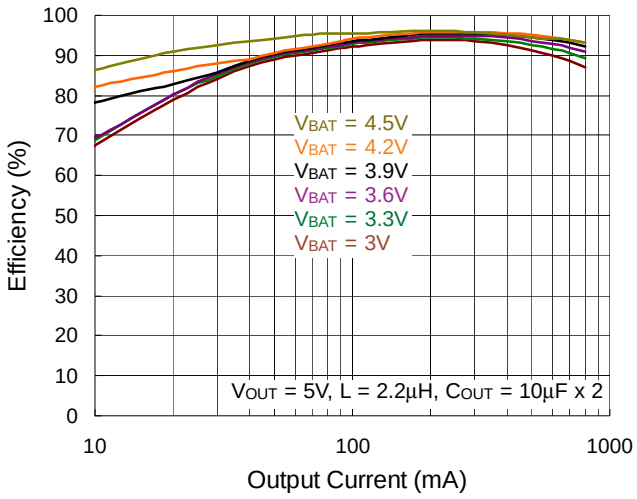


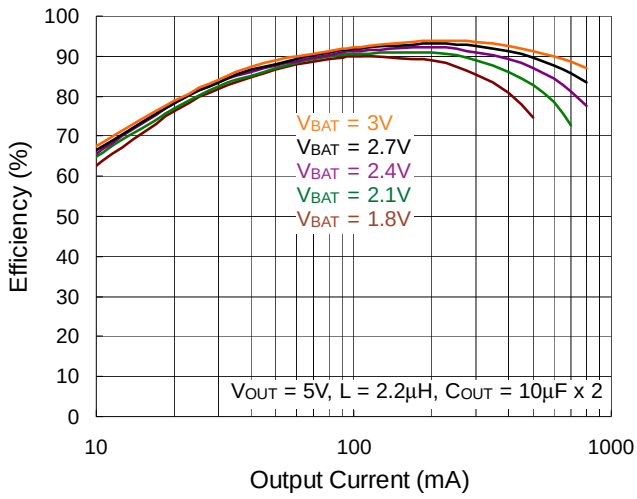
Figure 2. Application for V_{MEM} = 1.5V

Typical Operating Characteristics

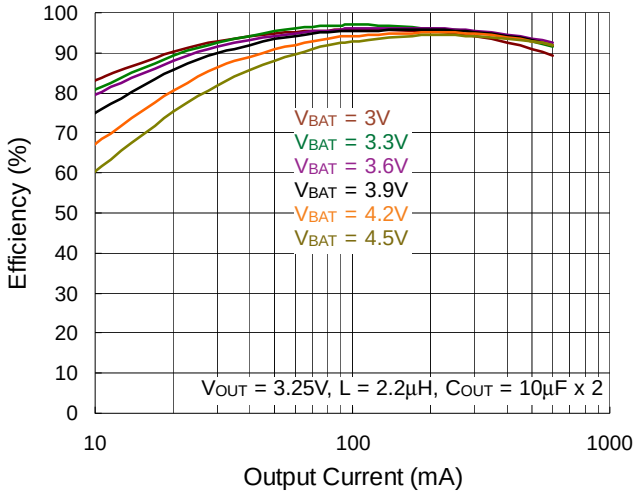
CH1 Boost Efficiency vs. Output Current



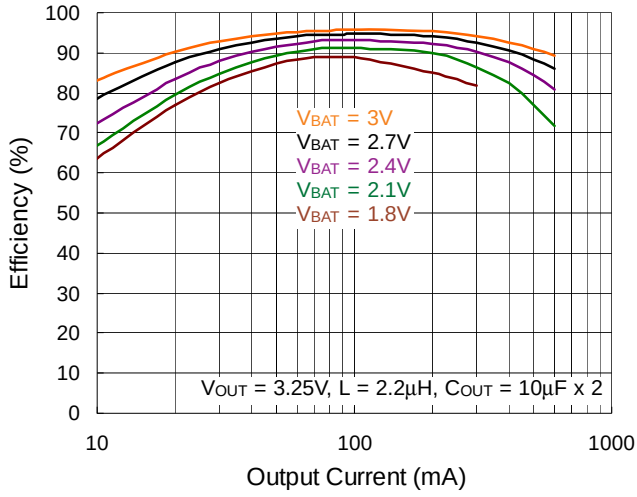
CH1 Boost Efficiency vs. Output Current



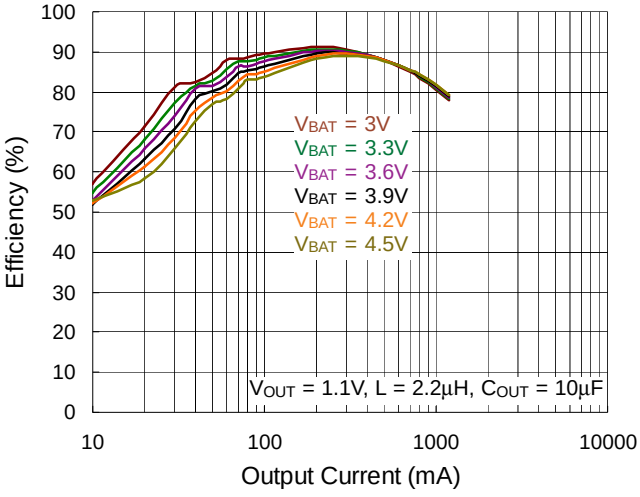
CH2 Buck-Boost Efficiency vs. Output Current



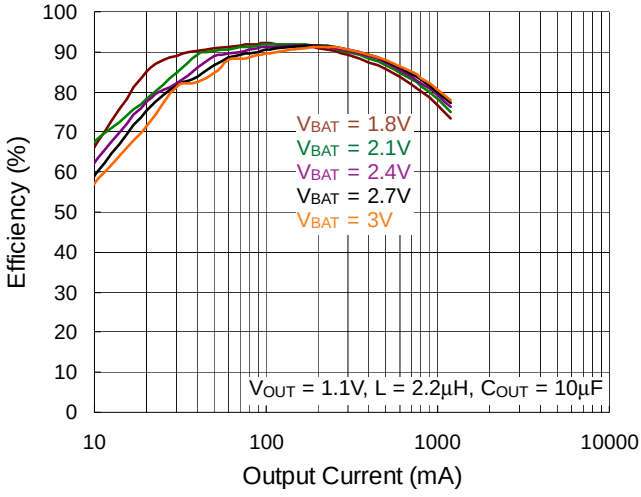
CH2 Buck-Boost Efficiency vs. Output Current



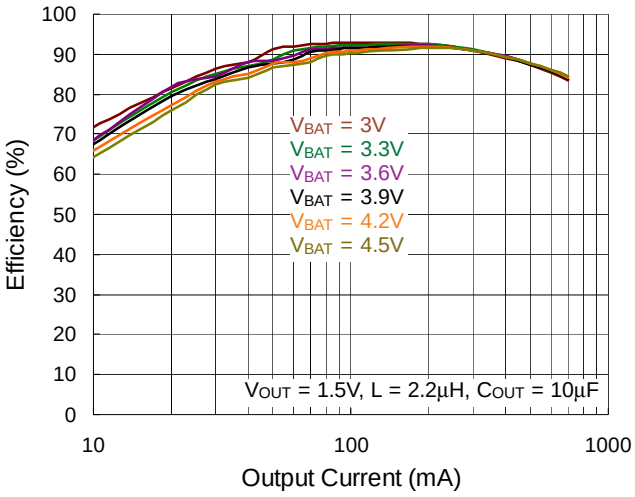
CH3 Buck Efficiency vs. Output Current



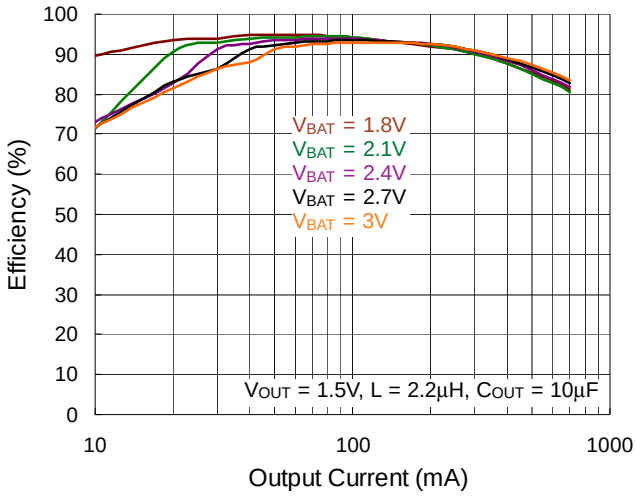
CH3 Buck Efficiency vs. Output Current



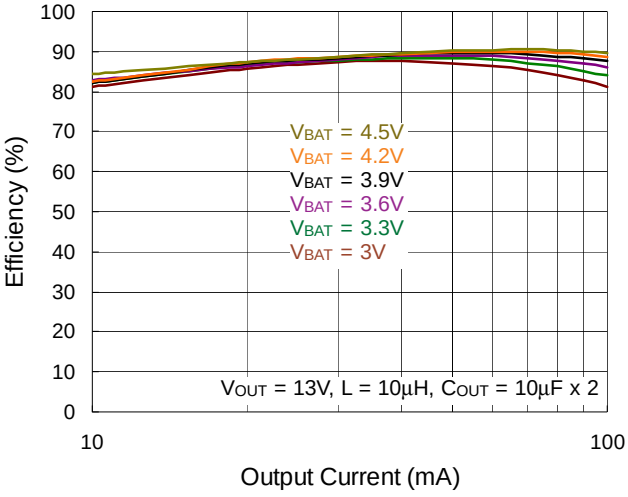
CH4 Buck Efficiency vs. Output Current



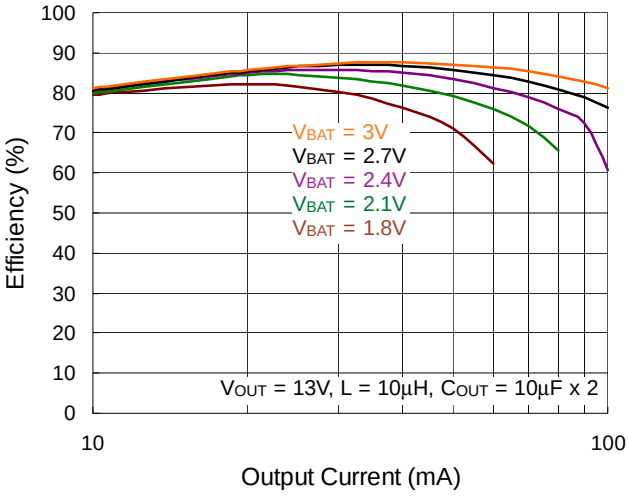
CH4 Buck Efficiency vs. Output Current



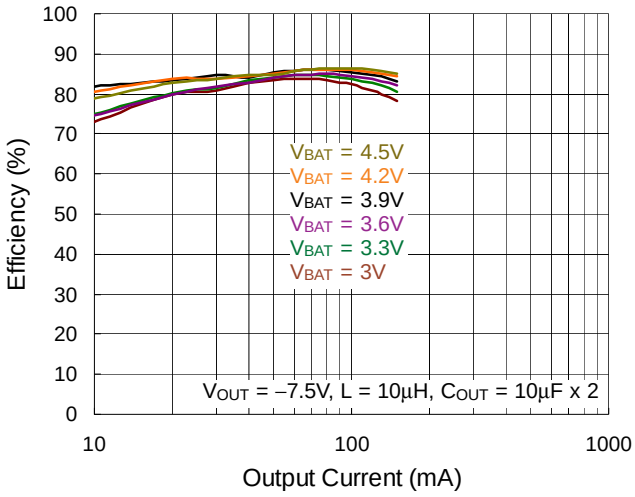
CH5 Boost Efficiency vs. Output Current



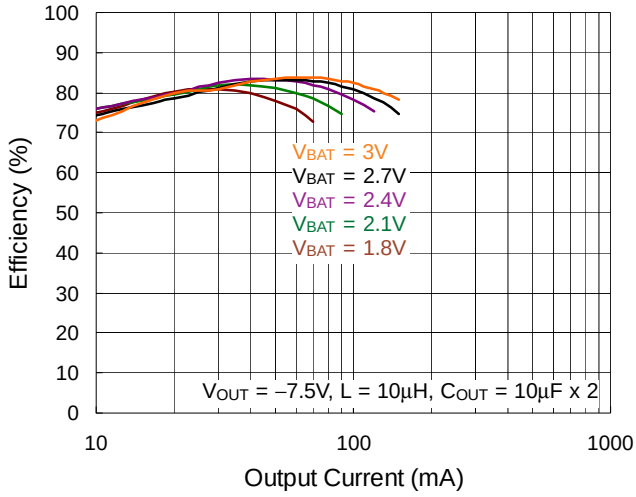
CH5 Boost Efficiency vs. Output Current



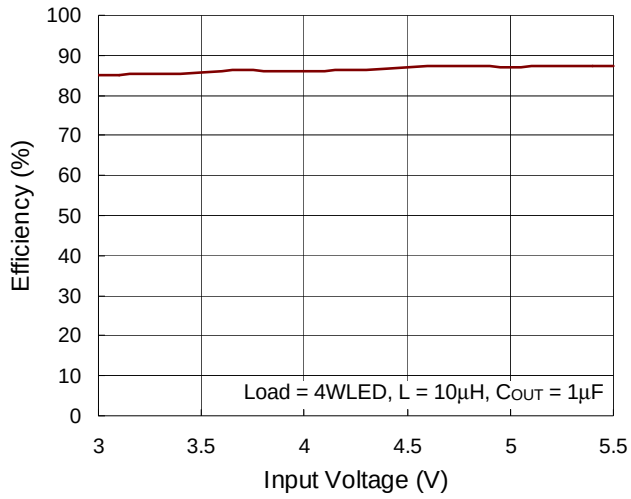
CH6 Inverting Efficiency vs. Output Current



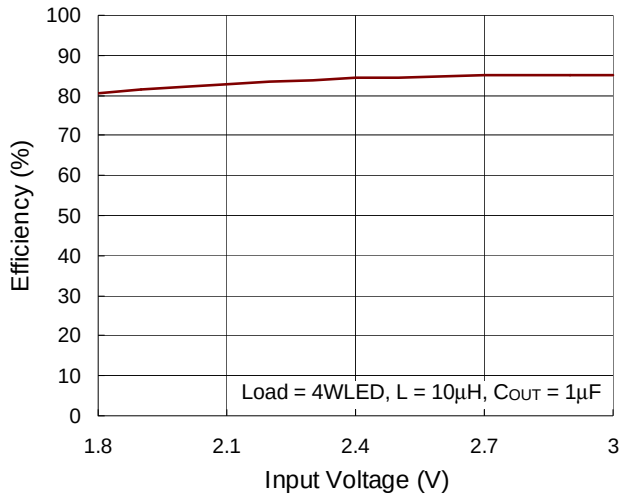
CH6 Inverting Efficiency vs. Output Current



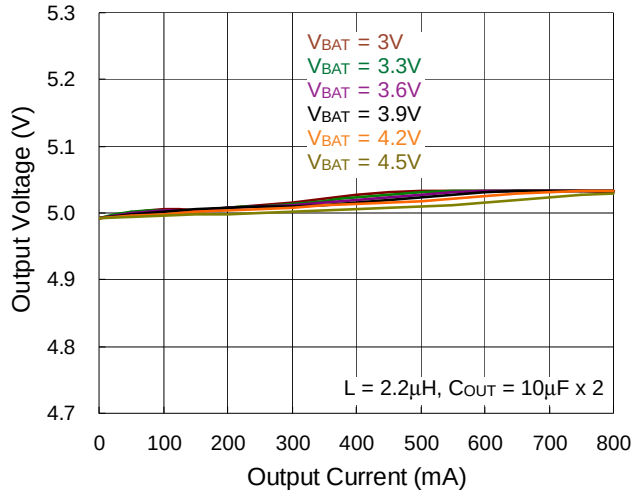
CH7 Efficiency vs. Input Voltage



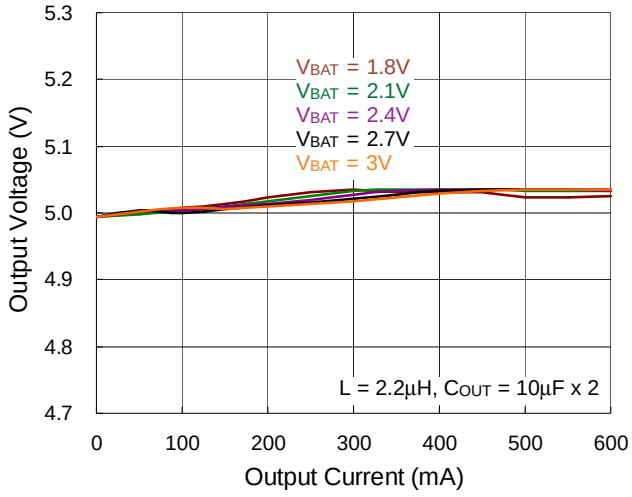
CH7 Efficiency vs. Input Voltage



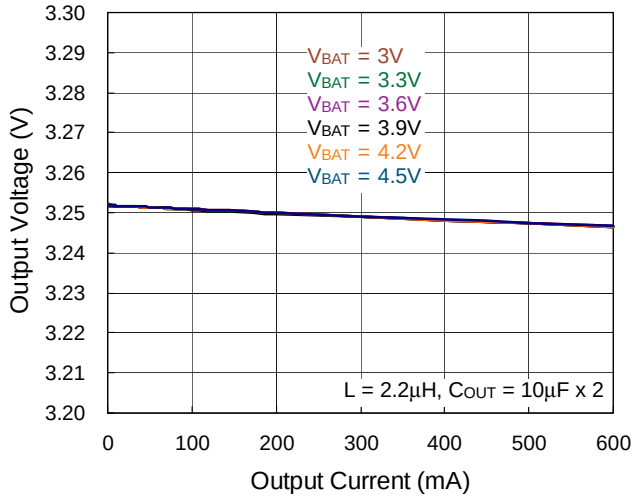
CH1 Boost Output Voltage vs. Output Current



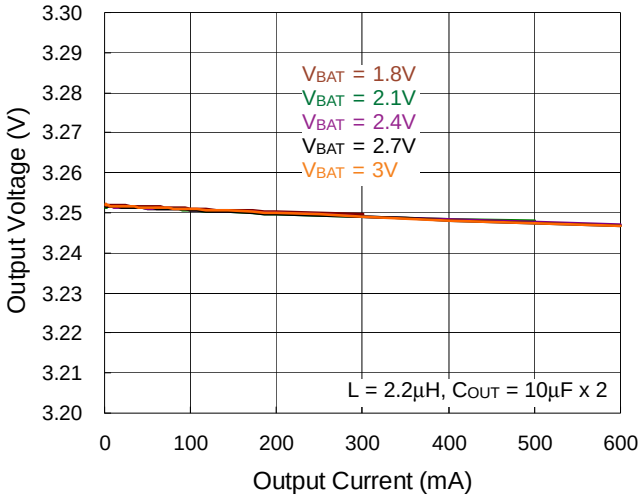
CH1 Boost Output Voltage vs. Output Current



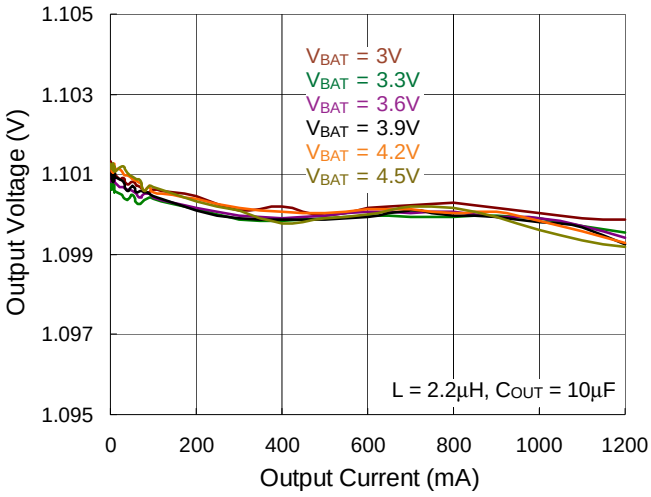
CH2 Buck-Boost Output Voltage vs. Output Current



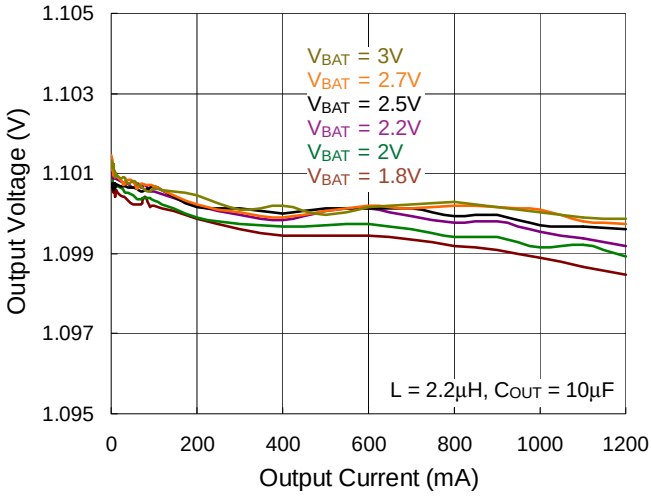
CH2 Buck-Boost Output Voltage vs. Output Current



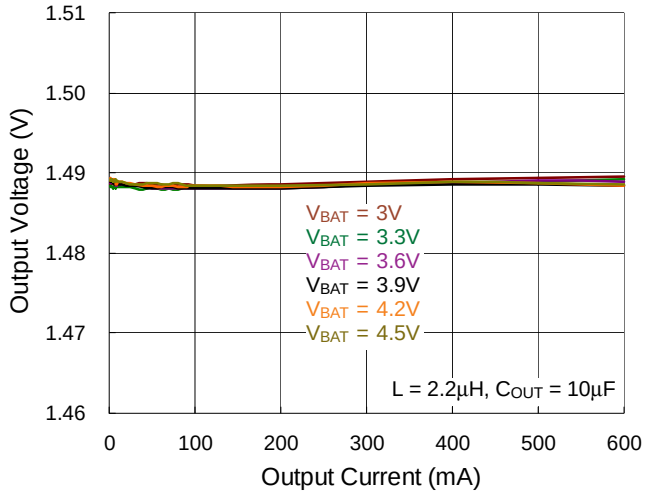
CH3 Buck Output Voltage vs. Output Current



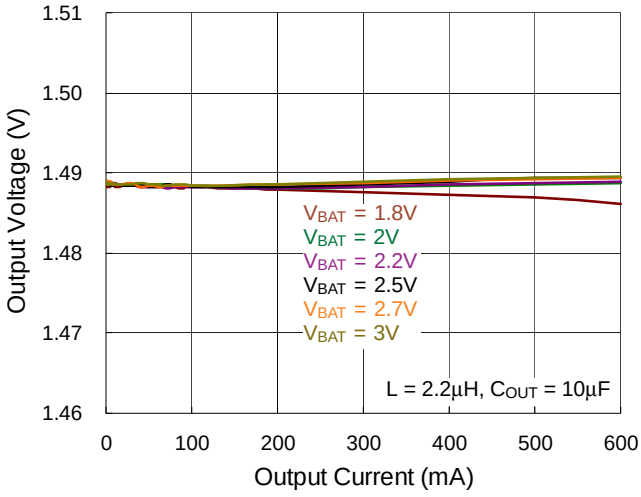
CH3 Buck Output Voltage vs. Output Current



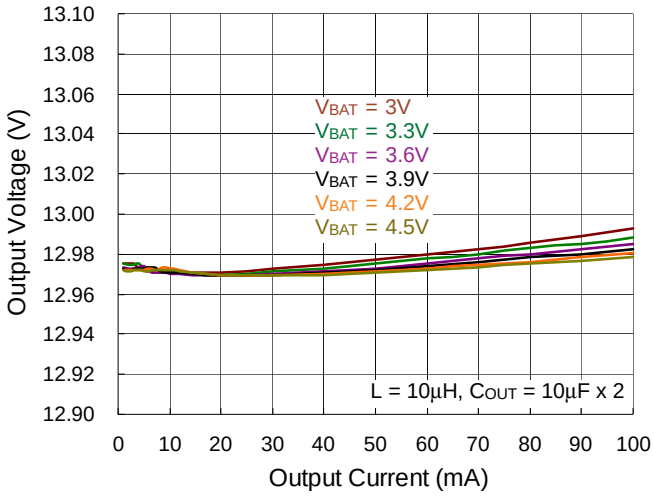
CH4 Buck Output Voltage vs. Output Current



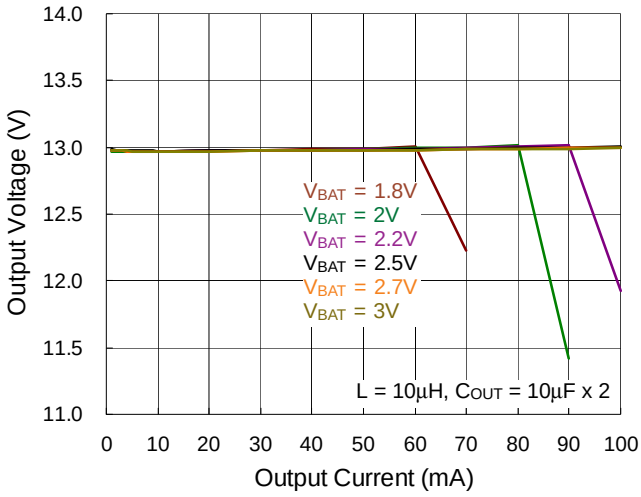
CH4 Buck Output Voltage vs. Output Current



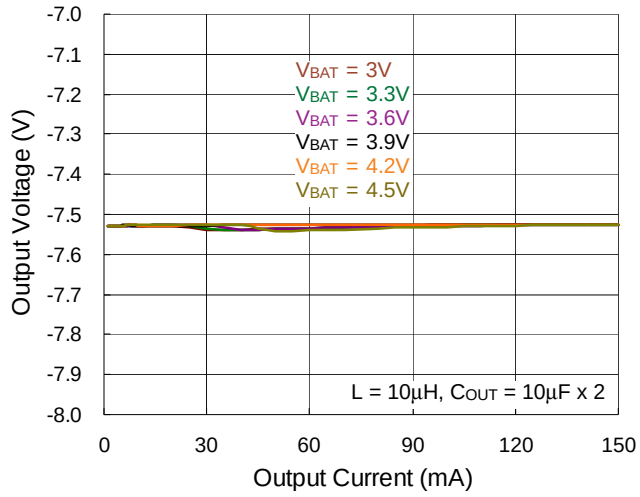
CH5 Boost Output Voltage vs. Output Current



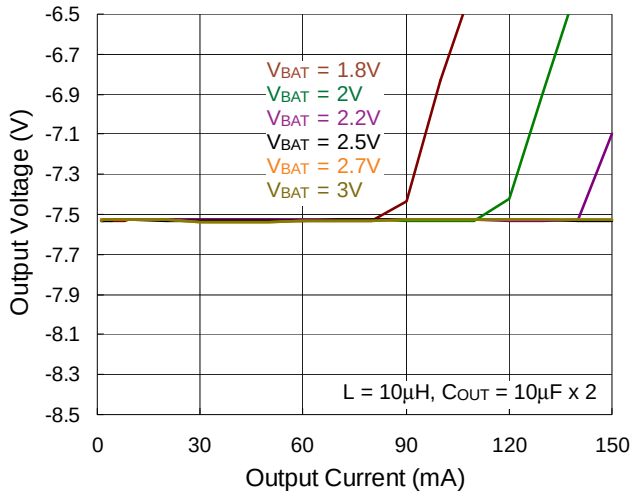
CH5 Boost Output Voltage vs. Output Current



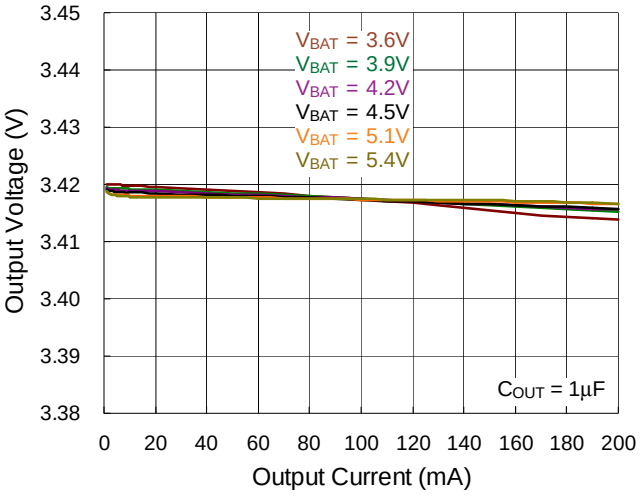
CH6 Inverting Output Voltage vs. Output Current



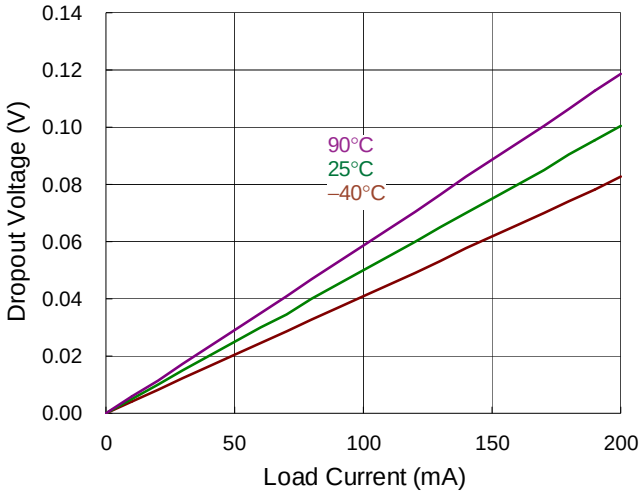
CH6 Inverting Output Voltage vs. Output Current



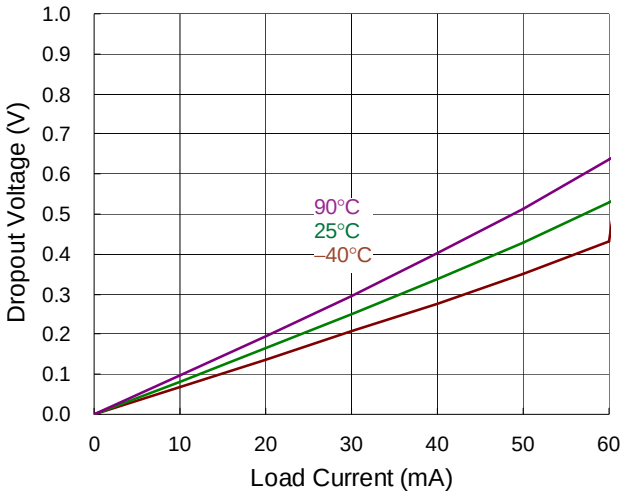
CH8 LDO Output Voltage vs. Output Current



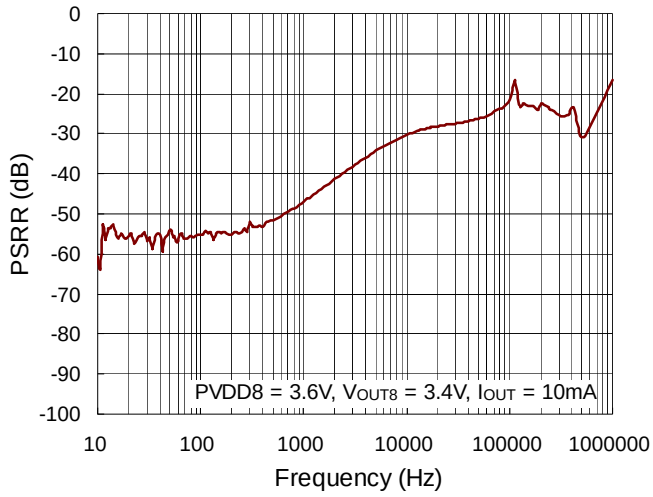
CH8 LDO Dropout Voltage vs. Load Current



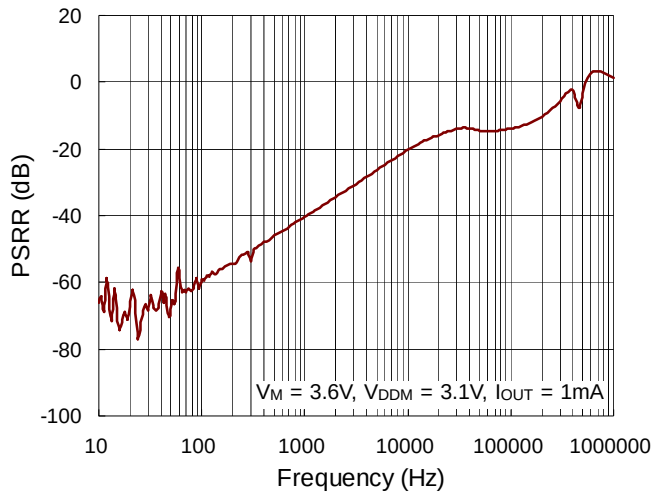
CH9 LDO Dropout Voltage vs. Load Current



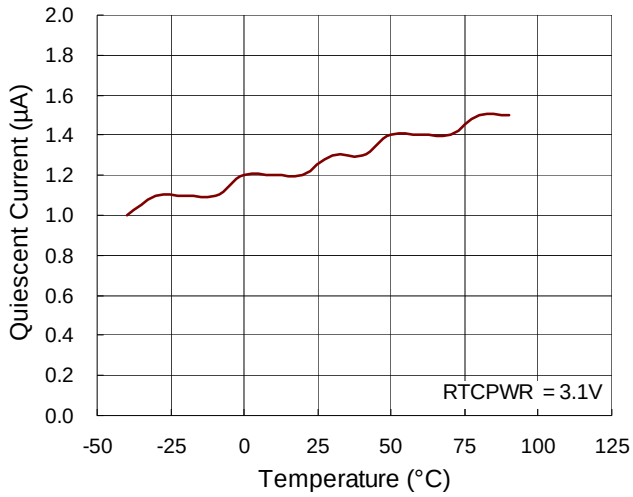
CH8 LDO PSRR



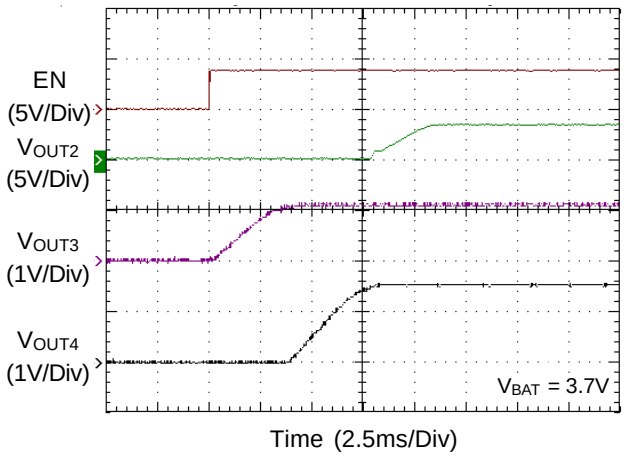
CH9 LDO PSRR



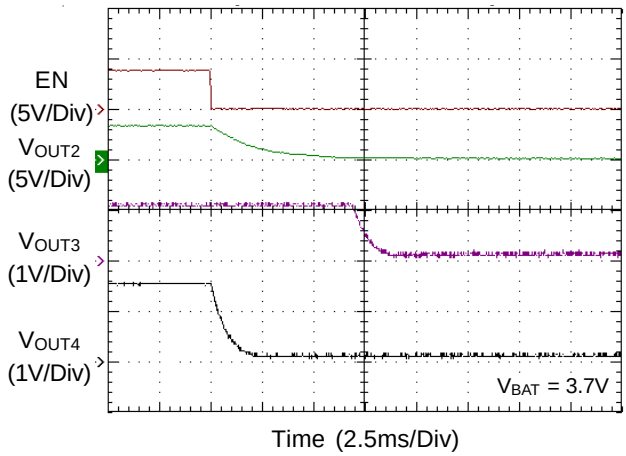
RTCPWR Quiescent Current vs. Temperature



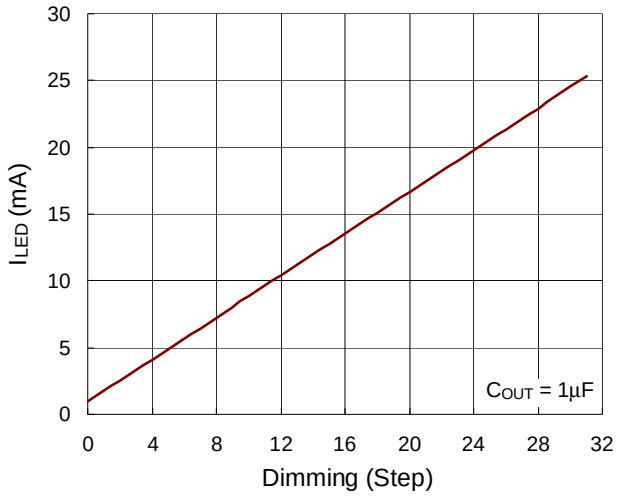
Power On Sequence



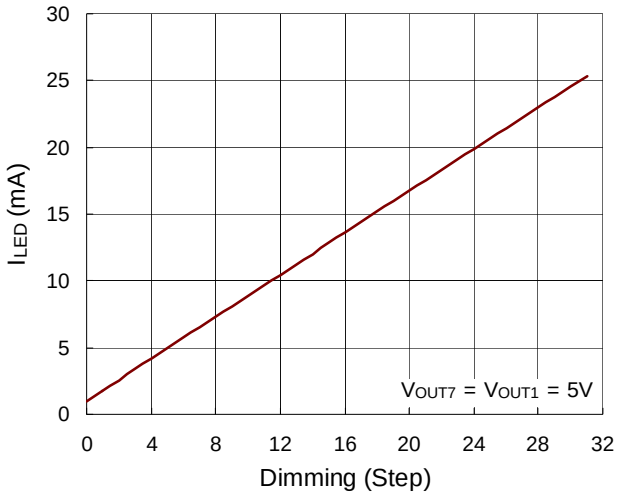
Power Off Sequence



CH7 Boost mode Dimming with 4 White LEDs



CH7 Current Source Dimming with 1 White LED



Application Information

The RT9999A/B is a highly-integrated DSC Power Management IC that contains 7CH switching DC/DC converters and one generic LDO, one keep-alive low-quiescent LDO, a switch with reverse leakage prevention from backup battery, and a Real-Time-Clock (RTC) including time counter and 32768Hz oscillator.

CH1 : Step-up operated in either Async PFM or Sync PWM current mode DC/DC converter. It includes internal power MOSFETs, compensation network and FB resistors. The P-MOSFET body can be controlled to disconnect the load. This is suitable for power of DSC Motor.

CH2 : Step-up/down (Buck-Boost) synchronous current mode DC/DC converter with internal power MOSFETs, compensation network and FB resistors. This channel supplies the power for I/O. This channel is always operated at CCM.

CH3 : Step-down synchronous current mode DC/DC converter with internal power MOSFETs, compensation network and FB resistors. This channel supplies the power for core. It can be operated at 100% maximum duty cycle to extend battery operating voltage range.

CH4 : Step-down synchronous current mode DC/DC converter with internal power MOSFETs, compensation network and FB resistors. This channel supplies the power for Memory. It can be operated at 100% maximum duty cycle to extend battery operating voltage range.

CH5 : High voltage step-up synchronous current mode DC/DC converter with internal power MOSFETs, compensation network and FB resistors. The P-MOSFET body can be controlled to disconnect the load. This channel supplies the CCD+ bias.

CH6 : Asynchronous inverting current mode DC/DC converter with internal power MOSFET, compensation network and FB resistors. It needs an external Schottky diode. This channel supplies the CCD– bias.

CH7 : A WLED driver operating in either current source mode or synchronous step-up mode with internal P-MOSFET and compensation network. WLED current and dimming level is determined by I^2C interface. The P-MOSFET body in step-up mode can be controlled to disconnect the load.

CH3 and CH4 operate in PWM mode with 2MHz, while CH1, CH2, CH5, CH6 and CH7 operate in PWM mode with 1MHz switching frequency.

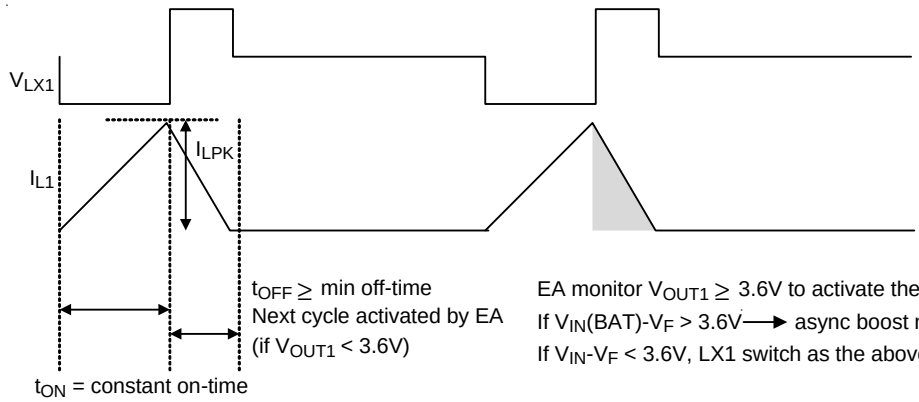
CH8 : A generic LDO output voltage is controlled by I^2C interface. This supplies the multiple purpose power.

CH9 : A keep-alive LDO supplies the power for backup battery.

CH1 : Step-Up DC/DC Converter

CH1 is a step-up converter for motor driver power in DSC system. The converter operates at async PFM or fixed frequency PWM current mode which can be set by I^2C. The converter integrates internal MOSFETs, FB resistors, compensation network and synchronous rectifier for up to 95% efficiency. The output voltage of CH1 is adjustable by the I^2C interface in the range of 3.6V to 5.3V.

CH1 operates at async PFM mode, LX1 switch as below waveform :



EA monitor $V_{OUT1} \geq 3.6V$ to activate the switching.
If $V_{IN}(BAT)-V_F > 3.6V$ ⟶ async boost not switch.
If $V_{IN}-V_F < 3.6V$, LX1 switch as the above waveform.

CH2 : Synchronous Step-Up / down DC/DC Converter

CH2 is a synchronous step-up / down converter for system I/O power. The converter operates at fixed frequency PWM Current Mode. The converter integrates internal MOSFETs, FB resistors, compensation network and synchronous rectifier for up to 95% efficiency.

The output voltage of CH2 can be adjusted by the I^2C interface in the range of 3.45V to 3.1V.

VNEG Charge Pump

The Charge pump is to increase the Vgs driving of big P-MOSFET in CH2/3/4/6.

When BAT < 3.6V and one of CH2/3/4/6 turns on, VNEG charge pump would turn on and start to pump. But when pumping, the BAT threshold to turn off and stop charge pump becomes 3.9V.

When pumping, the (BAT – VNEG) voltage would be clamped at 4.5V. But because of charge pumping architecture limitation, most negative level of the VNEG is only (–BAT).

Hence, if BAT < 4.5 / 2 = 2.25V, VNEG is limited to (–BAT).

When VNEG charge pump is off, VNEG is connected internally to GND.

CH3 : Synchronous Step-Down DC/DC Converter

CH3 is suitable for core power in DSC system. The converter operates in fixed frequency PWM mode with integrated internal MOSFETs, FB resistors and compensation network. The CH3 step-down converter can be operated at 100% maximum duty cycle to extend battery operating voltage range.

The output voltage of CH3 is adjustable by the I^2C interface in the range of 1.3V to 1V.

CH4 : Synchronous Step-Down DC/DC Converter

CH4 is suitable for memory power in DSC system. The converter operates in fixed frequency PWM mode with integrated internal MOSFETs, FB resistors and compensation network. The CH4 step-down converter can be operated at 100% maximum duty cycle to extend battery operating voltage range.

The output voltage of CH4 is adjustable by the I^2C interface in the range of 1.84V to 1.42V.

CH5 : Synchronous Step-Up DC/DC Converter

CH5 is a high voltage synchronous step-up converter for CCD positive power. The converter operates at fixed frequency PWM mode, and CCM with integrated internal MOSFETs, compensation network and load disconnect function.

The output voltage of CH5 is adjustable by the I^2C interface in the range of 15V to 12V or set by external feedback resistors.

The equation is as follows :

$V_{OUT\_CH5} = (1 + R1 / R2) \times V_{FB5}$

V_{FB5} is 1.25V typically.

CH6 : INV DC/DC Converter

This converter integrates an internal P-MOSFET with internal compensation and needs an external Schottky diode to provide CCD negative power supply.

The output voltage of CH6 is adjustable by the I^2C interface in the range of –5V to –8V or set by external feedback resistors.

The equations are as follows :

$V_{OUT\_CH6} = 0.2 – (R3 / R4) \times 1.24V$

Where R3 and R4 feedback resistors are connected to FB6, 1.24V equals to ($V_{REF} – V_{FB6}$).

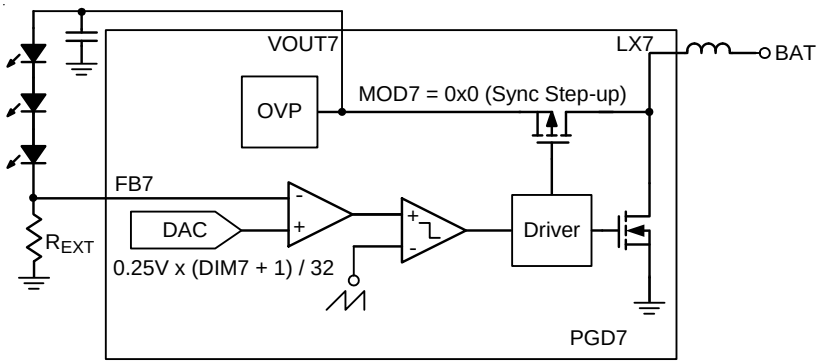
Reference Voltage

The RT9999A/B provides a precise 1.24V to 1.84V reference voltage, VREF, with souring capability of 200μA. Connect a 0.1μF ceramic capacitor from the VREF pin to GND. Reference voltage is enabled by I^2C interface. Furthermore, this reference voltage is internally pulled to GND at shutdown.

CH7 : WLED Driver

CH7 is a WLED driver that can operate in either current source mode or synchronous step-up mode, as determined by I^2C interface. When CH7 works in current source mode, it sources an LED current out of LX7 pin and regulates the current by FB7 voltage. The LED current is defined by

FB7 voltage and the external resistor between FB7 and GND. The FB7 regulation voltage can be set in 32 steps from 7.8mV to 250mV, typically, via I²C interface. If CH7 works in synchronous step-up mode, it integrates synchronous step-up mode with an internal MOSFET and internal compensation. The LED current is also set via an external resistor and FB7 regulation voltage.



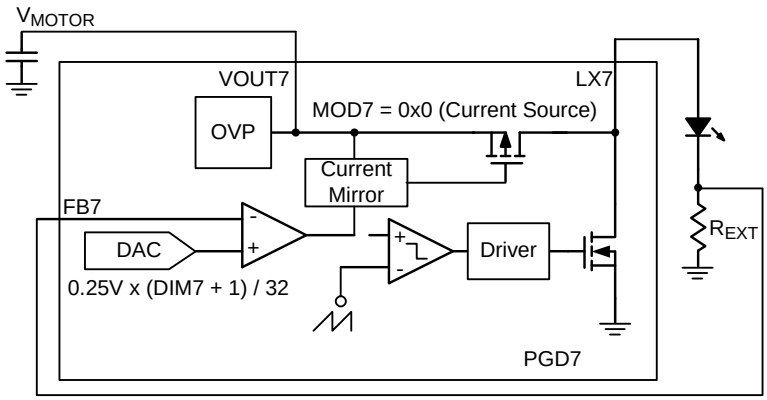
CH7 WLED Current Dimming Control

If CH7 is in synchronous step-up mode or current source mode, the WLED current is set by an external resistor. Regardless of the mode, dimming is always controlled by I²C interface.

The WLED current can be set by the following equation :

I_{LED} (mA) = [250mV / R (W)] x (DIM7 + 1) / 32

R is the current sense resistor from FB7 to GND and (DIM + 1) / 32 ratio refers to I²C control register file.



* Register DIM7 defines dimming FB7 regulation voltage for Both Sync Step-Up mode and Current Source mode. The regulation voltage = 0.25V x (DIM7 + 1) / 32, where (DIM7 + 1) / 32 = 1/32 to 32/32.

  0.25V voltage with accuracy ±5%. I_{LED} max is defined by the 0.25V/R_{EXT}.

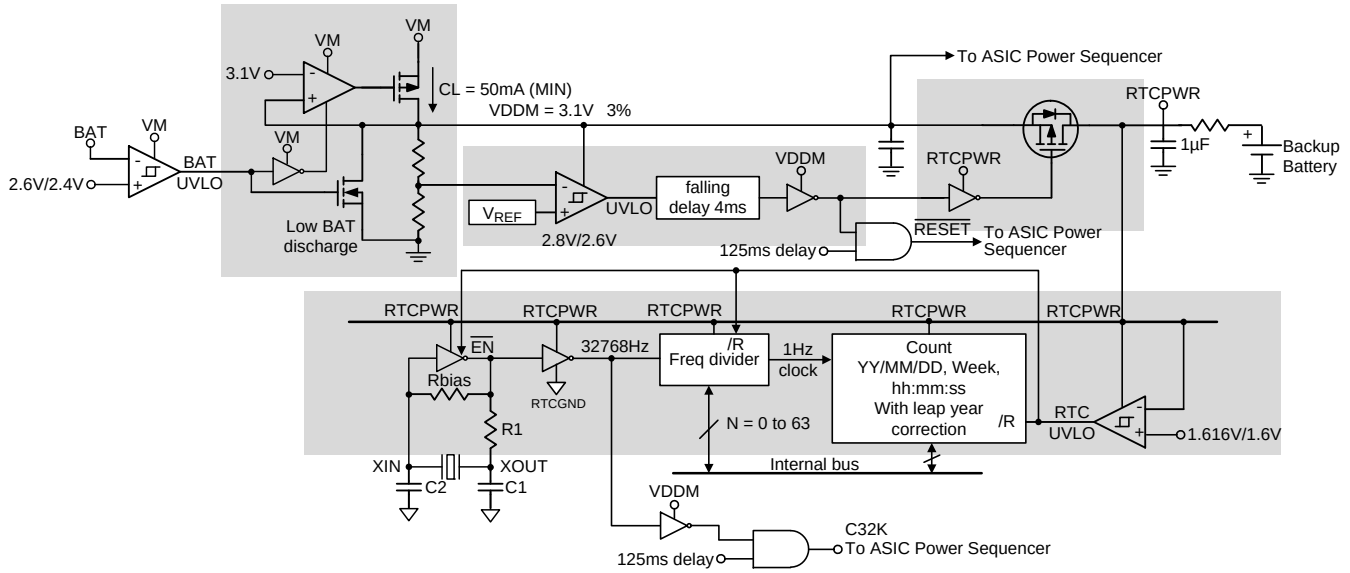
CH8 : Generic LDO

CH8 is a generic low voltage LDO for multiple purpose power.

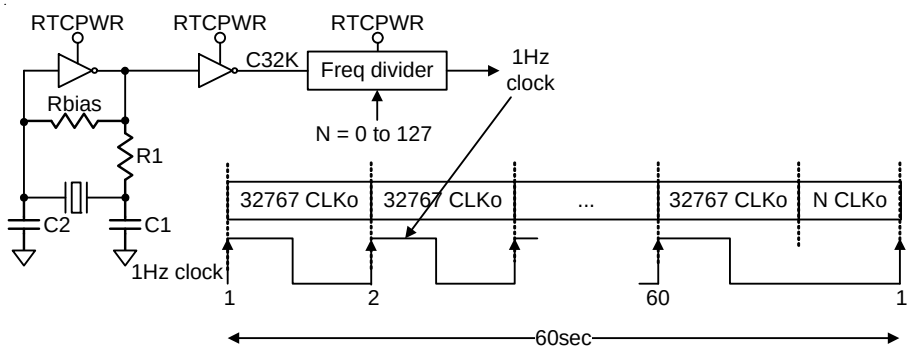
The CH8 is a linear regulator, designed to be stable over the entire operating load range with the use of external ceramic capacitors. CH8 have an ON/OFF control which can be set by I²C commands. The output voltage of CH8 is adjustable by the I²C interface in the range of 3.5V to 1.5V.

CH9 : Keep Alive LDO and RTC Related Function Block

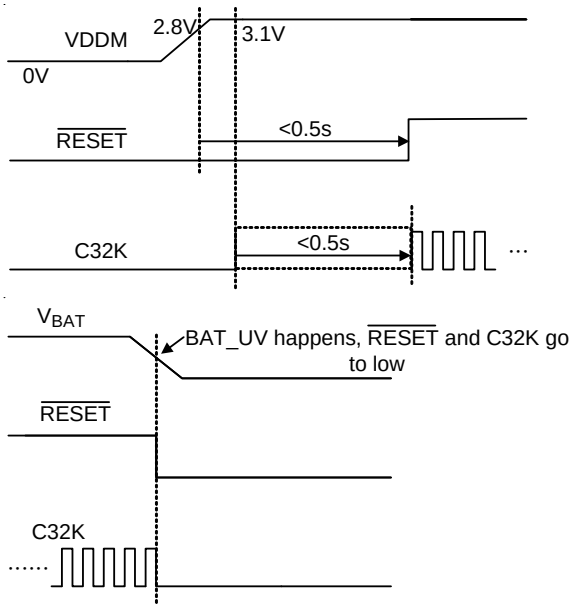
The RT9999A/B provides a 3.1V output LDO for all IC control circuits and real time clock. The LDO features low quiescent current (4μA) and high output voltage accuracy. This LDO is always on, even when the system is shut down. For better stability, it is recommended to connect a 1μF to the VDDM pin. The RTCPWR switch avoids back-charging from the RTCPWR node into the input node VDDM.



The Frequency Divider from 32768Hz to 1Hz would generate the below 1Hz wave that has a little jitter but the 1Hz average frequency can be finely tuned.



Fine tune 1Hz by digital divider can create
tuning range = (-60 to 67) / (32768Hz x 60s) = -30 to 33 ppm
each tune step size = 0.5 ppm.
But the 1Hz would include jitter and the C32K still is not tuned.



RTC Time Read/Write Method

When reading RTC time via I²C interface, suggest reading 6 bytes (address A11 to A16) together and finish reading within 0.5 second to avoid the second carry issue. A16. RTCT_SEC [0] can be used for checking whether second is carried during reading time.

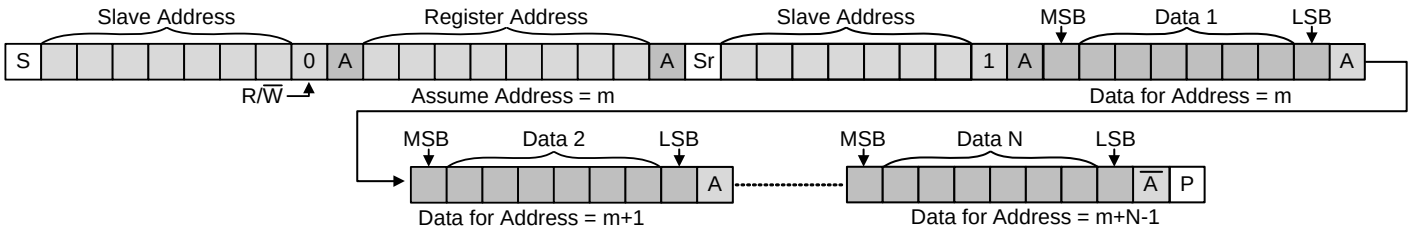
When writing RTC time via I²C interface, suggest writing 6 bytes (address A11 to A16) together. A11 is first and then A12, A13, A14, A15, A16. Suggest finishing writing within 0.5 second to avoid second carry issue during writing.

I²C Register Information

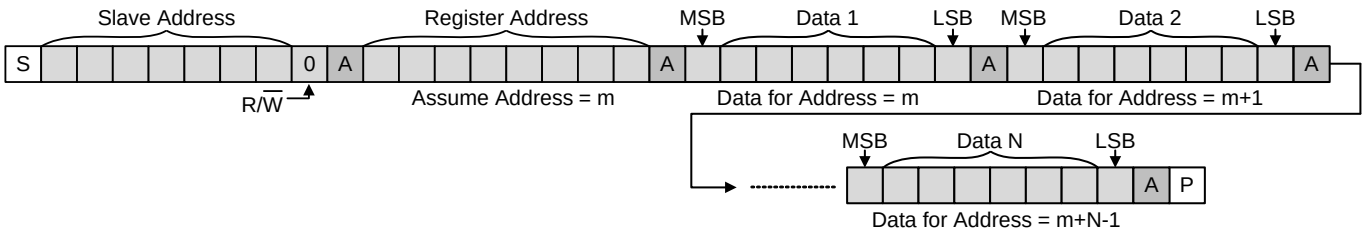
The RT9999A/B I²C interface power must be supplied by either VOUT2 or an equal potential node. If $\overline{\text{RESET}}$ = Low, I²C read/write can not function.

The RT9999A/B I²C slave address = 0011000 (7bits). I²C interface supports fast mode (bit rate up to 400kb/s). The write or read bit stream (N ≥ 1) is shown below :

Read N bytes from RT9999A/B

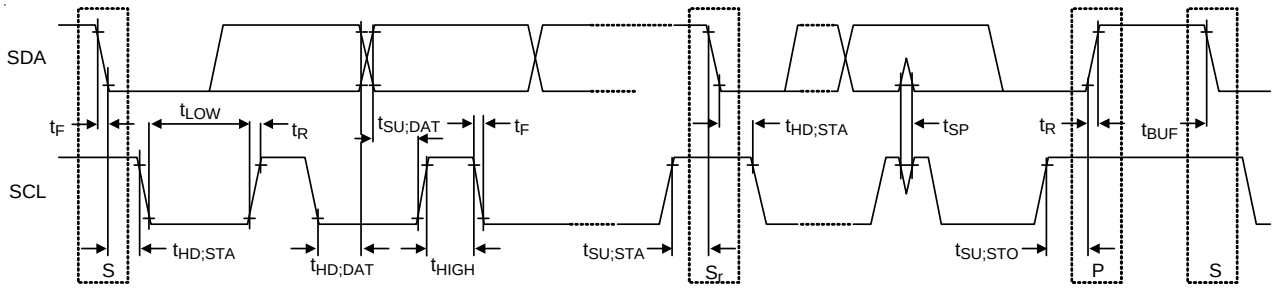


Write N bytes to RT9999A/B



Driven by Master, Driven by Slave (RT9999A/B), P Stop, S Start, Sr Repeat Start

I²C Waveform Information



I²C Register File

Address Name	Register Address	(MSB)				Bit Map, Read/Write, Default value			(LSB)
		b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]
A0	0x00	VOUT1				Reserved	VOUT2		
		R/W				--	R/W		
		1	1	1	1	x	1	0	0
A1	0x01	VOUT3				DIS4	VOUT4		
		R/W				R/W	R/W		
		1	0	1	0	1	$\overline{\text{MSEL}}$	0	1
A2	0x02	Reserved	VOUT5			Reserved	VOUT6		
		--	R/W			--	R/W		
		x	1	0	0	x	1	0	1
A3	0x03	VOUT8				DIM7			
		R/W				R/W			
		0	0	1	1	1	1	1	1

Address Name	Register Address	(MSB)	Bit Map, Read/Write, Default value						(LSB)
		b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]
A4	0x04	Reserved				MOD7	OVP7		
		--				R/W	R/W		
		x	x	x	x	0	1	1	0
A5	0x05	ENDLY3				ENDLY2			
		R/W				R/W			
		0	0	0	0	0	1	0	0
A6	0x06	Reserved				ENDLY4			
		--				R/W			
		x	x	x	x	0	0	1	0
A7	0x07	PWM1	Reserved	Reserved	EN4	EN5	EN6	EN7	EN8
		R/W	--	--	R/W	R/W	R/W	R/W	R/W
		0	x	x	1	0	0	0	0
A10	0x0A	Reserved	RTCAJ						
		--	R/W						
		x	0	1	1	1	0	1	1
A11	0x0B	Reserved	Reserved	RTCT_SEC[5:0]					
		--	--	R/W					
		x	x	0	0	0	0	0	0
A12	0x0C	Reserved	Reserved	RTCT_MIN[5:0]					
		--	--	R/W					
		x	x	0	0	0	0	0	0
A13	0x0D	Reserved	Reserved	Reserved	RTCT_HR[4:0]				
		--	--	--	R/W				
		x	x	x	0	0	0	0	0
A14	0x0E	Reserved	Reserved	Reserved	RTCT_DAY[4:0]				
		--	--	--	R/W				
		x	x	x	0	0	0	0	1
A15	0x0F	Reserved	RTCT_MON[3:0]				RTCT_WEK[2:0]		
		--	R/W				R/W		
		x	0	0	0	1	1	1	0
A16	0x10	RTCT_SEC[0]	Reserved	RTCT_YAR[5:0]					
		R	--	R/W					
		0	x	0	0	1	0	1	1
A17	0x11	USER[7:0]							
		R/W							
		0	0	0	0	0	0	0	0
A18	0x12	USER[15:8]							
		R/W							
		0	0	0	0	0	0	0	0

Address Name	Register Address	(MSB)			Bit Map, Read/Write, Default value				(LSB)
		b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]
A19	0x13	USER[23:16]							
		R/W							
		0	0	0	0	0	0	0	0
A20	0x14	USER[31:24]							
		R/W							
		0	0	0	0	0	0	0	0

Notes :

- VOUT1/2/3/4/5/6/8 at A0, A1, A2, A3.
- A1.DIS4 : can set whether CH4 discharges output node when it turns off.

  DIS4 = 1 : CH4 will discharge VOUT4 node when it turns off.

  DIS4 = 0 : CH4 will NOT discharge VOUT4 node when it turns off.
- A4.MOD7 : is used for selecting CH7 WLED operation mode.

  MOD7 = 0x0 means current source mode.

  MOD7 = 0x1 means sync step-up mode.
- A3.DIM7 : defines LED current dimming ratio of CH7. The dimming ratio is (DIM7 + 1) / 32. DIM7 define FB7 regulation voltage = 0.25V x (DIM7 + 1) / 32.
- A4.OVP7 : defines the over voltage protection threshold at VOUT7 node of CH7 in step-up mode. This allows users to choose the proper OVP threshold for series 2 to 5 WLED.

  The mode setting of CH7 must be ready before CH7 enable signal sent by I^2C.

OVP7 = 0	OVP7 = 1	OVP7 = 2	OVP7 = 3	OVP7 = 4	OVP7 = 5	OVP7 = 6	OVP7 = 7
8V	10V	12V	14V	16V	18V	20V	23V

- ENDLY1/2/3/4/8 at A4/5/6 : ENDLYx set CHx power on delay time (2ms x ENDLYx). Time counting starts once the EN pin goes high. Hence, ENDLYx can choose 0ms to 30ms. To turn on, CHx has to satisfy two conditions : one is the enable bit A8.ENx = 1 and the other is “delay time counting finish”.
- A7.PWM1 : defines CH1 operation mode PWM1 = 0 means CH1 is in PFM asynchronous rectified operation mode. PWM1 = 1 means CH1 is in peak current control PWM synchronous rectified operation mode.
- EN4/5/6/7/8 at A7 : enable (ENx = 1) or disable (ENx = 0) CH4/5/6/7/8. When the EN pin goes high, CHx turns on (after the delay time ENDLYx) if the bits ENx=1. CH5/6/7 has no ENDLYx setting. Hence, they turn on immediately once the EN pin goes high and the bit ENx = 1. The register byte A7 resets when the external EN input pin goes low.
- A10.RTCAJ : finely tune the RTC time counting frequency by adjusting (RTCAJ – 60)/2 ppm. Hence, the tuning range is –30ppm to 33ppm.
- RTCT_SEC [5:0] at A11 and RTCT_SEC [0] at A16 : stores the SECOND field of RTC time. That is 0 to 59. A16.RTCT_SEC[0] has the same storing value as A11.RTCT_SEC[0] Users can set SECOND value into address A11.Hence, when users read out the RTC time starting from A11 to A16, the SECOND of the RTC time may be carried. Thus, the A16.RTCT_SEC [0] will return a different value from A11.RTCT_SEC [0]. The difference allows users to deal with the carry on correction from the read RTC time.
- RTCT_MIN [5:0] at A12 : stores the MINUTE field of RTC time from 0 to 59.
- RTCT_HR [4:0] at A13 : stores the HOUR field of RTC time from 0 to 23 (24 hour format).
- RTCT_DAY [4:0] at A14 : stores the DATE field of RTC time from 1 to 31, depending on the month. RTCT_DAY [4:0] = 1 means 1st day of each month. The RT9999A/B supports leap year counting.

- RTCT_MON [3:0] at A15 : stores the MONTH field of RTC time from 1 to 12. RTCT_MON = 1 means January.
- RTCT_YAR [5:0] at A16 : stores the YEAR field of RTC time from 0 to 63. RTCT_YAR = 0 means the year 2000. Hence, RT9999A/B can count until the year 2063.
- RTCT_WEK [2:0] at A15 : stores the DAY-of-WEEK field of RTC time from 0 to 6. RTCT_WEK = 0 means Sunday and RTCT_WEK = 1 means Monday. The RT9999A/B can not automatically calculate the field based on other fields (YEAR, MONTH, DATE). Users have to write the right value into this field initially. The RT9999A/B just counts the field value among 0 to 6 when DATE field is carried.
- USER [31:0] at A17 to A20 : stores user's data, similar to accessing SRAM via I^2C.
- Register File Reset Moment

  A0 to A6 : Reset when $\overline{\text{RESET}}$ = L occurs.

  A7 : Reset when EN goes low.

  A10 to A16 : Reset when RTC Reset occurs.

  A17 to A20 : Reset when $\overline{\text{RESET}}$ = L occurs.

Output Voltage List

I^2C Register Value	VOUT1 4bit	VOUT2 I/O 3bit	VOUT3 CORE 4bit	VOUT4 MEM 3bit	VOUT5 CCD+ 3bit	VOUT6 CCD- 3bit	VOUT8 LDO 3bit
0	5.3	3.45	1.3	1.84	15	–5	3.5
1	5.2	3.4	1.28	1.8	14.5	–5.5	3.4
2	5.1	3.35	1.26	1.76	14	–6	3.3
3	5	3.3	1.24	1.58	13.5	–6.5	3.
4	4.9	3.25	1.22	1.54	13	–7	2.8
5	4.8	3.2	1.2	1.5	12.5	–7.5	2.5
6	4.7	3.15	1.18	1.46	12	–8	1.8
7	4.6	3.1	1.16	1.42	Ref	Ref	1.5
8	4.5	--	1.14	--	--	--	--
9	4.4	--	1.12	--	--	--	--
10	4.3	--	1.1	--	--	--	--
11	4.2	--	1.08	--	--	--	--
12	4	--	1.06	--	--	--	--
13	3.9	--	1.04	--	--	--	--
14	3.8	--	1.02	--	--	--	--
15	3.6	--	1	--	--	--	--

Ref means VOUT set by external feedback resistors.

FB5 regulation voltage = 1.25V for CH5

(V_{REF} – V_{FB6}) regulation voltage = 1.24V for CH6.

Typically, V_{FB6} is regulated at 0.2V.

VOUT4 Default Voltage is selected by the pin MSEL and latched at the moment when $\overline{\text{RESET}}$ goes high.
MSEL = H : default V_{OUT4} = 1.8V

MSEL = L : default V_{OUT4} = 1.5V.

Output Voltage Ramp Rate

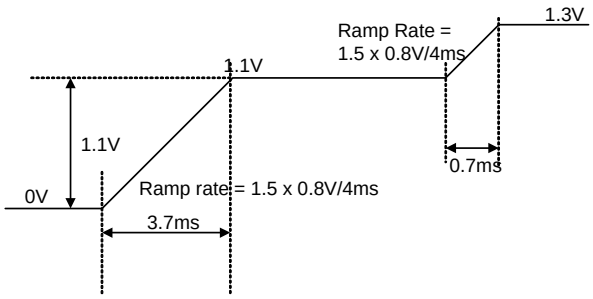
For instance, CH3 V_{CORE} output voltage ramp up rate = 1.5 x 0.8V/4ms = 0.3V/ms. The ramp up/down rate is kept the same for enabling soft-start or dynamic output voltage adjustment.

Each channel has a different ramp rate as shown in Electrical Characteristics.

From PWM1 = 1 to VOUT1 = 5V, the soft-start time ~ 4ms.

From EN8 = 1 to VOUT8 = 3.4V, the soft-start time ~ 4ms.

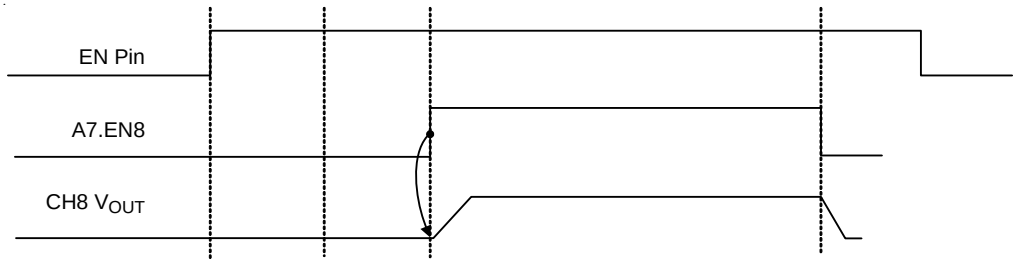
The soft-start time would be proportional to VOUT target voltage.



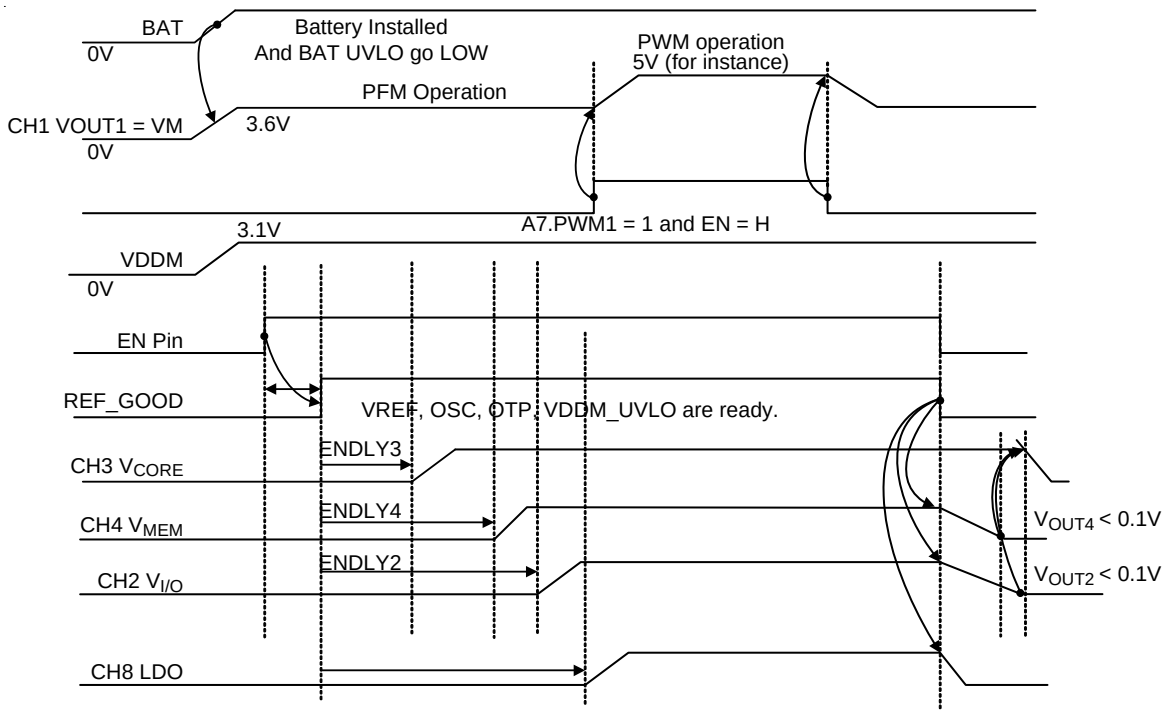
Note : CH1, CH3, CH4, CH8 output voltage and CH7 WLED current can be dynamically changed with inrush and V_{OUT}–ramping control when they have been turned on. CH2, CH5, CH6 are not.

Note : The Start point referred by ENDLYx delay time begins when the EN pin goes high.

Once, A7.EN8 = 1, CH8 turns on immediately.



Power On/Off Sequence



* if A7.EN4 = 1 and A7.EN8 = 1 in register file.

CH1 : As long as BAT doesn't trigger UVLO, CH1 remains active without EN pin = H. However, when A7.PWM1 = 1, EN pin = H and no VDDM_UVLO, CH1 will switch from PFM mode to PWM mode. Otherwise, it works in PFM mode.

CH2/3 : CH2 and CH3 are both enabled by the EN pin and have turn on delay time as defined in I^2C register A5. ENDLY2/3. When EN goes low, CH2 starts to turn off. After CH2 output voltage < 0.1V, CH3 will start to turn off.

If A1.DIS4 = 1, CH4 will internally discharge when turning off. In this case, CH3 will wait for V_{OUT2} < 0.1V, as well as V_{OUT4} < 0.1V before turning off.

CH4/8 : To enable CH4 and CH8, the bits A7.EN4 and A7.EN8 must be set to "1" and EN pin must be high. When the enable bits are set to "1", CH8 will turn on immediately, and CH4 will turn on after a delay time defined by ENDLY4.

Max Load of Every Channel

Purpose	RT9999A/B	Current Limit	Max Load	Condition (V_{IN} → V_{OUT})
VDDM and V_{MOTOR}	CH1	3A	800mA	3V → 5V
$V_{I/O}$	CH2	2A	600mA	3V → 3.3V
V_{CORE}	CH3	2A	1.2A	3V → 1.1V
V_{MEM}	CH4	1.5A	500mA	3V → 1.8V
CCD+	CH5	1.2A	100mA	3V → 16V
CCD-	CH6	1.5A	150mA	3V → –8V
WLED	CH7	0.8A	50mA	4 WLED
Generic LDO	CH8	300mA	200mA	$V_{IN} - V_{OUT}$ > 150mV
Keep Alive LDO	CH9	100mA	50mA	$V_{IN} - V_{OUT}$ > 300mV

Protection Act

	Protection Type	Threshold (typical value)	Delay Time	Protection Methods	Reset Method
VDDM	Over Voltage Protection	V_{DDM} > 6V	100ms	Turn off whole IC, Except CH9 and CH1 in PFM	Restart if VDDM < 5.8V
BAT	UVLO	V_{BAT} < 2.4V(RT9999A) V_{BAT} < 1.5V(RT9999B)	No Delay	Disable all Channels	Restart if V_{BAT} > 2.6V (RT9999A) V_{BAT} > 1.7V (RT9999B)
CH1	Current Limit (in PFM)	N-MOSFET current > 0.8A	No Delay	Turn off N-MOSFET	Reset after minimum off-time finish
	VOUT1 OVP (in PWM)	V_{OUT1} > 6V	No Delay	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = low
	OCP (in PWM)	N-MOSFET current > 3A	100ms	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = low
	VOUT1 UVP (in PWM)	V_{OUT1} < 2.25V	No Delay	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = low
	Over Load Protection (in PWM)	V_{OUT1} < Target – 0.6	100ms	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = low

	Protection Type	Threshold (typical value)	Delay Time	Protection Methods	Reset Method
CH2	Current Limit and OCP	Inductor Current > 2A	No Delay	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = low
	VOUT2 OVP	V_{OUT2} > 6V	No Delay	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = low
	VOUT2 UVP	V_{OUT2} < 1.6V	No Delay	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = low
	Over Load Protection	V_{OUT2} < Target – 0.4	100ms	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = low
CH3	OCP	P-MOSFET Current > 2A	100ms	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = Low
	VOUT3 UVP	V_{OUT3} < 0.6	No Delay	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = Low
	Over Load Protection	V_{OUT3} < Target – 0.15	100ms	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = Low
CH4	OCP	P-MOSFET Current > 1.5A	100ms	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = Low
	VOUT4 UVP	V_{OUT4} < 0.8	No Delay	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = Low
	Over Load Protection	V_{OUT4} < Target – 0.2	100ms	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = Low
CH5	OCP	N-MOSFET Current > 1.2A	100ms	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = Low
	OVP	V_{OUT5} > 19V	No Delay	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = Low
	UVP	V_{FB5} < 0.6V	100ms	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = Low
	Over Load Protection	V_{OUT5} < Target – 1.8	100ms	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = Low
CH6	OVP	V_{OUT6} < –11V	No Delay	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = Low
	OCP	P-MOSFET Current > 1.5A	100ms	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = Low
	VOUT6 UVP	V_{FB6} > 0.5V	100ms	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = Low
	Over Load Protection	V_{FB6} > 0.35V	100ms	Turn Off Whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = Low
CH7	OCP	N-MOSFET Current > 0.8A	100ms	Turn Off Whole IC	VDDM Power Reset or EN = Low
	OVP	V_{OUT7} > A4.OVP7 Threshold	No Delay	Turn Off CH7 only	VDDM Power Reset or EN = Low
CH8	UVP	V_{OUT8} < target x 0.5	No Delay	Turn off whole IC, Except CH9 and CH1 in PFM	VDDM Power Reset or EN = Low
	Current Limit	P-MOSFET Current > 300mA	No Delay	Limit P-MOSFET Current	Reset by Load
CH9	Current Limit	P-MOSFET Current > 100mA	No Delay	Limit P-MOSFET Current	Reset by Load
	VM UVLO	V_M < BAT – 1.1V	No Delay	Lower down CH1 PFM driving capability	Reset when V_M > BAT – 1.1V
	$\overline{\text{RESET}}$	V_{DDM} < 2.6V	No Delay	Turn Off Whole IC, Except CH9 and CH1 in PFM	Restart Whole IC if EN = High and VDDM > 2.8V

	Protection Type	Threshold (typical value)	Delay Time	Protection Methods	Reset Method
RTCPWR	UVLO	V_{RTCPWR} < 1.6V	No Delay	Clear RTC Registers	V_{RTCPWR} > 1.616V
Thermal	Thermal Shutdown	Temperature > 160°C	No Delay	Turn Off Whole IC, Except CH9 and CH1 in PFM	Restart Whole IC if EN = High and Temperature < 140°C

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-40L 5x5 package, the thermal resistance, θ_{JA}, is 36°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (36°C/W) = 2.778W for WQFN-40L 5x5 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

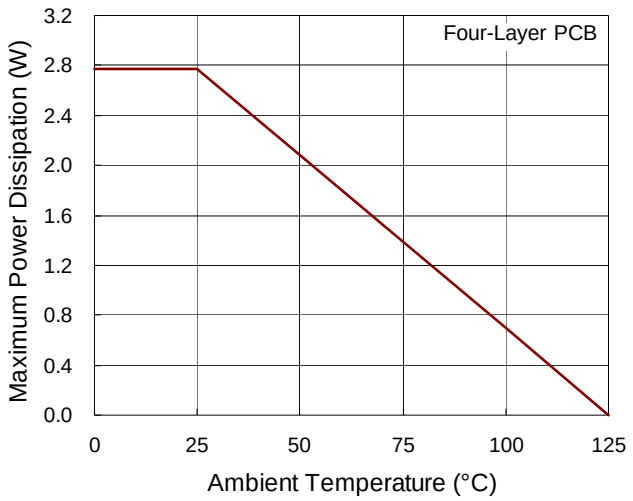


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

For the best performance of the RT9999A/B, the following PCB layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins respectively for good noise filtering.
- Keep the main power traces as wide and short as possible.
- The switching node area connected to LX and inductor should be minimized for lower EMI.
- Place the feedback components as close as possible to the FB pin and keep these components away from the noisy devices.
- Connect the GND and Exposed Pad to a strong ground plane for maximum thermal dissipation and noise protection.
- Directly connect the output capacitors to the feedback network of each channel to avoid bouncing caused by parasitic resistance and inductance from the PCB trace.

For the 32-kHz oscillator to the best performance, Please obey the following guidelines :

- Place the crystal and its components close to the oscillator side and the oscillator pins.
- Ensure that the ground plane under the oscillator and its components are of good quality.
- Avoid placing a separate ground under the oscillator and connecting it to the general ground through a single point.
- Avoid long connections to the crystal and to the load capacitor that create a large loop on the PCB .
- Use a short connection between the two crystal load capacitors and route the common connection to the oscillator ground reference.
- Place a ceramic capacitor for noise filtering from RTCPWR to RTCGND with short connections.
- Place the C32K (logic output signal) output so that the return ground current runs back to RTCGND. Do not route the trace close to the oscillator input.

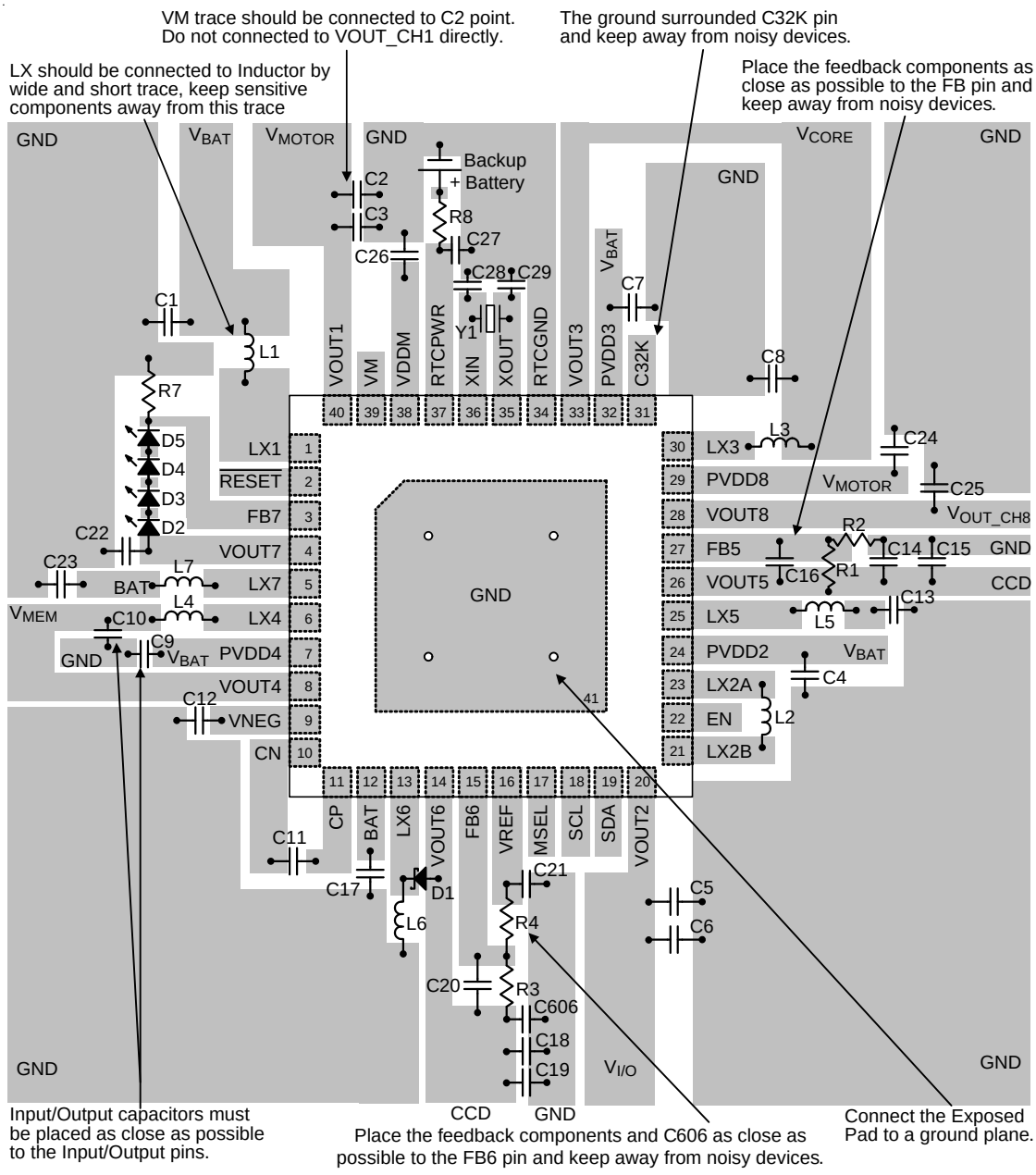
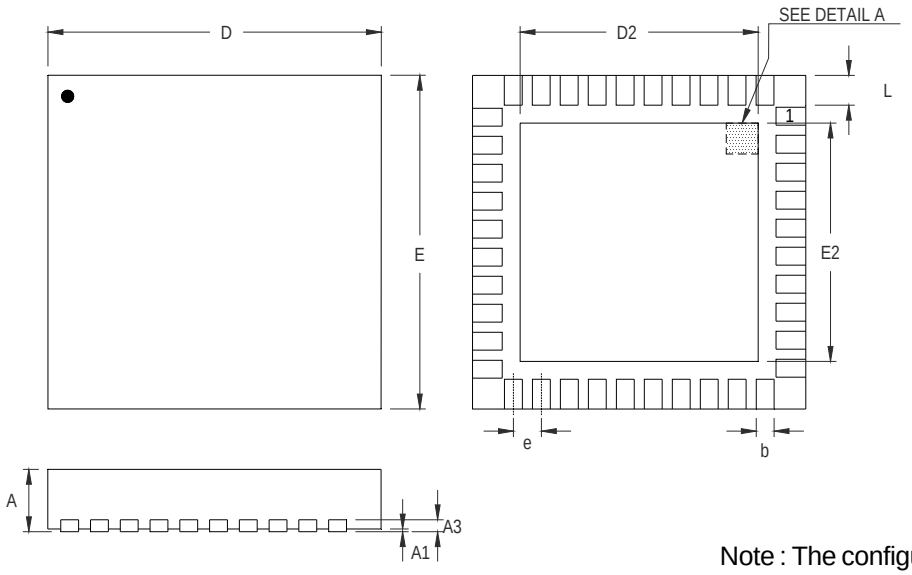
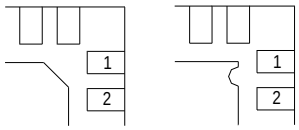


Figure 4. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

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