







RTQ1954

10V to 80V Hotswap Controller with Accurate Monitoring, PMBus Interface and Dynamic Transient Load Support

1 General Description

The RTQ1954 provides enterprise-level protection and high-performance monitoring for 10V to 80V systems such as 48V/54V datacenter network equipment. Subus response to short-circuit faults, multiple adjustable high-resolution overcurrent thresholds and remote temperature sensing with adjustable thresholds allow the RTQ1954 to protect and monitor critical systems including those with wide dynamic range transient Optional programmable MOSFET protection accurately controls maximum MOSFET power dissipation while MOSFET health algorithms monitor the MOSFET even when fully enhanced. An adjustable overcurrent fault timer avoids false trips during dynamic transient overload events while maintaining robust protection from real overload conditions.

For monitoring, the RTQ1954 measures real-time power, voltage, current, temperature and fault data, and transmits this information via an I²C/SMBus interface with PMBus compliant command structure. Precision telemetry enables intelligent power management functions, power optimization and early fault detection. The RTQ1954 also improves system diagnostics with adjustable telemetry averaging and peak power measurement.

The RTQ1954 is available in the TSSOP-28 (Exposed Pad) package. The recommended junction temperature range is -40°C to 125°C.

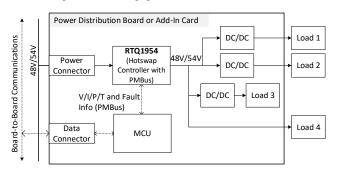
3 Features

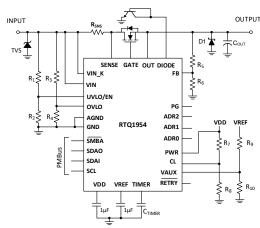
- VIN: 10V to 80V (100V AMR)
- VIN to VIN K: ±60V AMR
- OUT: -5V to 100V AMR
- 12-bit 1 kHz ADC Telemetry (-40°C to 125°C)
 - ±0.8% Voltage
 - ±1% Current
 - ±1.8% Power (Energy Monitoring Supported)
- Four levels of Overcurrent Protection
- 10 to 55mV Overcurrent Sense Voltage in 1mV Increments (±1mV Accuracy)
- Programmable MOSFET SOA Protection
- Fast 500ns Response to Short-Circuit
- MOSFET Health Warning/Detection
- Remote Temperature Sensing with Adjustable Warning/Shutdown Thresholds
- PROCHOT Output (VAUX)
- Programable UV, OV Thresholds
- PMBus[™] Compliant Command Structure
- -40°C < T_J < 125°C Operation
- Available in TSSOP-28 (Exposed Pad)

4 Applications

- 48V/54V Servers and Network Equipment
- Datacenter Rack Power Distribution
- Base Station Power Distribution
- PLC Power Management
- Industrial Systems

2 Simplified Application Circuit





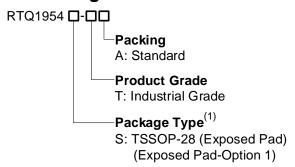
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5 Ordering Information



Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information

RTQ1954 ST YMDAN

RTQ1954ST: Product Code YMDAN: Date Code



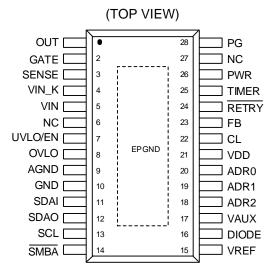
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7 Pin Configuration



TSSOP-28 (Exposed Pad)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	OUT	Output pin. Connect to the power output node. This pin monitors the output voltage and senses the MOSFET VDS voltage for power limiting.
2	GATE	Gate drive output pin. Connect to the external MOSFET gate.
3	SENSE	Current sense input pin. In conjunction with VIN_K, this pin measures the voltage across the current sense resistor (Rsns). If the voltage across RSns exceeds the overcurrent threshold, the load current is limited, and the fault timer activates.
4	VIN_K	Positive supply Kelvin pin. This pin senses the input voltage as well as the current sense voltage (in conjunction with SENSE).
5	VIN	Input power supply. This pin supplies power for the device including the internal VDD regulator. An R-C filter can help reduce noise on this pin (see section Input Voltage and Filtering).
6, 27	NC	No connection.
7	UVLO/EN	Undervoltage-lockout/enable pin. A resistor divider from VIN can set a precision undervoltage-lockout threshold. The pin enable threshold voltage is 2.48V. An internal 20µA current source provides UVLO hysteresis. This pin can also be used for remote shutdown control.
8	OVLO	Overvoltage lockout pin. A resistor divider from VIN can set a precision overvoltage lockout threshold. The pin disable threshold voltage is 2.46V. An internal 20µA current source provides OVLO hysteresis.
9	AGND	Analog device ground. Connect to GND at the pin.
10	GND	Device ground.
11	SDAI	SMBus Data Input pin. Connect to SDAO if the application does not need unidirectional isolation.
12	SDAO	SMBus Data Output pin. Connect to SDAI if the application does not need unidirectional isolation.
13	SCL	SMBus Clock pin.
14	SMBA/FLT	SMBus alert pin. Active low or FLT# open-drain output.

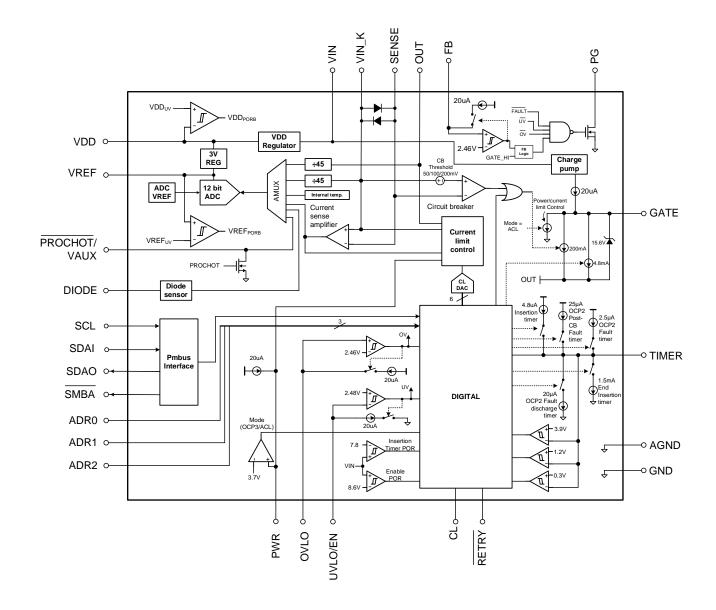
RTQ1954_DS-00



Pin No.	Pin Name	Pin Function
15	VREF	Internal sub-regulator output pin. This internally sub-regulated 3V bias supply requires an external $1\mu F$ capacitor to ground for bypassing. Do not connect to GND during start-up.
16	DIODE	External temperature diode pin. Connect this pin to a diode-configured MMBT3904 NPN transistor for temperature monitoring.
17	VAUX	Auxiliary voltage input pin. The internal telemetry system can measure the voltage on this pin from an external source with a full-scale input of 3V. This pin can be set as PROCHOT using PMBus. Alternatively, this pin can be used to set overcurrent protection (OCP2) threshold.
18	ADR2	SMBUS address line 2. Tri-state address line. Should be connected to GND, VDD, or left floating.
19	ADR1	SMBUS address line 1. Tri-state address line. Should be connected to GND, VDD, or left floating.
20	ADR0	SMBUS address line 0. Tri-state address line. Should be connected to GND, VDD, or left floating.
21	VDD	Internal sub-regulator output pin. This internally sub-regulated 4.9V bias supply requires an external $1\mu F$ capacitor to ground for bypassing.
22	CL	Overcurrent protection pin. Connect this pin to GND or leave floating to set the nominal overcurrent threshold OCP2 at 50 mV. Connecting CL to VDD sets the overcurrent threshold OCP2 at 26mV. Connect CL to a voltage between 2V and 3.9V to set the OCP2 threshold according to the VAUX pin voltage. The threshold can also be adjusted digitally.
23	FB	Power Good feedback pin. An external resistor divider from the output sets the PG output voltage level. The pin threshold is nominally 2.46 V. An internal 20- μ A current source provides hysteresis.
24	RETRY	Fault retry input pin. When this pin is connected to GND or left floating, the device will continually try to restore power after a fault. If the pin is connected to VDD, the device will latch off after a fault event. Connecting this pin to VREF will retry 8 times and then latch off.
25	TIMER	Timer capacitor pin. An external capacitor connected to this pin sets the insertion time delay (power-on delay), OCP2 fault timeout period, and restart timing.
26	PWR	Mode selection pin. An external resistor (RPWR) connected from this pin to GND sets the mode as Active Current/Power Limit (ACL) mode. The RPWR in conjunction with RsNs sets the maximum power dissipation allowed in the external MOSFET. Pulling up the PWR pin to VDD sets the mode to overcurrent protection, OCP3.
28	PG	Power Good open-drain output pin. This output assumes a high-impedance state when the FB pin voltage exceeds the FB threshold (nominally 2.46 V) and the input voltage is within its undervoltage and overvoltage thresholds and GATE-OUT > 9V.
EPGND	Exposed Pad	Exposed pad of the package. Must be soldered to a large ground plane for best thermal performance.



9 Functional Block Diagram





10 Absolute Maximum Ratings

(Note 2)

$\bullet \ \ VIN, \ VIN_K, \ GATE, \ UVLO/EN, \ SENSE, \ PG \ to \ GND$	-0.3V to 100V
• VIN to VIN_K	-60V to 60V
• VIN_K to SENSE	-1V to 1V
• AGND to GND	-0.3V to $0.3V$
• OVLO, FB, TIMER, PWR to GND	-0.3V to 7V
• OUT to GND	-5V to 100V
• SCL, SDAI, SDAO, CL, ADR0, ADR1, ADR2, VDD, VAUX, DIODE, RETRY to GND	-0.3V to 5.5V
• Junction Temperature, TJ	150°C
• Storage Temperature Range, Tstg	–65°C to 150°C

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability. The GATE pin voltage is typically 13.6V above VIN when the RTQ1954 is enabled. Therefore, the Absolute Maximum Rating for VIN applies only when the RTQ1954 is disabled, or for a momentary surge to that voltage because the Absolute Maximum Rating for the GATE pin is also 100V.

11 ESD Ratings

(Note 3)

ESD Susceptibility

HBM (Human Body Model)-----
±2KV

CDM (Charged Device Model) ----- ±500V

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

• Supply Input Voltage, VIN------ 10V to 80V

• Junction Temperature Range, TJ ----- -40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.



13 Thermal Characteristics

(Note 5 and Note 6)

	Thermal Parameter	TSSOP-28 (Exposed Pad)	Unit
θ JA	Junction-to-ambient thermal resistance	31.6	°C/W
θ JC(Top)	Junction-to-case (top) thermal resistance	18	°C/W
θ JC(Bottom)	Junction-to-case (bottom) thermal resistance	2.2	°C/W
θЈВ	Junction-to-board thermal resistance	13.3	°C/W
ΨJC(Top)	Junction-to-case (top) characterization parameter	0.3	°C/W
ΨJC(Bottom)	Junction-to-case (bottom) characterization parameter	1.7	°C/W
ΨЈВ	Junction-to-board characterization parameter	12.4	°C/W

Note 5. For more information about the thermal parameters, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. θ_{JA} , Ψ_{JC} , and Ψ_{JB} are simulated based on JEDEC 51-7 on a high effective-thermal-conductivity four-layer (2s2p) test board at 25°C and still air; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

(Unless otherwise stated, the following conditions apply: VIN = 48 V, -40°C < TJ < 125°C, V_{UVLO} = 3 V, V_{OVLO} = 0 V, R_{PWR} = 20kΩ. (Note 7))

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Input Supply (VIN)							
VIN POR Threshold to Trigger Insertion Timer	VIN _{POR_IT}	VIN Increasing	1	7.8	9	V	
VIN POR Threshold to Enable All Functions	VINPOR_EN	VIN Increasing	I	8.6	9.9	V	
VIN POR Enable Hysteresis	VINPOR_EN_H YS	VIN Decreasing		100		mV	
Input Current, Enabled	lin_en	V _{UVLO} = 3V, V _{OVLO} = 2V (active)	3	5	7	mA	
VIN_K							
VIN_K Bias Current	IVIN_K			330	600	μА	
VDD Regulator (VDD Pin)							
VDD Voltage	V _{DD}	I _{VDD} = 0mA	4.6	4.9	5.15	V	
VDD Voltage		I _{VDD} = 10mA	4.6	4.9	5.15	V	
VDD Current Limit	VDD_ILIM		-50	-30	-15	mA	
VDD Voltage Reset Threshold	V _{DD_POR}	VDD Rising		4.1		V	
UVLO/EN and OVLO (Pins)							
UVLO Threshold	VUVLO_L	Falling (low) threshold	2.41	2.48	2.55	V	
UVLO Hysteresis Current	luvlo_HYS	Vuvlo = 1V	16	20	24	μА	
UVLO Bias Current	IUVLO_BIAS	Vuvlo = 3V		0	1	μА	



Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
OVLO Threshold	Vovlo-H	Rising (high) threshold	2.39	2.46	2.53	V
OVLO Hysteresis Current	lovlo_HYS	Vovlo = 3V	-24	-20	-16	μА
OVLO Bias Current	IOVLO_BIAS	V _{OVLO} = 1V		0	1	μА
Power Good (PG)						
Output Low Voltage	VPG_L	ISINK = 2mA		200	400	mV
Off Leakage Current	VPG_ILK	Vpg = 80V		0	1	μА
FB		1	ı			
FB Threshold	VFB		2.41	2.46	2.52	V
FB Hysteresis Current	VFB_HYS	High threshold	-25	-20	-15	μА
Off Leakage Current	VFB_ILK	V _{FB} = 2.3V		0	1	μА
GATE Control	1	1	Į.		I	I
Source Current		Normal Operation	-25	-20	-15	μА
Fault Sink Current		VuvLo = 2V	4	4.8	5.5	mA
POR Circuit Breaker Sink Current	IGATE	VVIN_K - VSENSE = 60mV or VIN < VINPOR_IT, VGATE = 5V, OUT = 0V, CB/CL ratio bit = 0, CL = VDD	90	200	350	mA
Active CL Sink Current		VVIN_K - VSENSE = VCL+25mV, VGATE = 5V, OUT = 0V (Mode = ACL)	0.1	0.4	0.7	mA
Reverse-Bias Voltage of GATE to OUT	VGATEZ	VGATE – VOUT, IZ = –100μA	12	15.6	18	V
Peak charge pump voltage in normal operation (VIN = VOUT)	VGATECP	VGATE – VOUT	11	13	15	V
OUT						
OUT Bias Current, Enabled	IOUT-EN	VIN = VOUT, Normal Operation	55	80	100	μА
OUT Bias Current, Disabled	lout-dis	Vout = 0V, Vvin_k = Vsense, Ven/uvlo = 2V	-2.5	0	2.5	μА
Overcurrent Protection (O	CP) and Active	Current Limit (ACL)				
Overcurrent Protection Threshold Voltage, OCP1, VVIN_K – VSENSE	VOCP1	During start-up, disabled after PG goes high	1.5	2	2.5	mV
		CL = VDD	24.7	26	27.3	
Overcurrent Protection	\\\-\-\-\-\-\-\-\-\-\-\-\-\-\-\-\-\-\-	CL = GND	47.5	50	52.5	
Threshold Voltage, OCP2, VVIN_K – VSENSE	VOCP2	CL = 3V, VAUX = 0.057V	35.2	37	38.9	mV
		CL = 3V, VAUX = 2.74V	46.6	49	51.5	
CL Upper Threshold	VCL-H	OCP2 set based on VAUX		3.9		V
CL Lower Threshold	VCL-L	OCP2 set based on VAUX		2		V
VAUX Step Resolution		2V ≤ CL ≤ 3.9V		±114		mV
<u> </u>			J	1	l	l

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Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
PMBus Overcurrent		Min Threshold	9.5	10	10.5	mV
Protection, OCP2,	VOCP2	Max Threshold	52.25	55	57.75	mV
Threshold		DAC step resolution		1		mV
Overcurrent Protection		PWR=VDD (Mode = OCP3), CL = VDD	37.5	41	46	
Threshold Voltage, OCP3, VVIN_K - VSENSE	VOCP3	PWR=VDD (Mode = OCP3), CL = GND	63.1	66	71.7	mV
Overcurrent Protection Level -	Via	PWR = $2K\Omega$ to GND (Mode = ACL), CL = VDD	37.8	41	45.6	\/
Active Current Limit (ACL), VVIN_K – VSENSE	VacL	PWR = $2K\Omega$ to GND (Mode = ACL), CL = GND	63.1	66	71.7	mV
PWR Comparator Voltage Threshold	VPWR_CMP	To Switch between OCP3 and ACL modes	3.5	3.7	4.1	V
		Enabled, SENSE = OUT		0	1	
SENSE Input Current	ISENSE	Disabled, OUT = 0V		0	1	μΑ
		Enabled, OUT = 0V		0	1	1
CL Pin Input Leakage Current		CL = VDD		5		μА
Protection Mode: Active C	Current/Power L	Limit (ACL)				
	VPL	VIN = 48V, Vout = 0V, Rpwr = 60K	21.8	26.1	30.3	mV
		VIN = 48V, Vout = 0V, Rpwr = 20K	15.2	18.9	22.7	
Power Limit Sense Voltage, VVIN K – VSENSE		VIN = 48V, Vout = 24V, RPWR = 60K	32.3	38	43.7	
VVIII_K - VSENSE		VIN = 48V, Vout = 24V, RPWR = 20K	19.5	23.6	27.7	
		VIN = 48V, Vout = 0V, Rpwr = 100K	28.6	33.5	38.4	
PWR Pin Current	Ipwr	Vpwr = 2.5V		-20		μΑ
F WIN FIII Guileilt	IPWK	Vpwr = VDD		3		μΑ
Maximum RPWR	RPWR_MAX				100	ΚΩ
Circuit Breaker						
		CB/CL ratio bit = 0, Vocp2 ≥ 33mV	81	100	111	mV
Circuit Breaker Threshold	VCB	CB/CL ratio bit = 1, Vocp2 ≥ 33mV	160	200	230	mV
Voltage, Vvin_k – Vsense	VCB	CB/CL ratio bit = 0, Vocp2 ≤ 32mV	38	50	58	mV
		CB/CL ratio bit = 1, V _{OCP2} ≤ 32mV	80	100	112	mV



Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
TIMER (Pin)						
Upper Threshold	VTMRH		3.74	3.9	4.07	V
		Restart cycles	1	1.2	1.4	
Lower Threshold	VTMRL	End of eight cycle re-enabled threshold		0.3		V
Insertion Time Current			-5.9	-4.8	-3.3	μΑ
Sink Current, End of Insertion Time			0.9	1.5	2.1	mA
Fault Detection Current	ITIMER	VTIMER = 2V	-3.2	-2.5	-1.7	μΑ
Fault Sink Current after CB	DCFAULT	VIIMER - ZV	-32	-25	-17	μА
Fault Sink Current			14	20	26	μΑ
Fault Restart Duty Cycle				15		%
Internal Reference						
Reference Voltage	VREF		2.91	3	3.09	V
ADC and MUX						
Resolution				12		Bits
Integral Non-Linearity	INL	ADC only		±0.5		LSB
Oscillator Accuracy	fosc			±5		%
Acquisition + Conversion Time	tacquire	Any channel		129		μS
Acquisition Round Robin Time (Note 8)	trr	Cycle all channels		1.048		ms
Telemetry						
Current Input Full-Scale	IINFSR	Vocp2 ≥ 33mV	58.5	60	61.5	mV
Range	IINFOR	V _{OCP2} ≤ 32mV	26	27	29	mV
Current Input LSB	IINLSB	Vocp2 ≥ 33mV		14.7		μV
VAUX Input Full Scale		Vocp2 ≤ 32mV		6.6		μV
Range	VAUXFSR		2.93	2.97	3.01	V
VAUX Input LSB	VAUXLSB			7.139		mV
Input Voltage Full Scale Range	VINFSR		86	88.9	91	V
Input Voltage LSB	VINLSB			21.7		mV
Output Voltage Full-Scale Range	Voutesr		86	88.9	91	V
Output Voltage LSB	Voutlsb			21.7		mV



Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
		VIN, Vout = 80V	-0.8		0.8	%
VIN, VOUT Absolute Accuracy		VIN, Vout = 48V	-0.8		0.8	
,,	\/	VIN, V _{OUT} = 10V	-2.5		2.5	
VAUX Absolute Accuracy	VACC	VAUX = 2.8V	-0.8		0.8	
		VAUX = 1. 5V	-0.8		0.8	%
		VAUX = 0.75V	-0.8		0.8	
		VVIN_K - VSENSE = 22mV (81% INFSR), CL = VDD	-1		1	
		VVIN_K - VSENSE = 22mV (81% INFSR), CL = VDD -40°C < TJ < 85°C	-0.8		0.8	
		VVIN_K - VSENSE = 5mV (19% INFSR), CL = VDD	-5		5	
Input Current Absolute Accuracy	INACC	VVIN_K - VSENSE = 44mV (73% INFSR), CL = GND	-1		1	%
		VVIN_K - VSENSE = 44mV (73% IINFSR), CL = GND -40°C < TJ < 85°C	-0.8		0.8	
		VVIN_K - VSENSE = 25mV (42% INFSR), CL = GND	-1		1	
		VVIN_K - VSENSE = 9.5mV (16% INFSR), CL = GND	-5		5	
	PINACC	VVIN_K - VSENSE = 22mV (81% IINFSR), CL = VDD	-1.8		1.8	%
		VVIN_K - VSENSE = 22mV (81% IINFSR), CL = VDD -40°C < TJ < 85°C	-1.5		1.5	
		VVIN_K - VSENSE = 5mV (19% INFSR), CL = VDD	-5		5	
Input Power Accuracy		VVIN_K - VSENSE = 44mV (73% INFSR), CL = GND	-1.8		1.8	
		VVIN_K - VSENSE = 44mV (73% IINFSR), CL = GND -40°C < TJ < 85°C	-1.5		1.5	
		VVIN_K - VSENSE = 25mV (42% INFSR), CL = GND	-1.8		1.8	
		V _{VIN_K} - V _{SENSE} = 9.5mV (16% I _{INFSR}), CL = GND	-5		5	
Temperature Sense						
On Chip Temperature Accuracy	- TJACC	T _J = -40°C to 125°C	-8		8	°C
On Chip Temperature Resolution	TJACC			12		bits
Temperature Accuracy Using Remote Diode	- TACC	TA = 25°C to 85°C	-8		8	°C
Remote Diode Resolution	-			12		bits



Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
		High Level	-200	-160	-	
Remote Diode Current Source	IDIODE	Mid Level		-60		μА
		Low Level		-10		
Remote Diode Current	Invent on	High level to low level ratio	13.6	16	17.6	
Ratio	IDIODE_CR	High level to mid level ratio	2.14	2.67	3.2	μΑ/μΑ
Max Series Resistance with Remote Diode					300	Ω
PMBus Pin Thresholds (S	CL, SDA, SMB	A)				
Data, Clock Input Low Voltage	VIL	SCL, SDAI			0.8	V
Data, Clock Input High Voltage	VIH	SCL, SDAI	1.35		5.5	V
Data Output Low Voltage	VoL	SDAO, ISINK = 3mA	0		0.4	V
Input Leakage Current	ILEAK	SDAI, SMBA, SCL = 5V		0	1	μА
PROCHOT Output (If VAU	X is not used to	set OCP2)				
Output Low Voltage	VPROCHOT_LV	ISINK = 2mA		100	400	mV
Off Leakage Current	IPROCHOT_LK			0	1	μА
Configuration Pin Thresholds (RETRY)						
High Threshold Voltage	VIH		3.6	3.9	4.1	V
Low Threshold Voltage	VIL		1.7	2	2.2	V
Input Leakage Current	ILEAK	RETRY = 5V		5		μА

Note 7. Guaranteed by design.

Note 8. The sampling time increment is $t_{ACQUIRE} \times N$, where N is the number of active telemetry features (VIN, V_{OUT} , I_{IN} , TEMP_INTERNAL). If the TEMP_EXTERNAL telemetry is active, the sampling time increment is 1.048ms.



14.1 **SMBus Communications Timing Requirements and Definitions**

Parameter	Symbol	Min	Тур	Max	Unit
SMBus Operating Frequency	fsmb	10		1000	kHz
Bus Free Time Between Stop and Start Condition	tBUF	0.5			μS
Hold Time After (repeated) Start Condition. After this period, the first clock is generated.	tHD:STA	0.26			μS
Repeated Start Condition Setup Time	tsu:sta	0.26			μS
Stop Condition Setup Time	tsu:sto	0.26			μS
Data Hold Time (Note 9)	thd:dat	85			ns
Data Setup Time	tsu:dat	50			ns
Detect Clock Low Timeout (Note 10)	tтімеоит	25		35	ms
Clock Low Period	tLOW	0.5			μS
Clock High Period (Note 11)	thigh	0.26			μS
Cumulative Clock Low Extended Time (Slave Device) (Note 12)	tLOW:SEXT			25	ms
Cumulative Low Extend Time (Master Device) (Note 13)	tLOW:MEXT			10	ms
Clock/Data Fall Time (Note 14)	tR	20		120	ns
Clock/Data Rise Time	tF	20		120	ns

- Note 9. The device must internally provide sufficient hold time for the SDA signal (with respect to the V_{IH,MIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- Note 10. Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of t_{TIMEOUT.MIN} of 25ms. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than t_{TIMFOUT MAX} of 35ms.
- Note 11. tHIGH.MAX provides a simple guaranteed method for masters to detect bus idle conditions.
- Note 12. t_{LOW:SEXT} is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial START to the STOP.
- Note 13. tLOW:MEXT is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from START-to-ACK, ACK-to-ACK, or ACK-to-STOP.
- Note 14. Rise and fall times are defined as follows:

 $t_R = (V_{IL,MAX} - 0.15V)$ to $(V_{IH,MIN} + 0.15V)$, $t_F = (V_{IH,MIN} + 0.15V)$ to $(V_{IL,MAX} - 0.15V)$

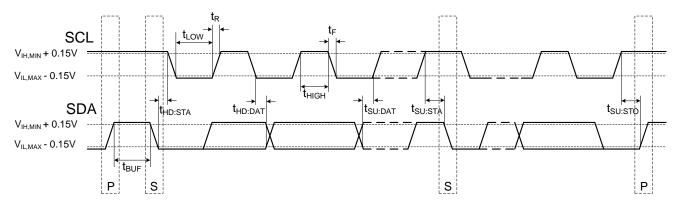


Figure 1. SMBus Timing Diagram

RTQ1954 DS-00



14.2 **Switching Characteristics**

(Unless otherwise stated, the following conditions apply: $V_{IN} = 48V$, $-40^{\circ}C < TJ < 125^{\circ}C$, $V_{UVLO} = 3$ V, $V_{OVLO} = 0$ V, $R_{PWR} = 100$ $20k\Omega$.)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
LIVI O Dolov	tun# 0 DEI	Delay to GATE high	7	10.7	12.7	
UVLO Delay	tuvlo_del	Delay to GATE low	5.5	9	11.5	μS
OVI O Delev	to	Delay to GATE high	7	10.7	12.7	_
OVLO Delay	tovlo_del	Delay to GATE low	5.5	9.3	11.5	μS
FB Delay	tFB DEL	Delay to PG high (FB and GATE_HI TRUE)	70	110	160	μS
	_	Delay to PG low	7	11.5	13.5	•
Circuit Breaker Response Time	tcB	VIN_K-SENSE stepped from 0 to 150mV, time to GATE-OUT<2V, no load, CB threshold=50mV		0.35	0.5	μS
Fault to GATE Low Delay	tFAULT_DEL	TIMER pin reaches the upper threshold	ı	2	4	μS
OCP1 Response Time	tocp1	Time from VIN_K-SENSE = 2mV to GATE starts to pull down, start-up or restart only	1	10		μS
OCP3/ACL Blanking Time	tblank	Mode = OCP3 or ACL	300	500	700	μS
ACL Max Regulation Time	tACL	Mode = ACL	480	530	576	μS



15 Typical Application Circuit

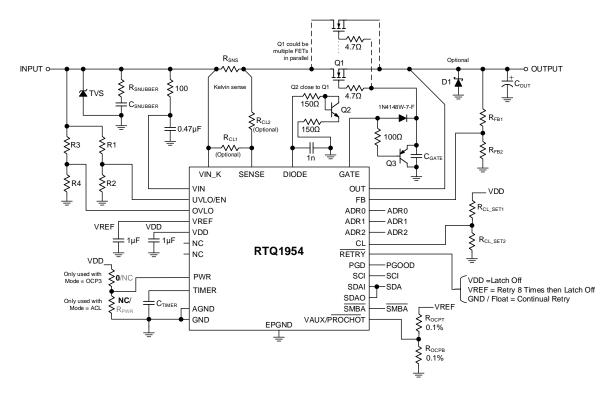
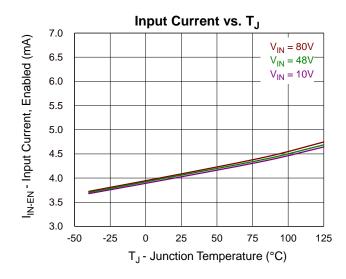


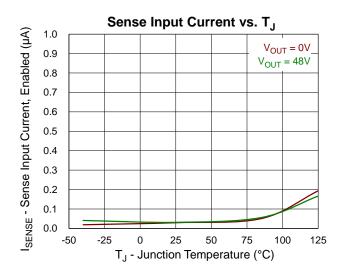
Figure 2. Typical Application Circuit in OCP Mode

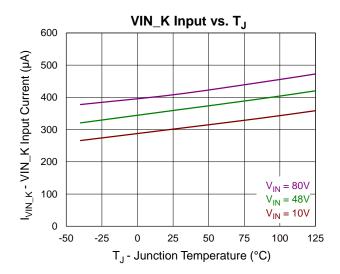


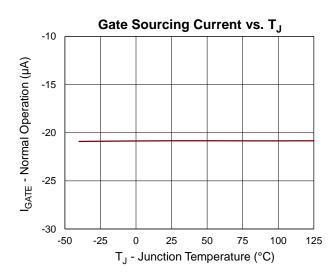
16 Typical Characteristics Curves

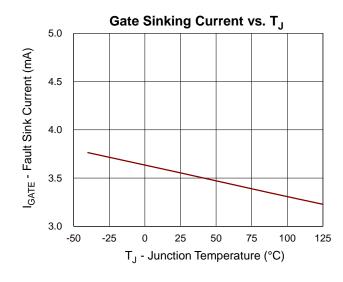
Unless otherwise stated, the following conditions apply: VIN = 48V, T_J = 25°C.

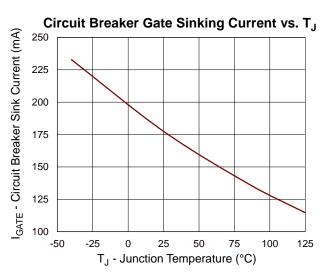










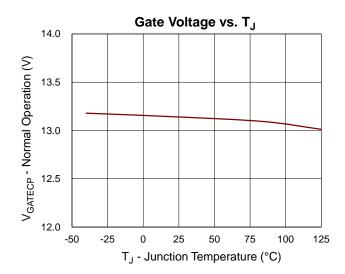


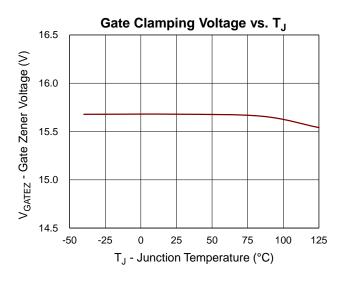
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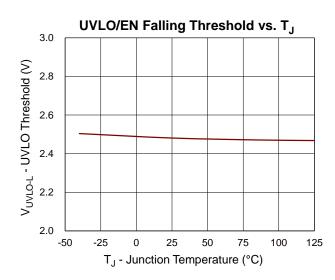
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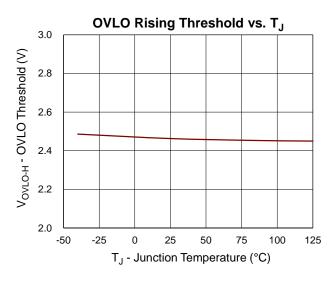
RTQ1954 DS-00

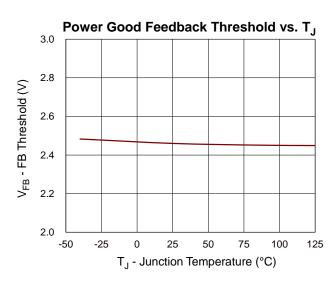


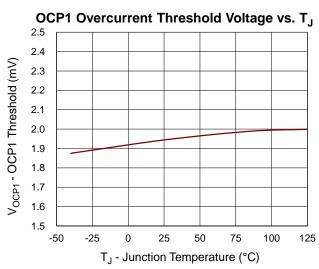




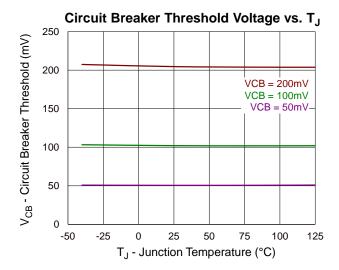


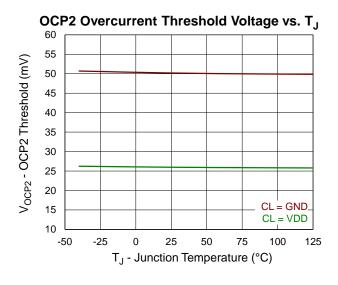


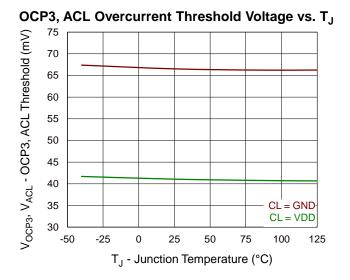


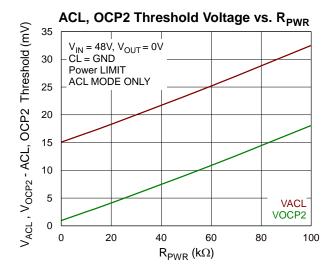














17 Application Information

(Note 15)

17.1 Overview

The RTQ1954 inline power protection controls inrush current when inserting an add-in-card or circuit card into a live (so called "hot") backplane power source. The controlled inrush current prevents voltage sagging on the backplane supply voltage and high dV/dt surge on the load. The RTQ1954 provides multi-level Over-Current Protection (OCP) features. During start-up, the RTQ1954 quickly detects overcurrent (OCP1, 2mV sense voltage typical) and disconnects the power flow. Similarly, when removing an add-in-card from a source, a controlled shutdown is implemented to prevent flash arc and possible damage.

In addition to a controlled hot swapping in/out of a power source and a dedicated start-up over-current protection level, the RTQ1954 provides three additional levels of fast and accurate protection to a variety of overload transients during operation. A high-resolution overcurrent protection (OCP2) with sense voltage programmability of 10mV to 55mV provides first-level fault/overcurrent protection along with a hardware adjustable fault timer. The timer is designed to avoid "fault accumulation" and false trips common with dynamic transient, but normal, overload events. The next level of protection, OCP3 (15mV higher sense voltage than OCP2, typical) has a fixed 0.5ms blanking timer to ensure fast unpredictable, but normal, overloads pass through without tripping a fault.

Some systems may benefit from an active current limit (ACL) in addition to overcurrent protection (OCP). ACL differs from OCP functionality by servoing the GATE pin in an attempt to control the system current using feedback. For example, if several hot swap power domains share a common power supply, active current limit can be used to ensure that no single domain consumes more than its share of current. For these systems, the RTQ1954 provides optional hardware adjustable active current/power limit (ACL). Using the same sense voltage as OCP3 (15mV higher than OCP2) and fixed 0.5ms blanking with an additional fixed 0.5ms timer, ACL mode actively monitors and controls current and maximum power dissipation in the MOSFET.

Finally, both OCP and ACL modes implement the same circuit-breaker response in the case of severe overcurrent events. The RTQ1954 has a sub-us response time to short circuit faults that exceed an adjustable circuit-breaker sense voltage threshold to ensure the external series-pass MOSFET will not get damaged.

If the RTQ1954 shuts down the series-pass MOSFET due to a fault, the state of the RETRY pin determines whether the system attempts to restart, and if so, the number of retries.

System software can initiate a system shutdown and restart using the PMBus smart reboot command with a programmable VOUT discharge voltage and reboot time of up to 65s.

Along with protection, the RTQ1954 provides accurate and precise real-time monitoring of power, voltage, current, temperature, and fault data which is transmitted via an I²C/SMBus interface with PMBus compliant command structure. Precision telemetry enables intelligent power management functions (e.g. Intel PROCHOT output), power optimization and early fault detection. The RTQ1954 also improves system diagnostics with adjustable telemetry averaging and peak power measurement. Remote temperature sensing with adjustable warning/shutdown thresholds provides additional protection and monitoring for the most critical systems.

Additional features include MOSFET health warning and detection algorithms which monitor the MOSFET even when fully enhanced. Programmable undervoltage lockout (UVLO) and overvoltage lockout (OVLO) shuts down the RTQ1954 when the input voltage is outside the normal operating region.

Input Voltage and Filtering 17.2

The RTQ1954 draws power from VIN, and this pin can be filtered from the primary input supply using an R-C network as shown in Typical Application Circuit. A time constant of several tens of microseconds should be



sufficient. While the Absolute Maximum Rating (AMR) of the difference between VIN and VIN K is ±60V, the differential voltage should be temporary. This is the case when first applying power to VIN K and VIN through the R-C filter or when a fault occurs resulting in an inductive spike on VIN_K while VIN remains filtered. However, the internal RTQ1954 charge pump is connected to VIN, so VGS of the external MOSFET will be reduced by (VIN K - VIN). Therefore, it is important that the differences between VIN and VIN K are transient and kept under ±1V during normal operation.

17.3 **Current Sense Inputs**

The RTQ1954 measures the load current by sensing the voltage across the external current sense resistor Rsns (VVIN K - VSENSE). To avoid instability in current loop control, it is recommended that the RSNS value be no higher than 200mΩ. For designs that require multiple sense resistors in parallel, care must be taken on the layout and connection of these resistors to minimize the effect of imbalance.

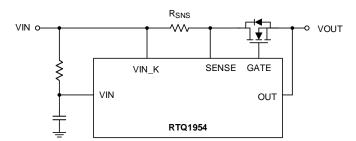


Figure 3. Connection of Sense Resistor to Hot Swap Controller

Overcurrent Protection 17.4

The RTQ1954 provides four levels of fast and accurate protection against a variety of overcurrent loads as follows:

- Start-up protection, OCP1: protects against unexpected and excessive inrush currents with VocP1 (2mV typical) sense voltage threshold.
- Normal operation, OCP2: hardware and PMBus adjustable sense voltage, Vocp2, of 10mV to 55mV with hardware adjustable non-accumulative fault TIMER. OCP2 is intended to be set above the highest expected steady-state load. OCP2 protects against soft shorts or unexpected overloads resulting in over-current for longer than expected transient overload conditions.
- Normal operation, OCP3: Vocp3 sense voltage is fixed 15mV (typical) above Vocp2 with a 0.5ms blanking timer. OCP3 allows even higher expected but unpredictable short overload pulses, while still protecting the system if the overload condition exceeds tBLANK (typically 0.5ms).
 - Optional hardware selectable active current/power limit (ACL) mode limits the current/power in the external MOSFET if the sense voltage exceeds VACL (VOCP2 + 15mV typical).
- Circuit breaker, CB: with sub-us response to extreme overcurrent events (sense voltage exceeding adjustable V_{CB}), circuit breaker is the RTQ1954's ultimate protection against severe fault conditions.

17.4.1 Start-up Protection, OCP1:

RTQ1954 DS-00

During the start-up if the voltage across the Rsns resistor (VVIN_K - VSENSE) exceeds VOCP1 (2mV typical), the RTQ1954 turns off the external MOSFET within 10µs (tocp1) using a 4.8mA GATE pulldown current, and the part enters into RETRY mode. In addition, the IIN_OC_Fault bit in the STATUS_INPUT (7Ch) register and the INPUT_STATUS bit in the STATUS_WORD (79h) register are toggled high and the SMBA pin is asserted, unless this feature is disabled using the ALERT_MASK (D8h) register. OCP1 is active following initial power up or

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following any RETRY event. These scenarios can be identified by observing PG is low. OCP1 deactivates following a successful start-up as indicated by PG transitioning high. All system loads should be gated by PG, and start-up inrush current should be set to less than the locp1 threshold to avoid tripping OCP1 during a normal start-up.

$$I_{\text{INRUSH}} < I_{\text{OCP1}} = \frac{2\text{mV}}{R_{\text{SNS}}}$$

$$I_{INRUSH} = C_{OUT} \times \frac{dV_{OUT}}{dt}$$

where dVout/dt is determined by CGATE (See <u>Typical Application Circuit</u>) and the RTQ1954 GATE pin source current (20uA typical). It is important to consider variations in COUT, CGATE and the GATE pin source current when calculating the worst-case inrush current.

17.4.2 Steady State Protection, OCP2:

After power-up, the RTQ1954 actively measures the load current by monitoring the voltage across Rsns. If the voltage across Rsns exceeds the OCP2 threshold (VoCP2), the fault timer is activated and charges CTIMER with 2.5μA as described in the Fault Timer section. If the current drops below the loCP2 threshold before the fault timer reaches the fault timeout period, toCP2, set by CTIMER (TIMER pin reaches 3.9V), the RTQ1954 resumes normal operation and CTIMER is discharged using 20μA. Otherwise, the RTQ1954 turns off the external MOSFET with a 4.8mA GATE pulldown and discharges CTIMER using 20μA. The IIN_OC_Fault bit in the STATUS_INPUT (7Ch) register and the INPUT_STATUS bit in the STATUS_WORD (79h) register are toggled high, PGD will deassert and SMBA pin will be asserted, and RTQ1954 moves to the RETRY phase. SMBA alert can be disabled using the ALERT_MASK (D8h) register. The toCP2 fault timer is set according to the following equation:

$$t_{OCP2} = C_{TIMER} \times \frac{3.9V}{2.5\mu A}$$

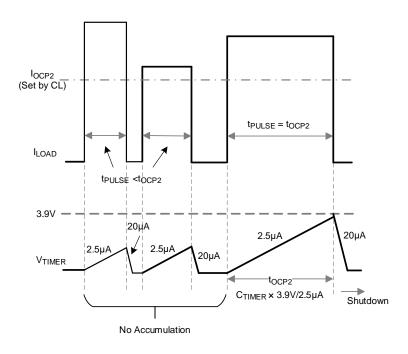


Figure 4. OCP2 Protection Behavior



The RTQ1954's 2.5μA/20μA charge/discharge current ratio (1:8) of the TIMER pin allows for a variety of wide and unpredictable overcurrent scenarios without VTIMER accumulation causing false fault tripping.

The RTQ1954 provides flexibility to set the OCP2 threshold voltage using both hardware setting and PMBus. The Vocp2 can be set by the CL pin (26mV if CL=VDD, 50mV if CL=GND, and based on the VAUX pin voltage if 2 ≤ CL ≤ 3.9) or overridden by setting relevant bits in the DEVICE_SETUP (D9h) and MFR_CL_THRESHOLD (F0h) registers (10 to 55mV with 1mV increments).

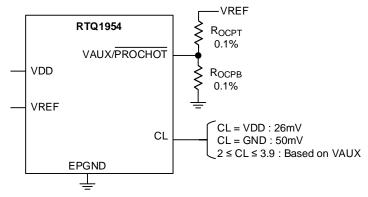


Figure 5. Connection of CL and VAUX Pins to set OCP2 Threshold

ROCPT (kΩ)	ROCPB (kΩ)	VAUX Voltage (V) (±114mV)	OCP2 Threshold (mV)
9.42	100	2.74	49
19.3	100	2.513	48
31.2	100	2.2845	47
45.9	100	2.056	46
64.2	100	1.8275	45
87.6	100	1.599	44
118	100	1.3705	43
162	100	1.1425	42
229	100	0.914	41
336	100	0.6855	40
556	100	0.457	39
1210	100	0.2285	38
5170	100	0.057 (GND)	37

17.4.3 Steady State Protection, OCP3:

The RTQ1954 provides another level of protection above OCP2 designed to pass through short high-current pulses avoiding undesired fault tripping. The IOCP3 threshold is set as

$$I_{OCP3} = I_{OCP2} + \frac{15mV}{R_{SNS}}$$

RTQ1954 DS-00

If the voltage across Rsns exceeds the OCP3 threshold (internally fixed at 15mV+VocP2), the RTQ1954 activates the blanking timer of 0.5ms (tBLANK). If the current in the MOSFET drops below IOCP3 before the blanking timer expires, the RTQ1954 resumes normal operation ensuring unpredictable short pulses pass through without tripping a fault. Otherwise, the RTQ1954 turns off the external MOSFET using a 4.8mA GATE pulldown current, and the IIN_OC_Fault bit in the STATUS_INPUT (7Ch) register and the INPUT_STATUS bit in the STATUS_WORD (79h) register are toggled high, PG will be deasserted, the SMBA pin will be asserted and the

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RTQ1954 moves to the RETRY phase. SMBA alert can be disabled using the ALERT MASK (D8h) register. This mode is activated by pulling up the PWR pin to VDD.

In scenarios where excessive load current can cause voltage sagging at the input bus and/or excessive power dissipation in the load that may violate the external MOSFET SOA limits, the RTQ1954 provides a hardware selectable option to select Active Current/Power (ACL) mode as described in the next section.

17.4.4 Steady State Protection, Active Current/Power Limit (ACL) Mode:

If the PWR pin is connected to GND through RPWR resistor, the RTQ1954 sets the protection mode as Active Current/Power (ACL) mode. In this mode, when the voltage across Rsns exceeds the VACL threshold (15mV + VOCP2), the RTQ1954 activates the blanking timer of 0.5ms (tBLANK). If the current in the MOSFET drops below IACL before the blanking timer expires, the RTQ1954 resumes normal operation. Otherwise, the RTQ1954 enters the ACL mode by actively regulating the external current or the power dissipation in the external MOSFET to the set values by adjusting the GATE pin voltage. The IACL current threshold is set as follows:

$$I_{ACL} = I_{OCP2} + \frac{15mV}{R_{SNS}}$$

The ACL regulation can last up to 0.53ms typical (t_{ACL}). If the current/power limit exists longer than t_{ACL}, the RTQ1954 turns off the external MOSFET using a 4.8mA pulldown current, and IIN_OC_Fault bit in the STATUS_INPUT (7Ch) register, the INPUT_STATUS bit in the STATUS_WORD (79h) register, and the IIN_OC/PFET_OP_FAULT bit in the READ_DIAGNOSTIC_WORD (E1h) register is toggled high and the SMBA pin is asserted, unless this feature is disabled using the ALERT_MASK (D8h) register.

In the ACL mode, the RTQ1954 either regulates the current or the power dissipation in the external MOSFET depending on which threshold is reached first. During current limiting, the RTQ1954 controls the GATE voltage to quickly limit the output current to IACL=VACL/RSNs. In fault conditions where Vds is high, such as short circuit, current-limit protection may not be enough and can violate the external MOSFET SOA due to excessive power dissipation. A MOSFET with a higher SOA curve can be chosen to alleviate this issue with the downside of overdesigning the system. The MOSFET SOA curve indicates the amount of power it can dissipate for a given amount of time before the junction temperature reaches its maximum value. The RTQ1954 implements a better solution which is a power limit feature that accurately limits the maximum power dissipation in the external MOSFET. The power dissipation is calculated by multiplying the current in Rsns and the voltage across the MOSFET (VSENSE - VOUT), and comparing with the programmed power limit threshold PLIM set by the PWR pin resistor (RpwR).

$$P_{LIM} = \frac{(R_{PWR} \times 7 \times 10^{-6} + 0.015 \times VDS + 0.043)}{R_{SNS}}$$

When the dissipated power reaches the power limit threshold, the RTQ1954 regulates the GATE voltage to limit the current (and hence the power dissipation) in the MOSFET to the set values.



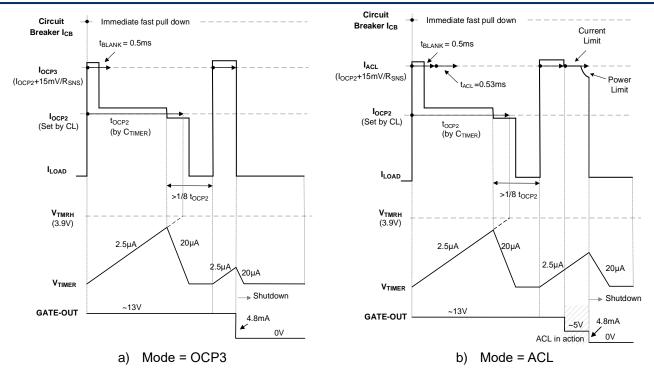


Figure 6. RTQ1954 OCP3 and ACL Protection Mode Behavior

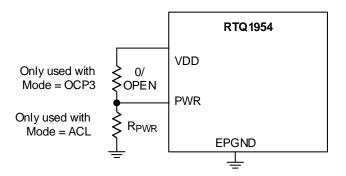


Figure 7. Connection of PWR Pin to Set Mode as OCP3 or ACL

17.4.5 Circuit Breaker

In a scenario such as output short circuit when the current in Rsns exceeds the IOCP2 and IOCP3/IACL thresholds faster than they trip a fault, the RTQ1954 protects the system using a circuit breaker (CB) mechanism. The circuit breaker mechanism is activated when the voltage across Rsns exceeds the threshold set by Vcb. The circuit breaker current is determined by the following equation:

$$I_{CB} = \frac{V_{CB}}{R_{SNS}}$$

In this event the RTQ1954 switches off the MOSFET using a 200mA GATE pull down current. When the voltage across Rsns falls below the VcB threshold, the 200mA current switches off and the GATE voltage starts ramping up to power on the MOSFET. If the fault still exists, the RTQ1954 will turn off the external MOSFET as either of OCP2 or OCP3/ACL triggers the fault. The OCP2 timer pin current is increased to 25µA after a circuit breaker event to quickly turn off the MOSFET and keep it within its SOA. After the timer pin reaches the fault threshold, GATE is shut off. The timer pin pull-up current reverts to 2.5uA in the subsequent cool-down period when auto-

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retry is enabled. A circuit breaker event will deassert PG and causes the CB_ FAULT bit to be toggled high in STATUS_WORD (79h), STATUS_OTHER (7Fh), STATUS_MFR_SPECIFIC (80h) and READ_DIAGNOSTIC_WORD (E1h). SMBA pin is pulled low and the RTQ1954 moves to the RETRY phase. SMBA alert can be disabled using the ALERT_MASK (D8h) register. The circuit breaker threshold can be set by relevant bits in DEVICE_SETUP (D9h) register.

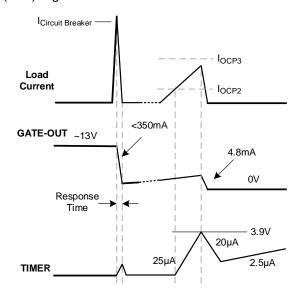


Figure 8. Circuit breaker Mechanism during Normal Operation Short Circuit (Auto-Retry enabled)

17.5 Undervoltage-Lockout (UVLO)

The RTQ1954 enables the external MOSFET when the input voltage (VIN) is within the operating range set by the UVLO and OVLO thresholds. When the voltage at the UVLO pin is less than the UVLO low threshold (VUVLO-L) of 2.48V, the external MOSFET is held off by a 4.8mA pulldown current at the GATE. At this condition, the 20μ A current sink at the UVLO pin is enabled to provide hysteresis. As the voltage at the UVLO pin increases beyond the UVLO threshold of 2.48V plus the hysteresis voltage (determined by the 20μ A sink and external resistor), the 20μ A current sink is disabled and the external MOSFET is turned on using a 20μ A charge pump at the GATE, provided that the insertion time has passed.

After power-up, a UVLO condition causes the INPUT_STATUS bit in the STATUS_WORD (79h) register, the VIN_UV_FAULT bit in the STATUS_BYTE (78h), STATUS_INPUT (7Ch) and READ_DIAGNOSTIC_WORD (E1h) registers to be toggled high and the SMBA pin is pulled low, unless this feature is disabled using the ALERT_MASK (D8h) register.

17.6 Overvoltage-Lockout (OVLO)

When the voltage at the OVLO pin is higher than the OVLO high threshold (VOVLO-H) of 2.46V, the external MOSFET is held off by a 4.8mA GATE pulldown current. At this condition, the 20μ A current source at the OVLO pin is enabled to provide hysteresis. As the voltage at the OVLO pin drops below the OVLO threshold of 2.46V minus hysteresis (determined by the 20μ A current source and external resistor), the external MOSFET is enabled. An OVLO condition toggles the VIN_OV_FAULT bit in the STATUS_INPUT (7Ch) and READ_DIAGNOSTIC_WORD (E1h) registers, and the INPUT_STATUS bit in the STATUS_WORD (79h) register. The $\overline{\text{SMBA}}$ pin is pulled low unless this feature is disabled using the ALERT_MASK (D8h) register.



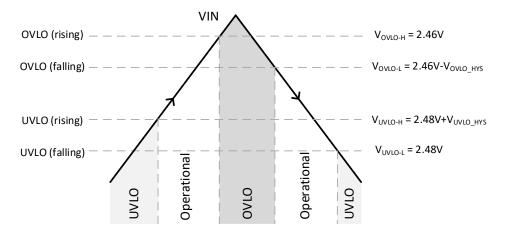


Figure 9. VIN UVLO and OVLO Conditions

Different configurations can be used to set the UVLO and OVLO thresholds using resistive dividers. To accurately set all the VIN OVLO (high and low) and UVLO (high and low) thresholds, it is recommended to use dedicated resistive dividers on UVLO and OVLO pins. However, to reduce the external BOM, the VIN UVLO (high and low) and OVLO (high only) can be set using three-resistor dividers as shown below. In this configuration, the VIN OVLO-L (low) is not set in advance.

$$R_1 = \frac{VIN_{UVLO-H} - VIN_{UVLO-L}}{20\mu A}$$

$$R_3 = \frac{R_1 \times VIN_{UVLO-L} \times 2.46V}{VIN_{OVLO-H} \times (VIN_{UVLO-L} - 2.48V)}$$

$$R_2 = \frac{2.48V \times R_1}{VIN_{UVLO-L} - 2.48V} - R_3$$

$$VIN_{OVLO-L} = \left(\frac{2.46V}{R_3} - 20\mu A\right) \times (R_1 + R_2) + 2.46V$$

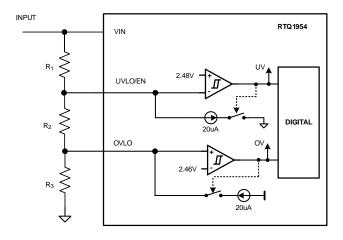


Figure 10. VIN UVLO and OVLO Setting Configuration

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Power Good Pin 17.7

Power Good (PG) is an open-drain output indicating the status of the output with the addition of an external pullup resistor. The internal PG circuitry monitors faults, VIN, FB and GATE-OUT voltage to determine the PG pin voltage status. If the FB pin voltage is below the threshold of 2.46V, the PG pin is pulled low. When the voltage at the FB pin increases beyond the threshold (2.46V) and GATE-OUT voltage is above the 9V threshold (GATE_HI signal), the PG open-drain output is turned off after 100 µs (provided VIN is within the operating range of UVLO and OVLO and no fault exists). Power good is then signaled by the external resistor pulling up on PG. An internal 20μA current source at the FB pin is enabled to create voltage hysteresis (with external resistors). Typically, Vout is connected to FB pin via a resistor divider although any voltage can be monitored as long as it is within the maximum rating of the FB pin. When VIN goes outside of the operating range set by UVLO and OVLO and/or fault is declared and/or the FB pin drops below its threshold, the PG is pulled low after 10µs. The status of the PG pin can be read through the PMBus interface in either the STATUS_WORD (79h) or READ_DIAGNOSTIC_WORD (E1h) registers.

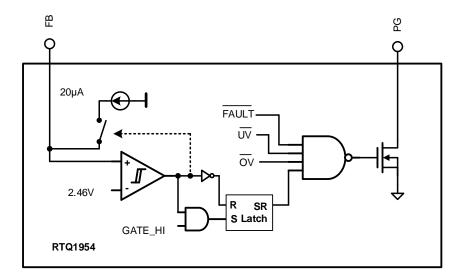


Figure 11. Power Good Logic Block Diagram

VIN UV	VIN OV	FAULT	FB. GATE_HI	PG	Description
L	L	L	Н	Н	Normal operation
H/L	H/L	H/L	L	L	The FB pin voltage drops below its threshold
Н	L	H/L	H/L	L	Input voltage drops below the UVLO threshold
L	Н	H/L	H/L	L	Input voltage goes above the OVLO threshold
H/L	H/L	Н	H/L	L	Fault is declared

VDD and VREF Sub-Regulators 17.8

The RTQ1954 includes internal sub-regulators to convert the input voltage VIN to 4.9V VDD that is used for internal low-voltage circuits and is used as a pull-up supply for external pins such as CL, RETRY, and ADR2-0, if they are tied high. It can also be used as a pull-up supply for SMBus and PG pins. There is a second sub-regulator LDO to convert VDD to VREF of 3V which is used to power internal circuitry. CL and RETRY can be connected to VREF for additional configurations. The VDD and VREF pins are current limited to protect in the event of short circuit.



The VDD and VREF pins should not be loaded by other external circuits due to the limited drive current of the subregulators. Place a 1μF 0603 ceramic capacitor close to the VDD and VREF pins to GND. VREF can be externally pulled low to re-latch the PMBus address and reset PMBus registers.

17.9 **Remote Temperature Sensing**

The temperature of an external element, such as the series-pass MOSFET can be measured using either an NPN or PNP transistor connected as a diode (base and collector connected together). If using an NPN transistor, the collector and base need to be shorted together and connected to the DIODE pin of the RTQ1954 and the emitter to the RTQ1954 GND (it is recommended to use a Kelvin connection for the device GND for accurate measurement). Transistors such as MMBT3904 or similar are suitable to use. If using a PNP (MMBT3906 or similar), the collector and base need to be connected to the device GND and the emitter to the DIODE pin.

To measure the series-pass MOSFET temperature, the transistor should be placed as close to the MOSFET as layout allows. To reduce the effect of noise on the measurement, a 1nF 0603 ceramic capacitor needs to be placed in parallel to the DIODE pin and the device GND.

To further reduce the noise, the RTQ1954 has a resistance cancellation feature, making it beneficial to use in noisy environments. It allows a low pass filter to be placed between the RTQ1954 and the remote transistor using two 150 Ω resistors and a 1nF capacitor, as shown in the figure below. The series resistance cancelation removes the effect of any resistance in series with the remote transistor. This low pass filter reduces both common and differential modes noises.

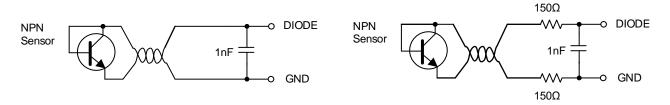


Figure 12. Connection of NPN sensor to device

Figure 13. Connection of NPN sensor through lowpass filter

The RTQ1954 periodically sources 10µA, 60µA and 160µA current pulses out of the DIODE pin and measures the temperature by measuring the voltage at the DIODE pin. For accurate temperature measurements, it is required the VIN be in the recommended operating range of 10V to 80V. The temperature can be read using the READ TEMPERATURE 1 (8Dh) PMBus command. By default, the temperature fault and warning thresholds of the RTQ1954 are set to 256°C and are effectively disabled. These thresholds can be reprogrammed through the PMBus interface using the OT_WARN_LIMIT (51h) and OT_FAULT_LIMIT (4Fh) commands. After the OT fault, the GATE is latched off and requires manual restart. The status of the OT fault and warning can be checked using STATUS_WORD (79h), STATUS_TEMPERATURE (7Dh), and READ_DIAGNOSTIC_WORD (E1h). If the temperature measurement and protection capability of the RTQ1954 are not used, the DIODE pin should be grounded.

17.10 MOSFET Health Monitoring

The RTQ1954 monitors the health condition of an external series-pass MOSFET for two different scenarios, FET SHORT and FET BAD. For the FET SHORT scenario, the RTQ1954 checks for a shorted MOSFET condition at the end of the insertion time (PORIT) while the GATE pin is low. If the voltage across RSNS is greater than 2mV or if the MOSFET VDS < 6V FET SHORT is declared. In this condition, the EXT MOSFET SHORT bit in the STATUS_MFR_SPECIFIC (80h) and READ_DIAGNOSTIC_WORD (E1h) registers are toggled high and the SMBA pin is asserted, unless this feature is disabled using the ALERT_MASK register (D8h).

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For the FET BAD scenario, the RTQ1954 checks FET BAD during normal operation after PG is asserted high. FET BAD is detected if the MOSFET gate current exceeds the IGATE source current (typically 20µA) or if VDs > 4.2V. If the FET BAD scenario remains for 100ms, PG is pulled low, and the FET FAULT bit in the STATUS_MFR_SPECIFIC (80h) register is toggled high, and the SMBA pin is asserted, unless this feature is disabled using the ALERT MASK register (D8h). On a FET BAD fault, the GATE is latched off and requires manual restart. FET BAD is disabled while the RTQ1954 is in the active current/power regulation (mode = ACL).

Slew Rate Limited Power-Up Sequence

During start-up, as the input Voltage VIN increases, the RTQ1954 initially holds GATE off using a 200mA pulldown current. Once VIN reaches the POR IT threshold of 7.8V, the insertion timer starts by charging CTIMER with 4.8µA. At the end of the insertion timer (when the TIMER voltage reaches 3.9V), the RTQ1954 checks for VIN to be within the UVLO and OVLO operating threshold and FET SHORT fault. If there is no fault, the external MOSFET is enabled and CTIMER is quickly discharged with a 1.5mA internal current sink.

The external MOSFET is turned on with a 20µA current source to charge the GATE capacitance. A capacitor from GATE to GND can be used to limit the Vout slew rate and keep the inrush current (INRUSH) low.

$$C_{GATE} = \frac{I_{GATE}}{I_{INRUSH}} \times C_{OUT}$$

where CGATE is the total GATE capacitance including parasitic capacitances, and IGATE is the GATE pull-up source current of 20µA. A limited slew rate can reduce the stress on the MOSFET by extending the startup time and spreading the power dissipation in the MOSFET for a longer period while the timer is off.

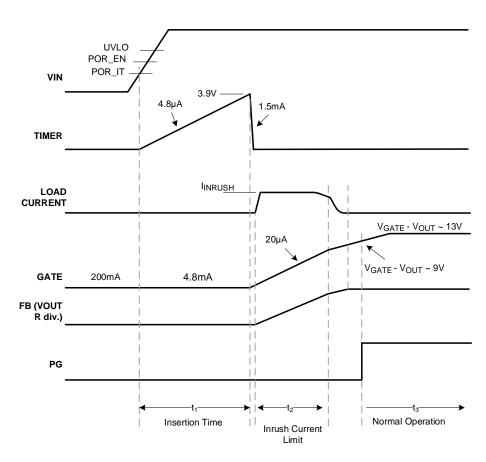


Figure 14. Startup Into Fixed dV/dt Mode (No-Load)



During start-up after VIN has passed POR_EN of 8.6V, the RTQ1954 asserts the DEFAULTS_LOADED bit in STATUS_MFR_SPECIFIC (80h) to indicate that the volatile memory and device settings are in the default state. The CONFIG_PRESET bit within the READ_DIAGNOSTIC_WORD register (E1h) indicates the default configuration of warning thresholds and device operation and remains high until a CLEAR_FAULTS (03h) command is received.

17.12 Gate Control

To charge the external MOSFET gate capacitance, the RTQ1954 sources 20μA current out of the GATE pin with an internal charge pump. The peak voltage of the charge pump is 15V, and in normal operation, the MOSFET's gate-source voltage is held sufficiently above 10V for the lowest RDSON. The GATE-OUT is internally limited to 15.6V to protect the external MOSFET's gate-source oxide from exceeding 20V in transient conditions. In some scenarios, the RTQ1954 needs to discharge the gate charge and modulate or turn off the MOSFET. During start-up, before VIN reaches POR_IT, the GATE is held low using a 200mA current sink, and during insertion time, the GATE is held low using a 4.8mA current sink. After OCP1, OCP2 and OCP3 faults, the GATE is pulled down with 4.8mA, and during ACL mode (if activated), the GATE is modulated to keep the current/power within the limits.

17.13 Fault Timer

When the current goes above the IoCP2 threshold, the CTIMER is charged using a $2.5\mu\text{A}$ current source, and toCP2 fault timeout period begins. If the current drops below IoCP2 before the TIMER pin reaches 3.9V, the CTIMER is discharged by a $20\mu\text{A}$ current sink and the RTQ1954 resumes operation. Otherwise, a fault is declared, the GATE pin pulls low using a 4.8mA current sink and CTIMER gets discharged using a $20\mu\text{A}$ current sink. The GATE will be held low until subsequent restart is performed depending on $\overline{\text{RETRY}}$ settings. The RTQ1954's $2.5\mu\text{A}/20\mu\text{A}$ charge/discharge current ratio (1:8) on the TIMER pin allows for a variety of wide and unpredictable overcurrent scenarios without VTIMER accumulating causing false tripping.

17.14 PROCHOT Output

The RTQ1954 has an early warning feature that lets the system management know that the current and/or power is too high so that the system takes proper action, such as reducing the load current. The warning is provided using the VAUX pin which can be set as $\overline{PROCHOT}$ using the relevant bit in the MFR_ADV_CFG_STATUS (F1h) register. The $\overline{PROCHOT}$ asserts (goes low) 100 μ s after the current goes above IOCP2 during normal operation, and deasserts immediately after the current drops below IOCP2. If the VAUX pin is used to set the OCP2 threshold, the $\overline{PROCHOT}$ output feature will not be available. The $\overline{PROCHOT}$ is kept deasserted (pulled high) during insertion time.

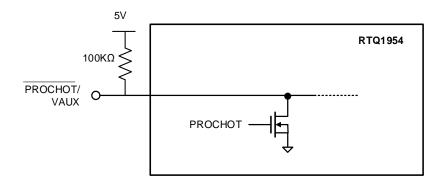


Figure 15. PROCHOT Pin can be Assigned on VAUX Pin using PMBus



17.15 Restart and Cooldown Time

If RETRY = VDD, no restart will be attempted, and the GATE is pulled low using a 4.8mA current until the RTQ1954 is externally restarted by either power cycling VIN or momentarily pulling UVLO/EN low. The TIMER_LATCHED_OFF bit in the READ_DIAGNOSTIC_WORD (E1h) register remains high while the latched off condition persists.

If RETRY = VREF, the RTQ1954 will restart 8 times, and if RETRY = GND/float, the RTQ1954 will restart continuously. Finer restart attempt counts can be selected by setting the appropriate bits in the DEVICE_SETUP (D9h) register. Each restart attempt consists of 8 cycles of the TIMER pin voltage cycling between 3.9V and 1.2V, and the period of each cycle depends on CTIMER. During the restart attempt, the GATE is held low using a 4.8mA sink current.

Before each restart attempt, the TIMER pin voltage must fall below 0.3V before the next restart is attempted.

After the 8th cycle, and when the TIMER voltage drops <0.3V, the GATE is charged using a 20μA current source, and the external MOSFET is turned on. If a fault still exists, the same sequence repeats.

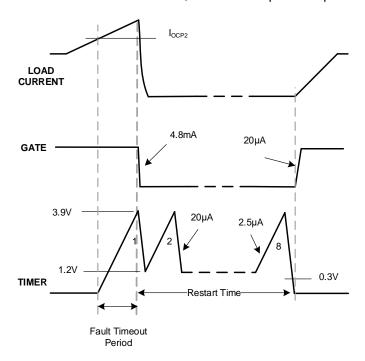


Figure 16. Single restart attempt, DEVICE_SETUP (D9h [7:5]) = [010]

In some high-power scenarios where the device and external MOSFET temperatures are high and/or large capacitance exists on the output, it may be beneficial to wait, after the 8th restart attempt, to allow the external MOSFET to cool down, and/or the output voltage to drop below a certain threshold before enabling the MOSFET again. The cooldown time after the last restart attempt can be set through MFR ADV COOLDOWN TIME (F5h) register. The output voltage threshold where the part will not restart until the VOUT drops below it can be set using VOUT_UV_RETRY_THRESHOLD (EFh).

17.16 Power Cycle

When operating in any state, the RTQ1954 power cycle feature turns off the power flow through the external MOSFET and allows it to turn back on after a certain period. When a power cycle command is issued through the PMBus POWER_CYCLE (FBh) register, the RTQ1954 pulls down the GATE using a 4.8mA current and the TIMER



pin using a 20μA current. If the PG is asserted, it will deassert after 10μs. The device then waits for a power cycle time between 0s to 65s defined by MFR_ADV_PWRCYCLE_TIME (F2H) register. When the timer ends, the RTQ1954 will attempt to restart. An extra condition can be applied before starting the power cycle timer by monitoring the Vout voltage and checking if it is less than a value defined by VOUT_UV_RETRY_THRESHOLD (EFh). This extra condition can be enabled by setting the relevant bit in the MFR_ADV_CFG_STATUS (F1h) register.

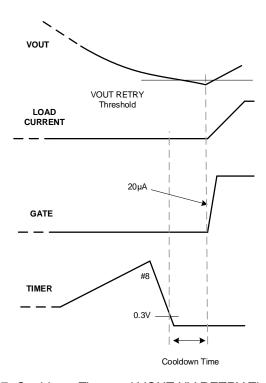


Figure 17. Cooldown Time and VOUT UV RETRY Threshold

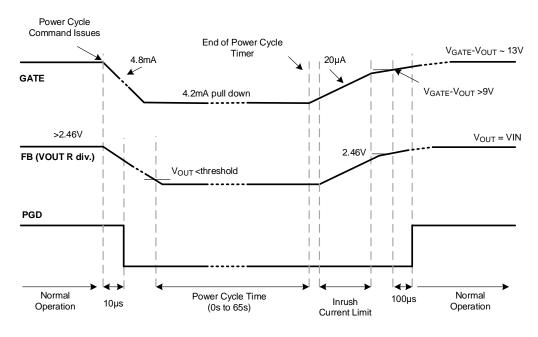


Figure 18. Power Cycle Timing Diagram Example, Restarting Into dV/dt Mode, Time not to Scale

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17.17 Enable/Disable, Shutdown and Reset Control

During normal operation, the output can be disabled by pulling the UVLO/EN pin or the OVLO pin below or above their thresholds, respectively. To remotely shutdown the load current, the UVLO/EN pin can be pulled low with an open-drain or open-collector device connected to the pin. When UVLO/EN is released, the RTQ1954 enables the GATE. When in a latched-off state after a fault, there are a few ways to manually restart the device, such as toggling UVLO/EN from low to high, power cycling VIN below/above the POR_EN threshold, changing the PMBus OPERATION (01h) register from OFF to ON, or power cycling through the POWER_CYCLE (FBh) register. The user-stored register settings data are preserved even after the output is disabled. The output may also be enabled or disabled by using the OPERATION (01h) register.

Note 15. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.



18 Functional Register Description

PMBus Commands Overview 18.1

Code	Command Name	Description	R/W	Bytes	Default
01h	OPERATION	Hot swap operation enable/disable	RW	1	80h
03h	CLEAR_FAULTS	Clears fault (non-active) and warning bits in all registers	W	0	-
19h	CAPABILITY	Retrieves the device capability	R	1	D0h
43h	VOUT_UV_WARN_LIMIT	Retrieves or stores output undervoltage warning threshold for the VOUT pin measurement	RW	2	0000h
4Fh	OT_FAULT_LIMIT	Retrieves or stores overtemperature fault threshold	RW	2	0FFFh
51h	OT_WARN_LIMIT	Retrieves or stores overtemperature warning threshold	RW	2	0FFFh
57h	VIN_OV_WARN_LIMIT	Retrieves or stores input overvoltage warning threshold	RW	2	0FFFh
58h	VIN_UV_WARN_LIMIT	Retrieves or stores input undervoltage warning threshold	RW	2	0000h
5Dh	IIN_OC_WARN_LIMIT	Retrieves or stores input overcurrent warning (mirror of command D3h)	RW	2	0FFFh
78h	STATUS_BYTE	Retrieves information about device operating status	R	1	00h
79h	STATUS_WORD	Retrieves information about device operating status	R	2	0000h
7Ah	STATUS_VOUT	Retrieves information about device output voltage status	R	1	00h
7Ch	STATUS_INPUT	Retrieves information about device input status	R	1	00h
7Dh	STATUS_TEMPERATURE	Retrieves information about temperature status	R	1	00h
7Eh	STATUS_CML	Retrieves information about communication status	R	1	00h
7Fh	STATUS_OTHER	Retrieves other status information	R	1	00h
80h	STATUS_MFR_SPECIFIC	Retrieves information about external MOSFET fault and device circuit breaker and internal die temperature	R	1	10h
86h	READ_EIN	Retrieves energy monitoring measurement	R	6	00h 00h 00h 00h 00h 00h
88h	READ_VIN	Retrieves input voltage measurement	R	2	0000h
89h	READ_IIN	Retrieves input current measurement (mirror of command D1h)	R	2	0000h
8Bh	READ_VOUT	Retrieves output voltage measurement	R	2	0000h
8Dh	READ_TEMPERATURE_ 1	Retrieves temperature measurement from DIODE pin	R	2	0000h
8Eh	READ_TEMPERATURE_ 2	Retrieves internal die temperature measurement	R	2	00h
97h	READ_PIN	Retrieves average input power measurement (mirror of command D2h and DFh)	R	2	00h
98h	PMBUS_REVISION	Retrieves PMBus revision	R	1	22h
99h	MFR_ID	Retrieves manufacturer ID	R	3	"RTK"
9Ah	MFR_MODEL	Retrieves part number	R	8	"RTQ19 54\0"
9Bh	MFR_REVISION	Retrieves part revision	R	2	"12"
D0h	READ_VAUX	Retrieves AUX pin voltage measurement	R	2	0000h
D1h	READ_IIN	Mirror of 89h	R	2	0000h
D2h	READ_PIN	Mirror of 97h and DFh	R	2	0000h

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Code	Command Name	Description	R/W	Bytes	Default
D3h	MFR_IIN_OC_WARN_LI MIT	Retrieves or stores input current warning threshold (mirror of command 5Dh)	RW	2	0FFFh
D4h	PIN_OP_WARN_LIMIT	Retrieves or stores input power limit warning threshold	RW	2	0FFFh
D5h	READ_PIN_PEAK	Retrieves peak input power measurement	R	2	0000h
D6h	CLEAR_PIN_PEAK	Clears the peak power measurement register	W	0	-
D7h	GATE_MASK	Allows to disable MOSFET shutdown for different faults	RW	1	00h
D8h	ALERT_MASK	Retrieves or stores user SMBA fault mask	RW	2	FD20h
D9h	DEVICE_SETUP	Retrieves or stores device settings about RETRY attempts, CL settings and CB ratio	RW	1	00h
DAh	BLOCK_READ	Retrieves most recent telemetry and diagnostic information	R	12	0880h 0000h 0000h 0000h 0000h
DBh	SAMPLES_FOR_AVG	Number of samples to be averaged (AVG=2^SAMPLES_FOR_AVERAGE). Also the average register update period (ms). Range from 00h to 0Ch.	RW	1	08h
DCh	READ_AVG_VIN	Retrieves average input voltage measurement	R	2	0000h
DDh	READ_AVG_VOUT	Retrieves average output voltage measurement	R	2	0000h
DEh	READ_AVG_IIN	Retrieves average input current measurement	R	2	0000h
DFh	READ_AVG_PIN	Retrieves average input power measurement (mirror of command 97h and D2h)	R	2	0000h
E0h	BLACK_BOX_READ	Retrieves telemetry and diagnostic data latched on the first assertion of SMBA	R	12	0000h 0000h 0000h 0000h 0000h
E1h	READ_DIAGNOSTIC_WO RD	MFR specific parallel of the STATUS_WORD to convey all FAULT/WARN data in a single transaction	R	2	0880h
E2h	AVG_BLOCK_READ	Retrieves most recent average telemetry and diagnostic information in a single transaction	R	12	0880h 0000h 0000h 0000h 0000h
EDh	READ_IIN_PEAK	Records or retrieves the peak value of READ_IIN	RW	2	0000h
EEh	READ_IIN_MIN	Records or retrieves the minimal value of READ_IIN	RW	2	0FFFh
EFh	VOUT_UV_RETRY_THR ESHOLD	Retrieves or stores the voltage value that VOUT has to drop below it before retry can be attempted.	RW	2	0FFFh
F0h	MFR_CL_THRESHOLD	Retrieves or stores the CL threshold in mV	RW	1	00h
F1h	MFR_ADV_CFG_STATUS	Allows for configuring the device settings.	RW	2	00h
F2h	MFR_ADV_PWRCYCLE_ TIME	Retrieves or stores the duration of power cycle timer	RW	2	2710h
F3h	MFR_ADV_RETRY_TIME OUT	Retrieves or stores the time limit duration of fault retry	RW	2	0000h
F5h	MFR_ADV_COOLDOWN _TIME	Retrieves or stores the cooldown time in ms before each subsequent retry attempt	RW	2	0000h



Code	Command Name	Description	R/W	Bytes	Default
F6h	MFR_TELEM_CFG	Configures the device telemetry settings	RW	2	005Fh
F9h	MFR_HOTSWAP_STATU S	Retrieves the current status of hotswap	RW	3	00000Fh
FBh	POWER_CYCLE	Causes the hot swap to shutdown and remain off for the period defined by F2h	WO	0	-



18.2 Data Format for Reading and Writing Telemetry and Fault/Warning Thresholds

The RTQ1954 uses the DIRECT format to read and write telemetry data and warning/fault thresholds as described in section 7.4.1 of PMBus Power System Management Protocol Specification 1.4 (Part II). Conversion of current, temperature, voltage and power from DIRECT format to real-world units is performed by the host system using the appropriate coefficients listed in the table below and using the following equation:

$$X = \frac{1}{m} (Y \times 10^{-R} - b)$$

where

- X, is the calculated, real-world value in the appropriate units (A, V, °C, W)
- m, the slope coefficient, is a two byte, two's complement integer
- Y, is a two byte two's complement integer received from the PMBus device
- b, the offset, is a two byte, two's complement integer
- R, the exponent, is a one byte, two's complement integer

Commands	Condition	Format	Bytes	m	b	R	Unit
VIN_OV_WARN_LIMIT							
VIN_UV_WARN_LIMIT		DIRECT	2	4617	-140	-2	V
READ_VIN							
READ_AVG_VIN							
READ_VOUT							
READ_AVG_VOUT		DIRECT	2	4602	500	-2	V
VOUT_UV_WARN_LIMIT							
VOUT_UV_RETRY_THRESHOLD							
READ_VAUX		DIRECT	2	1401	11999	-1	V
READ_IIN							
READ_AVG_IIN							(4)
READ_IIN_PEAK	CL<33mV	DIRECT	2	15076	-503.9	-2	A ⁽¹⁾
READ_IIN_MIN							
IIN_OC_WARN_LIMIT							
READ_IIN							
READ_AVG_IIN							(4)
READ_IIN_PEAK	CL≥33mV	DIRECT	2	6825	0	-2	A ⁽¹⁾
READ_IIN_MIN							
IIN_OC_WARN_LIMIT							
READ_PIN							
READ_AVG_PIN	CL<33mV	DIRECT	2	1701	-4000	-3	W ⁽¹⁾
PIN_OP_WARN_LIMIT	OL 300IIIV	DIRLOT	2	1701	4000		•
READ_PIN_PEAK							
READ_PIN							
READ_AVG_PIN	CL≥33mV	DIRECT	2	7677	0	-4	W ⁽¹⁾
PIN_OP_WARN_LIMIT	OL=00IIIV	DIRLOT	2	7077	O	-	•
READ_PIN_PEAK							
OT_FAULT_LIMIT							
OT_WARN_LIMIT		DIRECT	2	16000	0	-3	°C
READ_TEMPERATURE_1		DIILOI	_	10000	O	-0	
READ_TEMPERATURE_2							

(1) The coefficients listed for power/current measurements are normalized based on an Rsns of 1mΩ.



For registers that accept writing data, the same coefficients can be used to determine the Y value from read-world data as follows:

$$Y = (mX+b) \times 10^R$$

where

- X, is the calculated, real-world value in the appropriate units (A, V, °C, W)
- m, the slope coefficient, is a two-byte, two's complement integer
- Y, is a two-byte two's complement integer received from the PMBus device
- b, the offset, is a two-byte, two's complement integer
- R, the exponent, is a one-byte, two's complement integer

18.3 PMBus Address Lines (ADR0, ADR1, ADR2)

The tri-state address lines of ADR0, ADR1, and ADR2 can be set to high (VDD), low (connect to GND) or left floating (high impedance Z) to select one of the 27 addresses for communicating with the RTQ1954 as shown in the table below. Each address is 7-bits (bits 0 to 6) with the eighth bit being the read/write bit. If the OCP3 mode is set (ACL is not active), it is not recommended to connect VREF to GND after power-up to change the PMBus address.

ADR2	ADR1	ADR0	Decoded Address
Z	Z	Z	40h
Z	Z	GND	41h
Z	Z	VDD	42h
Z	GND	Z	43h
Z	GND	GND	44h
Z	GND	VDD	45h
Z	VDD	Z	46h
Z	VDD	GND	47h
Z	VDD	VDD	10h
GND	Z	Z	11h
GND	Z	GND	12h
GND	Z	VDD	13h
GND	GND	Z	14h
GND	GND	GND	15h
GND	GND	VDD	16h
GND	VDD	Z	17h
GND	VDD	GND	50h
GND	VDD	VDD	51h
VDD	Z	Z	52h
VDD	Z	GND	53h
VDD	Z	VDD	54h
VDD	GND	Z	55h
VDD	GND	GND	56h
VDD	GND	VDD	57h
VDD	VDD	Z	58h
VDD	VDD	GND	59h
VDD	VDD	VDD	5Ah

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18.4 **PMBus Command Descriptions**

18.4.1 Standard PMBus Commands

Operation (01h)

Command Code: 01h

Description: It is a standard PMBus command that switches the MOSFET on and off under host control. It is also used to re-enable the MOSFET after a fault triggered shutdown. Writing an OFF command, followed by an ON command, clears all faults and reenables the device. Writing only an ON after a fault-triggered shutdown does not clear the fault registers or reenable the device.

		Ť									
Name					OPER	ATION					
Format					Read/W	/rite Byte					
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
Read/V	Vrite	RW	R	R	R	R	R	R	R		
Default Value 0x1 0x00											
Bits	Name			Descr	iption						
				Hot S	wap Enable)					
[7]	ON			0 Hot	swap outpu	ut disabled					
				1 Hot	swap outpu	ut enabled					
[6:0]	Reserved	Always reads 0									

CLEAR_FAULTS (03h)

Command Code: 03h

Description: It is a standard PMBus command that resets all stored warning and fault flags and the SMBA signal. If a fault or warning condition still exists when the CLEAR_FAULTS command is issued, the SMBA signal may not clear or re-asserts almost immediately. Issuing a CLEAR_FAULTS command does not cause the MOSFET to switch back on in the event of a fault turnoff; that must be done by issuing an OPERATION command after the fault condition is cleared

the fault condition is cleared.													
Name					CLEAR_	_FAULTS							
Format					Send	d Byte							
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0				
Read/W	/rite	W	W	W	W	W	W	W	W				
Default	Value												
Bits	Name			Desci	Description								
NA	CLEAR_F	AULTS			s fault and that are stil				isters. Any n set.				

CAPABILITY (19h)

Comma	nd Code: 19	h										
Descript	ion: It is a st	andard PMI	Bus comma	and th	at pro	vides some	of key capa	abilities of R	TQ1954 de	evice.		
Name						CAPA	BILITY					
Format						Read	d Byte					
Bits		Bit 7	Bit 6	Bi	it 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
Read/Write R R R R R R										R		
Default \	Value	0x1	0:	x2	0x1 0x0							
Bits	Name				Descr	iption						
[7] PEC_SUPPORT Packet error correction (PEC) support												
[6:5]	MAX_BUS	_SPEED				num bus int I is 1MHz.	erface spee	ed. Always r	eads 2. Ma	ximum bus		



[4]	SMBALERT_SUPPORT	Always reads 1. Device supports SMBAlert and ARA
[3:0]	RESERVED	

VOUT_UV_WARN_LIMIT (43h)

Command Comman			rd PMI	Bus co	mmano	d that a	allows	to se	et and	read	the \	/OUT	unde	ervolta	ge wa	arning
threshold.																
Name						VOU	T_UV	_WAI	RN_LI	MIT						
Format							Read/	Write	Word							
Bits	Bit 15															
Read/Write	R	R R R RW R														
Default Value		0 0x000														
Bits		Name				Descr	ption									
[15:12]	Reserved Reserved															
[11:0]	VOUT_UV_WARN_LIMI T Undervoltage warning threshold for the VOUT pin measurement, expressed in direct format. A value of 0 is disabled.															

OT_FAULT_LIMIT (4Fh)

Command C	ode: 4F	-h														
Description:	lt is a s	tandard	d PMB	ıs comr	mand th	nat sets	and r	eads 1	the ov	ertem	perati	ure fa	ult det	tection	n thres	shold.
Name						С	T_FA	ULT_	LIMIT	•						
Format						F	Read/\	Vrite '	Word							
Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R	R R RW														
Default Value		0 0xFFF														
Bits		Name				Descri	ption									
[15:12]	Reserved Reserved															
[11:0]	OT_FAULT_LIMIT Overtemperature fault threshold for the DIODE pin measurement, expressed in direct format.															

OT_WARN_LIMIT (51h)

Command C	ode: 51	1h														
Description:	It is a	standa	ard PM	Bus co	omman	d that	sets a	and re	eads 1	the ov	/erten	nperat	ture v	varnin	g dete	ection
threshold.																
Name						C	DT_W	ARN_	LIMIT	•						
Format						F	Read/	Write	Word							
Bits	Bit 15	Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0														
Read/Write	R															
Default Value		()							0xFl	FF					
Bits	Name Description															
[15:12]	5:12] Reserved Reserved															
[11:0]	OT_WARN_LIMIT OVertemperature warning threshold for the DIODE pin measurement, expressed in direct format.															



VIN_OV_WARN_LIMIT (57h)

Command C	ode: 57	7h														
Description:	It is a s	tandard	d PMBu	is comr	nand th	at sets	and r	eads t	the VI	N ove	rvolta	ge wa	arning	thres	hold.	
Name						VIN	_OV_'	WARI	_LIM	IIT						
Format						F	Read/V	۷rite ۱	Nord							
Bits	Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0															
Read/Write	R															
Default Value		(0							0xFF	F					
Bits		Name				Descr	iption									
[15:12]	Reserved Reserved															
[11:0]	VIN_OV_WARN_LIMIT Overvoltage warning threshold for the OVLO pin measurement, expressed in direct format. 0xFFF is disabled															

VIN_UV_WARN_LIMIT (58h)

Command C	ode: 58	3h	•		•	•										
Description:	lt is a s	tandard	d PMBu	ıs comr	mand th	nat sets	and r	eads	the V	IN und	dervol	tage v	warnir	ng thre	esholo	l.
Name						VIN	_UV_	WARI	N_LIN	1IT						
Format						F	Read/\	Vrite '	Word							
Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R	R R RW														
Default Value		0 0x000														
Bits		Name				Descr	iption									
[15:12]	Reserved Reserved															
[11:0]	VIN_UV_WARN_LIMIT Undervoltage warning threshold for the EN/UVLO pin measurement, expressed in direct format. 0x000 is disabled															

IIN_OC_WARN_LIMIT (5Dh)

Command C																
Description:	lt is a s	tandar	d PMBu	is comr	nand th	at sets	and re	ads t	he inp	ut ov	ercurr	ent w	arning	thres	shold.	
Name						IIN_	OC_V	/ARN	_LIMI	Т						
Format						R	ead/V	/rite V	Vord							
Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R	R R R RW R														
Default Value		0 0xFFF														
Bits		Name				Descrip	otion									
[15:12]		Reser	ved			Reserv	ed									
[11:0]		IRSNS overcurrent warning, expressed in direct format. A value of 0xFFF disables.														
		This is a mirror of command D3h														



STATUS_BYTE (78h)

Comma	nd Code: 78	h										
Descrip	tion: The ST	ATUS_BYT	E comman	d returns o	ne byte of ir	nformation v	vith a sumn	nary of the r	most critical			
faults.		1										
Name					STATU	S_BYTE						
Format					Read	d Byte						
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0			
Read/W	/rite	R	R	R	R	R	R	R	R			
Default	Value	0x0	0x0	()x0	0x0	0x0	0x0	0x0			
Bits	Name			Desc	ription							
[7]	RESERVE	:D										
				Hot s	wap gate is	off. This bit	is live.					
				0 – T	he hot swap	gate drive	output is er	nabled.				
[6]	ПОТС/// Г	0.000			1 - The hot swap gate drive output is disabled, and the GA							
[6]	HOTSWAF	OFF			pin is pulled down. This can be due to, for example							
					current fault							
					rvoltage co RATION cor				use of the			
[5:4]	RESERVE	:D		01 L	IXATION COL	minaria to tt	iii iiie outp	ut on.				
[3]	VIN_UV_F			A VII	N UV fault ha	as occurred						
[2]	TEMP_FA			A temperature fault or warning has occurred								
[1] CML_FAULT					mmunication			···				
[0]	_	OVE STATI	IS		ılt or warning			has occurre	d			
[0]	INCINEADO	7VL_01A10		Aiac	ii oi waiiiii	j not nateu i		ias occurre	u			

STATUS WORD (79h)

	Command Code: 70h															
Command Co				.f.,	: · · · · i 4 l			-£41	:41' 4		al:4: -	D.		- 4l i:	- f	- 1 : - :-
Description: r		•					•								ntorm	ation
in these byte	s, the c	controlle	er can (get moi	re infor					propri	ate sta	atus r	egistei	rs.		
Name							STATL	JS_W	ORD							
Format							Rea	ad Wo	rd							
Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default Value	0	0	0	0	0	0	0	0×	(Ο	0	0×	(Ο	0	0	0	0
Bits		Name				Descri	ption									
[15]		VOUT_STATUS					put vo	oltage	fault c	or war	ning h	as oc	currec	t		
[14]		Reserved														
[13]		INPUT	_STA	ΓUS		An input voltage or current fault has occurred										
[12]		MFR_	SPECI	FIC		A STA		_MFR_	_SPE	CIFIC	fault	has	occui	rred o	other	than
[11]		POWE	R_GO	OD		The Po	ower (Good s	signal	has b	een n	egate	d			
[10]		Reserved														
[9]		CB_Fault Circuit breaker fault triggered														
[8:7]		Reserved														
						Hot sw	ap ga	ite is o	ff. Th	is bit i	s live.					
[6]		HOTSWAP_OFF					e hot	swap (gate c	lrive o	utput	is ena	abled.			
		1 – The hot swap gate drive output is disabled, and the GATE														



		pin is pulled down. This can be due to, for example, an overcurrent fault that causes the device to latch off, and undervoltage condition on the UV pin, or the use of the OPERATION command to turn the output off.
[5:4]	Reserved	
[3]	VIN_UV_FAULT	A VIN UV fault has occurred
[2]	TEMP_FAULT	A temperature fault or warning has occurred
[1]	CML_FAULT	A communication fault has occurred
[0]	NONEABOVE_STATUS	A fault or warning not listed in bits [7:1] has occurred

STATUS_VOUT (7Ah)

Comma	nd Code: 7A	h								
Descrip	tion: returns	one data by	te with con	tents as fo	llows.					
Name					STATU	S_VOUT				
Format					Read	d Byte				
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Read/W	/rite	R	R	R	R	R	R	R	R	
Default	Value	0)	0x0 0x0 0x0							
Bits	Name			Desc	ription					
[7:6]	RESERVE	D								
[5]	[5] VOUT_UV_WARN									
[4:0]	[4:0] RESERVED									

STATUS_INPUT (7Ch)

Comma	and Code: 70	 Ch											
	otion: returns		te with con	tents as fol	lows.								
Name					STATUS	S_INPUT							
Format					Read	d Byte							
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0				
Read/V	Vrite	R	R	R	R	R	R	R	R				
Default	Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0				
Bits	Name			Desc	Description								
[7]	VIN_OV_F	AULT		A VIN	A VIN OV fault has occurred								
[6]	VIN_OV_V	VARN		A VIN	OV warning	g has occur	red						
[5]	VIN_UV_V	VARN		startu	N UV warning, but is cle ases above	ared to 0 a	fter the first	time the in	llts to 1 on put voltage				
[4]	VIN_UV_F	AULT		A VIN	I UV fault ha	as occurred							
[3]	RESERVE	D											
[2]	IIN_OC_F	AULT		An IIN OC fault has occurred									
[1]	IIN_OC_W	An III	An IIN OC warning has occurred										
[0]	PIN_OP_V	VARN		A PIN	A PIN OP warning has occurred								



STATUS_TEMPERATURE (7Dh)

Comma	and Code: 7D)h										
Descrip	ption: returns	one data by	yte with con	tents as foll	lows.							
Name				S	TATUS_TE	MPERATU	RE					
Format	t				Read	d Byte						
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0			
Read/V	Vrite	R	R	R	R	R	R	R	R			
Default	t Value	0x0	0x0			0	x0					
Bits	Name			Description								
[7]	OT_FAULT	Г		STAT set, th	en this OT_	SPECIFIC.II _FAULT wa	NT_OT_TEI s an interna FEMP_FAUI	ıl die temp f	ault.			
[6]	OT_WARN	I		An O	An OT warning has occurred							
[5:0]	RESERVE	D										

STATUS_CML (7Eh)

	nd Code: 7E										
Descrip	tion: returns	one data by	te with con	tents as	follows.						
Name					STATU	JS_CML					
Format					Rea	d Byte					
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
Read/W	/rite	R	R	R	R	R	R	R	R		
Default	Default Value 0x0 0x0				0x0	0x0	0x0	0x0	0x0		
Bits					scription						
[7]	INVALID_0	CMD		An invalid or unsupported command was received							
[6]	INVALID_[DATA		Inv	alid or unsupp	orted data	was receive	d			
[5]	PEC_ERR	OR		Pa	Packet error check failed						
[4:2]											
[1] MISC_COM_FAULT				A r	niscellaneous	communica	ation fault ha	as occurred			
[0]	[0] MEM_ERROR				A OTP eFuse uncorrectable ECC error has occurred						

STATUS_OTHER (7Fh)

Comma	and Code: 7F	h							
Descrip	tion: returns	one data by	yte with con	tents as fo	llows.				
Name					STATUS	_OTHER			
Format					Read	d Byte			
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/W	Vrite	R	R	R	R	R	R	R	R
Default	Value	0:	x0	0x0			0x0		
Bits	Name			Desc	ription				
[7:6]	RESERVE	D							
[5]	CB_FAUL7	Ī		A circ	cuit breaker f	fault has oc	curred		
[4:0]	RESERVE	D							



STATUS_MFR_SPECIFIC (80h)

Comma	and Code: 80)h									
	tion: returns		te with cor	itents as fol	lows.						
Name				S	TATUS_MF	R_SPECIF	IC				
Format					Read	d Byte					
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
Read/W	/rite	R	R	R	R	R	R	R	R		
Default	Value	0x0	0x0	0x0	0x1	0x0	0x0	0	x0		
Bits	Name			Descr	ription						
[7]	CB_FAUL	Т		A circ	uit breaker f	fault has oc	curred				
[6]	EXT_MOS	FET_SHOF	RT	Exter	External MOSFET shorted fault						
[5]	FET_FAUI	LT		Vds o	r Vgs FET E	BAD fault					
[4]	DEFAULT	S_LOADED)		efault confiç F is pulled	•	been load	ed. Set on p	oower up or		
[3]	PROCHO	Γ		Sets i	Sets if PROCHOT is asserted. Cannot assert SMBAlert#						
[2]	INT_OT_T	EMP_FAUL	_T	Set if	internal die	temp excee	ds 150C.				
[1:0]	RESERVE	:D									

READ_EIN (86h)

Comma	Command Code: 86h Description: returns 6 bytes of information that can be used to calculate the input power on the device.											
			ormation that ca	n be used to c	calculate the inp	ut power on the	device.					
Name				RE	AD_EIN							
Format				Blo	ck Read							
Bits		Byte5	Byte4	Byte3	Byte2	Byte1	Byte0					
Read/W	rite	R	R	R	R	R	R					
Default '	Value	0x0	0x0	0x0 0x0 0x0 0x0 0x0								
Bits	Name		Description									
[47:24]	SAMPLE_	COUNT	JNT 24-bit unsigned integer that counts the number of samples of the instantaneous input power.									
[23:16]	ROLLOVE	R_COUNT				umber of times tunsigned integer	the accumulator (7FFFh) to 0.					
[15:0]	ENERGY_COUNT Accumulator output that continuously sums samples of the instantaneous input power.											

READ_VIN (88h)

Command Co	Command Code: 88h														
Description: r	eturns	the me	asure	d value	of the	input vo	oltage	•							
Name							RE	AD_VI	N						
Format							Rea	ad Wo	rd						
Bits	Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 3 Bit 2 Bit 1 Bit 0														
Read/Write	R														
Default Value		0	١							C)				
Bits	Name Description														
[15:12]		RESE	RVED												•
[11:0]		READ.	_VIN			12-bit	unsigr	ned nu	mber	, exp	ressec	d in d	irect fo	ormat	·

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READ_IIN (89h)

Command C	ode: 89	9h													
Description:	returns	the me	easure	d value	of the	input cu	urrent.								
Name							RE	AD_II	N						
Format							Rea	ad Wo	rd						
Bits	Bit 15														
Read/Write	R														
Default Value		()							0					
Bits		Name				Descri	iption								
[15:12]		RESERVED													
[11:0]		READ	_IIN	•		12-bit	unsigr	ned nu	mber	, expr	essed	in dir	ect for	mat	

READ_VOUT (8Bh)

_	(- /														
Command C	ode: 8E	3h													
Description:	returns	the me	easured	l value	of the o	output v	oltage) .							
Name							REA	D_VO	UT						
Format							Rea	ad Wo	rd						
Bits	Bit 15	15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0													
Read/Write	R														
Default Value		(0							0					
Bits		Name				Descri	ption								
[15:12]		RESERVED													
[11:0]		READ	_VOU			12-bit	unsigr	ned nu	mber	, exp	ressec	d in dir	ect for	rmat.	

READ_TEMPERATURE_1 (8Dh)

Command C	ode: 8l	Dh														
Description:	returns	the sig	ned va	lue of th	ne temp	perature	e meas	sured	by the	e exte	rnal te	emper	ature	sense	diode	
Name						READ	D_TEN	/IPER	ATUR	E_1						
Format							Rea	ad Woi	rd							
Bits	Bit 15	15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0														
Read/Write	R															
Default Value		R R R R R R R R R R														
Bits	Na	Name Description														
[15:0]	RI	EAD_TI	EMPER	RATURI	≣_1	16-bit 0xF00	_			expre	essed	in di	rect fo	ormat,	limite	ed to



READ_TEMPERATURE_2 (8Eh)

Command C	ode: 8E	Ēh														
Description:	returns	the sig	ned val	ue of th	ne mea	sured i	nterna	l die te	emper	ature.						
Name						REAL	D_TEN	MPER	ATUR	E_2						
Format							Rea	ad Wo	rd							
Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R	R R R R R R R R R R R R R														
Default Value																
Bits	Na	me				Descri	ption									
		Internal die temp														
[15:0]	RE	AD_TE	EMPER	ATURI	Ξ_2	16-bit 0xF00	_			expre	essed	in di	rect fo	ormat,	limite	ed to

READ_PIN (97h)

Command C	ode: 97	7h													
Description:	returns	the me	easured	d value	of the i	nput po	wer.								
Name							RE	AD_PI	IN						
Format							Rea	ad Wo	rd						
Bits	Bit 15	15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0													
Read/Write	R														
Default Value		(0							0					
Bits		Name				Descri	iption								
[15:12]	RESERVED														
[11:0]		READ	_PIN			12-bit	unsigr	ned nu	ımber	expr	essed	in dire	ect for	mat.	

PMBUS_REVISION (98h)

	and Code: 98 otion: returns		of the PME	Bus to whice	ch the device	e is compliar	nt.				
Name						REVISION					
Format					Read	d Byte					
Bits		Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0									
Read/W	Vrite	R	R	R	R	R	R	R	R		
Default	Value		0:	x2	•		0	x2			
Bits	Name			Desc	ription						
[7:4]	PART_I_R	_I_REVISION Compliant to PMBus Part I revision 1.2									
[3:0]	PART_II_F	REVISION		Com	pliant to PMI	Bus Part II r	evision 1.2				



MFR_ID (99h)

	nd Code: 99		. fact as	
Name	ion: returns	the identification of the ma	nutacturer. MFR_ID	
Format			Block Read	
Bits		Byte2	Byte1	Byte0
Read/W	'rite	R	R	R
Default	Value		"RTK"	·
Bits	Name		Description	
[23:0]	MFR_ID		ASCII string identifying man	ufacturer as Richtek (RTK).

MFR_MODEL (9Ah)

	nd Code: 9A		cturer's mo	del number	1							
Name			<u> </u>			MODEL						
Format			Block Read Byte7 Byte6 Byte5 Byte4 Byte3 Byte2 Byte1 Byte0									
Bits		Byte7 Byte6 Byte5 Byte4 Byte3 Byte2 Byte1 E										
Read/W	rite	R	R	R	R	R	R	R	R			
Default '	Value				"RTQ	1954\0"						
Bits	Name			Desci	ription							
[63:0]	MFR_MOD	MFR_MODEL ASCII string identifying model as the RTQ1954.										

MFR REVISION (9Bh)

_	•			
Command C	Code: 9	3h		
Description:	Return	s the manufacturer's revis	ion number.	
Name			MFR_F	REVISION
Format			Bloc	k Read
Bits		Byte 1		Byte 0
Read/Write		R		R
Default Value	ue	32h, "2'	,	31h, "1"
Bits	Name		Description	
[15:0]	MFR_	REVISION	ASCII string identi	fying hardware revision.



MFR Specific PMBus Commands 18.4.2

READ_VAUX (D0h)

Command C	ode: D	0h													
Description:	returns	the me	easured	value	of VAU	Χ.									
Name							REA	D_VAI	JX						
Format							Rea	ıd Wor	ď						
Bits	Bit 15														
Read/Write	R	R R R R R R R R R R R R R													
Default Value		0 0													
Bits	Name Description														
[15:12]		RESERVED													
[11:0]		READ	_VAUX	(12-bit	unsigr	ned nu	mber	, expr	essed	in dir	ect for	mat.	

READ_IIN (D1h)

Command C Description:			easured	d value	of the i	input cu	ırrent.								
Name						•	RE	EAD_II	N						
Format							Re	ad Wo	rd						
Bits	Bit 15	5 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0													
Read/Write	R	R R R R R R R R R R													
Default Value		()							0					
Bits		Name				Descri	ption								
[15:12]		Name Description RESERVED													
[11:0]		READ	_IIN			Mirror	of 89h	1							

READ_PIN (D2h)

Command C	ode: D	2h														
Description:	returns	the me	asured	value o	of the in	nput pov	ver.									
Name							RE	AD_P	IN							
Format							Rea	ad Wo	rd							
Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R	R R R R R R R R R R R R														
Default Value																
Bits		Name Description														
[15:12]		RESERVED														
[11:0]		READ	_PIN			Mirror	of 97h	1								



MFR_IIN_OC_WARN_LIMIT (D3h)

	_	L. Pol													
Command C	ode: D	3h													
Description:	sets an	d reads the in	put ove	ercurre	nt warn	ing thr	eshol	d.							
Name					MFR_	_IIN_C	C_W	ARN_	LIMIT						
Format						Read	/Write	Word							
Bits	Bit 15	Bit 14 Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R RW														
Default Value	0 0xFFF														
Bits		Name			Description										
[15:12]		RESERVED													
[11:0]	RN_LI	IRSNS overcurrent warning, expressed in direct format. A value of 0xFFF disables. Mirror of 5Dh									lue of				

PIN_OP_WARN_LIMIT (D4h)

	_														
Command C	ode: D	4h													
Description:	sets th	e value of the	input p	ower, ii	n watts,	that c	auses	a war	ning t	hat the	e inpu	t powe	er is h	igh	
Name					PIN	N_OP_	_WARI	N_LIM	IIT						
Format						Read	/Write	Word							
Bits	Bit 15	Bit 14 Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write		R													
Default Value		0							0xFF	F					
Bits		Name			Descri	ption									
[15:12]	RESERVED														
[11:0]		PIN_OP_WA	RN_LI	MIT	Overp expres			_		or the	VIN >	· IIN p	ower	calcula	ation,

READ_PIN_PEAK (D5h)

Command C	Command Code: D5h														
Description:	returns	the ma	aximum	n value	of inpu	t powei									
Name						F	READ.	_PIN_I	PEAK						
Format							Re	ad Wo	rd						
Bits	Bit 15	it 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0													
Read/Write		R R													
Default Value		()							0xFF	F				
Bits		Name				Descr	ption								
[15:12]	RESERVED														
[11:0]	READ_PIN_PEAK Maximum value for IIN × VIN since reset or last clear, expressed in direct format.														



CLEAR_PIN_PEAK (D6h)

Command Co	ode: D6h
Description: (Clears READ_PIN_PEAK
Name	CLEAR_PIN_PEAK
Format	Send Byte

GATE_MASK (D7h)

Comma	nd Code: D7	7h							
Descript	tion: This reg	gister preve	nts specific	fault cond	litions to turn	off the MO	SFET gate.		
Name					GATE	_MASK			
Format					Read/W	/rite Byte			
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/W	rite	RW	RW	RW	RW	RW	RW	R	RW
Default	Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Bits	Name			Des	cription				
[7]	GATE_MA	SK_FETFA	ULT						
[6]	GATE_MA	SK_FETSH	IORT						
[5]	GATE_MA	SK_VIN_U	V_FAULT						
[4]	GATE_MA	SK_VIN_O	V_FAULT						
[3]	GATE_MA	SK_IIN_PF	ET_FAULT						
[2]	GATE_MA	SK_OT_FA	ULT						
[1]	RESERVE	.D							
[0]	GATE_MA	SK_CB_FA	ULT						

ALERT_MASK (D8h)

Comman	d Co	de: D8	ßh														
Description	on: T	his cor	mmand	allows	s to co	nfigure	maski	ng SN	/IBA fo	r spec	ific fau	ılt or w	/arning] .			
Name								ALI	ERT_N	ИASK							
Format								Rea	d/Write	e Word	t						
Bits		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Wri	te	RW	RW	RW	RW	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	RW	RW
Default Value		1	1	1	1	1	1	0	1	0	0	1	0	0	0	0	0
Bits	Nar	ne					D	escrip	tion								
[15]	ALE	ERT_M	IASK_\	VOUT_	UV_W	'ARN											
[14]	ALE	ERT_M	IASK_I	IN_LIN	1_WAF	RN											
[13]	ALE	ERT_M	IASK_\	√IN_U\	/_WAF	RN											
[12]	ALE	ERT_M	IASK_\	\IN_O	√_WAF	RN											
[11]	ALE	ERT_M	IASK_F	POWE	R_NO	Γ_GOC	DD										
[10]	ALE	ERT_M	ASK_0	T_WA	ARN												
[9]	RES	SERVE	ED														
[8]	ALE	ERT_M	IASK_0	OP_LIN	Л_WAF	RN											
[7]	ALE	ERT_M	IASK_F	FET_F	AULT												
[6]	ALE	ERT_M	IASK_E	EXT_F	ET_SH	IORT											
[5]	ALE	ERT_M	IASK_\	√IN_U\	/_FAU	LT											
[4]	ALE	ERT_M	IASK_\	VIN_O	√_FAU	LT											



[3]	ALERT_MASK_IIN_PFET_FAULT	
[2]	ALERT_MASK_OT_FAULT	Masks OT_FAULT and INT_OT_FAULT
[1]	ALERT_MASK_CML_FAULT	
[0]	ALERT_MASK_CB_FAULT	

DEVICE_SETUP (D9h)

	nmand Code: D9h														
	iption: This command can be used to override pin settings to define the RTQ1954 operation.														
-	tion: This co	mmand can	be used to	override pi			RTQ1954	operation.							
Name															
Format				1	ı	rite Byte	T		T						
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0						
Read/W	rite		RW		RW	RW	RW	RW	RW						
Default '	Value		0x0		0x0	0x0	0x0	0x0	0x0						
Bits	Name			Descr	iption										
				111 =	Unlimited F	Retries									
				110 =	110 = Retry 16 times										
				101 =	101 = Retry 8 times										
[7.5]	DETDY O	ETTINIC		100 =	Retry 4 time	es									
[7:5]	RETRY_SI	ETTING		011 =	011 = Retry 2 times										
				010 =	010 = Retry 1 times										
				001 =	No Retries										
				000 =	Pin configu	red retries									
	01 05551			0 = Hi	0 = High setting (50mV)										
[4]	CL_SETTII	NG			ow setting (2	,									
					<u> </u>		for Vocp2	≤ 32mV, and							
[2]	CDCI DA	TIO			100mV for V			· · · · · · · · · · · · · · · · · · ·							
[3]	CBCL_RA	110		1 = Hi	gh setting (VcB=100m	V for Voce2	<u>≥</u> ≤ 32mV, an	ıd						
				Vcb=2	200mV for V	/OCP2≥ 33m	ıV)								
[2]	CL_CONF	IG		0 = Use pin settings											
[4]	OL_CONT			1 = Use SMBus settings											
				If CL_CONFIG is set to 1 and if this bit is set, the MFR CL THRESHOLD command sets the CL THRESHOLD											
[1]	USE_MFR	_CL_THRE	SHOLD		_			_							
					nines the C			0, then CL_	SETTING						
[0]	RESEVED Solution SE_TYTICESTICES.														
1,1	RESEVED														

BLOCK_READ (DAh)

Commar	Command Code: DAh Description: Concatenates the DIAGNOSIS_WORD with all the input and output telemetry data and temperature.													
Descripti	on: Conca	atenates the	DIAGN	IOSIS_V	VORD v	vith all th	ne input a	ınd outpu	ıt telemet	ry data a	nd temp	erature.		
Name						BLOCK	_READ							
Format	Block Read													
Bits	Byte 11 Byte 10 Byte 9 Byte 8 Byte 7 Byte 6 Byte 5 Byte 4 Byte 3 Byte 2 Byte 1 Byte 0													
Read/ Write	R													
Default Value	κ0	(00	0x	00	0x	00	0x	00	0x	00	0x0	0880		
Bits	Name Description													
[95:80]	TEMP_BLOCK													

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[79:64]	PIN_BLOCK	
[63:48]	VIN_BLOCK	
[47:32]	VOUT_BLOCK	
[31:16]	IIN_BLOCK	
[15:0]	DIAGNOSTIC_WORD	

SAMPLES FOR AVG (DRh)

SAMPLI	ES_FOR_AV	G (DBh)											
Comma	ınd Code: DE	3h											
			-		of samples u	sed in comp	outing the a	verage of \	VIN, VOUT,				
IIN and	PIN. It also	sets averag	e register u	pdate per	iod.								
Name					SAMPLES	_FOR_AVG	;						
Format					Read/W	/rite Byte							
Bits		Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0 e R RW											
Read/W	/rite	R	RW .	1									
Default	Value		0)	κ0	0x8								
Bits	Name			Des	cription								
[7:4]	RESERVE	D											
[3:0]	SAMPLES	_FOR_AVG	5	regi Avg 000 upd 110 ave	nber of samplester update points and samples and samples and samples and samples are period ob = 2 ¹² = 40 are period and samples are period	eriod. PER_AVG ample per a 96 samples period	verage cald per averag	culation, 1m	s average on, 4096 ms				
				_	ues 13, 14, ar a error	nd 15 are re	served and	will genera	te a CML				

READ_AVG_VIN (DCh)

Commar	nd Code	: DCh														
Descripti	on: Ret	urns the	2-bit	averag	je input	voltage	€.									
Name							READ	_AVG	_VIN							
Format							Re	ad Wo	rd							
Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/ Write	R R															
Default Value		O)							0x00)					
Bits	Name Description															
[15:12]	RESERVED															
[11:0]	READ_AVG_VIN 12-bit unsigned number, expressed in direct format.															



READ_AVG_VOUT (DDh)

Command C	ode: DI	Dh														
Description:	Returns	s the 12-	bit av	erage o	output v	voltage.										
Name						R	EAD_	AVG_	VOUT	Γ						
Format							Rea	ad Wo	rd							
Bits	Bit 15	Bit 14 E	3it 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write		R								R						
Default Value		0								0x0	0					
Bits		Name				Descri	ption									
[15:12]		RESER														
[11:0]		READ_	AVG_	VOUT		12-bit	unsigr	ned nu	mber	, expr	essed	in dire	ect for	mat.		

READ_AVG_IIN (DEh)

0	ommand Code: DEh															
Command C	oae: Di	⊨n														
Description:	Returns	s the 12	2-bit inp	out ave	rage cu	ırrent.										
Name							READ	_AVG	_IIN							
Format							Rea	ad Wo	rd							
Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write		F	₹							R						
Default		()							0x0	n					
Value		`	<i></i>							0.00	0					
Bits		Name				Descri	ption									
[15:12]		RESE	RVED													
[11:0]		READ	_AVG_	_IIN		12-bit	unsigr	ned nu	mber,	expr	essed	in dir	ect for	mat.		

READ_AVG_PIN (DFh)

Command C	ode: DI	Fh														
Description:	Returns	s the 12	2-bit inp	out ave	rage po	ower.										
Name							READ	_AVG	_PIN							
Format							Re	ad Wo	rd							
Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write		F	₹							R						
Default		(0							0x0	00					
Value																
Bits		Name				Descri	iption									
[15:12]		RESE	RVED													
[11:0]		READ	_AVG_	PIN												



BLACK_BOX_READ (E0h)

Command	d Code: E	-Oh										
Description	n: The co	ommand	retrieves	BLOCK	C_READ	data lat	ched on t	the first a	ssertion	of SMBA	<u> </u>	
Name					В	BLACK_E	BOX_REA	٩D				
Format						Bloc	k Read					
Bits	Byte 11	Byte 10	Byte 9	Byte 8	Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
Read/Wr ite	R	R	R	R	R	R	R	R	R	R	R	R
Default Value	0x	00	0x	00	0x	00	0x(00	0x	(00	Οχ	(00
Bits	Name				Descr	iption						
[95:80]	TEMP_	BLOCK										
[79:64]	PIN_B	LOCK										
[63:48]	VIN_B	LOCK										
[47:32]	VOUT	BLOCK										
[31:16]	IIN_BL	.OCK										
[15:0]	DIAGN	IOSTIC_	WORD									

READ_DIAGNOSTIC_WORD (E1h)

Comman				D.T.	24054												
Description	on: F	Returns	all of the	he RTC	ַ 1954	aults a						ction.					
Name							KEAL	_		TIC_V	VORD						
Format		D:: 45	D': 44	D:: 40	D': 40	D': 44	D': 40		ad Wo		D'' 0	D'' 5	D:: 4	D:: 0	D'' 0	D:: 4	D:: 0
Bits		Bit 15	Bit 14							Bit 7	Bit 6	Bit 5					Bit 0
Read/Wri	ite	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default Value		0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0
Bits	Nar	me					D	escrip	tion								
[15]	VO	UT_U\	/_WAR	N													
[14]	IIN_	_OP_V	VARN														
[13]	VIN	I_UV_\	NARN														
[12]	VIN	I_OV_\	WARN														
[11]	PC	WER_	GOOD														
[10]	OT.	_WARI	N														
[9]	TIM	1ER_L/	ATCHE	D_OFF	-												
[8]	EX	T_FET	_SHOR	RT													
[7]	CO	NFIG_	PRESE	Т													
[6]	DE,	VICE_0	OFF														
[5]	VIN	I_UV_F	FAULT														
[4]	VIN	I_OV_F	FAULT														
[3]	IIN_	_OC/PI	FET_O	P_FAU	LT												
[2]	OT.	_FAUL	Т.														
[1]	CM	L_FAL	JLT														
[0]	CB.	_FAUL	.T														



AVG_BLOCK_READ (E2h)

Commar	nd C	ode: E2h	l										
Descript	ion:	Concate	nates the	DIAGN	NOSIS_	WORD '	with all	the input	and ou	tput aver	age teler	netry da	ata and
tempera	ture.	1											
Name						A'	VG_BLC	CK_REA	AD				
Format							Block	k Read					
Bits		Byte 11	Byte 10	Byte 9	Byte 8	Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
Read/Wi	rite	R	R	R	R	R	R	R	R	R	R	R	R
Default Value		0x	00	0x	:00	0x	00	0x0	00	0x	00	0x0	880
Bits	Na	me				Descrip	tion						
[95:80]	TEI	MP1											
[79:64]	AV	G_PIN											
[63:48]	AV	G_VIN											
[47:32]	AV	G_VOUT	-										
[31:16]	AV	G_IIN											
[15:0]	DIA	AGNOST	IC_WORI	D									

READ_IIN_PEAK (EDh)

Command C	ode: El	Oh														
Description:	This co	mmand	d record	s the m	naximu	m value	of inp	out cur	rent.							
Name							REAL	D_IIN_	PEAK							
Format							Read	/Write	Word							
Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write			R							RW	'					
Default Value			0							0x00	0					
Bits		Name				Descri	iption									
[15:12]		RESE	RVED													
[11:0]		READ	_IIN_PE	EAK		Recore to clea						seen s	ince la	st res	et. Wı	rite 0

READ_IIN_MIN (EEh)

Command C	ode: E	Eh															
Description:	This co	mman	d record	ds th	ne r	minimu	m value	of inp	out cur	rent.							
Name								REA	D_IIN_	MIN							
Format								Read	/Write	Word							
Bits	Bit 15	Bit 14	Bit 13	Bit	12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write		F	₹								R۱	V					
Default Value		(0								0xF	FF					
Bits		Name					Descri	ption									
[15:12]		Name RESERVED															
[11:0]		READ	_IIN_N	1IN			Recor Write								since	e last	reset.



VOUT_UV_RETRY_THRESHOLD (EFh)

Commai	nd Co	de: EFh														
Descript	ion: Tl	nis com	mand s	ets the	voltage	thresh	old th	at the	RTQ19	954 wil	not re	estart u	ntil VC	DUT d	rops b	elow
this thre	shold.															
Name					•	VOUT_	UV_R	ETRY.	_THRE	SHOL	.D					
Format							Read	d/Write	Word							
Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/ Write			R							RW	I					
Default Value			0							0xFF	F					
Bits		Name				Descri	iption									
[15:12]		RESE	RVED													
[11:0]		VOUT ESHO	_UV_R LD	ETRY_	THR							il the \ T. Exp				

MFR_CL_THRESHOLD (F0h)

_		(- /							
Comma	nd Code: F0	h							
Descript	tion: This co	mmand sets	the OCP2	threshol	l in mV as me	easured acr	oss VIN_K-	SENSE.	
Name					MFR_CL_T	HRESHOL	D		
Format					Read/W	/rite Byte			
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/W	/rite	R	R	RW	RW	RW	RW	RW	RW
Default	Value	0>	(0			0	x0		
Bits	Name			Des	cription				
[7:6]	RESERVE	D							
					eshold = (MFI				
[5:0]	CL THRES	SHOLD		Ma	dimum value d	of this field i	s 45 (thresh	old of 55m	V). A write
[0.0]		SHOLD		with	a value over	45 will resu	ılt in		
				STA	TUS_CML.IN	NVALID_DA	TA setting.		

MFR_ADV_CFG_STATUS (F1h)

Comman				_	_				_								
Description	on: A	Illows fo	or config	guring	setting	s of the	RTC	21954 de	evice.								
Name							MF	FR_ADV	_CFG	_STA	TUS						
Format								Read	/Write	Word							
Bits		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 1	10 Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Wri	te	•	R		•		RW			R'	W		RW	RW	RW	RW	RW
Default Value	Pefault 0									C)		0	0	0	0	0
Bits	alue							Descrip	tion								
[15:12]	RE:	SERVE	D														
								Allows t faults.	he retr	y cour	nter to	reset	after a	perio	d of tii	ne wi	thout
[44.0]		· O - 4D -	4 D:					0 = rese	t retry	Cnt af	ter 1.3	s					
[11:9]	retr	yontke	esetPeri	oa				1 = rese	t retry	Cnt af	ter 2.6	s					
								2 = rese	t retry	Cnt af	ter 5.2	S					
								3 = rese	t retry	Cnt af	ter 10.	4s					



		≥ 4 is disabled: retryCnt will not reset
[8:5]	RESERVED	
[4]	PROCHOT_EN	If set, the PROCHOT output and STATUS_MFR_SPECIFIC are enabled.
[3]	vout_uv_thresh_pwrcycle_en	If set, the design will wait for VOUT to fall below VOUT_UV_RETRY_THRESHOLD before restarting after a POWER_CYCLE
[2]	vout_uv_thresh_operation_en	If set, the design will wait for VOUT to fall below VOUT_UV_RETRY_THRESHOLD before restarting after an OPERATION Off to On
[1]	vout_uv_thresh_uvlo_en	If set, the design will wait for VOUT to fall below VOUT_UV_RETRY_THRESHOLD before restarting after an UVLO Off to On or after OVLO event
[0]	vout_uv_thresh_fault_en	If set, the design will wait for VOUT to fall below VOUT_UV_RETRY_THRESHOLD before restarting after a fault off to on

MFR_ADV_PWRCYCLE_TIME (F2h)

	Command Code: F2b																
Command C	ode: F2	2h		•				•	•					•		•	•
Description:	Sets th	e powe	r cyc	e tim	er d	uratio	n in ms.	If the \	out_u	v_thre	esh_p	wrcycl	e_en b	oit in re	egistei	·F1h i	s set,
the RTQ1954	4 wait f	or the \	/OUT	to di	ор	below	VOUT_	UV_R	ETRY	_THR	ESHC)LD be	efore s	tarting	the ti	mer.	
Name							MFR_	ADV_F	PWRC	YCLE	_TIM	E					
Format		Read/Write Word															
Bits	Bit 15	t 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0															
Read/Write		RW															
Default								()x271(1							
Value								,	JAZ7 10								
Bits	Name Description																
[15:0]	PWRCYCLE_TIME This sets the duration of the power cycle timer, in milliseconds. Default is 10 seconds. Set to 0 to disable																

MFR_ADV_RETRY_TIMEOUT (F3h)

Command C	mand Code: F3h															
Description:	Sets th	e durat	ion of F	RETRY	in ms.											
Name						MFR_	ADV_I	RETR'	Y_TIM	1EOU	Τ					
Format							Read	/Write	Word							
Bits	Bit 15	it 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0														
Read/Write		RW														
Default Value								0x0								
Bits		Name Description														
[15:0]	RETRY_TIMEOUT This limits the duration of the fault retry, in milliseconds. Set to 0 to disable															



MFR_ADV_COOLDOWN_TIME (F5h)

		_														
Command C	ode: F	5h														
Description:	sets th	ne cool d	down ti	mer in r	ms that	t the R1	Q195	4 wait	s afte	er the I	ast RE	TRY :	attemp	ot befo	ore sta	arting
up.																
Name	ame MFR_ADV_COOLDOWN_TIME															
Format	nat Read/Write Word															
Bits	Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0															
Read/Write								RW								
Default Value		0x0														
Bits	Bits Name Description															
[15:0]	5:0] COOLDOWN_TIME Cooldown Time in milliseconds. Set to 0 to disable															

MFR_TELEM_CGF (F6h)

Command Co	de: F6h											
Description: T	his command is	used to co	nfigure	e the	telemetry	settings fo	r the RTC	Q1954.				
Name					MFR_TE	LEM_CGF	=					
Format					Read/W	rite Word						
Bits	Byte 1	Bit 7	Bit	6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
Read/Write	R	RW	R۱	Ν	RW	RW	RW	RW	RW	RW		
Default Value	0x00	0	1		0	1	1	1	1	1		
Bits	Name			Des	cription							
[15:8]	RESERVED											
7	TEMP_COMP	_RST			te 1 to resets back 0.	et the tem	perature	compensa	ation facto	r. Always		
6	TEMP_COMP	If set and INT_TEMP_TELEM_EN is set, then add measurements will be temperature compensated										
5	TELEM_OVER	R_SAMPLE		by a	is bit is set averaging raged with erated tele	4 samples n 2 samp	s togethe les and	r. All othe generated	er telemet d every 1	ry will be		
4	VAUX_TELEM	1_EN		Ena	bles VAUX	(telemetry	/ measure	ement				
3	VOUT_TELEM	1_EN		Ena	bles VOU	T telemetry	/ measure	ement				
2	VIN_TELEM_	N_TELEM_EN Enables VIN telemetry measurement. Enabling this bit plus VIN_TELEM_EN will generate a PIN measurement.										
1	IIN_TELEM_E	N			bles input TELEM_E					bit plus		
0	EXT_TEMP_T	EXT_TEMP_TELEM_EN Enables external temperature measurement										



MFR_HOTSWAP_STATUS (F9h)

	nd Code: F9	h s the state of the RTQ1	954 device	
Name		ine state of the first q.	MFR_HOTSWAP_STATUS	6
Format			Read/Write Block	-
Bits		Bit [23:17]	Bit [16:4]	Bit [3:0]
Read/W	rite	R	R	RW
Default '	Value	0	0	15
Bits	Name		Description	
[23:17]	RESERVE	D		
[16:4]	HOTSWAF	P_STATE		
[3:0]	HOTSWAF	P_OFF_REASON	Records the first reason why th value to this command to reset 0 = INSERTION 1 = FETSHORT 2 = VIN< POREN 3 = UVLO 4 = OVLO 5 = OT_FAULT 6 = FETFAULT 7 = Overcurrent 8 = Over power 9 = Circuit Breaker 10 = Pmbus Operation Comma 11 = Pmbus Power Cycle 12 = OTP Uncorrectable Error 13,14 = Reserved 15 = Armed	

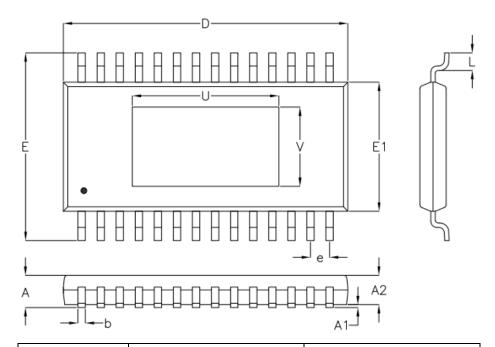


POWER_CYCLE (FBh)

	=												
Commar	nd Code: FB	h											
Descript	ion: Causes	the RTQ	1954 shut	down from	any state	and rema	ain off for	the time	defined by				
MFR_A	DV_PWRCY	CLE_TIME.							_				
Name	Name POWER_CYCLE												
Format	Format Send Byte												
Bits													
Read/W	rite	W	W	W	W	W	W	W	W				
Default \	/alue												
Bits	Name			Descr	iption								
NA POWER_CYCLE Causes the hot swap to shut down and remain off for the period of time defined by MFR_ADV_PWRCYCLE_TIME.													



19 Outline Dimension



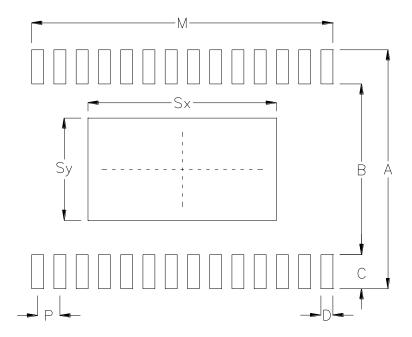
Symbo	s I	Dimensions	In Millimeters	Dimension	s In Inches
Syllibo	וכ	Min	Max	Min	Max
А		1.000	1.200	0.039	0.047
A1		0.000	0.150	0.000	0.006
A2		0.800	1.050	0.031	0.041
b		0.190	0.300	0.007	0.012
D		9.600	9.800	0.378	0.386
е		0.6	350	0.0)26
Е		6.300	6.500	0.248	0.256
E1		4.300	4.500	0.169	0.177
L		0.450	0.750	0.018	0.030
Ontion 1	כ	4.410	5.510	0.174	0.217
Option 1	V	2.400	3.000	0.094	0.118
Ontion 2	כ	5.500	6.170	0.217	0.243
Option 2	٧	1.600	2.210	0.063	0.087
Option 3	ט	5.800	6.200	0.228	0.244
Орион з	V	2.600	3.000	0.102	0.118

28-Lead TSSOP (Exposed Pad) Plastic Package

Note 16. The package of the RTQ1954 uses Option 1.



20 Footprint Information



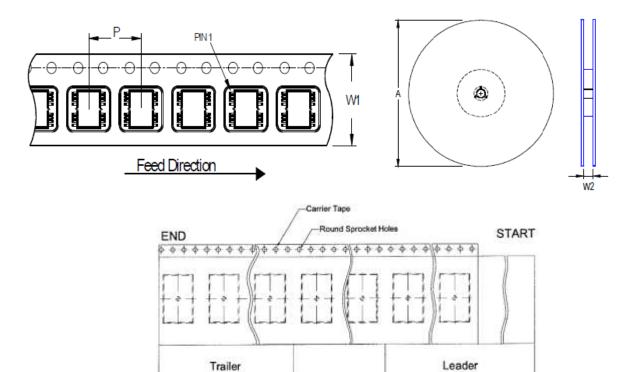
Dookoo	•	Number of			Foo	tprint	Dimen	sion (mm)		Tolerance
Packag	е	Pins	Р	Α	В	С	D	Sx	Sy	М	
	Option1							5.51	3.00		
TSSOP-28(PP)	Option2	28	0.65	7.00	5.00	1.00	0.35	6.17	2.21	8.80	±0.10
	Option3							6.20	3.00		

Note 17. The package of the RTQ1954 uses Option 1.



21 Packing Information

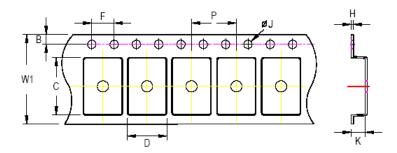
21.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Si	ze (A) (in)	Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
TSSOP-28	16	8	330	13	2,500	160	600	16.4/18.4

- Components -

160 mm minimum, -



- C, D, and K are determined by component size.

 The clearance between the components and the cavity is as follows:
- For 16mm carrier tape: 0.5mm max.

600 mm Minimum,

Tape Size	W1	F)	E	3	F	-	Ø	IJ	k	(Н
Tape Size	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
16mm	16.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.5mm	1.7mm	0.6mm

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21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	Reel 13"	4	1 reel per inner box Box G
2	HIC & Desiccant (2 Unit) inside	5	6 inner boxes per outer box
3	Caution label is on backside of Al bag	6	Outer box Carton A

Container	R	eel		Box			Carton	
Package	Size Units		Item	Reels	Units	Item	Boxes	Units
TSSOP-28	13" 2,500		Box G	1	2,500	Carton A	6	15,000



21.3 **Packing Material Anti-ESD Property**

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω /cm 2	10 ⁴ to 10 ¹¹					

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RTQ1954



22 Datasheet Revision History

Version	Date	Description
00	2025/9/25	First Edition