RICHTEK®

RTQ1962

80V, 20A Stackable eFuse with Fast Accurate Current Monitor

1 General Description

The RTQ1962 is a stackable eFuse that integrates several power components to provide high-current and high-voltage circuit protection in a compact form factor. With a simple application circuit, it protects against overloads, short-circuit faults, excessive inrush current and input overvoltage.

Start-up inrush current can be adjusted with a single external capacitor, and the active current limit during start-up with internal timer protects against start into short circuit. Steady state overcurrent protection with blanking timer and the fast overcurrent disconnect ensures robust protection while allowing transient overloads to pass through without disruption. Steady state overcurrent protection can be adjusted with a single resistor on the IMON pin.

The RTQ1962 provides fast and accurate current monitoring (IMON/ILIM) that allows for real-time power management (such as PSYS and PROCHOT) for optimized system performance in stacked or standalone eFuse operations. MOSFET health monitoring and reporting provides predictive maintenance.

Characterized to operate over a junction temperature range of –40°C to 125°C and available in 5mm ×6mm package, the RTQ1962 is well suited for enterprise applications.

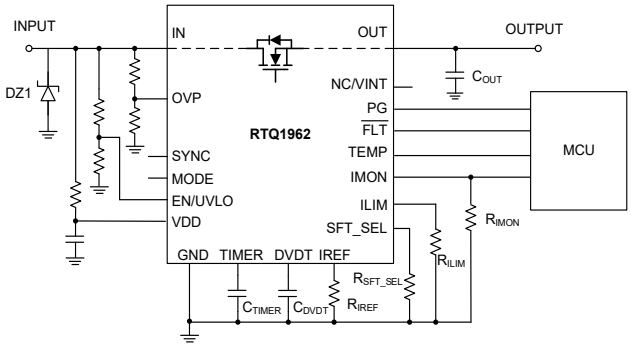
2 Features

- **20A Output Current Capability**
- **9V to 80V Input Operating Range**
  - **100V Input Absolute Maximum Voltage**
  - **-5V Output Voltage Tolerant**
- **3% Accurate Output Current Monitor with High Bandwidth (1MHz)**
- **Robust Overcurrent Protection**
  - **Start-up Active Current Limit with Internal Timer**
  - **Steady State Overcurrent Protection (OCP) with Adjustable Blanking Timer**
  - **Fast Overcurrent Trip for Short Circuit or Severe Overload Conditions**
- **Adjustable Overvoltage and Undervoltage Protection**
- **MOSFET Health Detection and Warning**
- **Over-Temperature (OTP) Protection with Analog Temp Output**
- **Support Parallel Connection of eFuses**
- **Fault and Power Good Outputs**
- **–40°C < T_J < 125°C Operation**
- **Small 5mm×6mm LQFN Package**

3 Applications

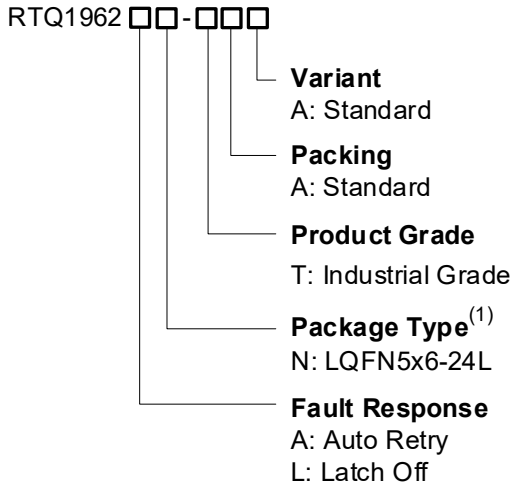
- Datacenter Servers, Switches, and Routers
- Cooling Fan Boards/Fan Trays
- GPU/xPU Add-in Cards
- Power Distribution Boards

4 Simplified Application Circuit



5 Ordering Information

5.1 Product Number Information



Note 1.

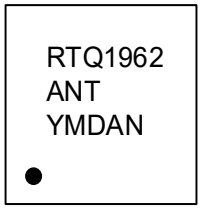
Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

5.2 Product Selection Table

Part Number	Fault Retry Behavior
RTQ1962AN-TAA	Auto Retry
RTQ1962LN-TAA	Latch Off

6 Marking Information

RTQ1962AN-TAA



RTQ1962AN: Product Code
YMDAN: Date Code

RTQ1962LN-TAA

RTQ1962LN: Product Code
YMDAN: Date Code

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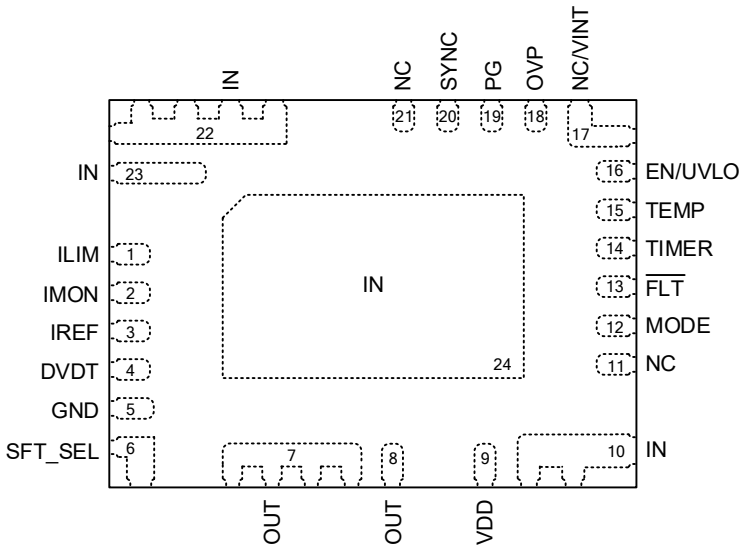
7 Pin Configuration

(TOP VIEW)



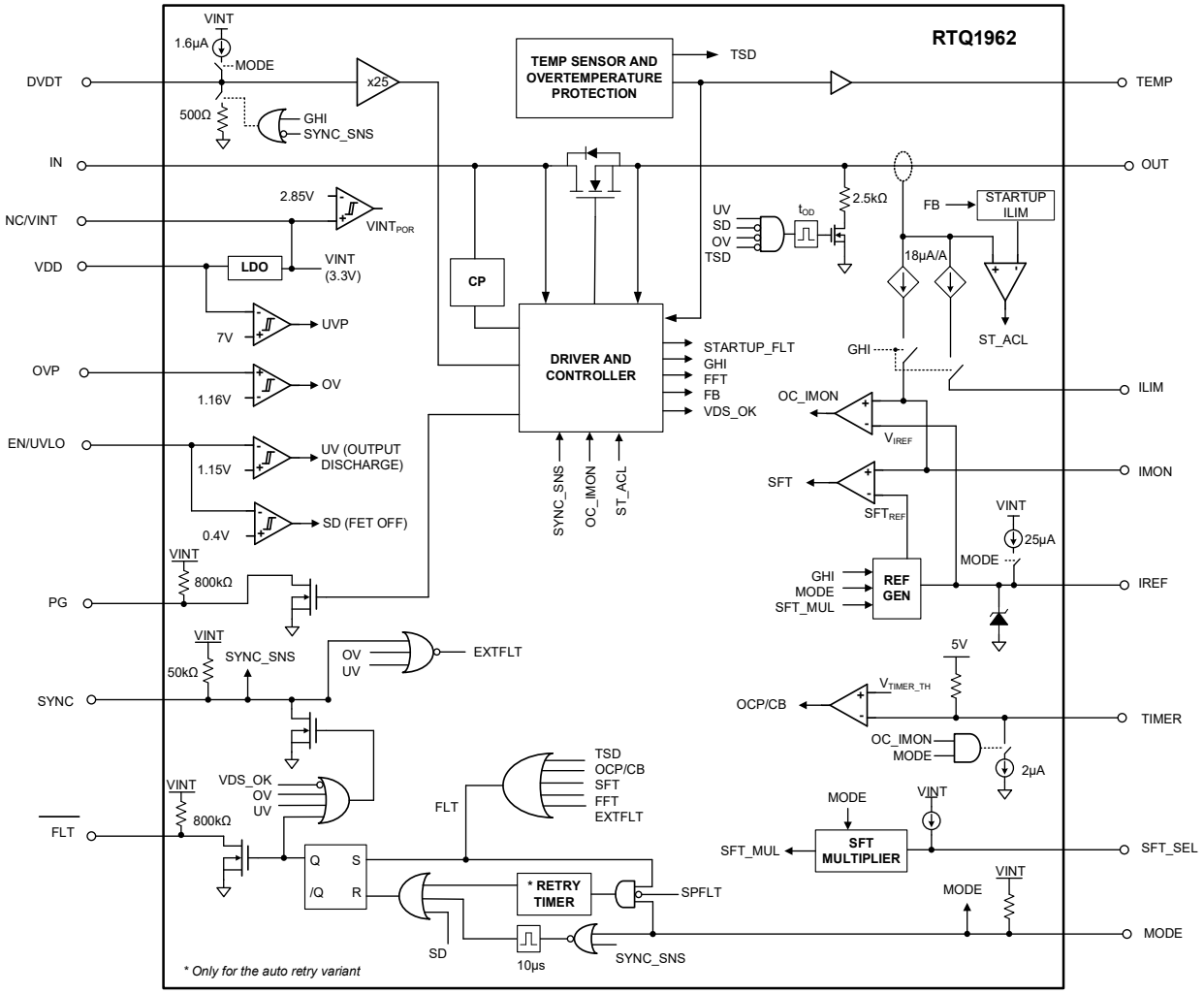
LQFN5x6-24L

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	ILIM	Current Monitor pin outputs 18.2μA/A of output current during steady state. An external resistor from this pin to GND provides voltage gain of individual eFuse current. *Do not leave floating.*
2	IMON	Current Monitor pin outputs 18.2μA/A of output current during steady state. A resistor to GND sets the overcurrent threshold as well as the fast trip threshold during normal operation. *Do not leave floating.*
3	IREF	Adjustable reference voltage for the overcurrent protection modes (steady state overcurrent circuit breaker and short circuit protection) using the internal current and an external resistor or driven from an external supply. *Do not leave floating.*
4	DVDT	V_{OUT} dV/dt soft-start control pin. Connect a capacitor to GND to adjust inrush current or output voltage slew rate.
5	GND	Device ground.
6	SFT_SEL	Scalable fast trip current multiplier pin selects the ratio between the circuit breaker threshold and the fast trip threshold. Not recommended to leave this pin floating.
7,8	OUT	Power output. Connect OUT using wide traces for high-current capability and maximum thermal dissipation.
9	VDD	Power supply for internal circuitry. Connect to V_{IN} through an R-C network to provide a low noise filtered supply voltage.
10, 22, 23, 24	IN	Power input. The exposed pad of the device is also connected to IN. Must be soldered to a large IN copper pour for best thermal performance.
11, 21	NC	No connect.
12	MODE	MODE pin configures the device a standalone or primary eFuse (leave pin floating) or as a secondary eFuse in a parallel chain (connect to GND).
13	$\overline{FLT}$	Open-drain Fault pin. Connect to an external pull-up resistor for an active low fault output.
14	TIMER	Overcurrent protection (circuit breaker) blanking timer pin. Connect a capacitor from this pin to GND to set the blanking time interval. Output current can exceed the I_{OCP} threshold for this duration without an overcurrent response (provided current is still lower than the fast-trip short circuit threshold).

Pin No.	Pin Name	Pin Function
15	TEMP	Temperature monitor pin. The analog output voltage is proportional to the die temperature and can be combined with other eFuse TEMP outputs for the peak device die temperature monitoring in parallel connection.
16	EN/UVLO	Enable input pin. A resistor divider from V_{IN} can set a precision undervoltage lock-out enable threshold.
17	NC/VINT	No connect pint. This pin is internal sub-regulator 3.3V output pin. An external capacitor is optional to this pin. Use only for connecting pull-up resistors.
18	OVP	Overvoltage protection input pin. Connect a resistor divider from V_{IN} to this pin to set the overvoltage protection threshold.
19	PG	Open-drain power good output. This pin assumes a high impedance state when soft-start is completed and the internal MOSFET is fully enhanced.
20	SYNC	Device status and control pin. The open-drain pin can be used for switch status as well as controlling the power switch state allowing for synchronized control in parallel device applications.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- IN, VDD to GND ---------- –0.3V to 100V
- OUT to GND ---------- –5V to 100V
- IN to OUT ---------- –0.3V to 82V
- IMON, ILIM, SFT_SEL, TIMER, MODE to GND (Internally Limited) ---------- –0.3V to 5V
- TEMP to GND ---------- –0.3V to 3.3V
- All Other Pins ---------- –0.3V to 5.5V
- Maximum PG, SYNC, $\overline{FLT}$ Sink Current ---------- 10mA
- Junction Temperature (Internally Limited), T_J ---------- 150°C
- Storage Temperature Range, T_{STG} ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

ESD Susceptibility

- HBM (Human Body Model) ---------- ±2KV
- CDM (Charged Device Model) ---------- ±500V

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Input Voltage Range, V_{IN} ---------- 9V to 80V
- Maximum Output Voltage, V_{OUT} ---------- V_{IN}
- Supply Voltage Range, V_{VDD} ---------- 9V to 80V
- Maximum Soft-start Pin Cap Voltage Rating, V_{DVDT} ---------- 4V
- Maximum EN/UVLO Pin Voltage, $V_{EN/UVLO}$ ---------- 5V
- Maximum TEMP Pin Voltage, V_{TEMP} ---------- 3.3V
- Maximum PG, $\overline{FLT}$ Pins Pull-up Voltages, V_{PG}, $V_{\overline{FLT}}$ ---------- 5V
- Maximum SYNC Pin Pull-up Voltage, V_{SYNC} ---------- 5V
- IREF Pin Voltage, V_{IREF} ---------- 0.3V to 1.2V
- Maximum ILIM Pin Voltage, V_{ILIM} ---------- 0.4V
- Maximum IMON Pin Voltage, V_{IMON} ---------- 1.2V
- Maximum Continuous Output Current, I_{OUT} ($T_J \leq 125°C$) ---------- 20A
- Peak Output Current $I_{OUT\text{-}Pulse}$ (duration ≤ 10ms, $T_A \leq 70°C$) ---------- 27A
- Junction Temperature Range, T_J ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Characteristics

(Note 5 and Note 6)

Thermal Parameter		LQFN5x6-24L	Unit
θ_{JA}	Junction-to-ambient thermal resistance	30	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	26	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	0.59	°C/W
θ_{JB}	Junction-to-board thermal resistance	13.7	°C/W
$\Psi_{JC(Top)}$	Junction-to-case (top) characterization parameter	0.5	°C/W
$\Psi_{JC(Bottom)}$	Junction-to-case (bottom) characterization parameter	0.63	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.2	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. Simulated based on JEDEC 51-7 on a high effective-thermal-conductivity four-layer (2s2p) test board at 25°C and still air; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

Unless otherwise stated, the following conditions apply: –40°C ≤ TJ ≤ 125°C, V_{IN} = VDD = 50V, OUT=Open, V_{IREF} = 1V, $\overline{FLT}$ = 33KΩ pull-up to 3.3V, PG = 33KΩ pull-up to 3.3V, C_{OUT} = 10μF, MODE = Open, $V_{EN/UVLO}$ = 2V, DVDT = Open, TIMER = Open, TEMP = Open.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply (VDD and IN)						
Input Voltage Range	V_{IN}		9		80	V
Input Supply Voltage Range	VDD		VIN		80	V
VDD Pin ON State Quiescent Current	I_{VDD-ON}	VDD > VDD_{UV-R}, V_{EN} ≥ V_{ENH-R}, V_{OVP} < V_{OVP-F}	--	1.2	4	mA
VDD Pin FET OFF Quiescent Current	$I_{VDD-OFF}$	V_{EN} = 0V	--	0.9	1.75	mA
VDD Undervoltage Rising Threshold	VDD_{UV-R}		--	8.5	8.9	V
VDD Undervoltage Falling Threshold	VDD_{UV-F}		6.7	7	--	V
IN Pin ON State Current	I_{IN-ON}	V_{EN} ≥ V_{ENH-R}, V_{OVP} < V_{OVP-F}	--	1	5	mA
IN Pin FET OFF Quiescent Current	I_{IN-OFF}	V_{EN} = 0V	--	0.21	0.5	mA
Enable and Undervoltage Protection (EN/UVLO)						
Enable High Rising Threshold	V_{ENH-R}	EN/UVLO Rising - device turn ON	1.21	1.27	1.32	V
Enable High Falling Threshold	V_{ENH-F}	EN/UVLO Falling – partial shutdown, FET OFF	1.06	1.12	1.15	V
Enable Low Rising Threshold	V_{ENL-R}	EN/UVLO Rising – partial ON	--	0.53	0.59	V
Enable Low Falling Threshold	V_{ENL-F}	EN/UVLO Falling – FET OFF	0.325	0.42	--	V
Enable Pin Leakage Current	I_{ENLKG}		–100	--	100	nA
Overvoltage Protection (OVP)						
Overvoltage Rising Threshold	V_{OVP-R}	OVP Rising	1.14	1.17	1.2	V
Overvoltage Falling Threshold	V_{OVP-F}	OVP Falling	1.08	1.11	1.15	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OVP Pin Leakage Current	I_{OVPLKG}		-100	--	100	nA
Output Pin (OUT)						
OUT Leakage Current	I_{OUTLKG}	V_{EN} = 0V, V_{OUT} = 0V	--	13	--	μA
ON Resistance (IN-OUT)						
Switch ON State Resistance	R_{ON}	I_{OUT} = 10A, T_J=25°C	--	3.8	5.75	mΩ
		I_{OUT} = 10A, T_J= -40°C to 125°C	--	--	8.65	
Start-Up Active Current Limit (ACL)						
Start-Up Active Current Limit	I_{ACL}	V_{OUT} > 2V (foldback voltage)	--	4	--	A
		V_{OUT} ≤ 2V (foldback voltage)	--	1	--	
Foldback Voltage	V_{FB}		1.9	2	2.1	V
Steady-State Current Monitor (ILIM)						
Current Monitor Gain vs I_{OUT}	G_{ILIM}	PG asserted (steady state), I_{OUT} = 10A	17	18.2	20.6	μA/A
Steady-State Current Monitor (IMON) and Overcurrent Protection (OCP)						
Current Monitor Gain vs I_{OUT}	G_{IMON}	PG asserted (steady state), 10A ≤ I_{OUT} ≤ 20A,	17.52	18.2	18.84	μA/A
		PG asserted (steady state), 10A ≤ I_{OUT} ≤ 20A, 25°C ≤ T_J ≤ 125°C	17.62	18.2	18.73	
		PG asserted (steady state), 10A ≤ I_{OUT} ≤ 20A, T_J = 25°C	17.85	18.2	18.7	
		PG asserted (steady state), I_{OUT} = 4A	16.82	18.15	19.45	
		PG asserted (steady state), I_{OUT} = 4A 25°C ≤ T_J ≤ 125°C	17.32	18.15	19	
		PG asserted (steady state), I_{OUT} = 4A T_J = 25°C	17.34	18.15	18.96	
Adjustable Overcurrent Protection (Circuit Breaker) Threshold (Note 7)	I_{OCP}	R_{IMON} = 2.55KΩ, V_{IREF} = 1V	20.5	21.5	22.5	A
OCP Blanking Timer (TIMER)						
TIMER Threshold FET Turn OFF	ΔV_{TIMER}	I_{OUT} > I_{OCP}, TIMER Falling	1.28	1.5	1.8	V
TIMER Internal Pull-Up Resistance	R_{TIMER}	Pull-up to $VINT_{TMR}$	10	12.5	15	kΩ
TIMER Internal Pull-Up Voltage	$VINT_{TMR}$	I_{OUT} < I_{OCP}	4.6	5	5.4	V
TIMER Internal Discharge Current Sink	I_{TIMER}	I_{OUT} > I_{OCP}, TIMER Falling	1.6	2	2.6	μA
TIMER Discharge Voltage to Current Ratio	$\Delta V_{TIMER}/I_{TIMER}$		0.38	0.75	1.13	V/μA
IREF (Pin)						

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IREF Recommended Voltage Range	V_{IREF}		0.3	--	1.2	V
IREF Internal Source Current	I_{IREF}	V_{IREF} = 1V	22	25	26.2	µA
Fast Turn Off Short Circuit Protection						
Fixed Fast Turn Off Threshold (Note 8)	I_{FFT}	PG asserted (steady state)	--	85	--	A
Scalable Fast Turn Off Threshold	I_{SFT}	PG asserted (steady state), R_{SFT_SEL} < 195kΩ, MODE = OPEN	--	2.5× I_{OCP}	--	A
		PG asserted (steady state), R_{SFT_SEL} < 195kΩ, MODE = GND	--	2.75× I_{OCP}	--	
		PG asserted (steady state), 205KΩ <R_{SFT_SEL} < 295kΩ, MODE = OPEN	--	2×I_{OCP}	--	
		PG asserted (steady state), 205KΩ <R_{SFT_SEL} < 295kΩ, MODE = GND	--	2.25× I_{OCP}	--	
		PG asserted (steady state), 305kΩ <R_{SFT_SEL}, MODE = OPEN	--	1.5× I_{OCP}	--	
		PG asserted (steady state), 305kΩ <R_{SFT_SEL}, MODE = GND	--	1.75× I_{OCP}	--	
Soft-Start and Inrush Current Limit (DVDT)						
DVDT Charging Current	I_{DVDT}	Primary (MODE = OPEN)	1.3	1.65	2	µA
DVDT Leakage Current	$I_{DVDT-LKG}$	Secondary (MODE = GND)	--	10	--	nA
DVDT Gain	G_{DVDT}	0.4V < V_{DVDT} < 2.4V	17	25	28	V/V
DVDT Pull-Down Resistance	R_{DVDT}	Discharge resistance to GND	--	500	--	Ω
MOSFET OFF Output Discharge						
Internal Output Discharge	I_{OD}	Through internal resistor to GND, V_{OUT}=50V	10	13	16	mA
		Through internal resistor to GND, V_{OUT}=12V	7	9.5	12	
Temperature Monitor Output (TEMP)						
TEMP Sensor Gain	G_{TEMP}		--	2.7	--	mV/°C
TEMP Output Voltage	V_{TEMP}	T_J = 25°C	670	685	700	mV
TEMP Sourcing Current	$I_{TEMP-SRC}$		200	230	250	µA
TEMP Sinking Current	$I_{TEMP-SNK}$		7	10	14	µA
Over-Temperature Protection (OTP)						
Thermal Shutdown Rising Threshold	TSD	T_J Rising	--	150	--	°C
Thermal Shutdown Hysteresis	TSD_{HYS}	T_J Falling	--	30	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
FET Health Monitor						
V_{IN}-V_{OUT} FET Short Threshold	V_{FET_SHORT}	At the end of debounce time, SYNC=L	--	6	--	V

Note 7. I_{OCP} threshold value derived from G_{IMON} value range.

Note 8. Guaranteed by design.

14.1 Logic Interface

Unless otherwise stated, the following conditions apply: –40°C ≤ TJ ≤ 125°C, V_{IN} = VDD = 50V, OUT=Open, V_{IREF} = 1V, $\overline{FLT}$ = 33KΩ pull-up to 3.3V, PG = 33KΩ pull-up to 3.3V, C_{OUT} = 10μF, MODE = Open, $V_{EN/UVLO}$ = 2V, DVDT = Open, TIMER = Open, TEMP = Open.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SYNC						
SYNC Pull-Down Resistance	R_{SYNC}	SYNC de-asserted low	--	20	--	Ω
SYNC Leakage Current	$I_{SYNC-KG}$	SYNC asserted high, pulled up to 3.3V	--	0.02	--	μA
Fault Indication ($\overline{FLT}$)						
$\overline{FLT}$ Pull-Down Resistance	R_{FLTB}	$\overline{FLT}$ asserted low	--	9	--	Ω
$\overline{FLT}$ Leakage Current	$I_{FLT-LKG}$	$\overline{FLT}$ de-asserted high, pulled up to 3.3V through 33KΩ	--	0.02	--	μA
Power Good (PG)						
PG Pull-Down Resistance	R_{PG}	PG de-asserted low	--	9	--	Ω
PG Leakage Current	I_{PG-LKG}	PG asserted high, pulled up to 3.3V through 33KΩ	--	0.02	--	μA

14.2 Timing Characteristics

Unless otherwise stated, the following conditions apply: –40°C ≤ TJ ≤ 125°C, V_{IN} = VDD = 50V, OUT=Open, V_{IREF} = 1V, $\overline{FLT}$ = 33KΩ pull-up to 3.3V, PG = 33KΩ pull-up to 3.3V, C_{OUT} = 10μF, MODE = Open, $V_{EN/UVLO}$ = 2V, DVDT = Open, TIMER = Open, TEMP = Open. (Note 9)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Debounce (Insertion) Delay	t_{DBNS}	V_{EN} > V_{ENH-R} to SYNC rising	--	10	--	ms
Fixed Fast Turn OFF Response Time	t_{FFT}	V_{IN}-V_{OUT} > V_{DSCOMP} to FET turn off	--	400	--	ns
Scalable Fast Turn OFF Response Time	t_{SFT}	I_{OUT} > 3 x I_{OCP} to I_{OUT} falling	--	400	--	ns
Adjustable Overcurrent Blanking Timer	t_{TIMER}	I_{OUT} = 1.5x I_{OCP}, C_{TIMER} = 4.7nF	--	3.5	--	ms
		I_{OUT} = 1.5 x I_{OCP}, C_{TIMER} open	--	0	--	ms
		I_{OUT} = 1.5 x I_{OCP}, V_{TIMER}>$V_{TIMER-TH}$	--	12	--	ms
Overvoltage Protection Response Time	t_{OVP}	V_{OVP} > V_{OVP-R} to SYNC falling	--	2	--	μs
Overvoltage Wait Time	t_{OVP_WIAT}	Minimum time from OVP detection until retry	--	60	--	μs

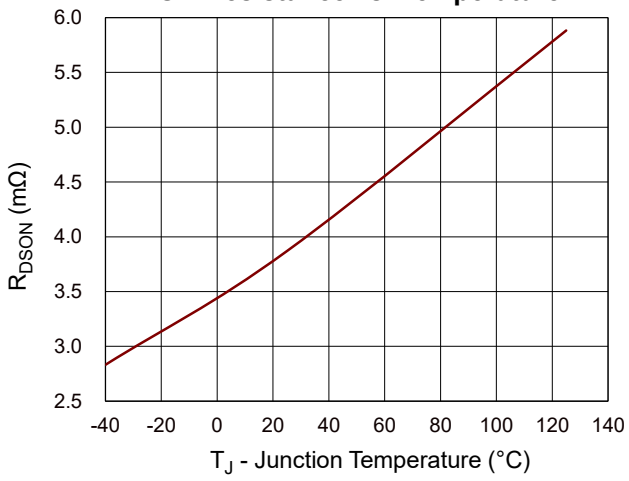
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Start-Up Active Current Limit Period	t_{ACL}	V_{IN}-V_{OUT} > 1V	--	250	--	μs
Startup Total Allowable Time	t_{ST-MAX}	From start of debounce time to PG rising	--	5	--	s
Output Discharge Enable Timer	t_{OD}	V_{ENL-F} < $V_{EN/UVLO}$ < V_{ENH-F}	--	16	--	μs
Discharge Time	$t_{Discharge}$	V_{ENL-F} < $V_{EN/UVLO}$ < V_{ENH-F} for 16μs, C_{OUT}=0.5mF, 90% to 10%	--	1.27	--	s
Retry Cool Down Time	t_{RETRY}	Retry interval in steady state (Auto Retry variant)	--	680	--	ms

Note 9. Guaranteed by design.

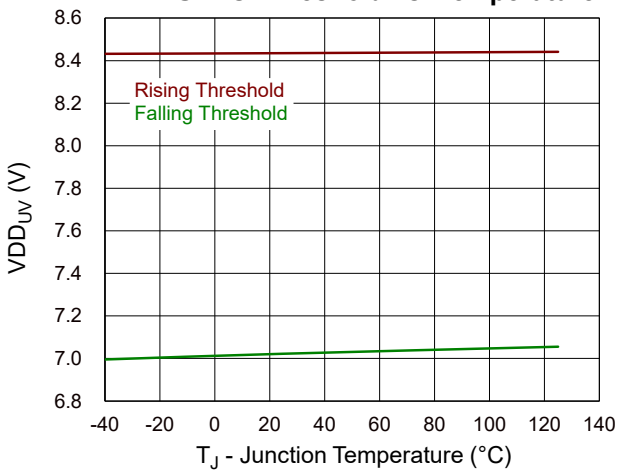
15 Typical Characteristics Curves

Unless otherwise stated, the following conditions apply: V_{IN} = 50 V, T_J = 25°C.

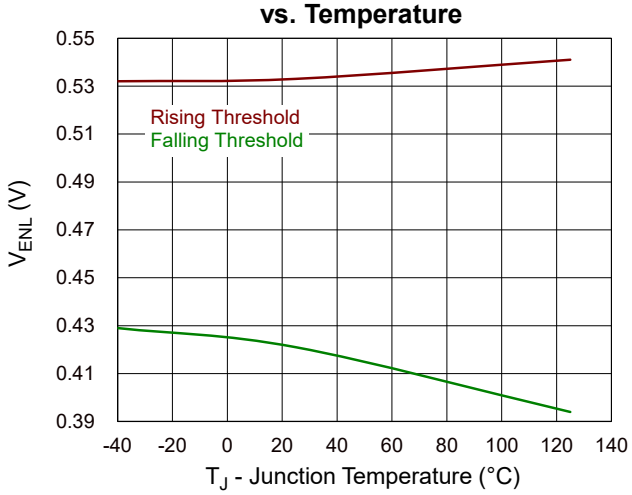
ON Resistance vs. Temperature



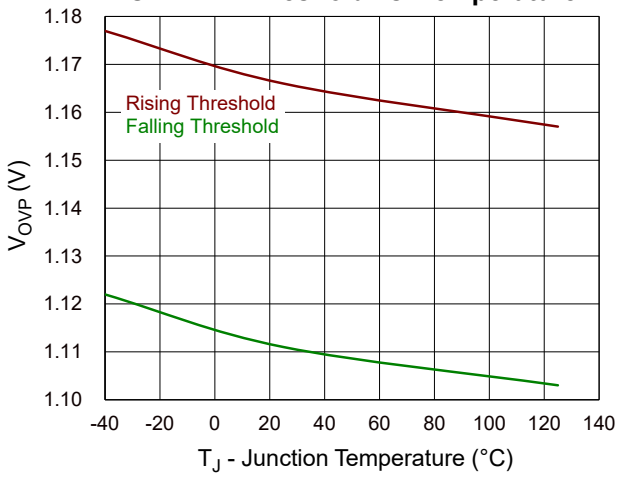
VDD UVLO Threshold vs. Temperature



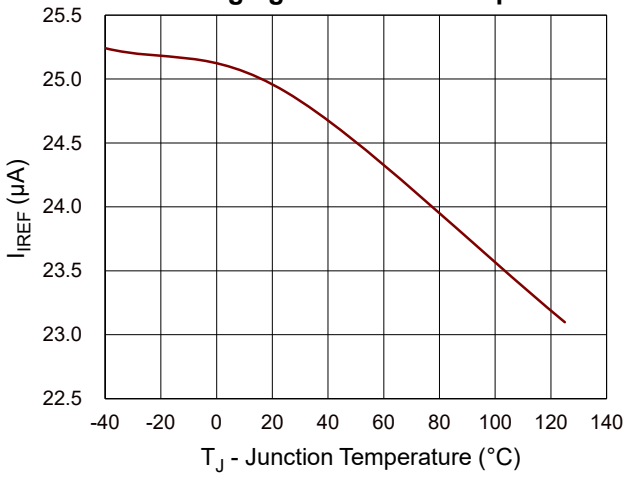
Enable Based Shutdown Threshold vs. Temperature



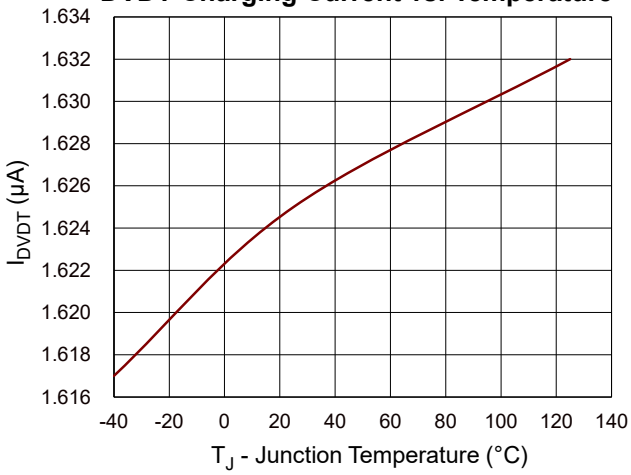
OVP Pin Threshold vs. Temperature

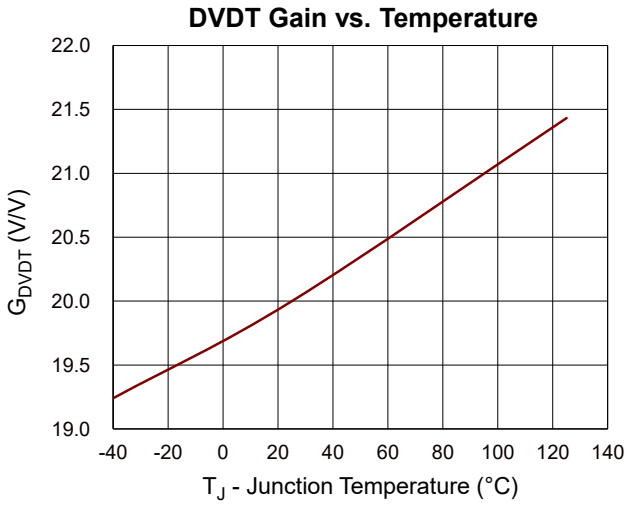


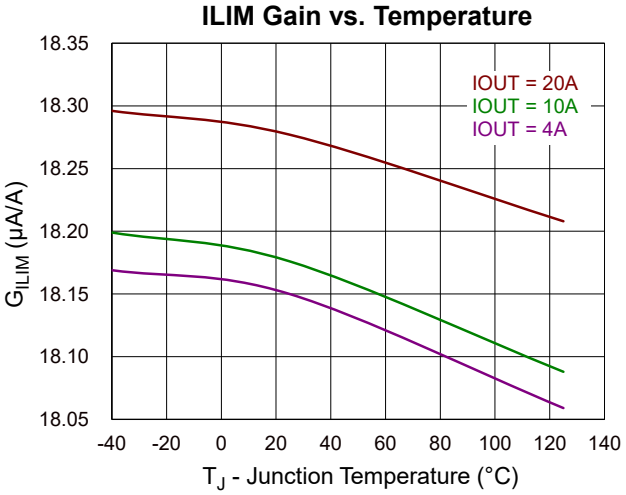
IREF Charging Current vs. Temperature

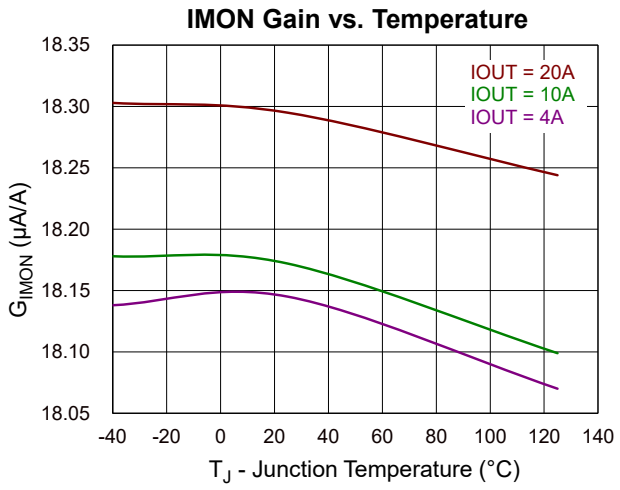


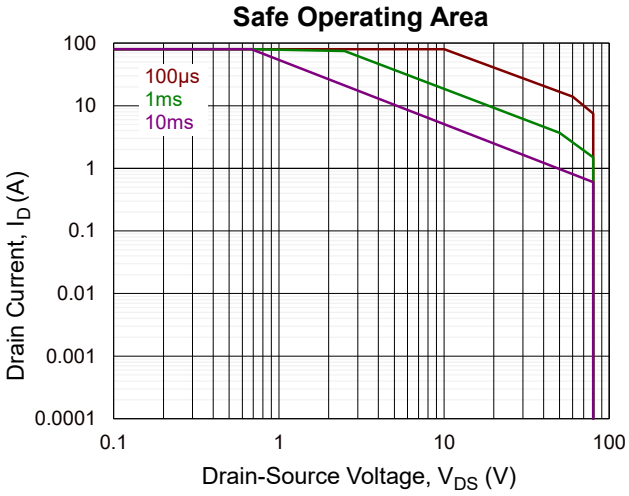
DVDT Charging Current vs. Temperature



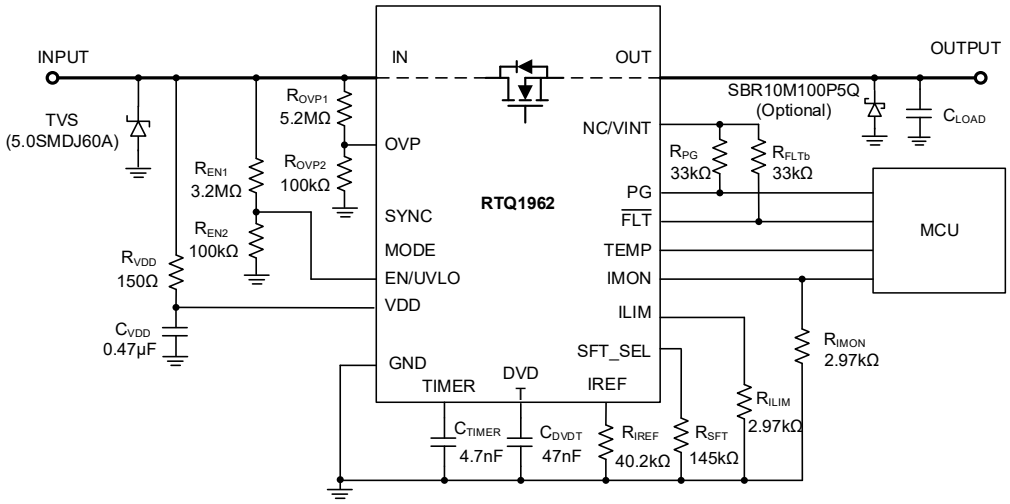




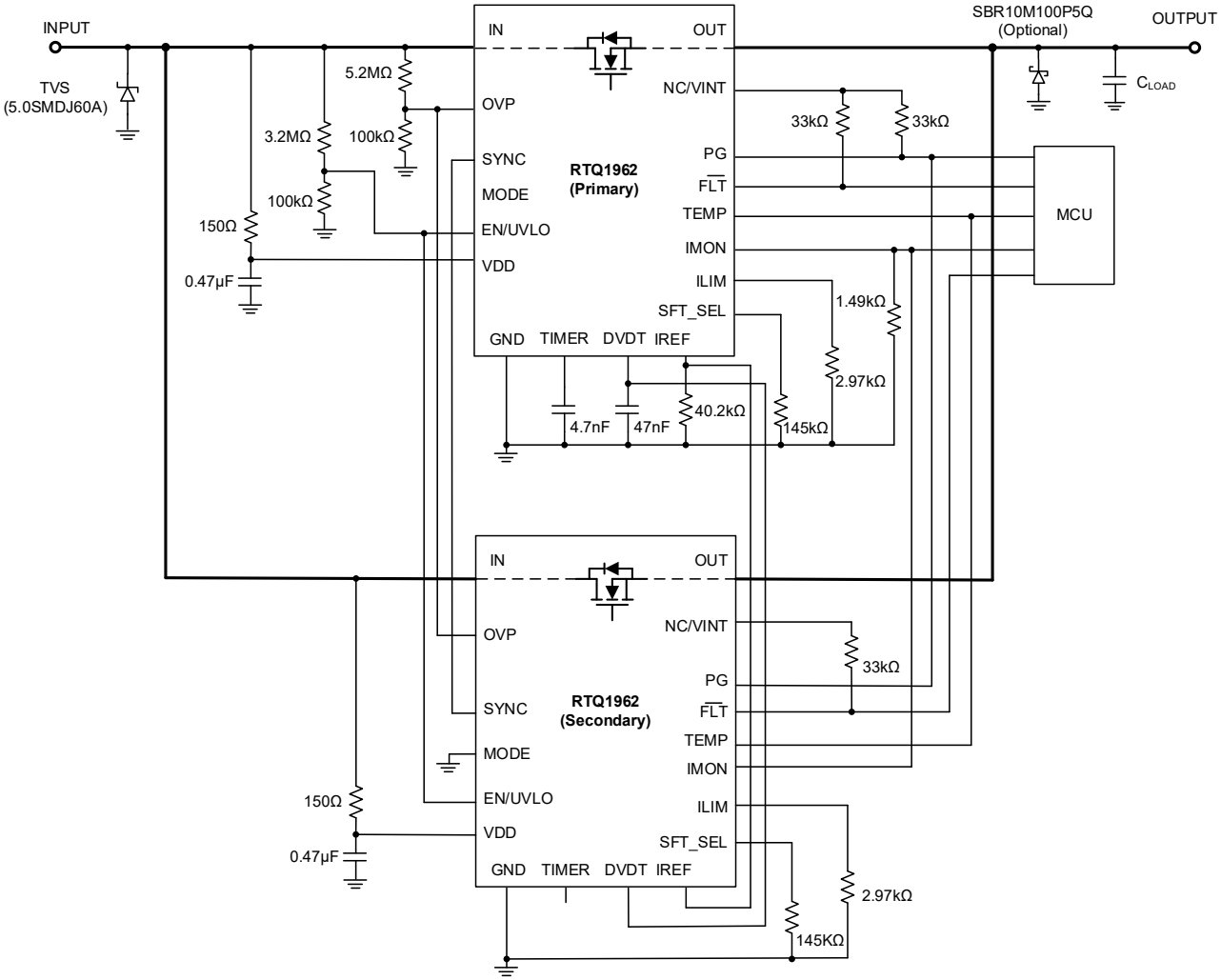




16 Typical Application Circuit



Typical Application Circuit in Standalone Operation



Typical Application Circuit with two RTQ1962 eFuses in Parallel, Primary-Secondary

17 Application Information

(Note 10)

17.1 Overview

The RTQ1962 is a stackable eFuse that integrates several power components to provide high-current and high-voltage circuit protection in a compact form factor. With a simple application circuit, it protects against overloads, short circuit faults, excessive inrush current and input overvoltage.

The RTQ1962 implements adjustable output slew rate control to limit the inrush current during start-up, preventing failure when plugging into large capacitive loads. It also provides start-up active current limit with internal timer to protect against starting into short circuit and potential thermal runaway.

The RTQ1962 protects against input voltage fluctuations using overvoltage and undervoltage lock-out mechanism. The internal MOSFET temperature is continuously monitored and protected using over-temperature protection. While the MOSFET health monitoring and reporting provides predictive maintenance.

During operation, the RTQ1962 provides multiple overcurrent protections that can be adjusted for specific load profiles. The adjustable circuit breaker overcurrent protection with adjustable blanking timer ensures transient surges pass through while protecting against sustained overcurrent events. And flexible and fixed fast turn off mechanism protects against short circuit events.

For high-power applications, multiple RTQ1962 eFuse can be connected in parallel in a synchronous operation. Accurate current sensing (IMON/ILIM) is provided to enable real-time power management (e.g. Intel PSYS and PROCHOT) for optimized system performance in enterprise applications. The IMON pin is used to adjust overcurrent protection during normal operation for standalone or stacked eFuses. While the secondary current sense pin, ILIM can be used to monitor individual eFuse currents.

17.2 Start-Up Sequence

As the input voltage V_{IN} rises above its internal threshold of 8.5V (VDD_{UV-R}), the RTQ1962 enters standby mode while the FET is kept OFF and the internal voltage VINT rising to a regulated voltage of 3.3V.

After the VINT goes above the POR threshold (2.85V rising threshold with 100mV hysteresis) and $V_{EN}>V_{ENH-R}$ and V_{IN} is below V_{OVP}, the RTQ1962 enters the start-up mode and 10ms debounce timer (t_{DBNS}) starts, Figure 1. The debounce (or insertion) delay is to make sure the input supply has been stabilized before turning ON the device. During the debounce time, the output is pulled low.

17.3 FET Health Detection and Warning

At the end of debounce time and before turning ON the MOSFET, the RTQ1962 checks on the internal MOSFET short by making sure V_{IN}-V_{OUT} is above the FET_SHORT threshold of 6V and asserts SYNC; otherwise, it will return to the start-up mode and start another debounce time. During this time the $\overline{FLT}$ pin is at high-Z state. If the FET_SHORT condition exists for 5s (t_{ST-MAX}), the $\overline{FLT}$ pulls low indicating fault condition and the device latches off. The part can restart by pulling EN low or input power cycle.

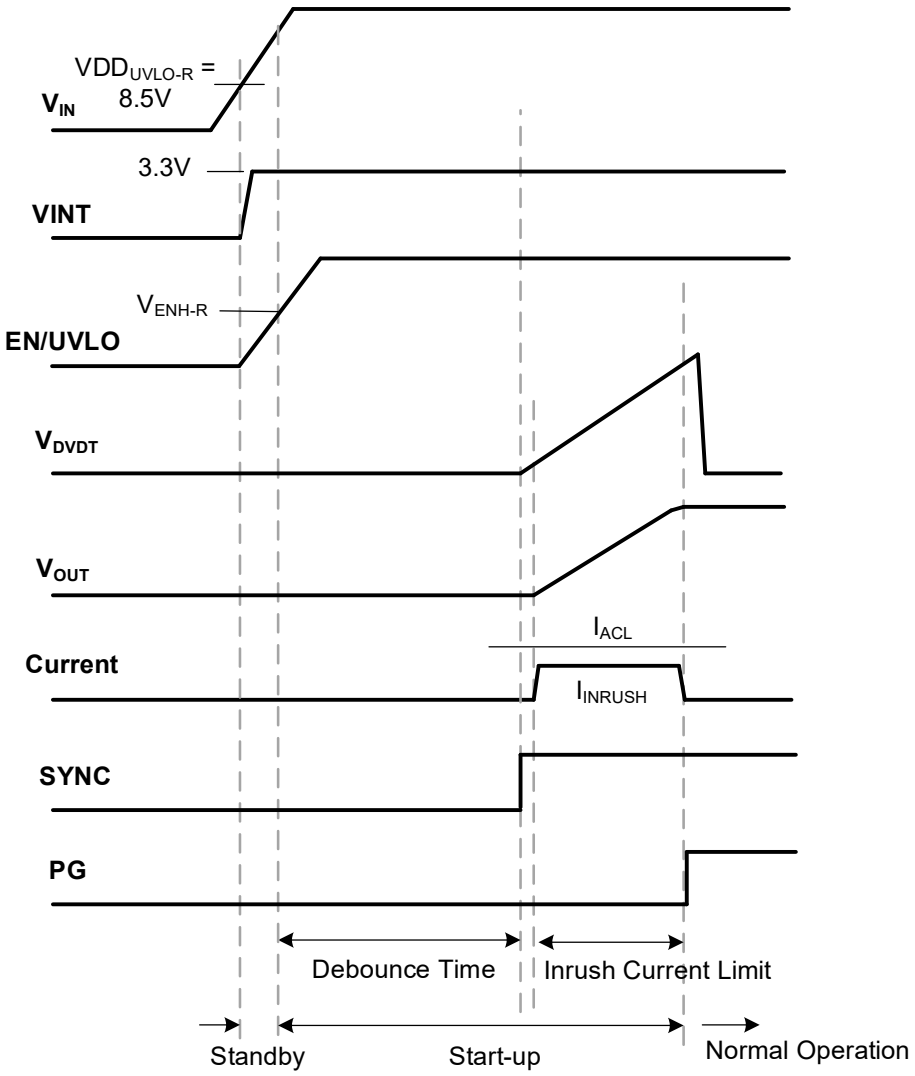


Figure 1. Start-Up Sequence with EN/UVLO Connected to VIN Through Resistive Divider

17.4 Overcurrent Protection

RTQ1962 incorporates three levels of overcurrent protection as follows:

- Pre-defined active current limit during start-up (I_{ACL}) with 250µs timer
- Adjustable steady state overcurrent protection (I_{OCP}) with blanking timer (t_{TIMER})
- Fixed and scalable fast turn off short circuit protection (I_{SFT} and I_{FFT})

17.5 Start-Up Inrush Current Control and Active Current Limit (ACL)

During hot plugs into large output capacitance, a large inrush current can damage the input supply connectors and cause input supply droop. The inrush current is directly proportional to output capacitance and the V_{OUT} slew rate. For a given load capacitance, the required slew rate can be determined according to:

$$SR\ (V/ms) = \frac{I_{INRUSH}(A)}{C_{OUT}(mF)}$$

The V_{OUT} rising slew rate can be adjusted by connecting a capacitor to the DVDT pin of RTQ1962 to lower the inrush current. The required C_{DVDT} capacitance for a given slew rate can be determined by:

$$C_{DVDT}(nF)=\frac{41}{SR(V/ms)}$$

During startup, the inrush current value, set by C_{DVDT}, C_{OUT} and slew rate, should be set lower than the active current-limit threshold I_{ACL} (I_{INRUSH} <I_{ACL}) to allow for charging the output cap without triggering the ACL timer (t_{ACL}). Leaving DVDT pin open will lead to fastest output slew rate.

To protect the MOSFET from getting over-stressed during start-up, the RTQ1962 implements active current limiting that regulates the current at I_{ACL} when current exceeds the limit threshold, Figure 2. During current regulation, the output voltage drops, resulting in increased power dissipation in the MOSFET. Therefore, the RTQ1962 employs foldback mechanism during start-up based on the output voltage value. The active current limit servos the current to I_{ACL} = 4A when V_{OUT} is above foldback voltage of 2V. In the low impedance short situation, where V_{OUT} stays below 2V, the I_{ACL} level is reduced to 1A to further protect the device. When the RTQ1962 goes into ACL, the internal timer t_{ACL} starts. If the current limiting condition disappears before 250µs t_{ACL} timer expires, the internal timer is gradually reset with a fraction (10%) of the ramp-up speed. This will help reduce the stress on the MOSFET if there is an immediate ACL event by reducing the time it takes for the not-fully-reset t_{ACL} timer to timeout. If the current limit condition stays longer than the t_{ACL} timer, the MOSFET turns off, and $\overline{FLT}$ and SYNC pins pull low. The device will retry or will remain latched-off depending on the configuration.

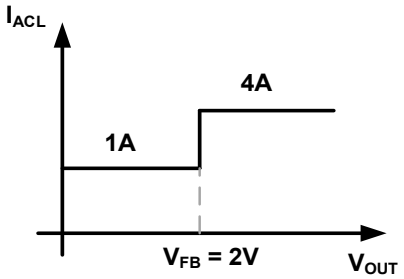


Figure 2. Start-Up Protection Mechanism with Foldback Voltage

17.5.1 Start-Up Maximum Timeout

The RTQ1962 has a maximum start-up timeout protection mechanism that latches off if the device fails to move past start-up into normal operation within t_{ST-MAX} of 5s. The conditions that can cause this include persistent ACL retry (retry variant), FET_SHORT at the end of debounce time, and persistent OVP. After the maximum timeout latch off, the part can restart by pulling EN low or input power cycle.

17.6 Analog Current Monitoring (IMON and ILIM)

The RTQ1962 provides high bandwidth and accurate analog current monitoring output (IMON) that can be used for system power management. The current signal through the IMON pin is proportional to the current flowing through the internal MOSFET with the gain of G_{IMON}=18.2µA/A. Due to current output of the IMON pin, it can be routed on the board to the point of sense without significant error of voltage drop or noise coupling. A resistor (R_{IMON}) between the IMON pin and GND can be used at the point of sense to convert current sense gain to voltage gain.

$$I_{OUT}=\frac{V_{IMON}}{G_{IMON}\times R_{IMON}}$$

In high-power applications with multiple eFuses connected in parallel, the IMON pins of all devices are tied together to provide the total system current. The RTQ1962 provides individual eFuse current through the ILIM pin with similar gain as IMON. A resistor from the ILIM pin to GND can be used to convert the current signal into voltage signal and be used for monitoring individual eFuse current.

17.7 Steady State Overcurrent Protection and Blanking Interval

During steady state operation (PG asserted high), the RTQ1962 monitors the output current and performs circuit breaker operation if the current exceeds the overcurrent protection threshold I_{OCP} ($V_{IMON} \geq V_{IREF}$) for longer than the blanking interval t_{TIMER}. The I_{OCP} threshold is determined by comparing V_{IMON} and V_{IREF}.

$$I_{OCP} = \frac{V_{IREF}}{G_{IMON} \times R_{IMON}}$$

The V_{IREF} is the reference voltage on the IREF pin which can be controlled in two ways.

- In the standalone or primary operation, the V_{IREF} is determined using internal current source interacting through external resistor at the IREF pin (R_{IREF}).

  $V_{IREF} = I_{IREF} \times R_{IREF}$
- In the parallel operation, the primary eFuse externally drives the V_{IREF} voltage at all the secondary eFuse IREF pins.

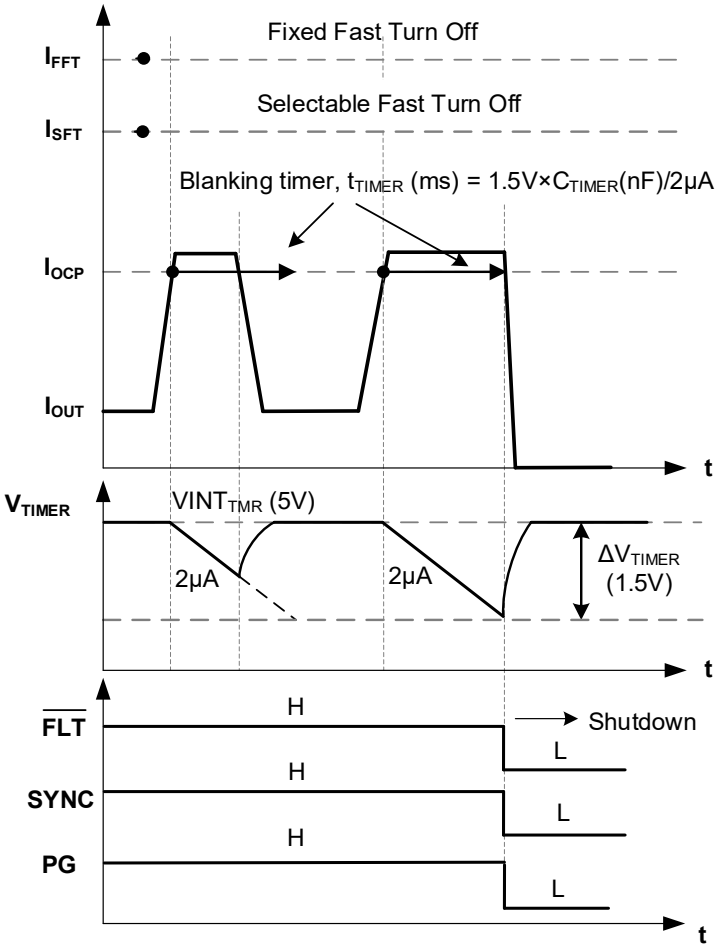


Figure 3. Overcurrent Protection Response and Blanking Timer

To allow for short overcurrent transients above I_{OCP} (but lower than I_{SFT} and I_{FT}) to pass through without turning off the device, user-adjustable blanking interval is implemented. If the output current exceeds the I_{OCP} threshold, the blanking timer starts by discharging the external capacitance at the TIMER pin (C_{TIMER}) using the 2μA internal current sink. If the load current drops below the I_{OCP} threshold before the timer expires (C_{TIMER} voltage discharges by ΔV_{TIMER} of 1.5V), the internal pull-up resistor resets the TIMER pin (to initial state of $VINT_{TMR}$) so that it is at the default voltage before the next overcurrent event starts. If the overcurrent condition persists beyond the blanking timer, the RTQ1962 turns off the MOSFET immediately and pulls the $\overline{FLT}$ pin low. The device will auto retry or latch-off depend on the configuration. The transient blanking timer interval can be adjusted using a capacitance at the TIMER pin according to equation below:

$$t_{TIMER} = \frac{C_{TIMER} \times \Delta V_{TIMER}}{I_{TIMER}}$$

Care must be taken when increasing the TIMER capacitance value to increase the blanking time. The longer the blanking time is, the longer it takes for the C_{TIMER} voltage to charge back to $VINT_{TMR}$ before the next overcurrent event occurs. If the next overcurrent event occurs before the C_{TIMER} is fully charged to $VINT_{TMR}$, it takes less time for the C_{TIMER} voltage to drop to V_{TIMER} threshold, leading to shorter blanking interval.

In addition, there is a 12ms back-up timer that shuts down the device if the OCP is detected but TIMER pin does not drop below the threshold. In other words, the designed fault timer cannot be above the back-up timer.

17.8 Fast Turn OFF Short Circuit Protection

During output short circuit events, as the current through the internal MOSFET rises rapidly above the fast turn off threshold I_{FT}, the RTQ1962 turns off the MOSFET immediately to prevent it from damage and excessive supply droop. There are two types of fast turn off current thresholds during steady state, scalable and fixed.

The scalable fast turn off current threshold I_{SFT} can be adjusted via a resistor at the SFT_SEL pin to GND. This allows for configurable threshold level per system rating. After the current exceeds I_{SFT}, the RTQ1962 turns off the MOSFET within t_{SFT} time.

The fixed fast turn off current threshold I_{FFT} is to protect against hard shorts. After the current exceeds I_{FFT}, the MOSFET is turned off within t_{FFT}. After either SFT or FFT fault is detected, the device will turn off, pull $\overline{FLT}$ low, and will retry or remain latched-off depending on the configuration.

Table 1. Scalable Fast Turn Off Selection Pin

SFT_SEL pin	I_{SFT}	MODE
R_{SFT_SEL} < 195kΩ	2.5 × I_{OCP}	Open
R_{SFT_SEL} < 195kΩ	2.8 × I_{OCP}	GND
205kΩ < R_{SFT_SEL} < 295kΩ	2 × I_{OCP}	Open
205kΩ < R_{SFT_SEL} < 295kΩ	2.3 × I_{OCP}	GND
305kΩ < R_{SFT_SEL}	1.5 × I_{OCP}	Open
305kΩ < R_{SFT_SEL}	1.7 × I_{OCP}	GND

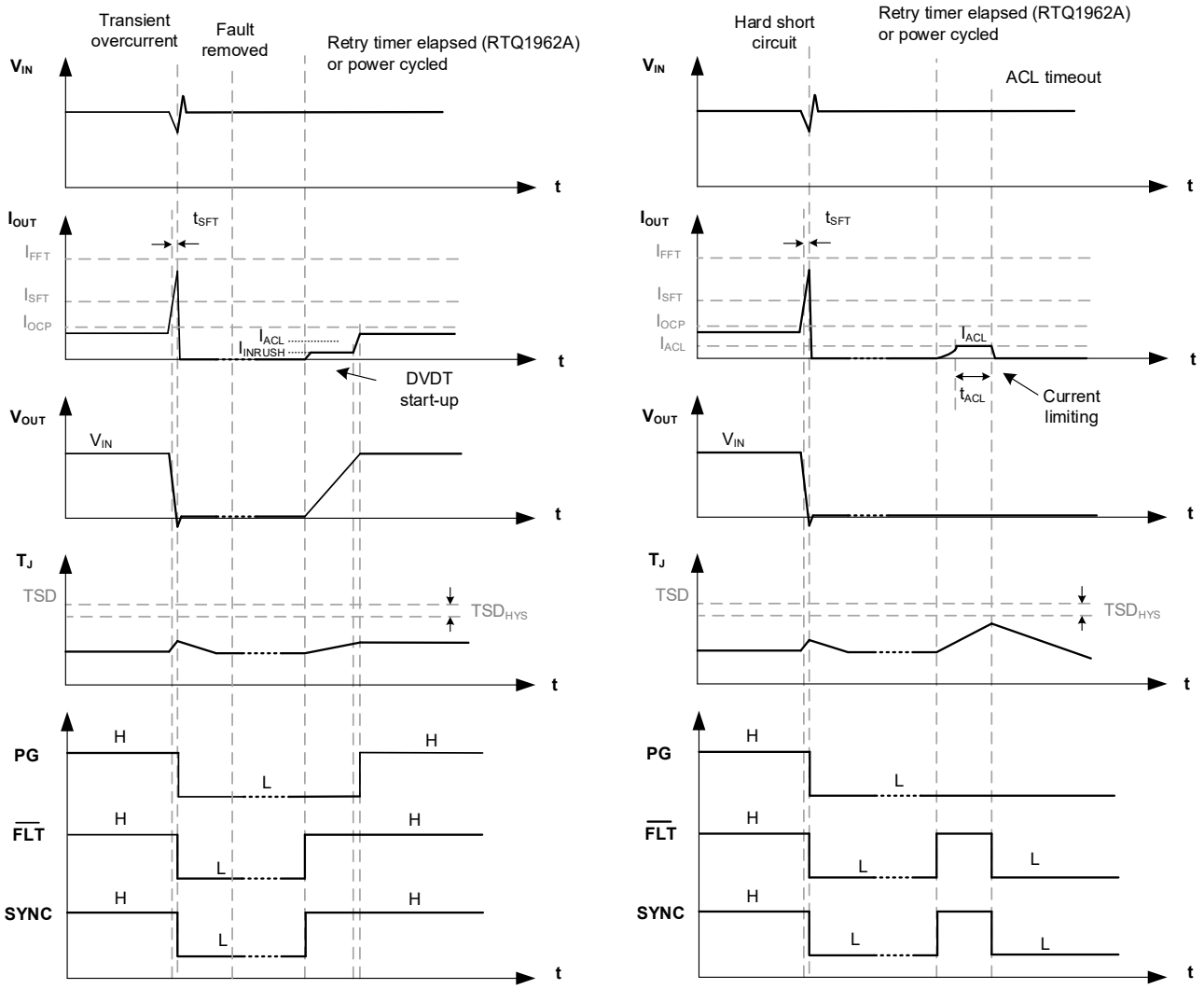


Figure 4. Fast Turn Off Behavior during Transient and Persistent Short Circuit Events

17.9 Single Point Failure Mechanism

The RTQ1962 provides overcurrent protection mechanism using IMON, IREF and TIMER pins. If the components on these pins are damaged (shorted to GND or open), it can compromise overcurrent protection. The RTQ1962 provides single point failure mechanisms to make sure component failure on these pins do not compromise the overall protection.

17.9.1 TIMER Pin Single Point Failure

If the TIMER pin is open or shorted to GND, this leads to immediate response to OCP event. If the OCP is detected but the TIMER pin voltage does not drop below the V_{TIMER_TH} (for example in case of the pin being forced to a voltage above $V_{TIMER-TH}$), there is a 12ms back-up timer that will fault and latch-off after the timer is elapsed beyond the OCP event.

17.9.2 IMON Pin Single Point Failure

If the IMON pin is open, the device performs circuit breaker (OCP) action even though there is not much current flowing through the device. If the IMON pin is shorted to GND, the OCP action does not engage even if there is

significant current through the device. The RTQ1962 has fixed fast turn off current, I_{FFT}, that protects against excessive currents.

17.9.3 IREF Pin Single Point Failure

If the IREF pin is shorted to GND, the device performs circuit breaker (OCP) action even though there is not much current flowing through the device. If the IREF pin is open (or externally forced higher than 2V), the part will latch off requiring power cycle to restart.

17.10 Undervoltage Protection

The RTQ1962 has undervoltage lock-out mechanism on VDD and IN that actively checks if the voltage has dropped too low for the device to function properly. The UVLO threshold for VDD is internally fixed (VDD_{UV}) while the V_{IN} UVLO threshold is adjusted externally using resistive divider on EN/UVLO pin.

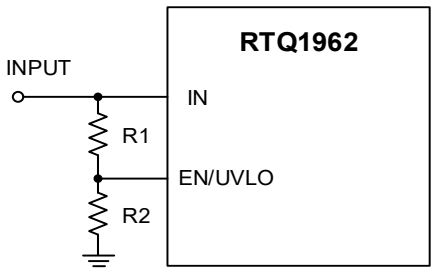


Figure 5. Undervoltage Resistive Divider

$$V_{IN(UVLO-R)}=V_{ENH-R}\frac{R_1+R_2}{R_2}$$

The EN/UVLO has a bi-level threshold levels that allows for multiple configurations on device turn ON as follows:

Table 2. EN/UVLO Pin Configurations

EN/UVLO Pin Voltage	Device State	Output Discharge	Comment
$V_{EN/UVLO} > V_{ENH-R}$	Fully ON	Disabled	Device fully functioning
$V_{ENL-F} < V_{EN/UVLO} < V_{ENH-F}$	MOSFET OFF	Enabled	If the $V_{EN/UVLO}$ stays in this range for t > t_{OD} (16µs), device will discharge the output.
$V_{EN/UVLO} < V_{ENL-F}$	MOSFET OFF	Disabled	Device will turn off the MOSFET and reset the faults.

17.10.1 Output Discharge

The RTQ1962 has a discharge function switch that discharges the output capacitor to GND using an integrated resistor to GND. The output discharge helps removing the residual charge on the output capacitors, preventing the output bus from staying on unspecified pre-bias voltage for long durations. In order to activate the output discharge, the EN/UVLO voltage needs to be held $V_{ENL-F} < V_{EN/UVLO} < V_{ENH-F}$ for minimum duration of t_{OD}=16µs. The output discharge is deactivated if the device detects an OV, or if junction temperature exceeds TSD.

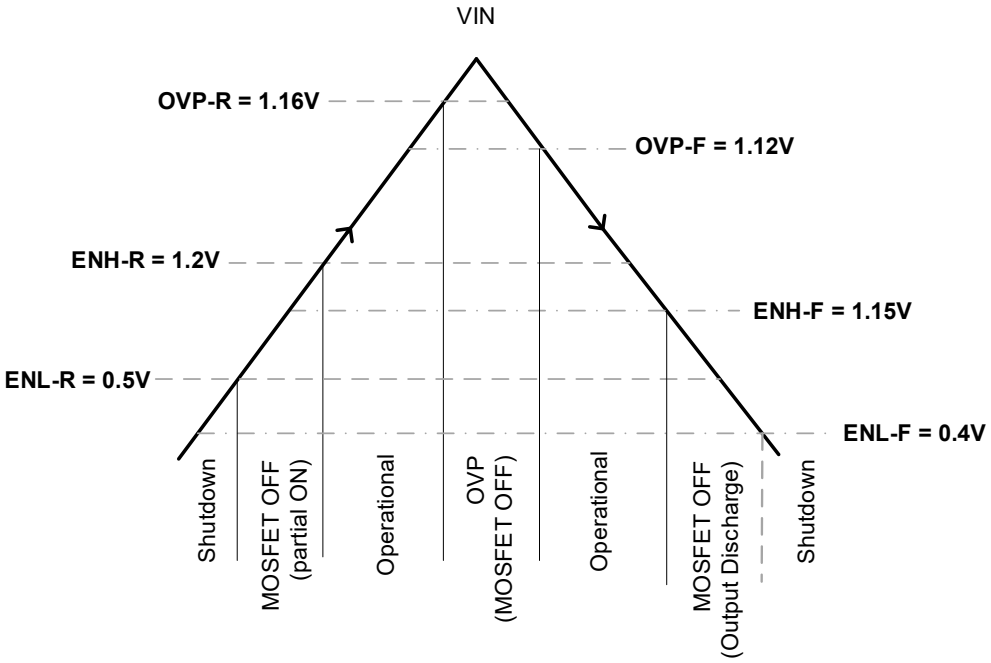


Figure 6. Undervoltage and Overvoltage Protection Settings on EN/UVLO and OVP Pins

17.11 Overvoltage Protection

The RTQ1962 has an overvoltage lock-out mechanism on V_{IN} that actively checks the input voltage and protects the system from overvoltage conditions. The OVP threshold on V_{IN} is adjusted externally using resistive divider on OVP pin.

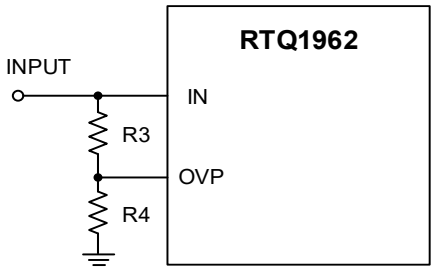


Figure 7. Overvoltage Resistive Divider

$$V_{IN(OVP-R)}=V_{OVP-R}\frac{R_3+R_4}{R_4}$$

When V_{IN} exceeds this value, the RTQ1962 protects the system from overvoltage condition by turning off the MOSFET. The device waits 60μs and then checks for overvoltage condition. If the OVP is cleared, the device will start from the start-up DVDT mode. Otherwise, the device will wait until the OVP condition is cleared before going to start-up. If the device fails to restart for t_{ST-MAX} of 5s (voltage does not drop below V_{OVP-F}), the device will latch off requiring power cycle.

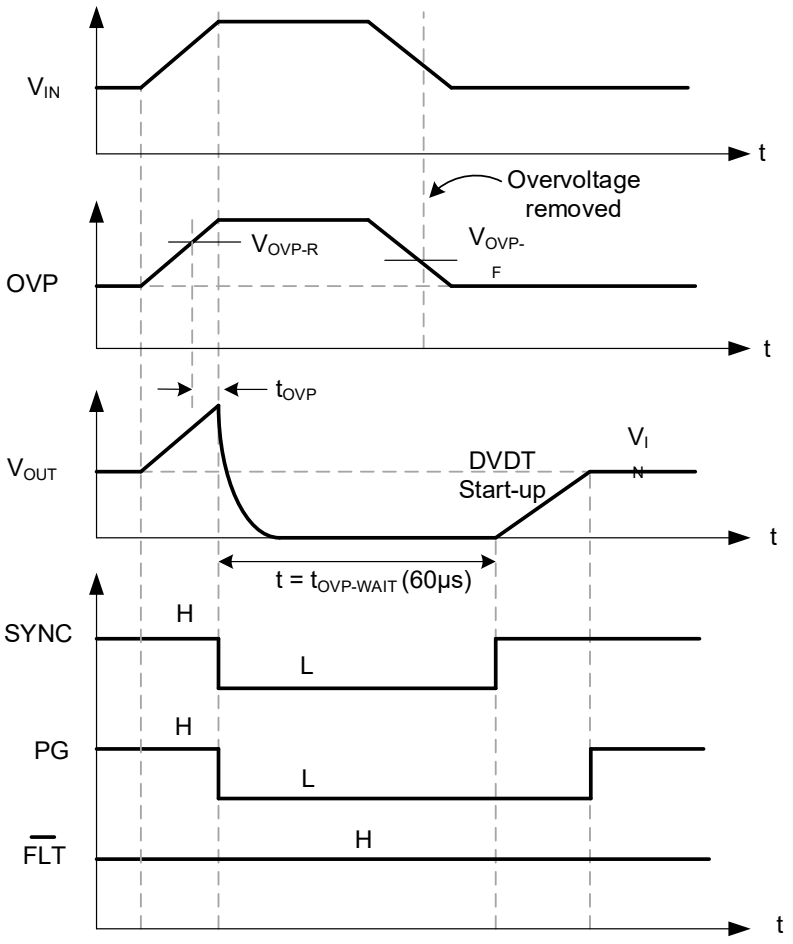


Figure 8. Overvoltage Protection Response

17.12 Temperature Monitoring and Over-Temperature Protection (OTP)

The RTQ1962 provides accurate analog junction temperature, T_J, monitoring that can be connected to the host controller with ADC for digital telemetry. The T_J is provided through the TEMP pin with a gain of 2.7mV/°C according to

V_{TEMP}=685mV+2.7mV/°C (T_J-25°C)

When using multiple eFuses, the TEMP output of all devices can be tied together which will report the temperature of the hottest eFuse in the chain.

Table 3. Over-Temperature Protection Behavior

Device Variant	Enters TSD	Exist TSD
Auto Retry	$T_J \geq TSD$	$T_J < TSD - TSD_{HYS}$ Followed by 680ms cool down time or power cycle
Latch-Off	$T_J \geq TSD$	$T_J < TSD - TSD_{HYS}$ Followed by power cycle

The RTQ1962 provides over-temperature protection (OTP) mechanism that shuts down the device when the internal junction temperature exceeds the TSD (150°C). If the thermal shutdown happens during start-up, the RTQ1962 will remain latched-off. If the thermal shut down occurs during steady state, the device remains latched-off until temperature drops by 30°C (TSD_{HYS}) followed by either device being power cycled (latch-off variant) or the cool down time of 680ms (t_{RETRY}) has elapsed (auto retry variant). If the TSD fault happens again during the retry cool down time, the retry timer starts over again once the temperature drops by 30°C.

17.13 Stacking eFuses for Parallel Power Path

For high power applications, the total current may exceed the current rating of the RTQ1962. In this case, the RTQ1962 supports parallel connection of multiple devices to increase the current rating of the parallel chain. In order to do so, the parallel RTQ1962 eFuse devices should be connected according to:

- **MODE pin**: The primary device MODE is open (internally pulled up to VINT) and the secondary device MODE pin is connected to GND.
- **SYNC pin**: The SYNC pin of the eFuses are connected together.
- **IMON pin**: The IMON pin of all the eFuses are connected together, with a single IMON resistor (R_{IMON}) to GND. The total system current overcurrent protection $I_{OCP-TOTAL}$ is determined according to:

$$I_{OCP-TOTAL} = \frac{V_{IREF}}{G_{IMON} \times R_{IMON}}$$

- **ILIM pin**: The ILIM pin is not intended to be connected together, instead it is used to report the current through each individual eFuse.
- **IREF pin**: The IREF pin of all the devices connected together, with a resistor to GND. The primary device will set the V_{IREF} using 25μA current source.
- **SFT_SEL pin**: The I_{SFT} current threshold for each individual device is set using a resistor from this pin to GND.
- **EN/UVLO pin**: To activate output discharge for all the devices in the chain, the EN/UVLO pins of the devices need to be tied together and the EN/UVLO pin voltage needs to be held at $V_{ENL-F} < V_{EN/UVLO} < V_{ENH-F}$ for minimum duration of t_{OD}=16μs
- **TIMER pin**: The secondary device TIMER pin is open. Only the primary device TIMER will be active during overcurrent circuit breaker event.
- **DVDT pin**: The DVDT pin of all the devices connected together, with a capacitor to GND. The primary device will set the soft-start time using 1.6μA current source.
- **TEMP pin**: The TEMP pin of all devices can be connected together to report the highest temperature of the chain. Following TSD event by any of the devices in parallel, the SYNC pin will be pulled low indicating fault. For the RTQ1962L (latch version), the devices remain latched. For RTQ1962A (auto retry version), the retry time starts after all the parallel devices have cleared the thermal shutdown event (the junction temperature drops by hysteresis).

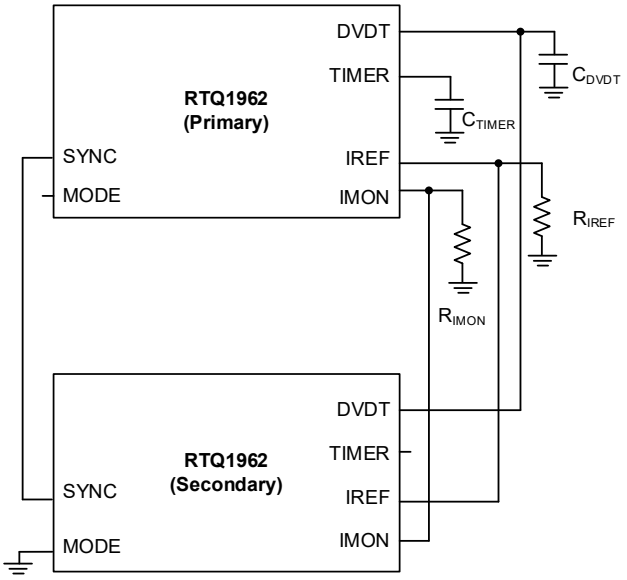


Figure 9. The Required Connections of Pins for Parallel Operation, Refer to the Typical Application Circuit for Detailed Schematic

17.14 Mode Selection (MODE)

This pin is used to configure a RTQ1962 device as primary or secondary in the parallel chain. Leaving this pin open configures the RTQ1962 as primary and connecting the MODE pin to GND sets the RTQ1962 as secondary. Depending on the primary or secondary configurations, certain settings of the RTQ1962 will be altered to provide proper parallel stacking operation.

The following functions are *disabled* in a secondary configured RTQ1962:

1. IREF internal current source. Only the primary device will have the current source to this pin.
2. DVDT internal current source. Only the primary device will have the current source to this pin.
3. OCP TIMER in steady state. The TIMER pin remains open; the primary device will set the timer.
4. PG pulldown (de-assertion) during steady state
5. Latch-off after fault

The following functions are *still active* in a secondary configured RTQ1962:

1. Overtemperature protection. It protects individual devices.
2. Start-up active current limit and timer.
3. OCP detection in steady state but does not initiate circuit breaker action, it relies on primary to initiate OCP detection and TIMER count down.
4. Scalable and fast turn off overcurrent protection. When configured as secondary, the I_{SFT} and I_{FFT} are set slightly higher so that the primary device can lower it for the whole system.
5. Overvoltage protection
6. $\overline{FLT}$ assertion based on individual device faults other than OCP circuit breaker.
7. PG de-assertion during inrush and PG assertion after inrush control complete.
8. SYNC assertion and de-assertion based on internal faults, and MOSFET on and off control based on pin status.

17.15 Device Fault Behavior Modes

The RTQ1962 provides two variants for post-fault behavior, auto retry variant (RTQ1962A) with 680ms cooldown time or latch-off variant (RTQ1962L). For the auto retry variant, once the device detects the fault and latches off, it will wait for the cooldown time before initiating a DVDT start-up.

However, there are certain faults that always result in permanent latch-off (for both RTQ1962A/L variants), shown in table below. Such faults need power cycling the device or pulling the EN/UVLO pin voltage below V_{ENH-F} to clear the fault and de-assert the pin. Other faults such as OCP circuit breaker, SFT, FFT, and TSD depend on the retry configuration.

Table 4. Faults That Always Lead to Permanent Latch-Off

Fault	Fault Detection	EXIT
Start-up maximum time-out	Persistent ACL timer faults (auto retry variant)	Power cycle ($V_{EN/UVLO}$ < V_{ENH-F} or VDD < VDD_{UV-F})
	FET_SHORT at the end of debounce time	
	Persistent OVP prior to soft-start	
	VDS does not reach level needed for operation	
	VGS does not reach level needed for operation	
OCP backup TIMER time-out	TIMER pin open, and back-up timer expires	
IREF overvoltage	Overvoltage on IREF pin	
TSD	Overtemperature fault during start-up	

Table 5. $\overline{FLT}$ Pin Overview

Device State or Event	Device Response	Fault Latched Internally (Y: Latch/Retry)	$\overline{FLT}$	Delay
Steady state	None	N/A	H	
Inrush	None	N/A	H	
TSD (steady state)	Shutdown	Y	L	
TSD (start-up)	Shutdown	Y (permanent)	L	
Undervoltage (EN/UVLO)	Shutdown	N	H	
Undervoltage (VDD UVP)	Shutdown	N	H	
Overvoltage (OVP, steady state)	Shutdown	N	H	
Persistent overvoltage (OVP, start-up)	Shutdown	Y (permanent)	L	t_{ST-MAX}
Transient overcurrent	None	N	H	
OCP (steady state)	Circuit breaker	Y	L	t_{TIMER}
ACL (start-up)	Current limit	Y	L	t_{ACL}
Selectable fast trip	Shutdown	Y	L	t_{SFT}
Fixed fast trip	Shutdown	Y	L	t_{FFT}
IMON pin open (steady state)	Circuit breaker	Y	L	t_{TIMER}
IMON pin short (steady state)	Fixed fast turn off	Y	L	t_{FFT}

TIMER pin forced to high voltage	Circuit breaker	Y	L	12ms
IREF pin short (steady state)	Circuit breaker	Y	L	t_{TIMER}
IREF pin overvoltage	Shutdown	Y (permanent)	L	
Start-up timeout	Shutdown	Y (permanent)	L	t_{ST-MAX}
External fault (SYNC low while not in UV or OV)	Shutdown	Y	L	10µs
FET_SHORT at the end of debounce time	Shutdown	Y	L	
Persistent FET_SHORT at the end of debounce time	Shutdown	Y (permanent)	L	t_{ST-MAX}

17.16 Parallel Device Synchronization and Enable Control (SYNC)

The SYNC pin serves as both handshake as well as control signal that allows multiple parallel connected RTQ1962 devices to have synchronized MOSFET on and off transitions. When the signal is high (open drain signal with weak internal pull-up to VINT), it signals the RTQ1962 driver to turn on the MOSFET. If the signal is driven low (internally or externally), it signals the driver to turn off the MOSFET. In standalone operation, this signal can be used to monitor the device status. In primary-secondary operation, the SYNC pin of all the devices are tied together. This pin is used to communicate any faults happening on each of the devices in the parallel chain and to synchronously turn off other devices to prevent damage. This pin is also used to communicate status readiness of each device in the chain, and it must be asserted before start-up soft-start can initiate.

Table 6. SYNC Pin Overview

Device State or Event	MOSFET Driver Status	SYNC
Steady state	ON	H
Inrush	ON	H
TSD	OFF	L
Auto retry timer running	OFF	L
Undervoltage (EN/UVLO)	OFF	L
Undervoltage (VDD UVP)	OFF	L
Overvoltage (OVP)	OFF	L
Debounce time	OFF	L
Transient overcurrent	ON	H
OCP circuit breaker (TIMER expiry)	OFF	L
Selectable and fixed fast trip	OFF	L
IMON pin open (steady state)	OFF	L
IMON pin short (steady state)	OFF	L
FET health fault	OFF	L

17.17 Power Good Indication (PG)

The power good indication (PG) pin is an active high output that indicates the device is ready to deliver power to the load. The PG pin is open drain and must be pulled up to external supply (VINT pin can be used as external supply). If the PG pin is connected to an independent external supply other than VINT pin, case must be taken to minimize the pin sink current when the device is not powered up to keep the PG pin voltage low and prevent being detected as logic high to other external circuits.

During initial power up, the PG is pulled low (de-asserted) while the device charges the output capacitor through DVDT controlled start-up. Once the inrush is completed and output voltage has reached the final value, the PG is asserted. The PG is de-asserted if the FET is turned off at any point during normal operation.

If the device is set as secondary (MODE=GND) in a parallel chain, it will control the PG assertion during start-up; however, in steady state the secondary device has no control on PG de-assertion.

Table 7. PG Pin Overview

Device State or Event	MOSFET Driver Status	PG
Steady state	ON	H
Inrush	ON	L
TSD	OFF	L (MODE=H) H (MODE=L)
Undervoltage (EN/UVLO)	OFF	L
Undervoltage (VDD UVP)	OFF	L
Overvoltage (OVP)	OFF	L
Transient overcurrent	ON	H
OCP circuit breaker (TIMER expiry)	OFF	L (MODE=H) H (MODE=L)
Selectable and fixed fast trip	OFF	L (MODE=H) H (MODE=L)

17.18 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a LQFN5x6-24L package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C)/(30°C/W) = 3.33W for a LQFN5x6-24L package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}.

The derating curve in Figure 10 allows the user to see the effect of rising ambient temperature on the maximum power dissipation.

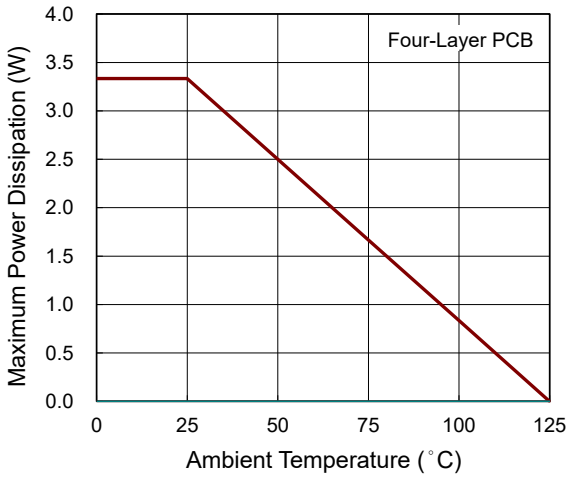
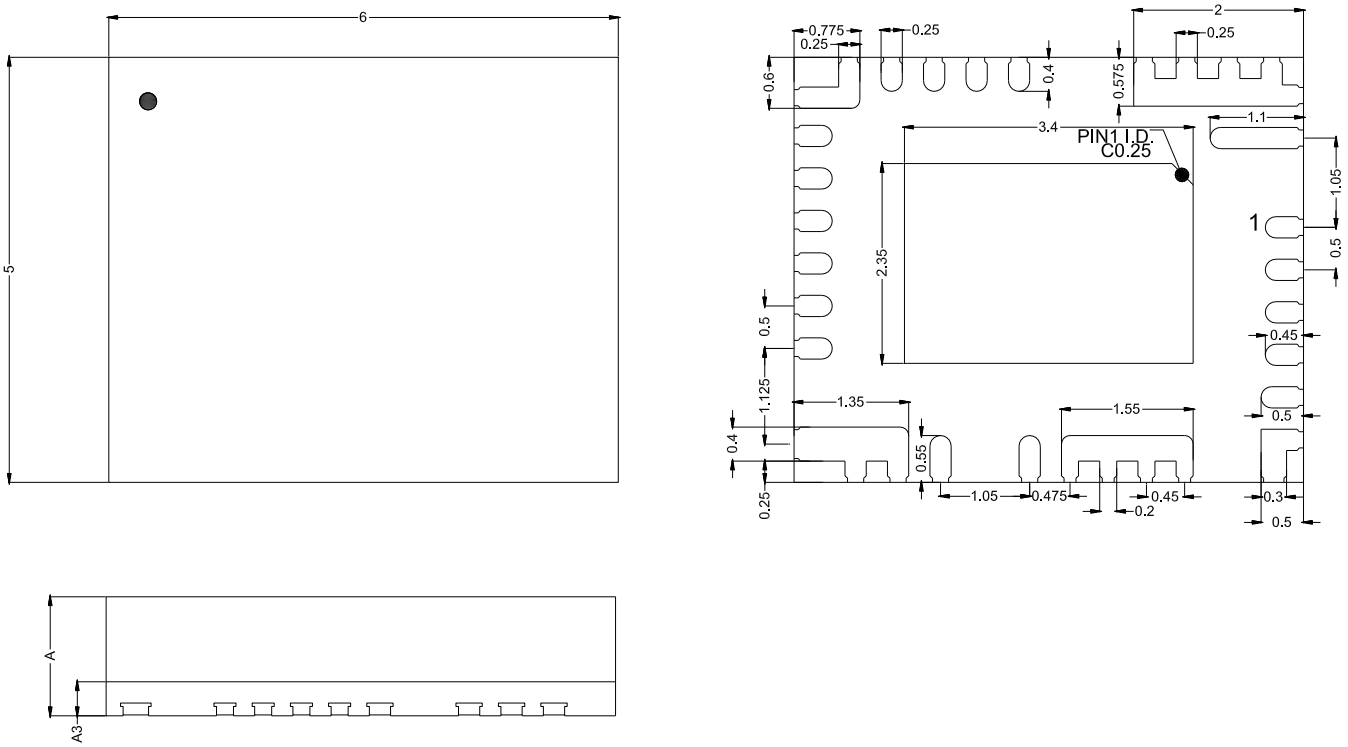


Figure 10. Derating Curve of Maximum Power Dissipation

Note 10. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

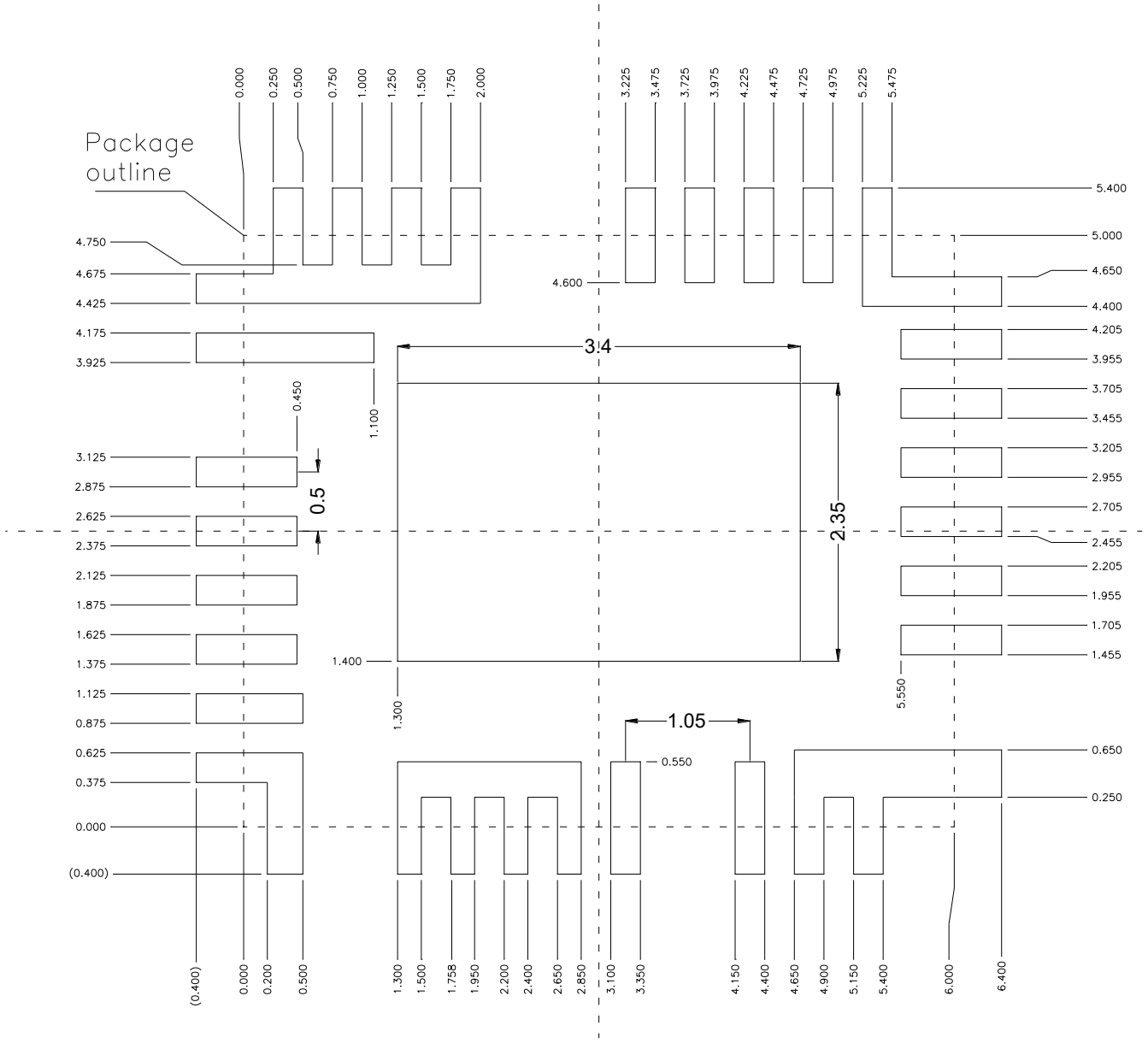
18 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min	Max	Min	Max	
A	1.350	1.450	0.053	0.057	Tolerance
A3	0.370	0.430	0.015	0.017	±0.050 mm

LQFN5x6-24L Package

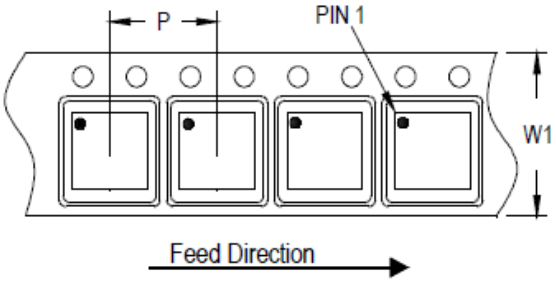
19 Footprint Information

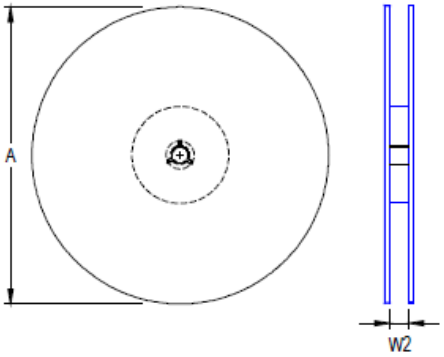


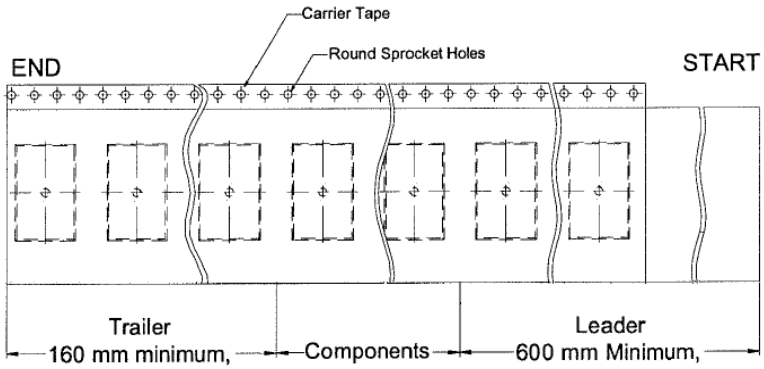
Package	Number of Pin	Tolerance
LQFN5x6-24L	24	±0.05

20 Packing Information

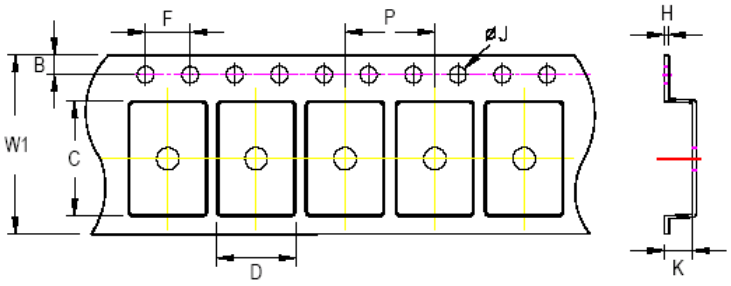
20.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W)QFN/ DFN 5x6	16	12	330	13	2,500	160	600	16.4/18.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 16mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
16mm	16.3mm	11.9mm	12.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
(V, W)QFN and DFN 5x6	13”	2,500	Box G	1	2,500	Carton A	6	15,000

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover Tape	Carrier Tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description
00	2026/7/24	First Edition