1.5A, 6V, Low I_Q ACOT® Synchronous Step-Down Converter

General Description

The RTQ2102A and RTQ2102B are 1.5A, high-efficiency, Advanced Constant-On-Time (ACOT®) synchronous step-down converters. The device operates with input voltages from 3V to 6V. The device can program the output voltage between 0.45V to VIN. The low quiescent current design with the integrated low $R_{DS(ON)}$ power MOSFETs achieves high efficiency over the wide load range. The advanced COT operation allows transient responses to be optimized over a wide range of loads, and output capacitors to efficiently reduce external component count. The RTQ2102A and RTQ2102B provide up to 2.7MHz switching frequency to minimize the size of output inductor and capacitors.

The RTQ2102A and RTQ2102B provide complete protection functions such as input undervoltage lockout, output undervoltage protection, overcurrent protection, and thermal shutdown.

The cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. The RTQ2102A and RTQ2102B are available in WDFN-8L 3x3 package.

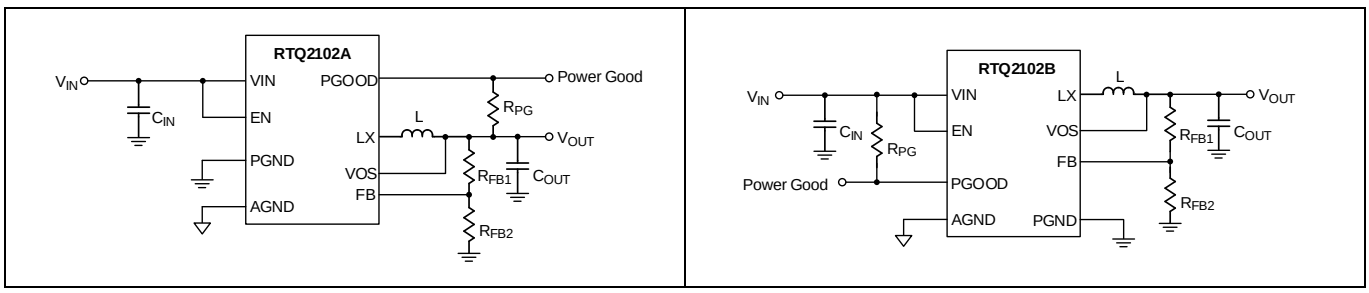
Features

- **AEC-Q100 Grade 1 Qualified**
- **Input Supply Voltage Range: 3V to 6V**
- **Output Voltage Range: 0.45V to V_{IN}**
- **1.5A Converter Integrated 110mΩ and 90mΩ FETS in WDFN-8L 3x3 Package**
- **Advanced Constant On-Time (ACOT®) Control**
  - **Ultrafast Transient Response**
  - **No Needs for External Compensations**
  - **Optimized for Low-ESR Ceramic Output Capacitors**
- **Low Quiescent Current: 30μA**
- **Steady Switching Frequency: 2.7MHz**
  - **Automatic Power Saving Mode (PSM)**
- **Input Undervoltage Lockout (UVLO)**
- **Output Undervoltage Protection (UVP) with Hiccup Mode**
- **Over-Temperature Protection (OTP)**
- **Power Good Indication**

Applications

- Mobile Phones and Handheld Devices
- STB, Cable Modem, and xDSL Platforms
- WLAN ASIC Power/Storage (SSD and HDD)
- General Purpose for POL LV Buck Converter
- Automotive Infotainment
- Automotive Instrument Clusters & HUD
- Car Connectivity

Simplified Application Circuit



Ordering Information

RTQ2102A/B □□-QA

- Grade
  QA : AEC-Q100 Qualified and Screened by High Temperature
- Package Type
  QW : WDFN-8L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

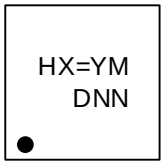
Note:

Richtek products are:

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

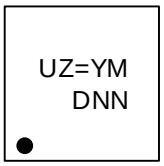
Marking Information

RTQ2102AGQW-QA



HX= : Product Code
YMDNN : Date Code

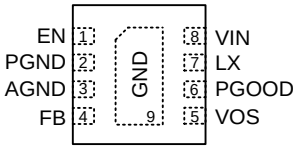
RTQ2102BGQW-QA



UZ= : Product Code
YMDNN : Date Code

Pin Configuration

(TOP VIEW)

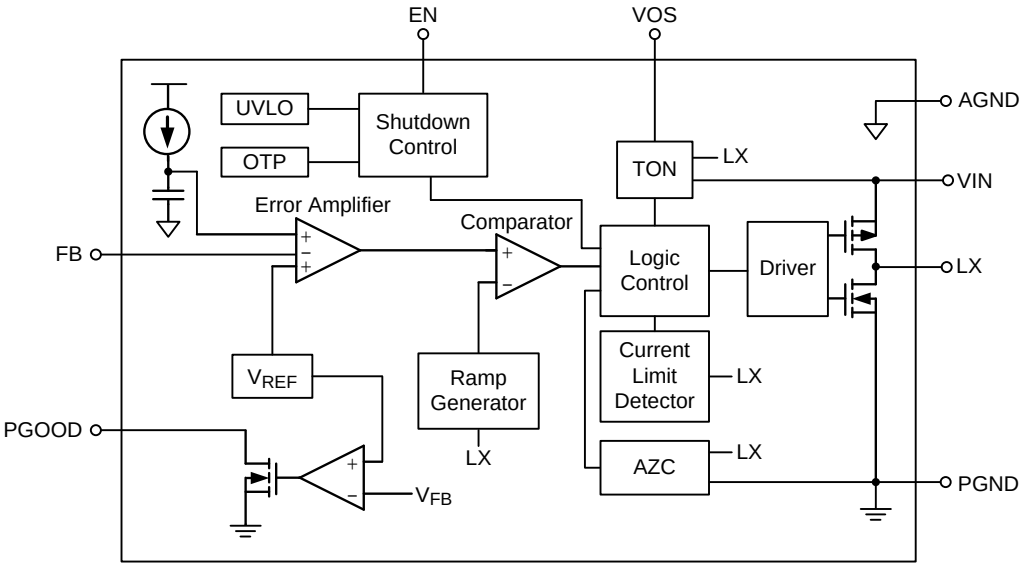


WDFN-8L 3x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Enable control input. Connect this pin to logic high to enable the device and connect this pin to GND to disable the device.
2, 9 (Exposed Pad)	PGND	Power ground. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.
3	AGND	Analog ground. Should be electrically connected to GND close to the device.
4	FB	Feedback voltage input. Connect this pin to the midpoint of the external feedback resistive divider to set the output voltage of the converter to the desired regulation level. The device regulates the FB voltage at Feedback Reference Voltage, typically 0.45V.
5	VOS	Output voltage sense pin for the internal control loop. Must be connected to output.
6	PGOOD	Power good open-drain output. This pin is pulled to low if the output voltage is below regulation limits. Can be left floating if not used.
7	LX	Switch node. The Source of the internal high-side power MOSFET, and Drain of the internal low-side (synchronous) rectifier MOSFET.
8	VIN	Power input supply voltage, 3V to 6V.

Functional Block Diagram



Operation

The RTQ2102A and RTQ2102B are low voltage synchronous step-down converters that can support input voltage ranging from 3V to 6V and the output current can be up to 1.5A. The RTQ2102A and RTQ2102B use ACOT® mode control. To achieve good stability with low-ESR ceramic capacitors, the ACOT® uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

In steady-state operation, the feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference, the on-time one-shot is triggered, as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short so that rapidly-repeated on-times can raise the inductor current quickly when needed.

PWM Frequency and Adaptive On-Time Control

The on-time can be roughly estimated by the equation:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{OSC}}$$

where f_{OSC} is nominal 2.7MHz.

Power Saving Mode

The RTQ2102A and RTQ2102B automatically enter power saving mode (PSM) at light load to maintain high efficiency. As the load current decreases, the inductor current ripple valley eventually touches the zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side switch is turned off when the zero inductor current is detected. In this case, the output capacitor is only discharged by load current, so the switching frequency decreases. As the result, the light-load efficiency can be enhanced due to lower switching loss.

Input Undervoltage Lockout

In addition to the EN pin, the RTQ2102A and RTQ2102B also provide enable control through the VIN pin. If V_{EN} rises above V_{EN_H} first, switching will still be inhibited until the VIN voltage rises above V_{UVLO}. It is to

ensure that the internal regulator is ready so that operation with not-fully-enhanced internal MOSFET switches can be prevented. After the device is powered up, if the input voltage VIN goes below the UVLO falling threshold voltage ($V_{UVLO} - \Delta V_{UVLO}$), this switching will be inhibited; if VIN rises above the UVLO rising threshold (V_{UVLO}), the device will resume normal operation with a complete soft-start.

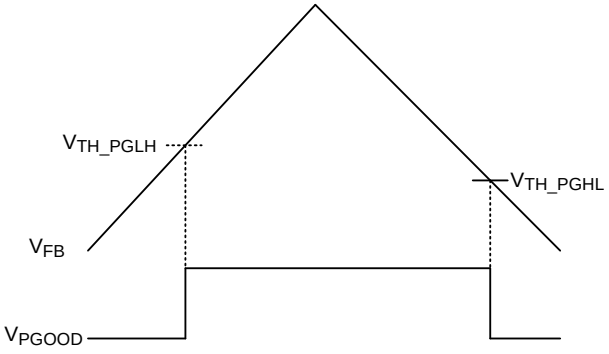
Power Good Indication

The RTQ2102A and RTQ2102B feature an open-drain power-good output (PGOOD) to monitor the output voltage status. The output delay of comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. When VIN voltage rises above V_{UVLO}, the power-good function is activated. After soft-start is finished, the PGOOD pin is controlled by a comparator connected to the feedback signal V_{FB}. Table 1 shows the PG pin status for both RTQ2102A and RTQ2102B. It is connected to a voltage source through a pull-up resistor. The PG pin logic of RTQ2102A and RTQ2102B are different, so RTQ2102A PGOOD is connected to V_{OUT} while RTQ2102B PGOOD is connected to V_{OUT} or an external voltage source.

Table 1. PG Pin Status

Conditions		PG Pin Logic Status	
		RTQ2102A	RTQ2102B
Enable	$V_{EN} > V_{EN\_H}$, $V_{FB} > V_{TH\_PGLH}$	High Z	High Z
	$V_{EN} > V_{EN\_H}$, $V_{FB} < V_{TH\_PGHL}$	Low	Low
Shutdown	$V_{EN} < V_{EN\_L}$	High Z	Low
OTP	$T_J > T_{SD}$	High Z	Low

If V_{FB} rises above a power-good high threshold (V_{TH_PGLH}) (typically 90% of the reference voltage), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high. When V_{FB} falls short of power-good low threshold (V_{TH_PGHL}) (typically 85% of the reference voltage), the PGOOD pin will be pulled low. The power good indication profile is shown as followed.



Output Undervoltage Protection and Hiccup Mode

The RTQ2102A and RTQ2102B include output undervoltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the undervoltage protection trip threshold (typically 66% of the internal feedback reference voltage), the UV comparator will go high to turn off both the internal high-side and low-side MOSFET switches. The RTQ2102A and RTQ2102B will enter output undervoltage protection with hiccup mode. Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed.

The Overcurrent Protection

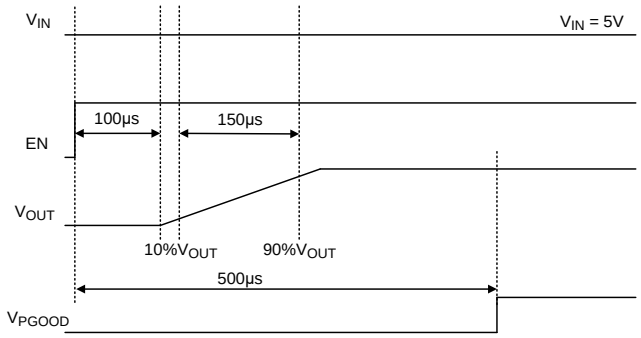
The RTQ2102A and RTQ2102B feature cycle-by-cycle current-limit protection on both the high-side and low-side MOSFETs and this prevents the device from the catastrophic damage in output short circuit, overcurrent or inductor saturation.

The high-side MOSFET overcurrent protection is achieved by an internal current comparator that monitors the current in the high-side MOSFET during each on-time. The switch current is compared with the high-side switch peak-current limit (I_{LIM_H}) after a certain amount of delay when the high-side switch being turned on each cycle. If an overcurrent condition occurs, the converter will immediately turn off the high-side switch and turn on the low-side switch to prevent the inductor current exceeding the high-side current limit.

The low-side MOSFET overcurrent protection is achieved by measuring the inductor current through the synchronous rectifier (low-side switch) during the low-side on-time. Once the current rises above the low-side switch valley current limit (I_{LIM_L}), the on-time one-shot will be inhibited until the inductor current ramps down to the current limit level (I_{LIM_L}), that is, another on-time can only be triggered when the inductor current goes below the low-side current limit. If the output load current exceeds the available inductor current (clamped by the low-side current limit), the output capacitor needs to supply the extra current such that the output voltage will begin to drop. If it drops below the output undervoltage protection trip threshold, the IC will stop switching to avoid excessive heat.

Soft-Start (SS)

The RTQ2102A and RTQ2102B provide an internal soft-start feature for inrush control. At power up, the internal capacitor is charged by an internal current source to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. The device will initiate switching and the output voltage will smoothly ramp up to its targeted regulation voltage only after this ramp voltage is greater than the feedback voltage V_{FB} to ensure the converters have a smooth start-up from pre-biased output. The output voltage starts to rise in 100μs from EN rising, and the soft-start ramp-up time (10%V_{OUT} to 90%V_{OUT}) is 150μs.



Thermal Shutdown

The RTQ2102A and RTQ2102B include an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold (T_{SD}). Once the junction temperature cools down by a thermal shutdown hysteresis (ΔT_{SD}), the IC will resume normal operation with a complete soft-start.

Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe. Operating continuously above the specified absolute maximum junction temperature may impact device reliability or permanently damage the device.

Maximum Duty Cycle Operation

The RTQ2102A and RTQ2102B are designed to operate in dropout at the high duty cycle approaching 100%. If the operational duty cycle is large and the required off-time becomes smaller than minimum off-time, the RTQ2102A and RTQ2102B start to enable skip off-time function and keeps high-side MOSFET switch on continuously. The RTQ2102A and RTQ2102B implement skip off-time function to achieve high duty approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application if input voltage momentarily falls down to the normal output voltage requirement. The input voltage at which the devices enter dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 7V
- LX Pin Switch Voltage, LX ---------- –0.3V to (V_{IN} + 0.3V)
  <100ns ---------- –5V to 9V
- Other I/O Pin Voltages ---------- –0.3V to (V_{IN} + 0.3V)
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

ESD Ratings

- ESD Susceptibility (Note 2)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 3)

- Supply Input Voltage, VIN ---------- 3V to 6V
- Ambient Temperature Range ---------- –40°C to 125°C
- Junction Temperature Range ---------- –40°C to 125°C

Thermal Information (Note 4 and Note 5)

Thermal Parameter		WDFN-8L 3x3	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	52.1	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	5.21	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	11.5	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	47.7	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	4.96	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	29.3	°C/W

Electrical Characteristics

(V_{IN} = 3.6V, T_A = T_J = –40°C to 125°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Undervoltage Lockout Threshold		V_{UVLO}	V_{CC} rising	--	2.35	2.52	V
Undervoltage Lockout Hysteresis		V_{UVLOHY}		--	400	--	mV
Shutdown Supply Current		I_{SHDN}	EN = 0V	--	--	2	μA
Quiescent Current		I_Q	Active, V_{FB} = 0.5V, no switching	--	30	--	μA
Voltage Reference		V_{REF}	RTQ2102A	0.443	0.45	0.457	V
			RTQ2102B	0.441	0.45	0.459	
Current Limit	High-Side	I_{LIM_H}	RTQ2102A	2.4	3.2	4	A
			RTQ2102B	2.4	3.2	4.4	
	Low-Side	I_{LIM_L}	RTQ2102A	1.8	2.4	2.9	
			RTQ2102B	1.8	2.4	3.1	
Power Good Threshold		V_{PGTH}	V_{OUT} falling referenced to V_{OUT} nominal	–15	–10	–5	%
Power Good Hysteresis		V_{PGHY}	Hysteresis referenced to V_{OUT} nominal	--	5	--	%
Power Good Leakage Current		I_{PG}	V_{PG} = 5V	--	0.01	0.1	μA
Power Good Low Level Voltage		V_{PGL}	I_{sink} = 500μA	--	--	0.3	V
EN Threshold Voltage	H-Level	V_{EN_H}	EN rising	1	--	--	V
	L-Level	V_{EN_L}	EN falling	--	--	0.4	V
Switch On-Resistance	High-Side	$R_{P-MOSFET}$		--	110	--	mΩ
	Low-Side	$R_{N-MOSFET}$		--	90	--	
Thermal Shutdown Temperature				130	150	--	°C
Thermal Shutdown Hysteresis				--	20	--	°C
Switching Frequency		f_{OSC}	(Note 6)	2.2	2.7	3	MHz
Output Discharge Resistor				--	1	--	kΩ

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. Devices are ESD sensitive. Handling precautions are recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 5. $\theta_{JA(EVB)}$, $\Psi_{JC(Top)}$ and Ψ_{JB} are measured on a high effective-thermal-conductivity two-layer test board which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

Note 6. Measured switching frequency may not meet the declared range due to different operation modes and output voltages.

For operating in PSM, the f_{OSC} varies according to the load condition. For operating in dropout at the high duty cycle approaching 100%, the f_{OSC} reduces while the duty cycle increases. For V_{OUT} < 1V, the f_{OSC} may be reduced while the duty cycle is too small.

Typical Application Circuit

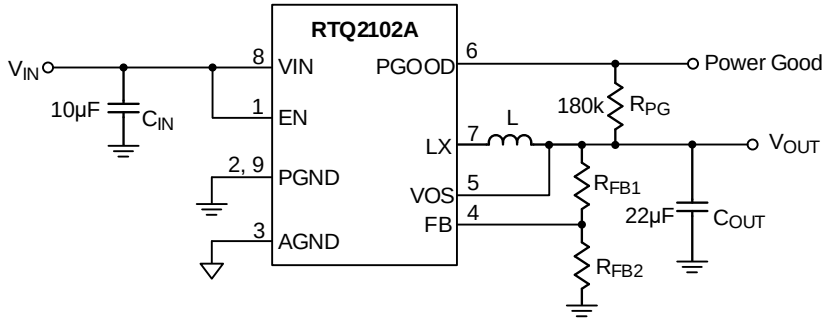


Figure 1. RTQ2102A Typical Application Circuit

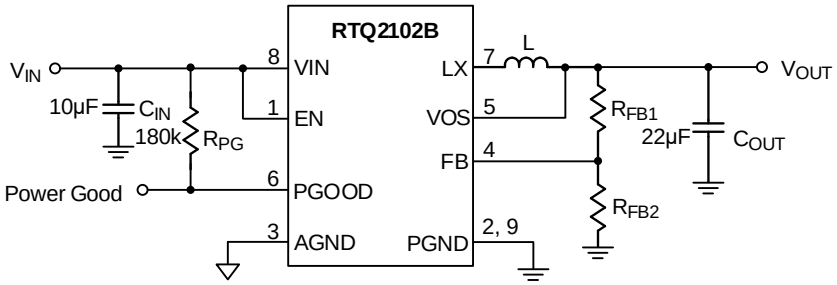


Figure 2. RTQ2102B Typical Application Circuit

Table 2. Suggested Component Values for Different Output Voltage Setting

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	L (µH)	C_{OUT} (µF)
1.2V	64.9	39.2	0.47	22
1.8V	118	39.2	1	22
2.5V	178	39.2	1	22
3.3V	249	39.2	1	22

Table 3. Recommended External Components for 1.5A Maximum Load Current

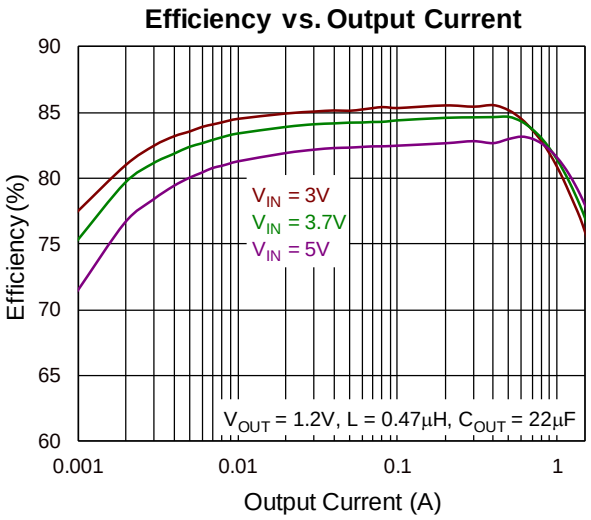
Component	Description	Vendor P/N
L (1)	0.47µH, 2016 (3.8A, 32mΩ)	DFE201612PD-R47M =P2 (Murata)
	1µH, 2520 (3.8A, 42mΩ)	DFE252012PD-1R0M =P2 (Murata)
C_{IN} (2)	10µF, 10V, X7R, 1206	GRM31CR71A106KA01L (Murata)
C_{OUT} (2)	22µF, 10V, X7R, 1206	GRM31CR71A226ME15K (Murata)

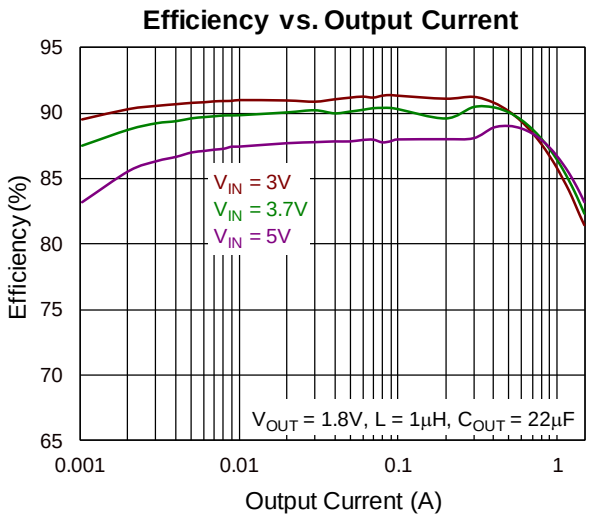
Note:

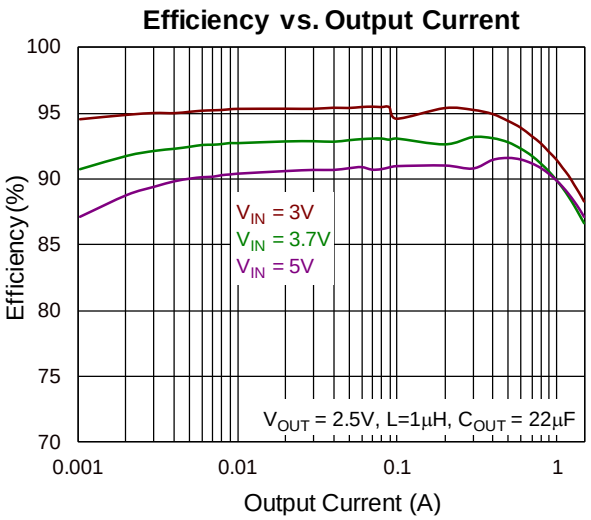
(1) Considering stability of the device, it is recommended to adopt L=0.47µH for lower output voltage setting (V_{OUT} ≤ 1.2V) while L=1µH is recommended for higher output voltage setting (1.2V < V_{OUT} ≤ 3.3V).

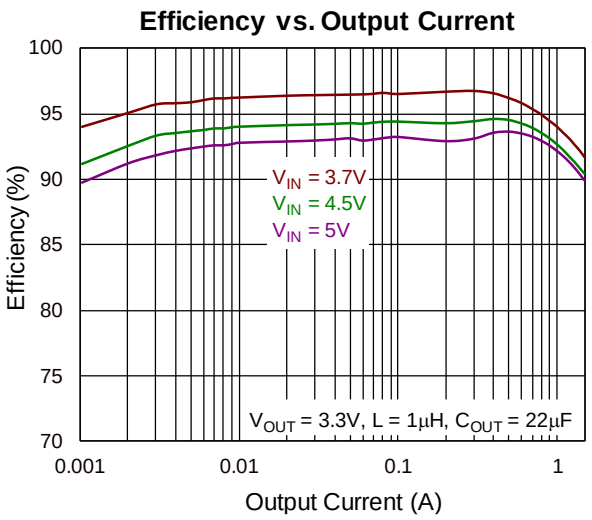
(2) All the input and output capacitors are the suggested values, referring to the effective capacitance which is related to biased voltage level and capacitor size. To make the converter operate in stable and normal, the effective capacitance of C_{OUT} should be larger than 14µF. Operating temperature range must be considered while choosing the input and output capacitor.

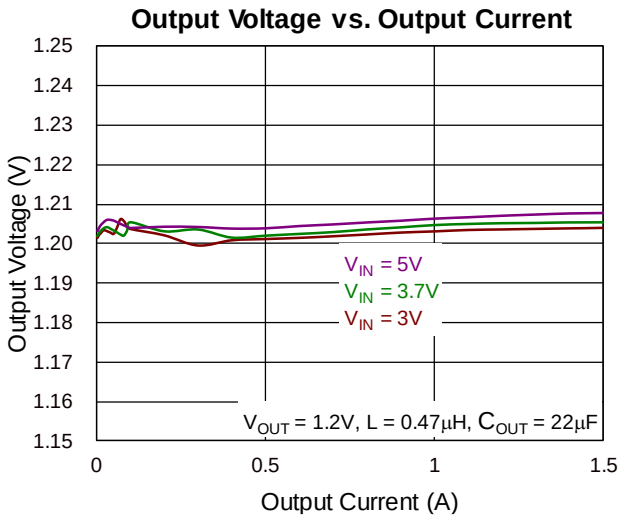
Typical Operating Characteristics

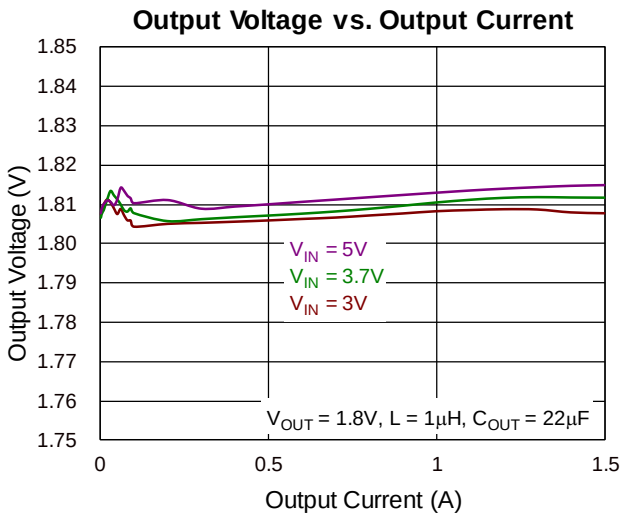




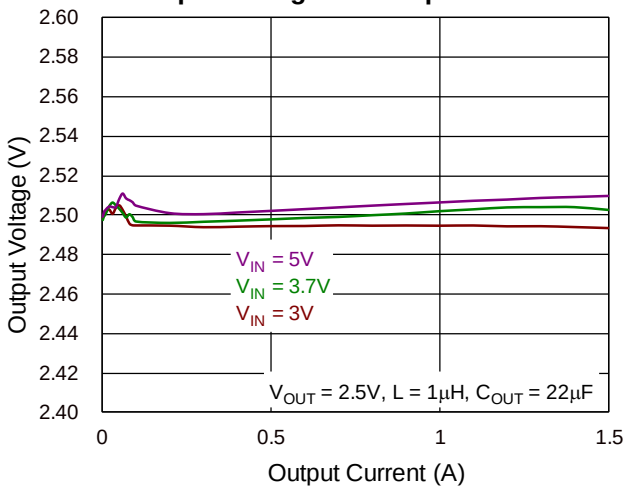




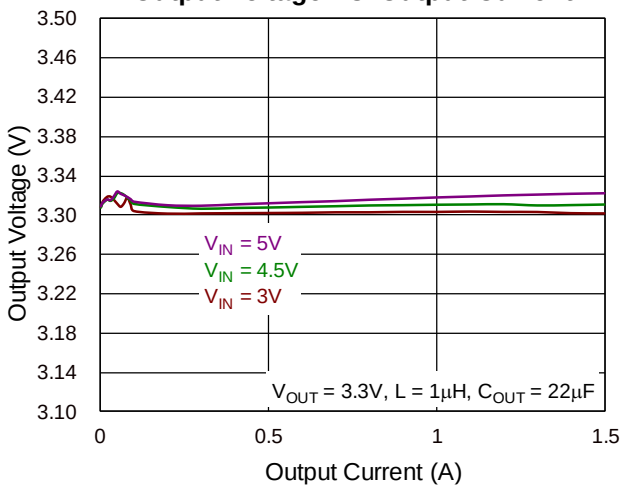




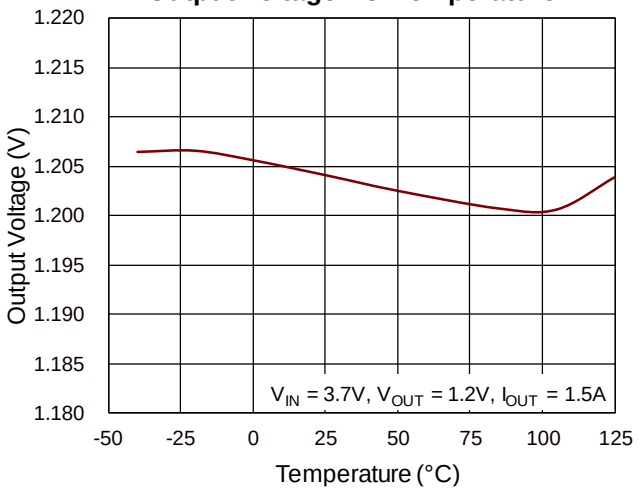
Output Voltage vs. Output Current



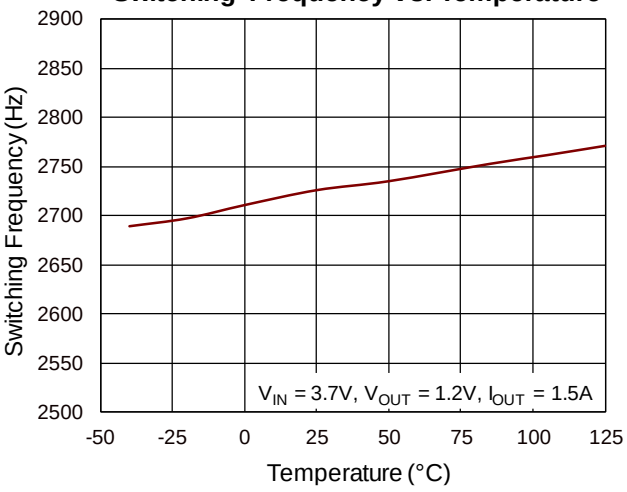
Output Voltage vs. Output Current



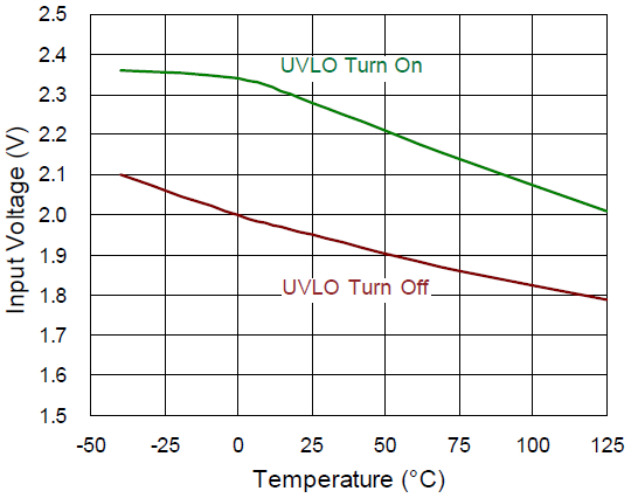
Output Voltage vs. Temperature



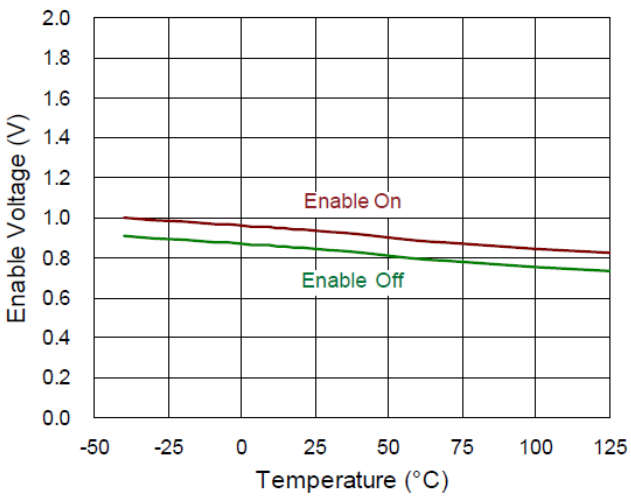
Switching Frequency vs. Temperature



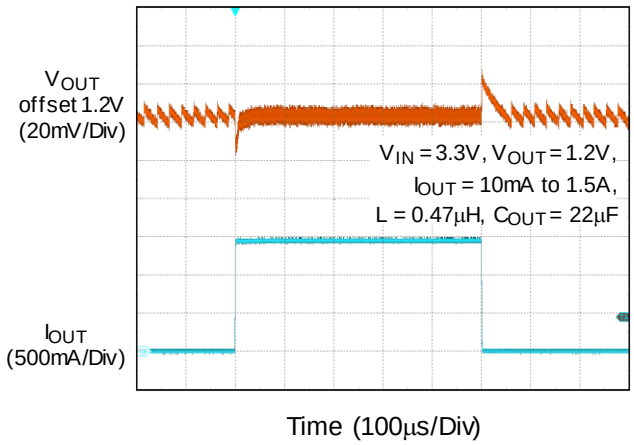
Input Voltage vs. Temperature



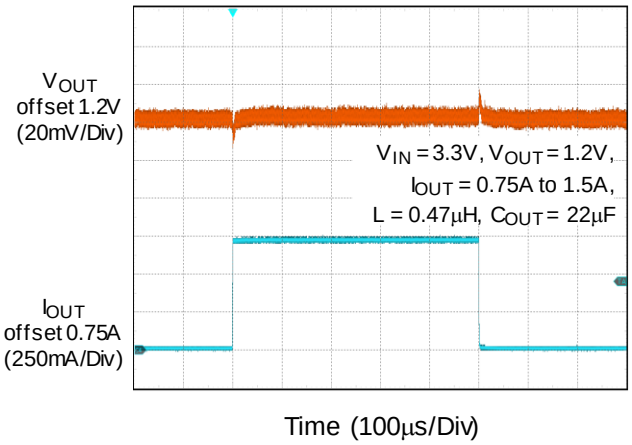
Enable Threshold vs. Temperature



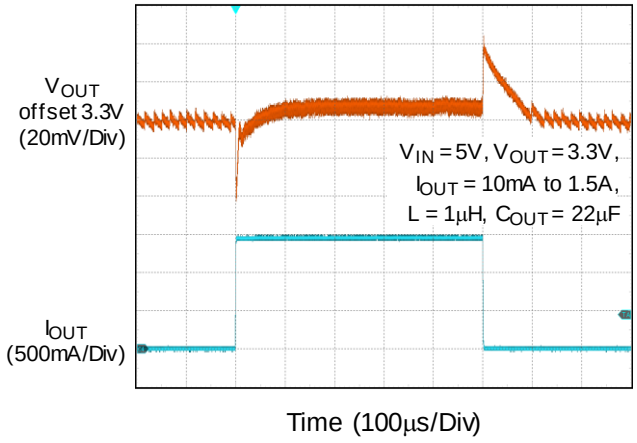
Load Transient Response



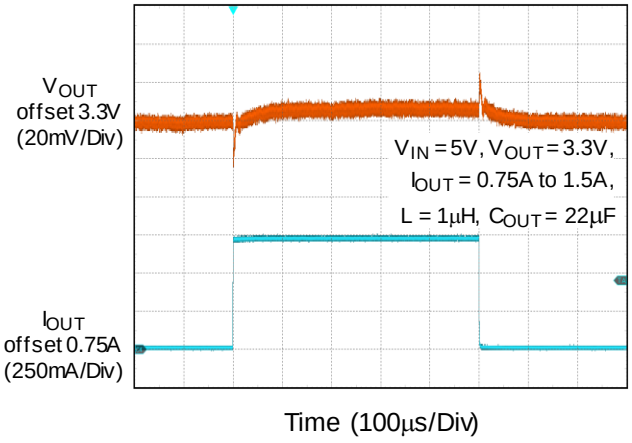
Load Transient Response



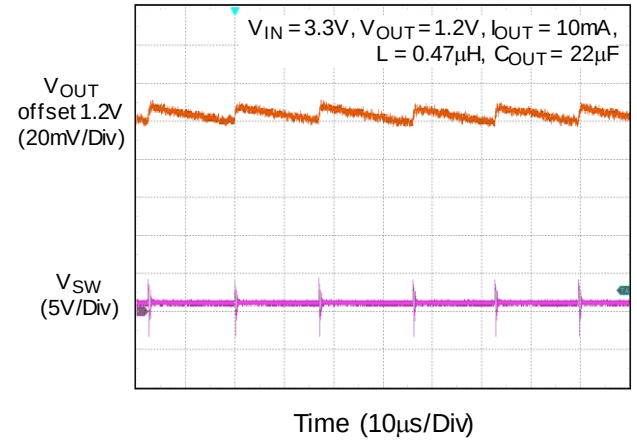
Load Transient Response



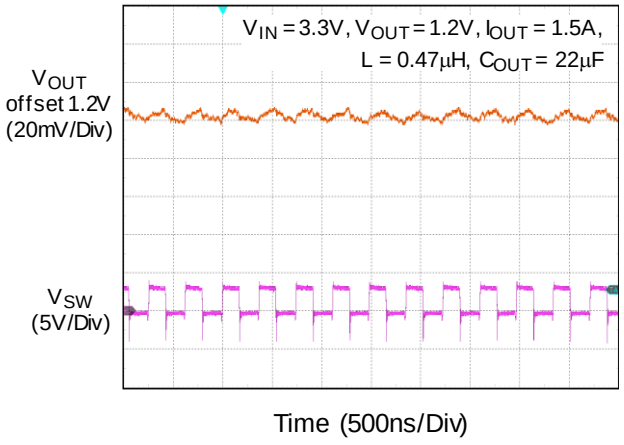
Load Transient Response



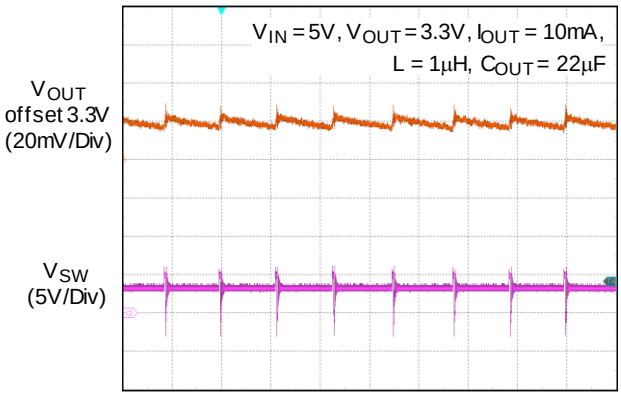
Output Voltage Ripple



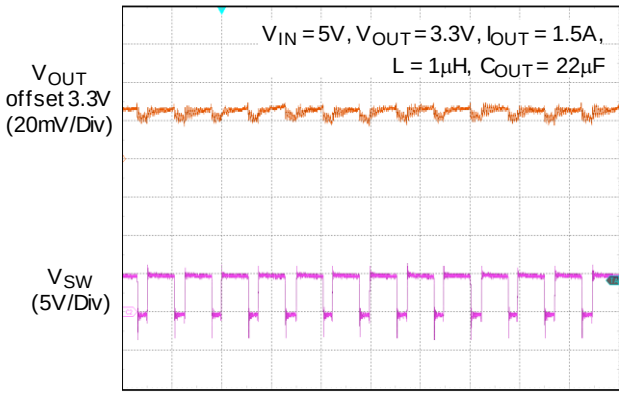
Output Voltage Ripple



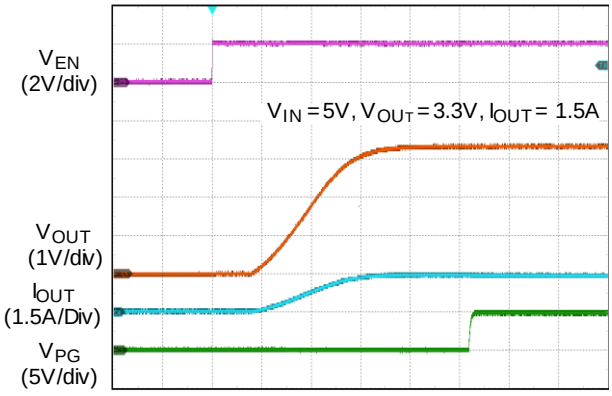
Output Voltage Ripple



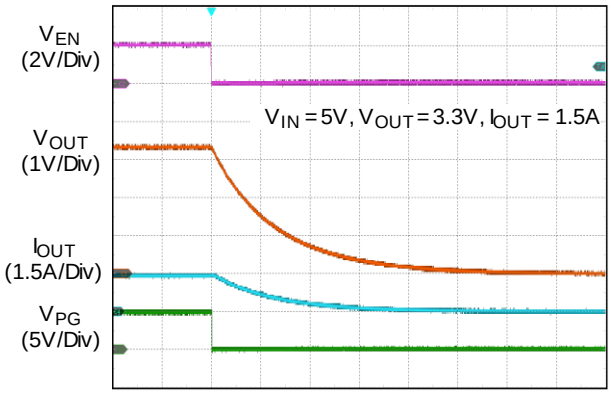
Output Voltage Ripple



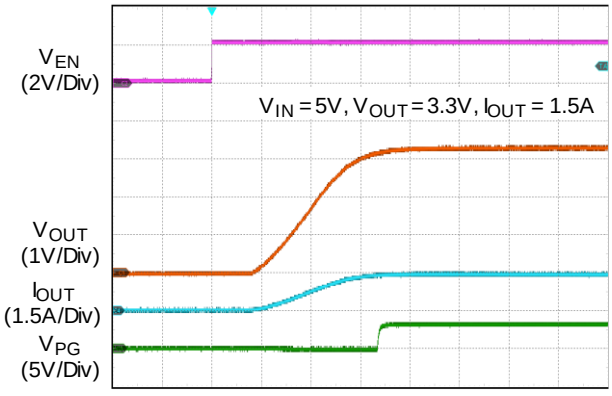
Power On from EN (RTQ2102B)



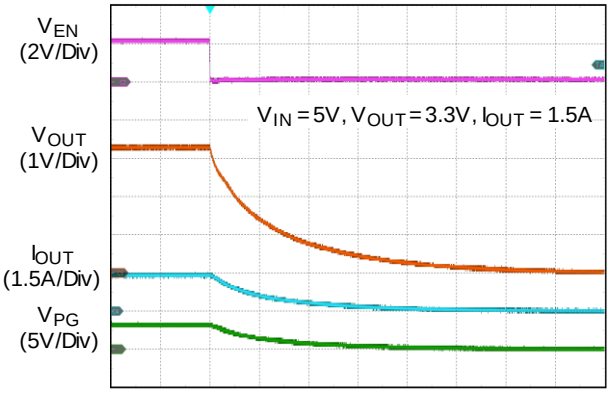
Power Off from EN (RTQ2102B)



Power On from EN (RTQ2102A)



Power Off from EN (RTQ2102A)



Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

The basic RTQ2102A and RTQ2102B application circuit are shown in Typical Application Circuit. External components selection is determined by considering both application request and device capability including device switching frequency, input and output voltage range and maximum load current.

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current, ΔI_L, increases with higher V_{IN} and decreases with higher inductance, as shown in the equation below:

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

where f is the operating frequency and L is the inductance. Lower ripple current reduces not only ESR losses in the output capacitors, but also the output voltage ripple. Higher operating frequency combined with smaller ripple current is necessary to achieve high efficiency. Thus, a large inductor is required to attain this goal.

The largest ripple current occurs at the highest V_{IN}. A reasonable starting point for selecting the ripple current is ΔI_L = 0.3 x I_{MAX} to 0.4 x I_{MAX}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Input and Output Capacitor Selection

An input capacitor, C_{IN}, is needed to filter out the trapezoidal current at the source of the high-side MOSFET.

To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at V_{IN} = 2V_{OUT}, where I_{RMS} = $I_{OUT(MAX)}$/2. This simple worst-case condition is commonly used for design.

Several capacitors may also be paralleled to meet the size or height requirements of the design. Ceramic capacitors have high ripple current, high voltage rating and low ESR, which makes them ideal for switching regulator applications.

However, they can also have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can lead to significant ringing. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. Thus, care must be taken to select a suitable input capacitor.

The selection of C_{OUT} is determined by the required ESR to minimize output voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response.

The output voltage ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right]$$

Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected to FB, as shown in Figure 3. The output voltage is set according to the following equation:

V_{OUT} = 0.45V x (1 + R_{FB1}/R_{FB2})

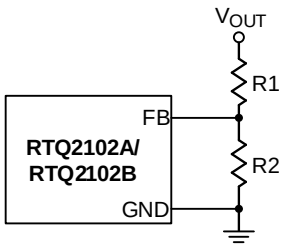


Figure 3. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. For output voltage accuracy, use divider resistors with 1% or better tolerance.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. The thermal resistance, $\theta_{JA(EVB)}$, is 47.7°C/W on a high effective-thermal-conductivity two-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C)/(47.7°C/W) = 2.09W for a WDFN-8L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The derating curves in Figure 4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

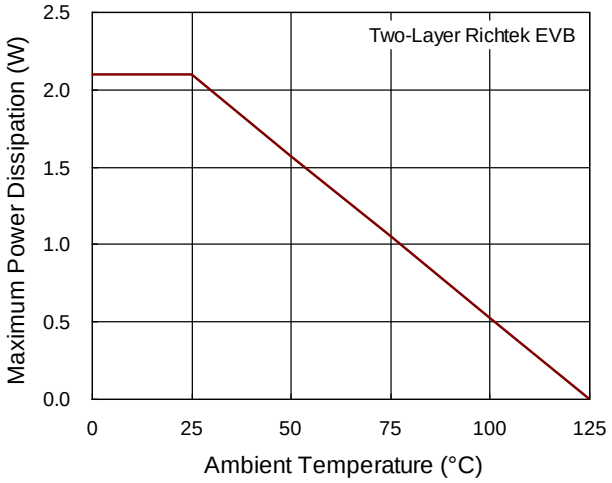


Figure 4. Derating Curve of Maximum Power Dissipation

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the device.

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high current path comprising of input capacitor, high-side FET, inductor, and the output capacitor should be as short as possible. This practice is essential for high efficiency.
- Place the input MLCC capacitors as close to the VIN and GND pins as possible. The major MLCC capacitors should be placed on the same layer as the RTQ2102A and RTQ2102B.
- LX node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the LX node to prevent stray capacitive noise pickup.
- Connect feedback network behind the output capacitors. Place the feedback components next to the FB pin.
- For better thermal performance, to design a wide and thick plane for GND pin or to add a lot of vias to GND plane.

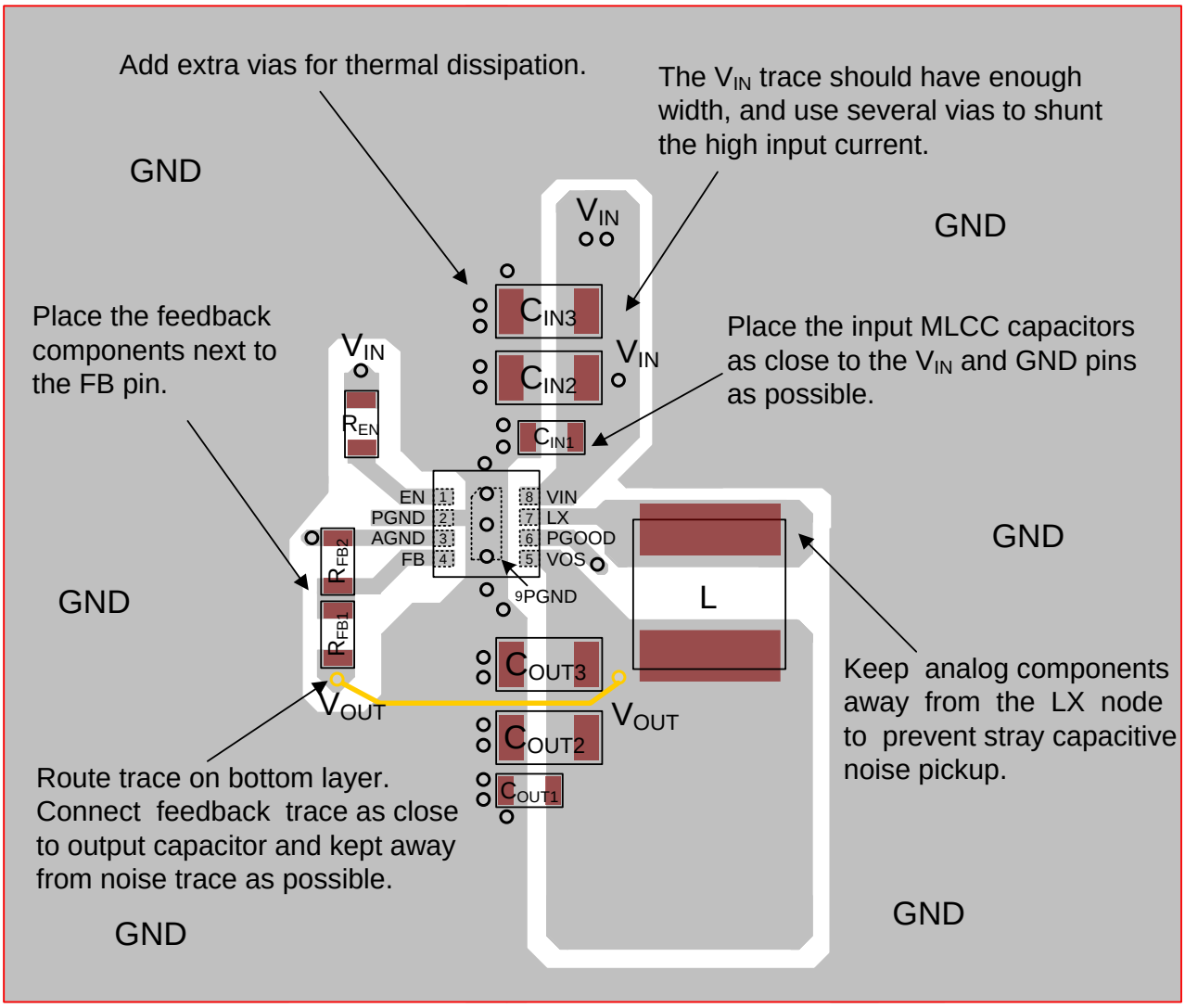
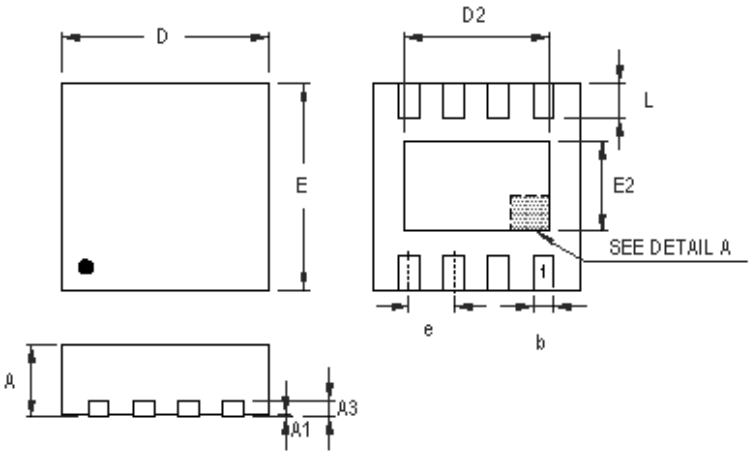
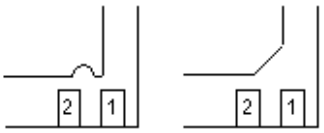


Figure 5. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

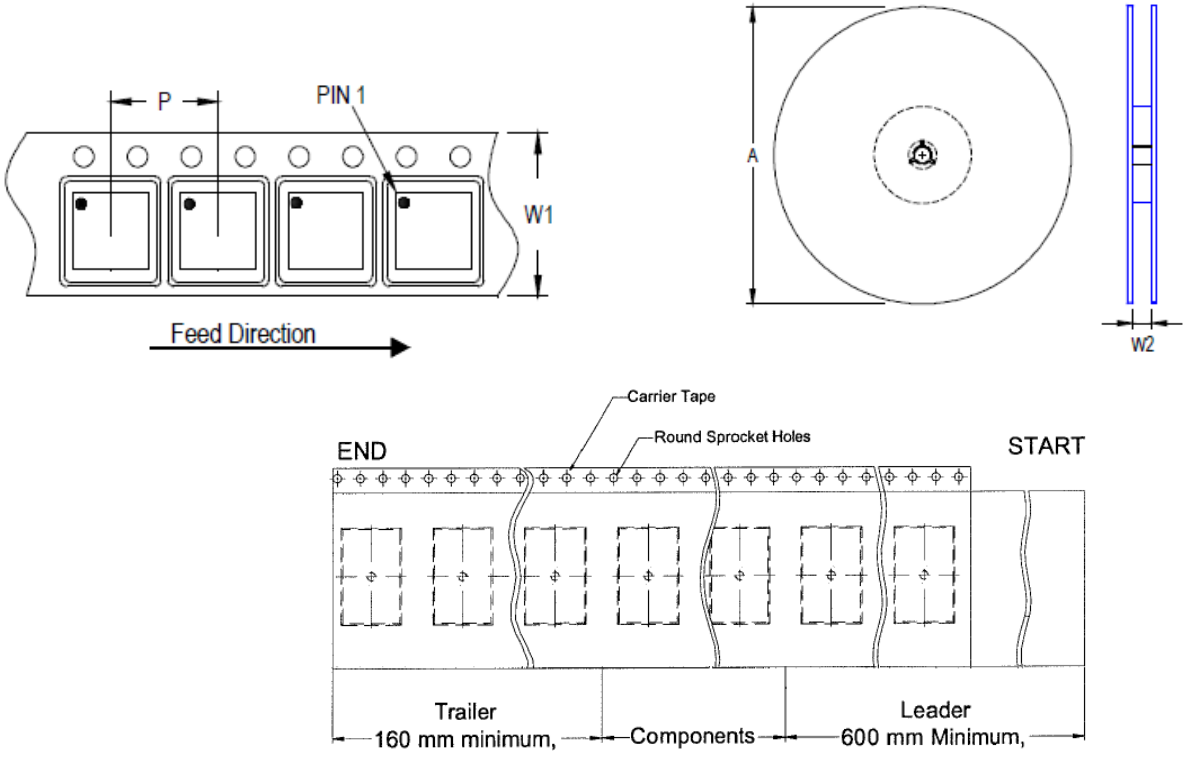
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	2.950	3.050	0.116	0.120
D2	2.100	2.350	0.083	0.093
E	2.950	3.050	0.116	0.120
E2	1.350	1.600	0.053	0.063
e	0.650		0.026	
L	0.425	0.525	0.017	0.021

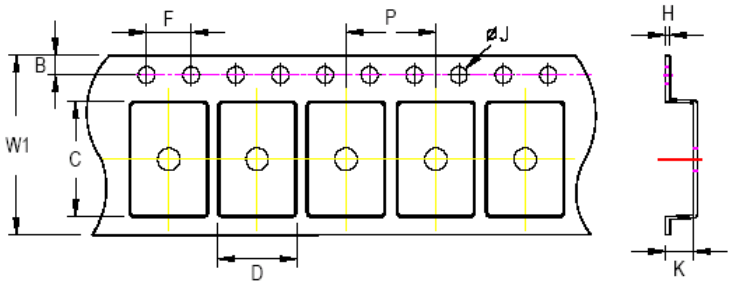
W-Type 8L DFN 3x3 Package

Packing Information

Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN & DFN 3x3	7”	1,500	Box A	18.3*18.3*8.0	3	4,500	Carton A	38.3*27.2*38.3	12	54,000
			Box E	18.6*18.6*3.5	1	1,500	For Combined or Partial Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

Datasheet Revision History

Version	Date	Description	Item
03	2023/4/12	Modify	Add RTQ2102B-QA General Description on P1 Features on P1 Simplified Application Circuit on P1 Ordering Information on P2 Marking Information on P2 Functional Pin Description on P3 Functional Block Diagram on P4 Operation on P4, 5, 6 Absolute Maximum Ratings on P7 Thermal Information on P7 Electrical Characteristics on P8 Typical Operating Characteristics P10, 11, 12, 13, 14 Note 2, Note 3, Note 4, Note 5 Note 6 on P8 Typical Application Circuit on P9 Application Information on P15, 16, 17 Packing Information on P18, 19, 20