36V$_{IN}$, 3A, High Efficiency, 2.1MHz, Synchronous Step-Down Converter

General Description

The RTQ2104BP is a 3A, high-efficiency, current mode synchronous step-down converter which is optimized for automotive applications. The device operates with input voltage from 3V to 36V and is protected from load dump transients up to 42V which eases input surge protection design. The device can program the output voltage between 0.8V and V_{IN}. The peak current mode control with simple internal compensation allows the use of small inductors and results in fast transient response and good loop stability.

The ultra-low minimum on-time enables constant-frequency operation even at very high step-down ratios. The built-in spread-spectrum frequency modulation further helps system designers with better EMC management.

The RTQ2104BP provides complete protection functions such as input under-voltage lockout, output under-voltage protection, over-current protection, and thermal shutdown. Cycle-by-cycle current limit provides protection against shorted outputs, and soft-start eliminates input current surge during start-up. The RTQ2104BP is available in a SOP-8 (Exposed Pad) package.

Applications

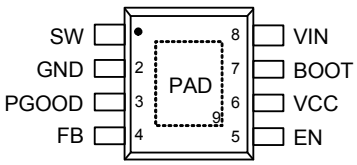
- Automotive Systems
- Car Camera Module and Car Cockpit Systems
- Connected Car Systems
- Point of Load Regulator in Distributed Power Systems
- Digital Set-Top Boxes
- Broadband Communications

Features

- **AEC-Q100 Grade 1 Qualified**
- **Wide Input Voltage Range**
  - **4V to 36V**
  - **3V to 36V (Soft-start is finished)**
- **Wide Output Voltage Range : 0.8V to V_{IN}**
- **Maximum Output Current : 3A**
- **Peak Current Mode Control**
- **Integrated 80mΩ Switch and 80mΩ Synchronous Rectifier**
- **Fast 60ns Minimum Switch On-Time**
- **Ultra-Short 65ns Minimum Switch Off-Time**
- **Fixed Switching Frequency : 2.1MHz**
- **Built-In Spread-Spectrum Frequency Modulation for Low EMI**
- **Power Good Indication**
- **Enable Control**
- **0.8V ±1.5% Reference Accuracy**
- **Adjacent Pin-Short Protection**
- **Built-In UVLO, OCP, UVP, OTP**

Pin Configuration

(TOP VIEW)



SOP-8 (Exposed Pad)

Ordering Information

RTQ2104BP□□-QA

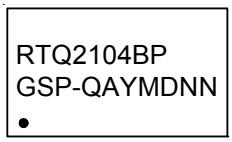
- Grade
  QA : AEC-Q100 Qualified and Screened by High Temperature
- Package Type
  SP : SOP-8 (Exposed Pad-Option 2)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



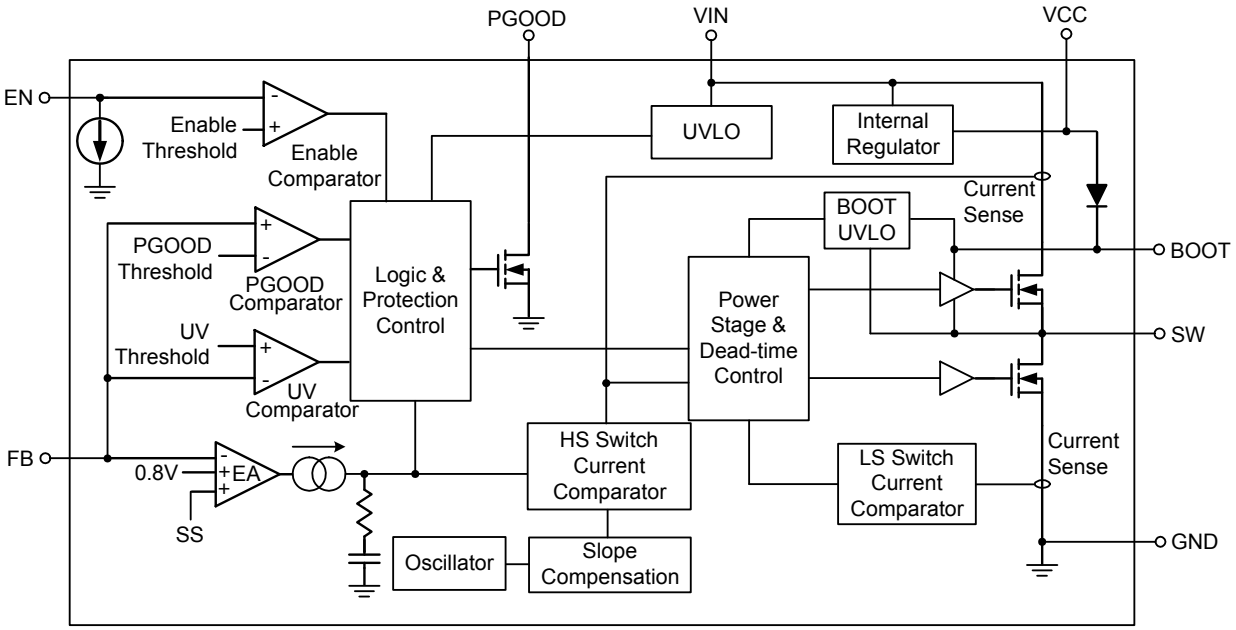
RTQ2104BPGSP-QA : Product Number

YMDNN : Date Code

Functional Pin Description

PIN NO.	PIN NAME	PIN FUNCTION
1	SW	Switch node. SW is the switching node that supplies power to the output and connects the output LC filter from SW to the output load.
2	GND	Ground. Provide the ground return path for the control circuitry and low-side power MOSFET. Connect this pin to the negative terminals of the input capacitor and output capacitor.
3	PGOOD	Open-drain power-good indication output. Once soft-start is finished, PGOOD will be pulled low to ground if any internal protection is triggered.
4	FB	Feedback voltage input. Connect this pin to the midpoint of the external feedback resistive divider to set the output voltage of the converter to the desired regulation level. The device regulates the FB voltage at a feedback reference voltage, typically 0.8V.
5	EN	Enable control input. A logic-high enables the converter; a logic-low forces the device into shutdown mode.
6	VCC	Linear regulator output. VCC is the output of the internal 5V linear regulator powered by VIN. Decouple with a 10μF, X7R ceramic capacitor from VCC to ground for normal operation.
7	BOOT	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.1μF, X7R ceramic capacitor in series with a 10Ω resistance between this pin and SW pin.
8	VIN	Power input. The input voltage range is from 3V to 36V after soft-start is finished. Connect input capacitors between this pin and GND. It is recommended to use a 4.7μF, X7R and a 0.1μF, X7R capacitors.
9 (Exposed Pad)	PAD	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large GND plane. Connect this GND plane to other layers with thermal vias to help dissipate heat from the device.

Functional Block Diagram



Operation

Control Loop

The RTQ2104BP is a high efficiency step-down converter utilizes the peak current mode control. An internal oscillator initiates turn-on the high-side MOSFET switch. At the beginning of each clock cycle, the internal high-side MOSFET switch turns on, allowing current to ramp up in the inductor. The inductor current is internally monitored during each switching cycle. The output voltage is sensed on the FB pin via the resistor divider, R1 and R2, and compared with the internal reference voltage (V_{REF}) to generate a compensation signal (V_{COMP}). A control signal derived from the inductor current is compared to the V_{COMP}, derived from the feedback voltage. When the inductor current reaches its threshold, the high-side MOSFET switch is turned off and inductor current ramps down. While the high-side MOSFET switch is off, the inductor current is supplied through the low-side MOSFET switch. This cycle repeats at the next clock cycle. In this way, duty-cycle and output voltage are controlled by regulating inductor current.

Forced-PWM Mode

The RTQ2104BP operates in Forced-PWM Mode (FPWM).

Forced-PWM operation provides constant frequency operation at all loads and is useful in applications sensitive to switching frequency. This mode provides low output voltage ripple, tight output voltage regulation, and constant switching frequency. In this mode, a negative current limit of ISK_L is imposed to prevent damage to the low-side MOSFET switch of the regulator. This feature ensures that the switching frequency stays away from the AM frequency band, while operating between the minimum and maximum duty cycle limits.

Input Voltage Range

The minimum on-time, t_{ON_MIN}, is the smallest duration of time which the high-side MOSFET switch can be in its "on" state. Considering the minimum on-time, the allowed maximum input voltage, V_{IN_MAX}, is calculated by :

$$V_{IN\_MAX} \leq \frac{V_{OUT}}{t_{ON\_MIN} \times f_{SW}}$$

where the minimum on-time of the RTQ2104BP is 60ns (typically), and f_{SW} is the maximum operating frequency. The maximum operating frequency of the RTQ2104BP is 2.45MHz considering the built-in spread-spectrum frequency modulation.

In contrast, the minimum off-time determines the allowed minimum operating input voltage, V_{IN_MIN}, to maintain the the fixed frequency operation. The minimum off-time, t_{OFF_MIN}, is the smallest amount of time that the RTQ2104BP is capable of turning on the low-side MOSFET switch, tripping the current comparator, and turning the MOSFET switch back off. Below shows minimum off-time calculation that considers the loss terms :

$$V_{IN\_MIN} \geq \left[\frac{V_{OUT} + I_{OUT\_MAX} \times \left(R_{DS(ON)\_L} + DCR\right)}{1 - t_{OFF\_MIN} \times f_{SW}} \right] + I_{OUT\_MAX} \times \left(R_{DS(ON)\_H} - R_{DS(ON)\_L}\right)$$

where the minimum off-time of the RTQ2104BP is 65ns (typically), $R_{DS(ON)\_H}$ is the on-resistance of the high-side MOSFET switch, $R_{DS(ON)\_L}$ is the on-resistance of the low-side MOSFET switch, and DCR is the DC resistance of inductor.

Maximum Duty Cycle Operation

The RTQ2104BP is designed to operate in dropout at the high duty cycle approaching 100%. If the operational duty cycle is large and the required off-time becomes smaller than minimum off-time, the RTQ2104BP starts to enable skip off-time function and keeps high-side MOSFET switch on continuously. The RTQ2104BP implements skip off-time function to achieve high duty approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application. The input voltage at which the devices enter dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

BOOT UVLO

The BOOT UVLO circuit is implemented to ensure a sufficient voltage of BOOT capacitor for turning on the high-side MOSFET switch at any conditions. The BOOT UVLO usually actives at extremely high conversion ratio. With such conditions, the low-side MOSFET switch may not

have sufficient turn-on time to charge the BOOT capacitor. The device monitors the BOOT pin capacitor voltage and forces to turn on the low-side MOSFET switch when the BOOT to SW voltage falls below $V_{BOOT\_UVLO\_L}$ (typically, 2.3V). Meanwhile, the minimum off-time is extended to 150ns (typically), hence prolong the BOOT capacitor charging time. The BOOT UVLO is sustained until the $V_{BOOT-SW}$ is higher than $V_{BOOT\_UVLO\_H}$ (typically, 2.4V).

Internal Regulator

The device integrates a 5V linear regulator (V_{CC}) that is supplied by VIN, and provides power to the internal circuitry. The internal regulator operates in low dropout mode when V_{IN} is below 5V. The V_{CC} can be used as the PGOOD pull-up supply but it is "NOT" allowed to power other device or circuitry. The VCC pin must be bypassed to ground with a minimum value of effective VCC capacitance 3μF.

Enable Control

The RTQ2104BP provides an EN pin, as an external chip enable control, to enable or disable the device. If V_{EN} is held below a logic-low threshold voltage (V_{ENL}), switching is inhibited even if the VIN voltage is above VIN under-voltage lockout threshold (V_{UVLOH}). If V_{EN} is held below 0.4V, the converter will enter into shutdown mode, that is, the converter is disabled. During shutdown mode, the supply current can be reduced to I_{SHDN} (5μA or below). If the EN voltage rises above the logic-high threshold voltage (V_{ENH}) while the VIN voltage is higher than V_{UVLOH}, the device will be turned on, that is, switching being enabled and soft-start sequence being initiated. The current source of EN typically sinks 1.2μA.

Soft-Start

The soft-start function is used to prevent large inrush currents while the converter is being powered up. The RTQ2104BP provides an internal soft-start feature for inrush currents control. During the start-up sequence, the internal soft-start capacitor is charged by an internal current source (I_{SS}) to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. If the output is pre-biased to a certain voltage during start-up for some reason, the device will not start switching until the voltage difference between internal soft-start voltage and FB pin is larger than 400mV (i.e. $V_{SS} - V_{FB} > 400mV$, typically). Only when the internal soft-start ramp voltage is higher than the feedback voltage V_{FB}, the switching will be resumed. The output voltage can then ramp up smoothly to its targeted regulation voltage, and the converter can have a monotonic smooth start-up. The PGOOD pin will be in high impedance and the V_{PGOOD} will be held high in the 1.6ms (typically). The typical start-up waveform shown in Figure 1 indicates the sequence and timing between the output voltage and related voltage.

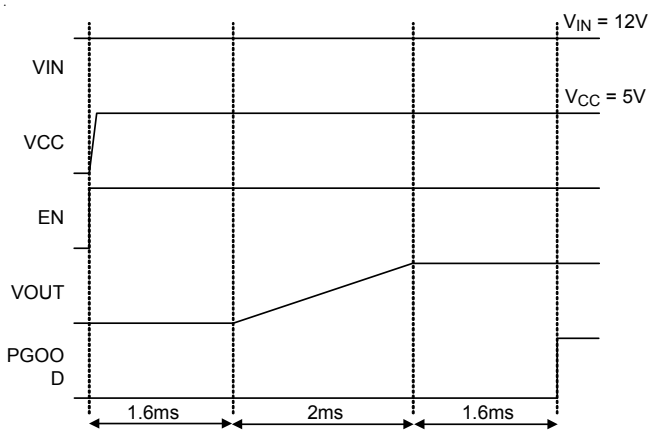


Figure 1. Start-Up Sequence

Power Good Indication

The RTQ2104BP features an open-drain power-good output (PGOOD) to monitor the output voltage status. The output delay of comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Pull-up PGOOD with a resistor to V_{CC} or an external voltage below 5.5V. The power-good function is activated after soft-start is finished and is controlled by a comparator connected to the feedback signal V_{FB}. If V_{FB} rises above the power-good high threshold (V_{TH_PGLH1}) (typically 90% of the reference voltage), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapsed. When V_{FB} exceeds V_{TH_PGHL1} (typically 120% of the reference voltage), the PGOOD pin will be pulled low. Moreover, the IC turns off high-side MOSFET switch and turns on low-side MOSFET switch until the inductor current reaches I_{SK_L}. If the VFB is still higher than VTH_PGHL1, the RTQ2104BP enters low-side MOSFET switch sinking current limit operation.

For V_{FB} higher than V_{TH_PGHL1}, V_{PGOOD} can be pulled high again if V_{FB} drops back by a power-good high threshold (V_{TH_PGLH2}) (typically 117% of the reference voltage). When V_{FB} falls below power-good low threshold (V_{TH_PGHL2}) (typically 85% of the reference voltage), the PGOOD pin will be pulled low. Once being started-up, if any internal protection is triggered, PGOOD will be pulled low to GND. The internal open-drain pull-down device (10Ω, typically) will pull the PGOOD pin low. The power good indication profile is shown in Figure 2.

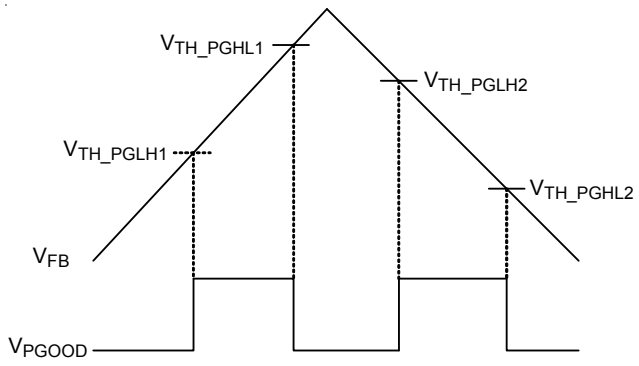


Figure 2. The Logic of PGOOD

Spread-Spectrum Operation

Due to the periodicity of the switching signals, the energy concentrates in one particular frequency and also in its harmonics. These levels or energy is radiated and therefore this is where a potential EMI issue arises. The built-in spread-spectrum frequency modulation further helps system designers with better EMC management. The spread spectrum can be active when soft-start is finished . The spread-spectrum is implemented by a pseudo random sequence and uses +6% spread of the switching frequency, that is, the frequency will vary from 2.1MHz to 2.226MHz. Therefore, the RTQ2104BP still guarantees that the 2.1MHz switching frequency does not drop into the AM band limit of 1.8MHz.

Input Under-Voltage Lockout

In addition to the EN pin, the RTQ2104BP also provides enable control through the VIN pin. If V_{EN} rises above V_{ENH} first, the switching will be inhibited until the VIN voltage rises above V_{UVLOH}. It is to ensure that the internal regulator is ready so that operation with not-fully-enhanced internal MOSFET switches can be prevented. After the device is powered up, if the VIN voltage goes below the UVLO falling threshold voltage (V_{UVLOL}), this switching will be inhibited; if VIN voltage rises above the UVLO rising threshold (V_{UVLOH}), the device will resume switching. Note that V_{IN} = 3V is only designed for cold crank requirement, and normal input voltage should be larger than V_{UVLOH}.

High-Side Switch Peak Current-Limit Protection

The RTQ2104BP includes a cycle-by-cycle high-side switch peak current-limit protection against the condition that the inductor current increasing abnormally, even over the inductor saturation current rating. The high-side MOSFET switch peak current limit of the RTQ2104BP is 5A (typically). The inductor current through the high-side MOSFET switch will be measured after a certain amount of delay when the high-side MOSFET switch being turned on. If an over-current condition occurs, the converter will immediately turn off the high-side MOSFET switch and turn on the low-side MOSFET switch to prevent the inductor current exceeding the high-side MOSFET switch peak current limit (I_{LIM_H}).

Low-Side Switch Current-Limit Protection

The RTQ2104BP not only implements the high-side MOSFET switch peak current limit but also provides the sourcing current limit and sinking current limit for low-side MOSFET switch. With these current protections, the IC can easily control inductor current at both side MOSFET switches and avoid current runaway for short-circuit condition.

For the low-side MOSFET switch sourcing current limit, there is a specific comparator in internal circuitry to compare the low-side MOSFET switch sourcing current to the low-side MOSFET switch sourcing current limit at the end of every clock cycle. When the low-side MOSFET switch sourcing current is higher than the low-side MOSFET switch sourcing current limit which is high-side MOSFET switch current limit (I_{LIM_H}) multiplied by 0.95 (typically), the new switching cycle is not initiated until inductor current drops below the low-side MOSFET switch sourcing current limit.

For the low-side MOSFET switch sinking current limit protection, it is implemented by detecting the voltage across the low-side MOSFET switch. If the low-side MOSFET switch sinking current exceeds the low-side MOSFET switch sinking current limit (I_{SK_L}) (typically, 2A), the converter will immediately turn off the low-side MOSFET switch and turn on the high-side MOSFET switch. "Do Not" choose too small inductance, which may trigger the low side MOSFET switch sinking current limit protection.

Output Under-Voltage Protection

The RTQ2104BP includes output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage (V_{FB}). If V_{FB} drops below the under-voltage protection trip threshold (typically 50% of the internal reference voltage), the UV comparator will go high to turn off the high-side MOSFET switch and then turn off the low-side MOSFET switch when the inductor current drops to zero. If the output under-voltage condition continues for a period of time, the RTQ2104BP enters output under-voltage protection with hiccup mode and discharges the internal V_{SS}. During hiccup mode, the device remains shutdown. After the internal V_{SS} is discharged to less than 150mV (typically), the RT2104 attempts to re-start up again. The high-side MOSFET switch will start switching when voltage difference between internal V_{SS} and V_{FB} is larger than 400mV (i.e. $V_{SS} - V_{FB} > 400mV$, typically). If the fault condition is not removed, the high-side MOSFET switch stops switching when the voltage difference between internal V_{SS} and V_{FB} is 700mV (i.e. $V_{SS} - V_{FB} = 700mV$, typically). Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed. A short circuit protection and recovery profile is shown in Figure 3.

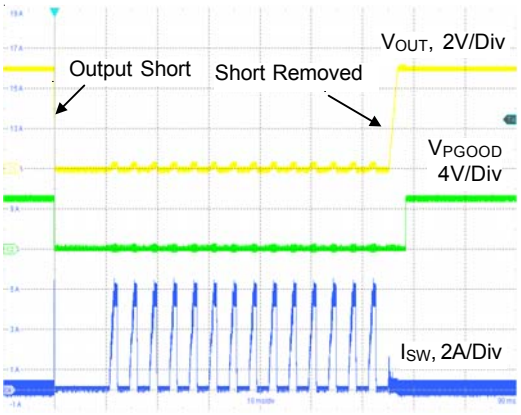


Figure 3. Short Circuit Protection and Recovery

Over-Temperature Protection

The RTQ2104BP includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold T_{SD}. Once the junction temperature cools down by a thermal shutdown hysteresis (ΔT_{SD}), the IC will resume normal operation with a complete soft-start.

Pin-Short Protection

The RTQ2104BP provides pin-short protection for neighbor pins. The internal protection fuse will be burned out to prevent IC smoke, fire and spark when BOOT pin is shorted to VIN pin. The hiccup mode protection will be triggered to avoid IC burn-out when SW pin is shorted to ground when internal high-side MOSFET turns on.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 42V
- Switch Voltage, SW ---------- –0.3V to 42V
  <50ns ---------- –5V to 46.3V
- BOOT Voltage, V_{BOOT} ---------- –0.3V to 48V
- BOOT to SW, $V_{BOOT} – V_{SW}$ ---------- –0.3V to 6V
- EN, Voltage ---------- –0.3V to 42V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 (Exposed Pad) ---------- 4.31W
- Package Thermal Resistance (Note 2)
  SOP-8 (Exposed Pad), θ_{JA} ---------- 29°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 6.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage ---------- 3V to 36V
- Output Voltage ---------- 0.8V to V_{IN}
- Junction Temperature Range ---------- –40°C to 150°C
- Ambient Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, T_A = T_J = –40°C to 125°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
Operating Input Voltage	V_{IN}	Soft-start is finished	3	--	36	V
VIN Under-Voltage Lockout Threshold	V_{UVLOH}	V_{IN} rising	3.6	3.8	4	V
	V_{UVLOL}	V_{IN} falling	2.7	2.85	3	
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	5	μA
Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = 0.82V, not switching, FPWM	--	1.2	--	mA
Output Voltage						
Reference Voltage	V_{REF}	3V < V_{IN} < 36V, PWM T_A = T_J = 25°C	0.792	0.8	0.808	V
		3V < V_{IN} < 36V, PWM T_A = T_J = –40°C to 125°C	0.788	0.8	0.812	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Enable Voltage						
Enable Threshold Voltage	V_{ENH}	V_{EN} rising	1.15	1.25	1.35	V
	V_{ENL}	V_{EN} falling	0.9	1.05	1.15	
Current Limit						
High-Side Switch Current Limit	I_{LIM_H}	$V_{BOOT} - V_{SW}$ = 4.8V Min. Duty Cycle	4.25	5	5.75	A
Low-Side Switch Sinking Current Limit	I_{SK_L}	From drain to source	--	2	--	A
Switching						
Switching Frequency	f_{SW}		1.89	2.1	2.31	MHz
Minimum On-Time	t_{ON_MIN}		--	60	80	ns
Minimum Off-Time	t_{OFF_MIN}		--	65	80	ns
Internal MOSFET						
High-Side Switch On-Resistance	$R_{DS(ON)\_H}$		--	80	150	mΩ
Low-Side Switch On-Resistance	$R_{DS(ON)\_L}$		--	80	150	mΩ
High-Side Switch Leakage Current	I_{LK_H}	V_{EN} = 0V, V_{SW} = 0V	--	--	1	μA
Soft-Start						
Soft-Start Period	t_{SS}	10% to 90%	1.4	2	2.6	ms
Power Good						
Power Good Threshold	V_{TH_PGLH1}	V_{FB} rising, % of V_{REF}, PGOOD from low to high	85	90	95	%
	V_{TH_PGHL1}	V_{FB} rising, % of V_{REF}, PGOOD from high to low	--	120	--	
	V_{TH_PGHL2}	V_{FB} falling, % of V_{REF}, PGOOD from high to low	80	85	90	%
	V_{TH_PGLH2}	V_{FB} falling, % of V_{REF}, PGOOD from low to high	--	117	--	
Power Good Leakage Current	I_{LK_PGOOD}	PGOOD signal good, V_{FB} = V_{REF}, V_{PGOOD} = 5.5V	--	--	0.5	μA
Power Good Sink Current Capability	I_{SK_PGOOD}	PGOOD signal fault, I_{PGOOD} sinks 2mA	--	--	0.3	V
Spread Spectrum						
Spread-Spectrum Range	SS		--	+6	--	%
Over-Temperature Protection						
Thermal Shutdown	T_{SD}		--	175	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	15	--	°C
Output Under-Voltage Protection						
UVP Trip Threshold	V_{UVP}	UVP detect	0.35	0.4	0.45	V

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

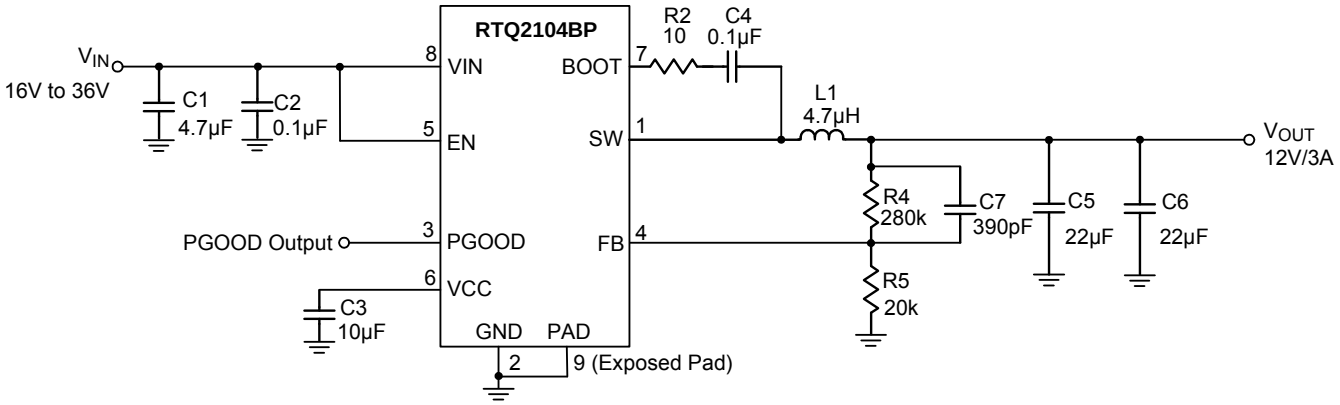
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. The first layer is filled with copper. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

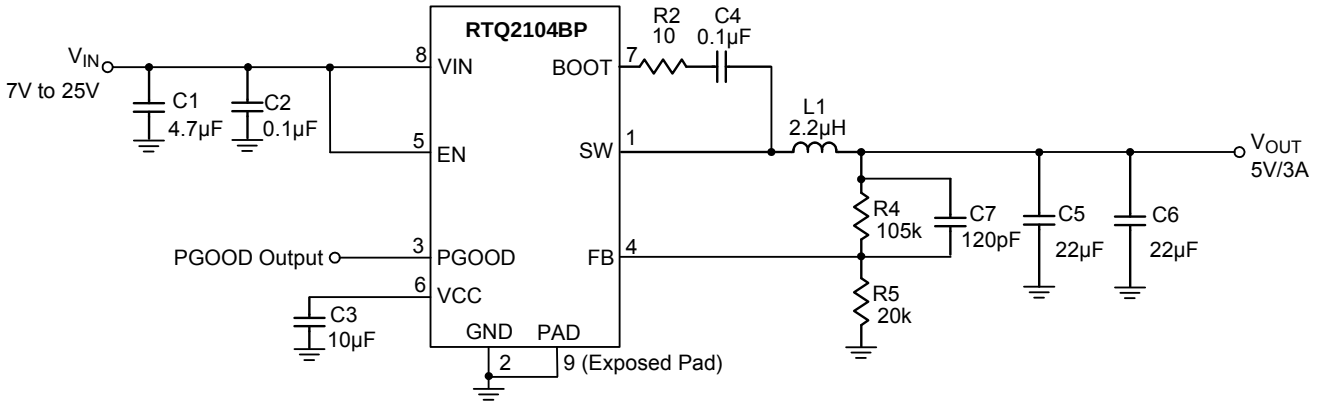
Typical Application Circuit

12V, 3A Step-Down Converter



L1 = Cyntec-VCHA075D-4R7MS6
C5/C6 = GCM32EC71E226KE36L
C1 = GRM31CR71H475KA12L

5V, 3A Step-Down Converter

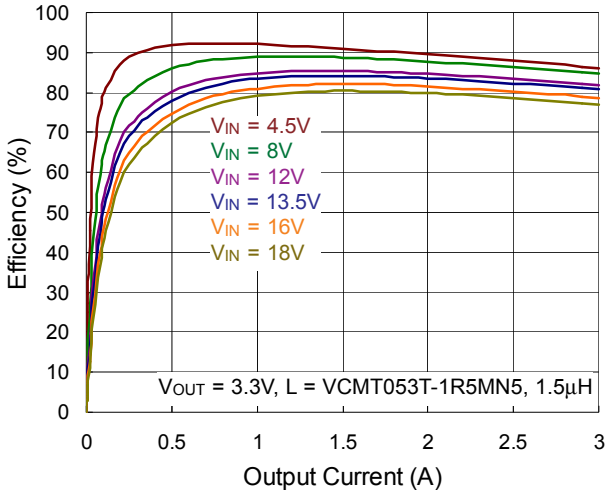


L1 = Cyntec-VCMT063T-2R2MN5
C5/C6 = GRM31CR71A226KE15L
C1 = GRM31CR71H475KA12L

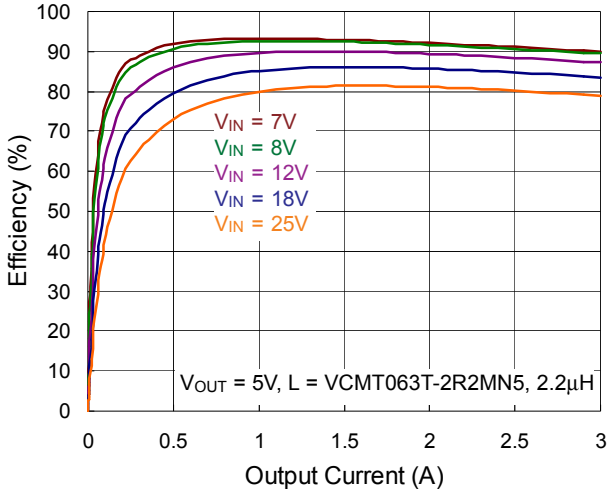
Typical Operating Characteristics

Unless otherwise specified the following conditions apply : V_{IN} = 12V, T_A = 25°C. Specified temperatures are ambient.

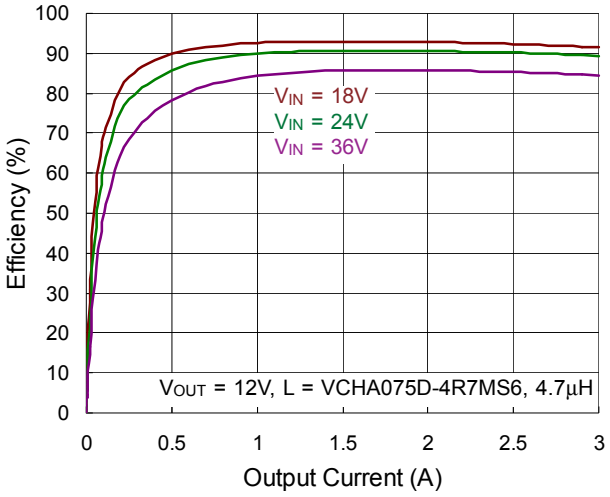
Efficiency vs. Output Current



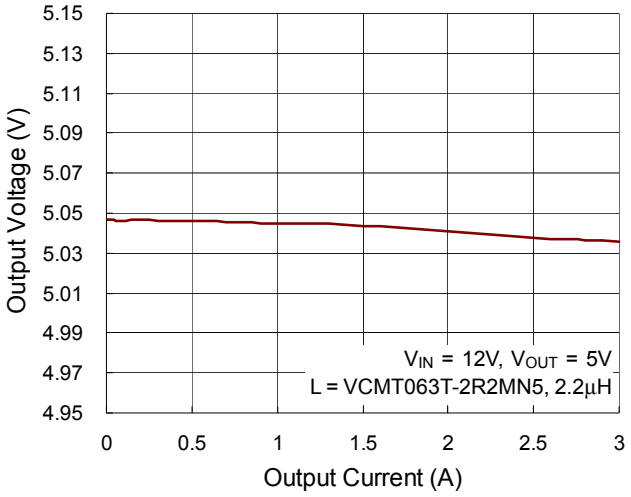
Efficiency vs. Output Current



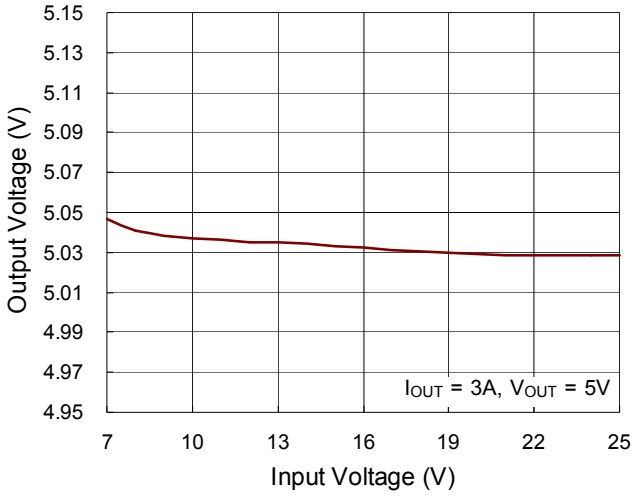
Efficiency vs. Output Current



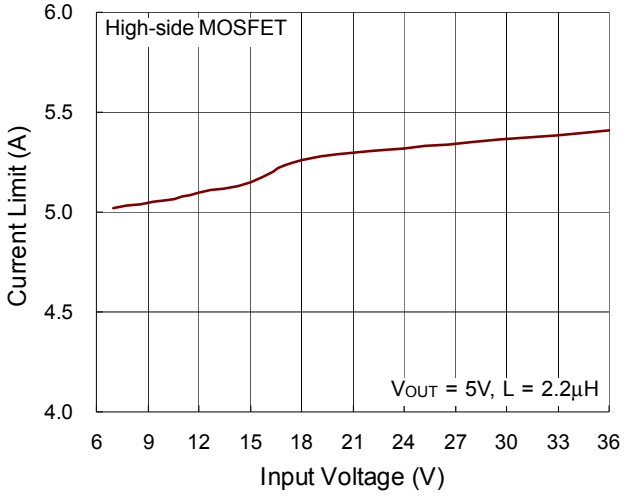
Output Voltage vs. Output Current



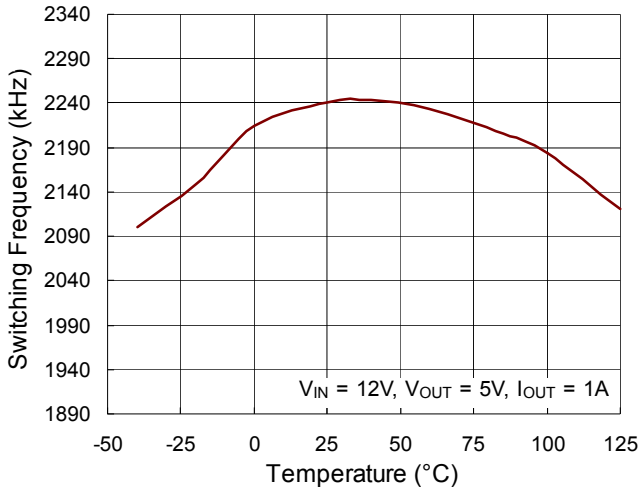
Output Voltage vs. Input Voltage



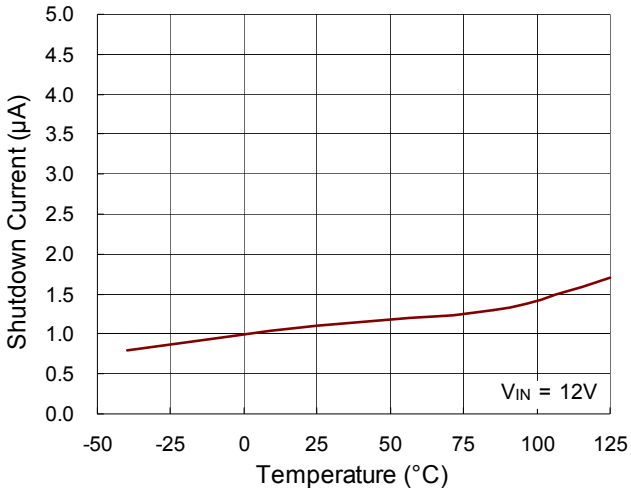
Current Limit vs. Input Voltage



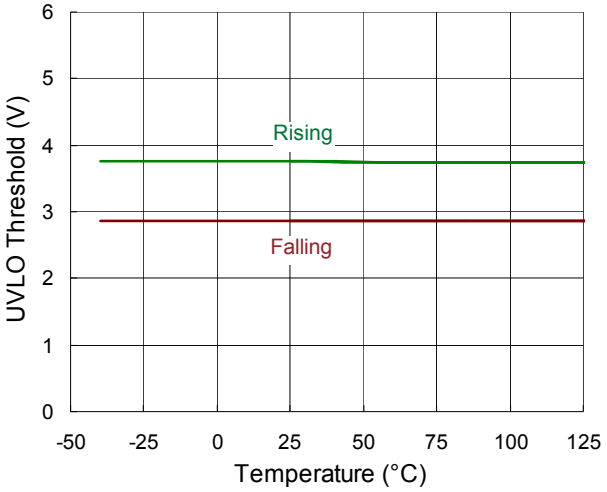
Switching Frequency vs. Temperature



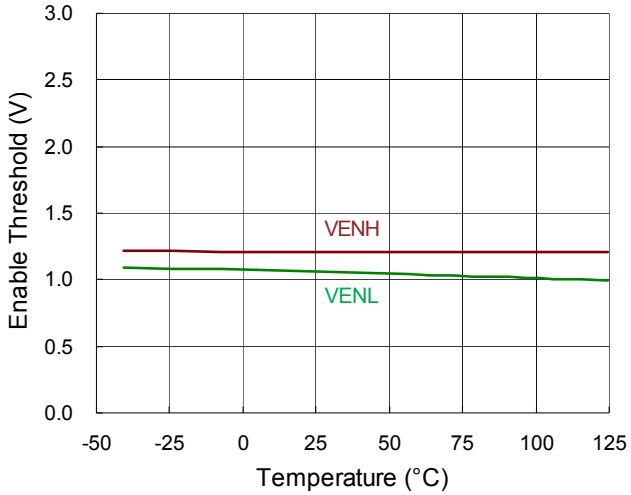
Shutdown Current vs. Temperature



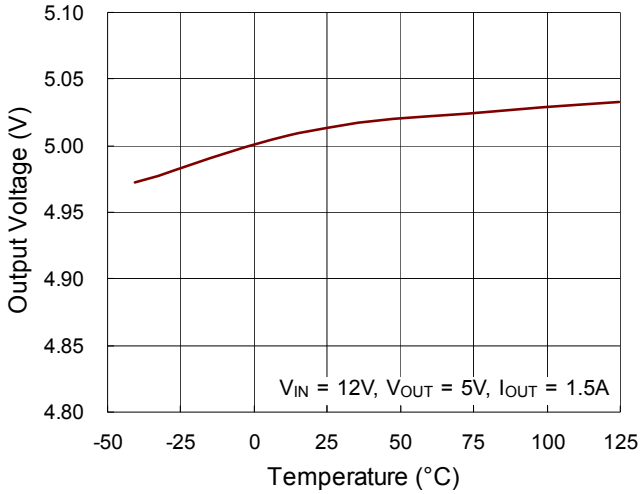
UVLO Threshold vs. Temperature



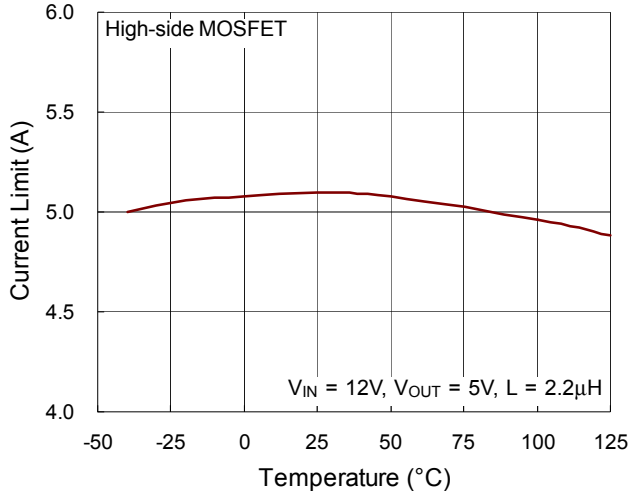
Enable Threshold vs. Temperature



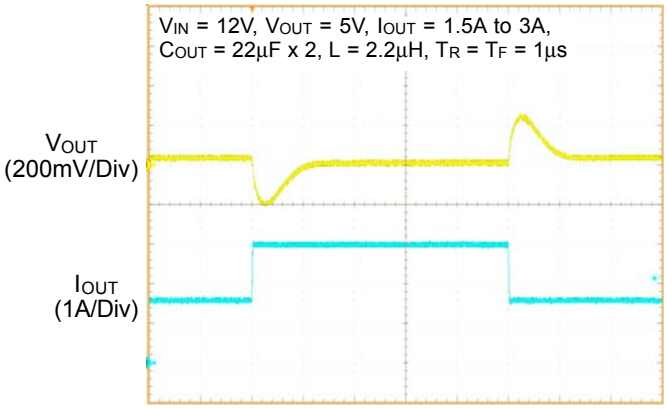
Output Voltage vs. Temperature



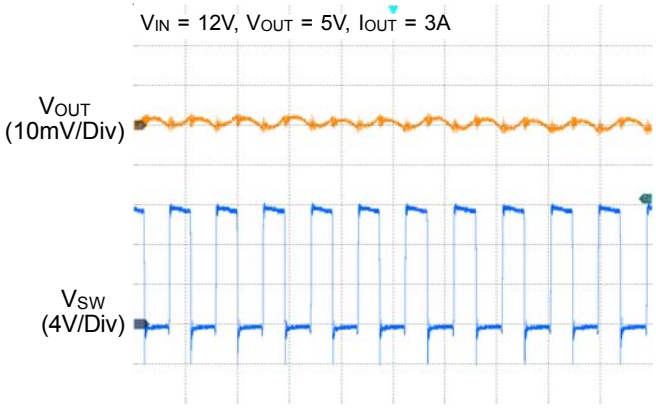
Current Limit vs. Temperature



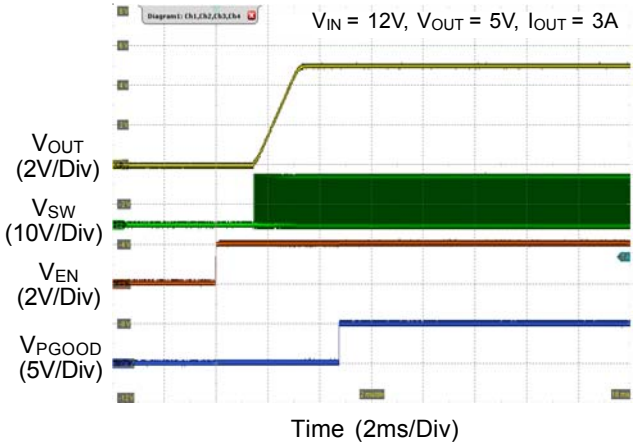
Load Transient Response



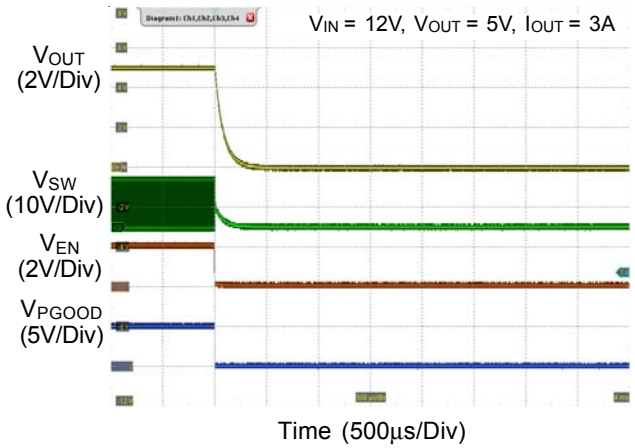
Output Ripple Voltage



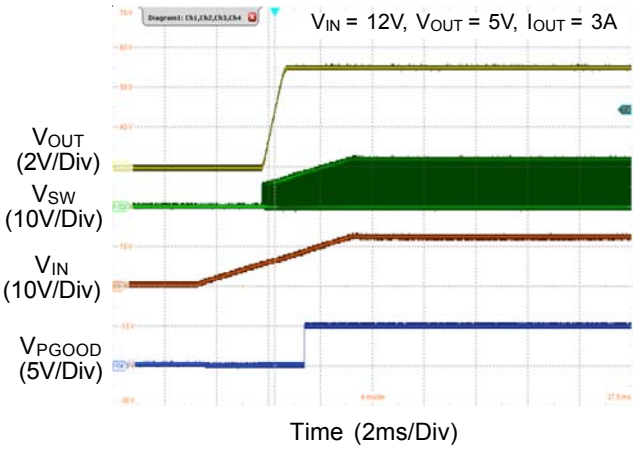
Power On from EN



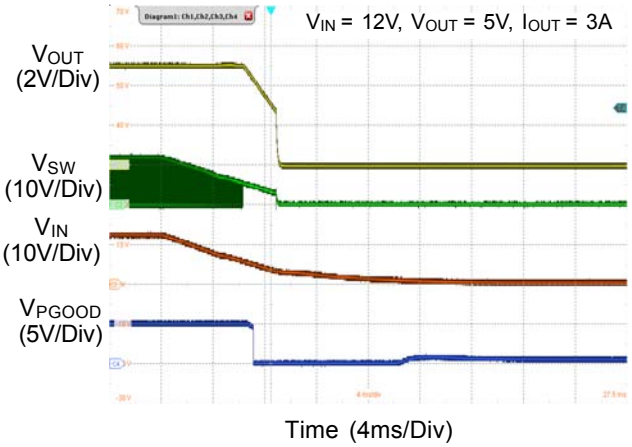
Power Off from EN



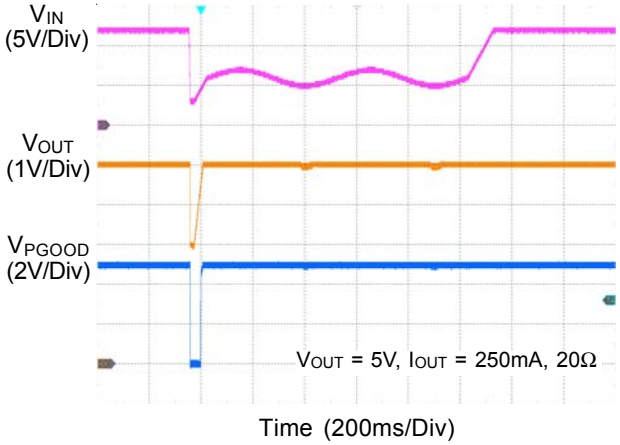
Power On from VIN



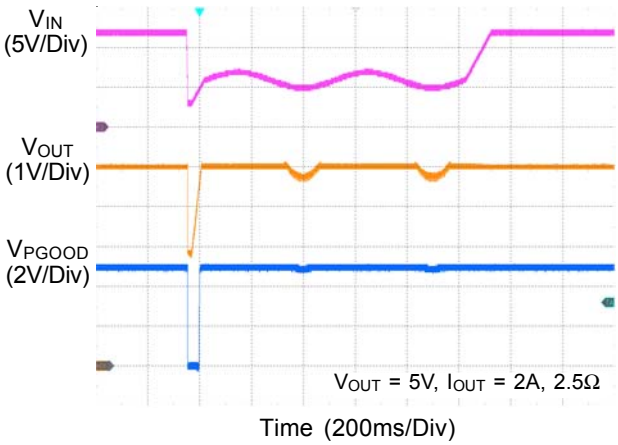
Power Off from VIN



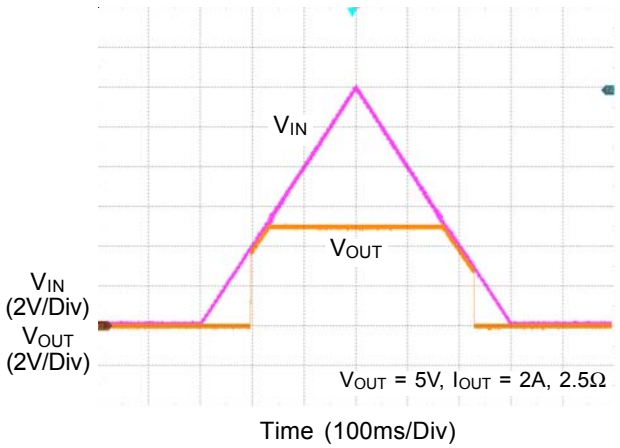
Level III of Starting Profile (ISO16750-2)



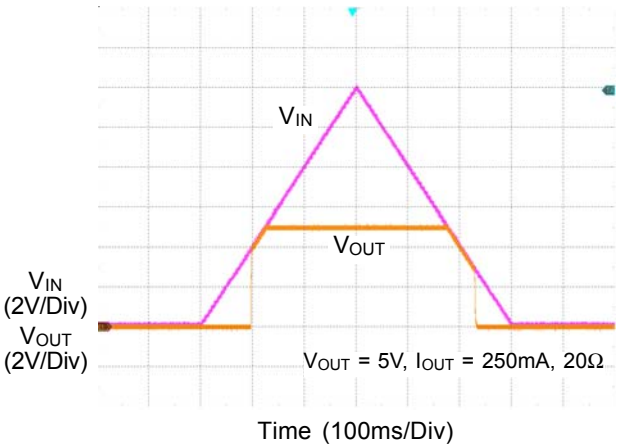
Level III of Starting Profile (ISO16750-2)



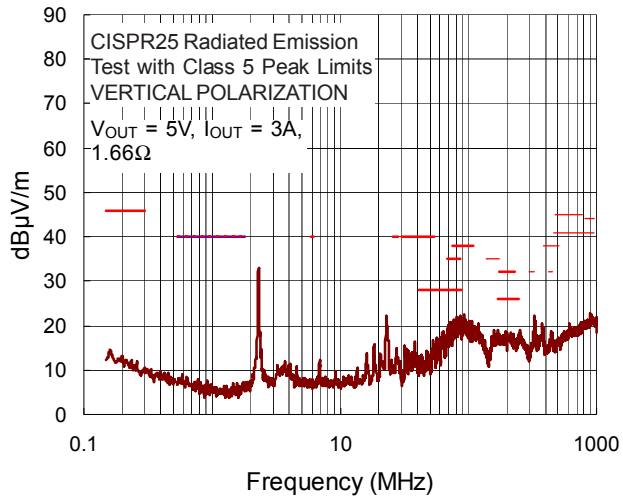
Start-Up Dropout Performance



Start-Up Dropout Performance



Radiated EMI Performance



Application Information

A general the RTQ2104BP application circuit is shown in typical application circuit section. External component selection is largely driven by the load requirement. Next, the inductor L, the input capacitor C_{IN}, and the output capacitor C_{OUT} are chosen. Next, feedback resistors and compensation circuit are selected to set the desired output voltage and crossover frequency. Next, the internal regulator capacitor C_{VCC}, the bootstrap resistor R_{BOOT}, and the bootstrap capacitor C_{BOOT} can be selected. Finally, the remaining optional external components can be selected for functions such as the EN and PGOOD.

Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. This results in additional phase lag in the loop and reduces the crossover frequency. As the ratio of the slope-compensation ramp to the sensed-current ramp increases, the current-mode system tilts towards voltage-mode control. Lower inductance values allow for smaller case size, but the increased ripple lowers the effective current limit threshold, increases the AC losses in the inductor and may trigger low-side switch sinking current limit at FPWM. It also causes insufficient slope compensation and ultimately loop instability as duty cycle approaches or exceeds 50%. A good compromise among size, efficiency, and transient response can be achieved by setting an inductor current ripple (ΔI_L) with about 10% to 50% of the maximum rated output current (3A).

To enhance the efficiency, choose a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The inductor value determines not only the ripple current but also the load-current value at which DCM/CCM switchover occurs. The selected inductor should have a saturation current rating greater than the peak current limit of the device. The core must be large enough not to saturate at the peak inductor current (I_{L_PEAK}) :

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2} \Delta I_L$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the high-side switch peak current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the high-side switch peak current limit rather than the peak inductor current. It is recommended to use shielded inductors for good EMI performance.

Input Capacitor Selection

Input capacitor, C_{IN}, is needed to filter the pulsating current at the drain of the high-side MOSFET switch. The C_{IN} should be sized to do this without causing a large variation in input voltage. The peak-to-peak voltage ripple on input capacitor can be estimated as equation below :

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + ESR \times I_{OUT}$$

where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

Figure 4 shows the C_{IN} ripple current flowing through the input capacitors and the resulting voltage ripple across the capacitors. For ceramic capacitors, the equivalent series resistance (ESR) is very low, the ripple which is caused by ESR can be ignored, and the minimum value of effective input capacitance can be estimated as equation below :

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

where $\Delta V_{CIN\_MAX} \leq 200mV$

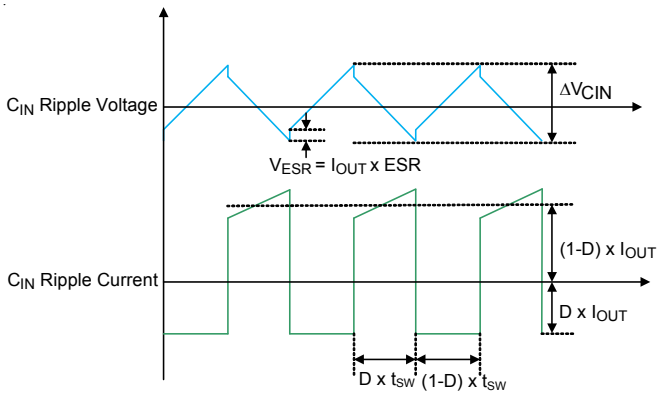


Figure 4. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current. The RMS ripple current (I_{RMS}) of the regulator can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) as the following equation :

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

From the above, the maximum RMS input ripple current occurs at maximum output load, which will be used as the requirements to consider the current capabilities of the input capacitors. The maximum ripple voltage usually occurs at 50% duty cycle, that is, V_{IN} = 2 x V_{OUT}. It is common to use the worse $I_{RMS} \cong 0.5 \times I_{OUT\_MAX}$ at V_{IN} = 2 x V_{OUT} for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes. Ceramic capacitors are ideal for switching regulator applications because of its small size, robustness, and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the RTQ2104BP circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pin with a low inductance connection to the GND of the IC. It is recommended to connect a 4.7µF, X7R capacitor between the VIN pin and the GND pin. For filtering high frequency noise, an additional small 0.1µF capacitor should be placed close to the part and the capacitor should be 0402 or 0603 in size. X7R capacitors are recommended for best performance across temperature and input voltage variations.

Output Capacitor Selection

The selection of C_{OUT} is determined by considering to satisfy the voltage ripple and the transient loads. The peak-to-peak output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} = \Delta I_L \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right)$$

where the ΔI_L is the peak-to-peak inductor ripple current. The highest output ripple is at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding to the transient loads, the V_{SAG} and V_{SOAR} requirement should be taken into consideration for choosing the effective output capacitance value. The amount of output sag/soar is a function of the crossover frequency factor at PWM, and can be calculated from below equation :

$$V_{SAG} = V_{SOAR} = \frac{\Delta I_{OUT}}{2 \times \pi \times C_{OUT} \times f_C}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. The X7R dielectric capacitor is recommended for the best performance across temperature and input voltage variations. The variation of the capacitance value with temperature, DC bias voltage and switching frequency needs to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias

across the capacitor increases. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated values when used near their rated voltage.

Transient performance can be improved with a higher value of output capacitor. Increasing the output capacitance will also decrease the output voltage ripple.

In some applications, for example those with large amount of output capacitance, the output voltage will probably not be regulated to its setting since C_{OUT} is not fully charged when soft-start period is end. In this case, the device detects UVP and enters into hiccup operation. Determine the output capacitance appropriately to ensure the C_{OUT} is fully charged before the soft-start period is finished.

Output Voltage Programming

The output voltage can be programmed by a resistive divider from the output to ground with the midpoint connected to the FB pin. The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 5. The output voltage is set according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where the reference voltage, V_{REF}, is 0.8V (typically).

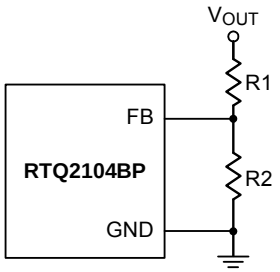


Figure 5. Output Voltage Setting

The placement of the resistive divider should be within 5mm of the FB pin. The resistance of R2 should not be larger than 170kΩ for noise immunity consideration. The resistance of R1 can then be obtained as below :

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

Feed-forward Capacitor Design

The purpose of loop compensation is to ensure stable operation while maximizing the dynamic performance. An undercompensated system may result in unstable operation. Typical symptoms of an unstable power supply include: audible noise from the magnetic components or ceramic capacitors, jittering in the switching waveforms, oscillation of output voltage, overheating of power MOSFETs and so on.

The RTQ2104BP integrates simple internal compensation and the performance of a current mode synchronous step-down DC-DC converter can be optimized by adding one feed-forward capacitor (C_{FF}) to boost the crossover frequency (f_C) and phase margin while it can improve transient response, as shown in Figure 6. The C_{FF} and resistive divider of output voltage generates one more zero, and forms one pole in the system, which can optimize either higher bandwidth or greater phase margin to meet specific performance requirements. In general, larger values of C_{FF} provide greater bandwidth improvements. However, if C_{FF} is too large, it causes the high crossover frequency (f_C) and the phase margin is insufficient, resulting in unacceptable phase margin or instability. The method presented here is easy to calculate and design. It is always necessary to make a measurement before releasing the design for final production to take full account of circuit parasitic and component nonlinearity, such as the ESR variations of output capacitors, the nonlinearity of inductors and capacitors, etc. Also, circuit PCB noise and limited measurement accuracy may also cause measurement errors. A Bode plot is ideally measured with a network analyzer while Richtek application note AN038 provides an alternative way to check the stability quickly and easily. Generally, follow the steps below to calculate the compensation components :

1. Check the crossover frequency without feed-forward capacitor (C_{FF}), $f_{C\_ORIGINAL}$. The $f_{C\_ORIGINAL}$ can be measured by using a network analyzer. For stability purposes, the target is to have a loop gain slope that is –20dB/decade from a very low frequency to beyond the crossover frequency. Do "NOT" design the crossover frequency over 80kHz with the RTQ2104BP. For dynamic purposes, the higher the bandwidth, the faster the load

transient response. The downside of the high bandwidth is that it increases the susceptibility of the regulators to board noise which ultimately leads to excessive falling edge jitter of the switch node voltage.

2. Feed-forward capacitor (C_{FF}) selection. The feed-forward capacitor (C_{FF}) can be determined by calculating the geometric mean of the zero and pole frequencies to boost the crossover frequency (f_C) and phase margin. Setting the geometric mean frequency equals to the converter crossover frequency without C_{FF} to boost the maximum phase.

$$f_{mean} = f_{C\_ORIGINAL} = \sqrt{f_Z \times f_P}$$

where

$$f_Z = \frac{1}{2\pi \times R1 \times C_{FF}}$$

$$f_P = \frac{1}{2\pi \times (\frac{R1 \times R2}{R1 + R2}) \times C_{FF}}$$

The C_{FF} can be determined by following equation :

$$C_{FF} = \frac{1}{2\pi \times f_{C\_ORIGINAL}} \times \sqrt{\frac{R1 + R2}{R1 \times (R1 \times R2)}}$$

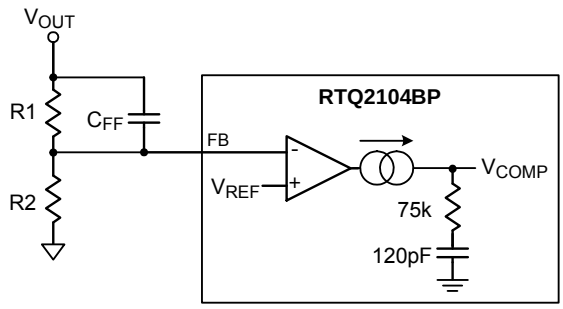


Figure 6. Compensation Network with Feed forward Capacitor

Internal Regulator

The VCC can be used as the PGOOD pull-up supply but it is "NOT" allowed to power other device or circuitry. The VCC pin must be bypassed to ground with a minimum effective capacitance 3μF capacitor. In many applications, a 10μF, X7R is recommended and it needs to be placed as close as possible to the VCC pin. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Many ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

Bootstrap Driver Supply

The bootstrap capacitor (C_{BOOT}) and bootstrap resistor (R_{BOOT}) between the BOOT pin and the SW pin is used to create a voltage rail above the applied input voltage, V_{IN}. Specifically, the bootstrap capacitor is charged through an internal diode to a voltage equal to approximately V_{VCC} each time the low-side switch is turned on. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle. For most applications, a 0.1μF, 0603 ceramic capacitor with X7R is recommended, and the capacitor should have a 6.3V or higher voltage rating. The R_{BOOT} must be 10 ohms and it could be 0402 or 0603 in size, the recommended application circuit is shown in Figure 7.

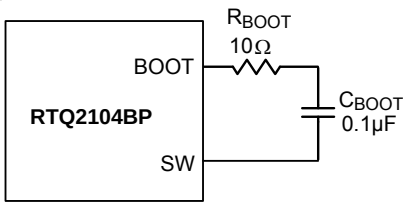


Figure 7. Bootstrap Driver Supply

External Bootstrap Diode (Option)

It is recommended to add an external bootstrap diode between an external 5V voltage supply and the BOOT pin to improve enhancement of the high-side switch and improve efficiency when the input voltage is below 5.5V. The bootstrap diode can be a low-cost one, such as 1N4148 with AEC-Q101 standard qualified. The external 5V can be a fixed 5V voltage supply from the system, or a 5V output voltage generated by the RTQ2104BP. Note that the $V_{BOOT-SW}$ must be lower than 5.5V. The recommended application circuit is shown in Figure 8, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} being placed between the BOOT pin and the capacitor/diode connection. Figure 9 shows efficiency comparison between with and without bootstrap diode.

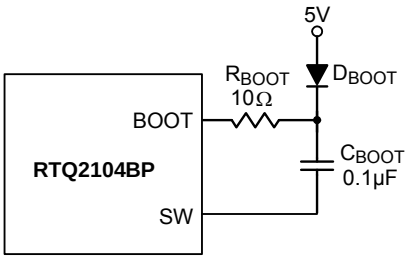


Figure 8. External Bootstrap Diode and Resistor at the BOOT Pin

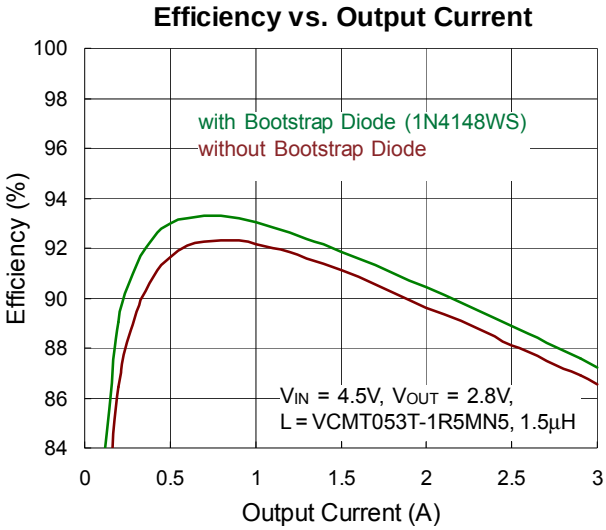


Figure 9. Efficiency Comparison between with and without Bootstrap Diode

EN Pin for Start-Up and Shutdown Operation

For automatic start-up, the EN pin, with high-voltage rating, can be connected to the input supply V_{IN} directly. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to V_{IN} by adding a resistor R_{EN} and a capacitor C_{EN} to have an additional delay as shown in Figure 11. The time delay can be calculated with the EN's internal threshold, at which switching operation begins (typically 1.25V).

An external MOSFET can be added for the EN pin to be logic-controlled as shown in Figure 12. In this case, a pull-up resistor, R_{EN}, is connected between VIN and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin. To prevent the device from being enabled when V_{IN} is smaller than the V_{OUT} target level or some other desired voltage level, a resistive divider (R_{EN1} and R_{EN2}) can be used to externally set the input under-voltage lockout threshold as shown in Figure 13.

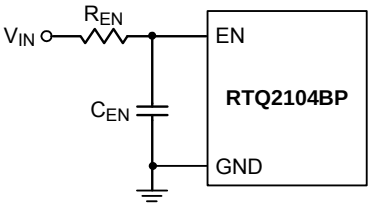


Figure 11. Enable Timing Control

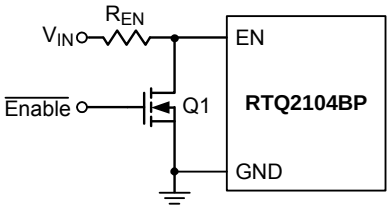


Figure 12. Logic Control for the EN Pin

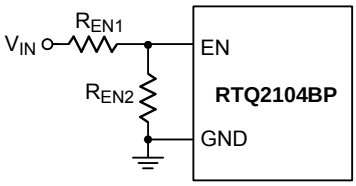


Figure 13. Resistive Divider for Under-Voltage Lockout Threshold Setting

Power-Good Output

The PGOOD pin is an open-drain power-good indication output and is to be connected to an external voltage source through a pull-up resistor.

The external voltage source can be an external voltage supply below 5.5V, VCC, or the output of the RTQ2104BP if the output voltage is regulated under 5.5V. It is recommended to connect a 100kΩ between external voltage source to PGOOD pin.

Thermal Considerations

In many applications, the RTQ2104BP does not generate much heat due to its high efficiency and low thermal resistance of its SOP-8 (Exposed Pad) package. However, in applications which the RTQ2104BP runs at a high ambient temperature and high input voltage or high switching frequency, the generated heat may exceed the maximum junction temperature of the part.

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. If the junction temperature reaches approximately 175°C, the RTQ2104BP stops switching the power MOSFETs until the temperature cools down by 15°C.

The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = \left(T_{J(MAX)} - T_A\right) / \theta_{JA(EFFECTIVE)}$$

where

$T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 150°C. T_A is the ambient operating temperature, $\theta_{JA(EFFECTIVE)}$ is the system-level junction to ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system.

The thermal resistance of the device strongly depends on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance.

Experiments in the Richtek thermal lab show that simply set $\theta_{JA(EFFECTIVE)}$ as 110% to 120% of the θ_{JA} is reasonable to obtain the allowed $P_{D(MAX)}$.

As an example, considering the RTQ2104BP is used in applications where V_{IN} = 12V, I_{OUT} = 3A, V_{OUT} = 5V. The efficiency at 5V, 3A is 90% by using Cyntec-VCMT063T-2R2MN5 (2.2µH, 15mΩ DCR) as the inductor and measured at room temperature. The core loss, 37.1mW, can be obtained from its website. In this case, the power dissipation of the RTQ2104BP is

$$P_{D,\,RT} = \frac{1-\eta}{\eta} \times P_{OUT} - \left(I_O^2 \times DCR + P_{CORE}\right) = 1.495W$$

Considering the $\theta_{JA(EFFECTIVE)}$ is 32.64°C/W by using the RTQ2104BP evaluation board with 4 layers and 2 OZ. copper thickness on the outer layers and 1 OZ. copper thickness on the inner layers copper thickness. The junction temperature of the regulator operating in a 25°C ambient temperature is approximately :

$$T_J = 1.495W \times 32.64°C/W + 25°C = 73.7°C$$

Figure 15 shows the RTQ2104BP $R_{DS(ON)}$ versus different junction temperatures. If the application requires a higher ambient temperature, the power dissipation and the junction temperature of the device need to be recalculated based on a higher $R_{DS(ON)}$ since it increases with temperature.

Using 65°C ambient temperature as an example, the change of the equivalent $R_{DS(ON)}$ can be obtained from Figure 14 and yields a new power dissipation of 1.7W. Therefore, the estimated new junction temperature is

$$T_J' = 1.7W \times 32.64°C/W + 65°C = 120.5°C$$

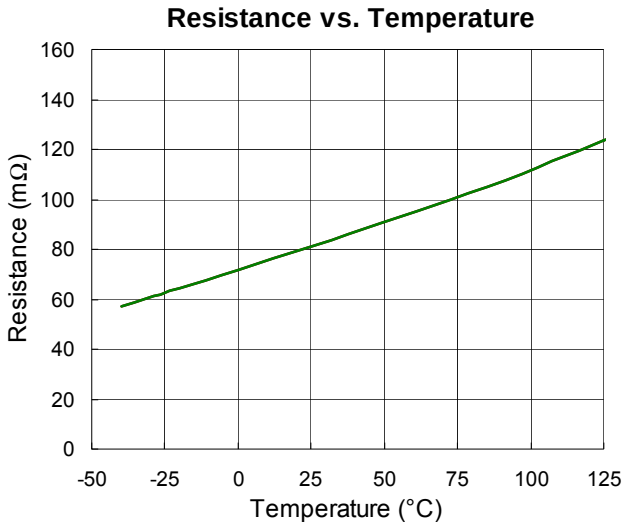


Figure 14. RTQ2104BP $R_{DS(ON)}$ vs. Temperature

If the application requires a higher ambient temperature and may exceed the recommended maximum junction temperature of 150°C, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow. Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary failsafe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Layout Guidelines

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RTQ2104BP :

- Four-layer or six-layer PCB with maximum ground plane is strongly recommended for good thermal performance.
- Keep the traces of the main current paths wide and short.
- Place high frequency decoupling capacitor C_{IN2} as close as possible to the IC to reduce the loop impedance and minimize switch node ringing.
- Place the VCC decoupling capacitor, C_{VCC}, as close to the VCC pin as possible.
- Place bootstrap capacitor, C_{BST}, as close to the IC as possible. Routing the trace with width of 20mil or wider.
- Place multiple vias under the device near VIN and GND, and close to input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible. And add thermal vias under and near the RTQ2104BP to additional ground planes within the circuit board and on the bottom side.
- The high frequency switching nodes, SW and BOOT, should be as small as possible. Keep analog components away from the SW and BOOT nodes.
- Reducing the area size of the SW exposed copper to reduce the electrically coupling from this voltage.
- Connect the feedback sense network behind via of output capacitor.
- Place the feedback components R_{FB1} / R_{FB2} / C_{FF} near the IC.

Figure 15 is the layout example which uses 70mm x 100mm, four-layer PCB with 2 OZ. Cu on the outer layers and 1 OZ. Cu on the inner layers.

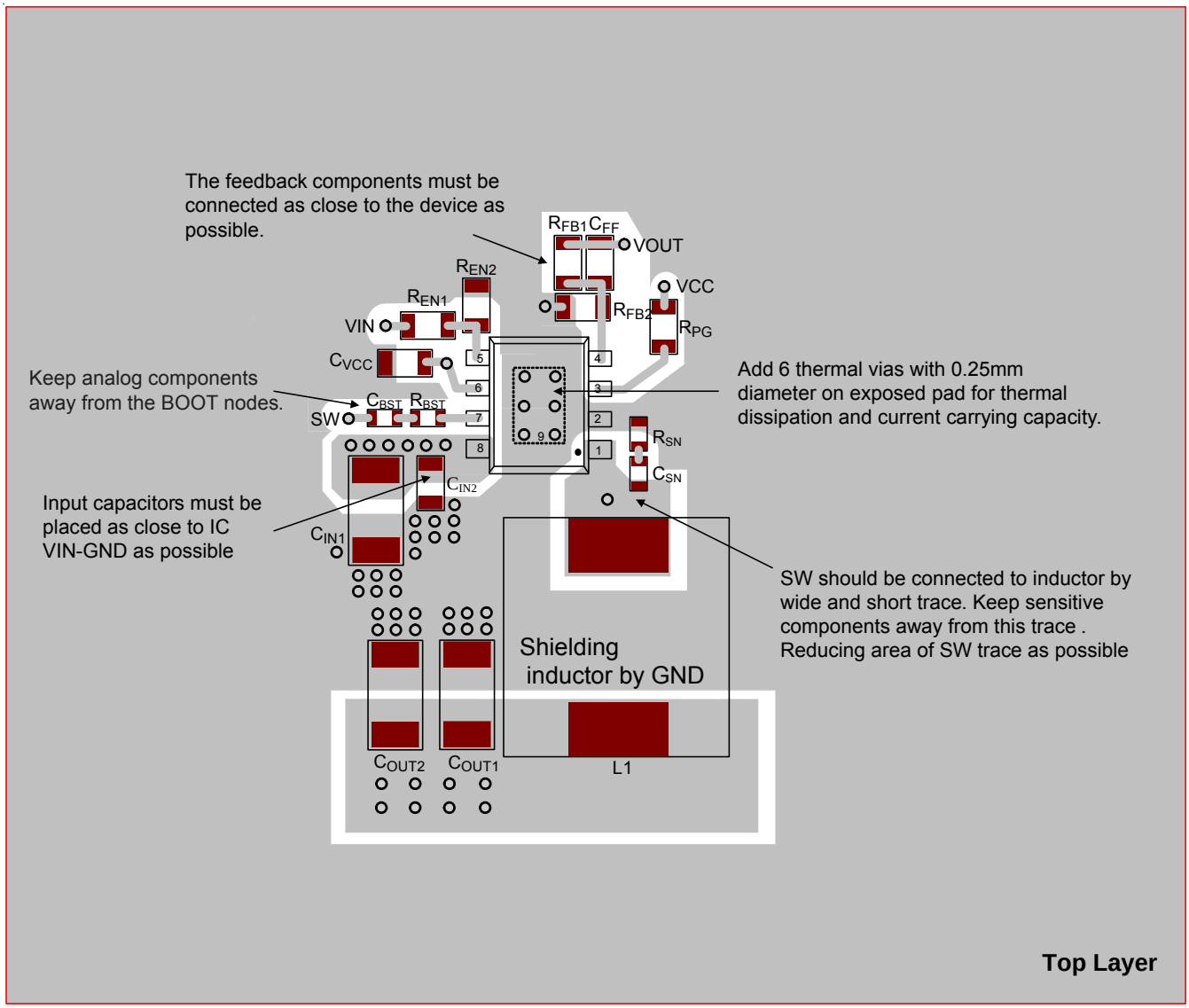
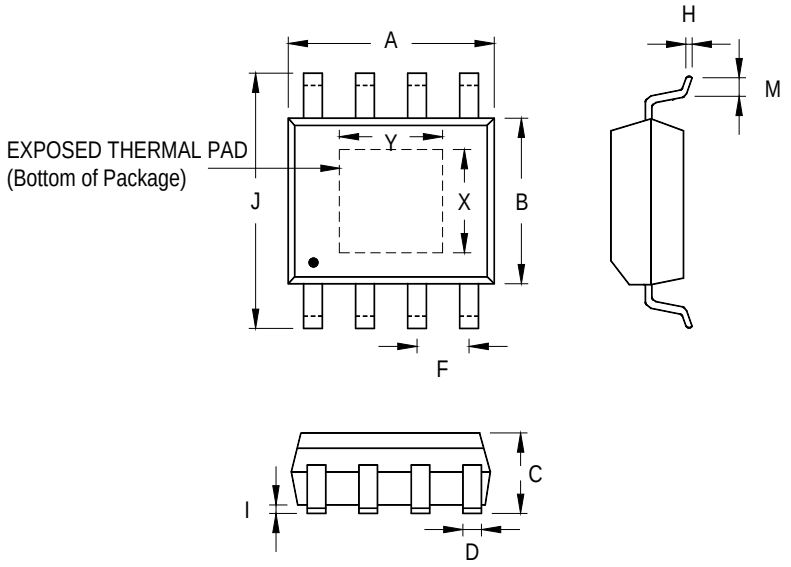


Figure 15. Layout Guide (Top Layer)

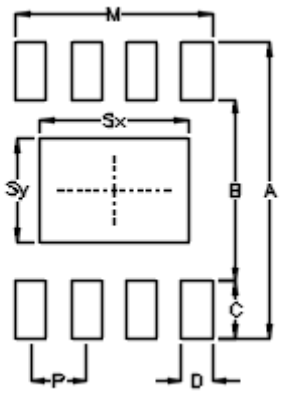
Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

Footprint Information



Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
PSOP-8	Option1	8	1.27	6.80	4.20	1.30	0.70	2.30	2.30	4.51	±0.10
	Option2							3.40	2.40		

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