RICHTEK®

RTQ2106-QA

36V_{IN}, 3A, High Efficiency, 2.1MHz, Synchronous Buck Converter with Low Quiescent Current

1 General Description

The RTQ2106-QA is a 3A, high-efficiency, current mode synchronous buck converter optimized for automotive applications. The device operates with input voltages from 4V to 36V and is protected from load dump transients up to 42V, eases input surge protection design. The device can program the output voltage between 0.8V to V_{IN}. The low quiescent current design with the integrated low $R_{DS(ON)}$ power MOSFETs achieves high efficiency over the wide load range. The peak current mode control with simple external compensation allows the use of small inductors and results in fast transient response and good loop stability.

The ultra-low minimum on-time enable constant-frequency operation even at very high step-down ratios. For switching noise sensitive applications, it can be externally synchronized from 300kHz to 2200kHz. The built-in spread spectrum frequency modulation further helping systems designers with better EMC management.

The RTQ2106-QA provides complete protection functions such as input undervoltage-lockout, output undervoltage protection, overcurrent protection, and over-temperature protection. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. The RTQ2106-QA is available in TSSOP-14 (Exposed Pad) package. The recommended junction temperature range is –40°C to 150°C, and the ambient temperature range is –40°C to 125°C.

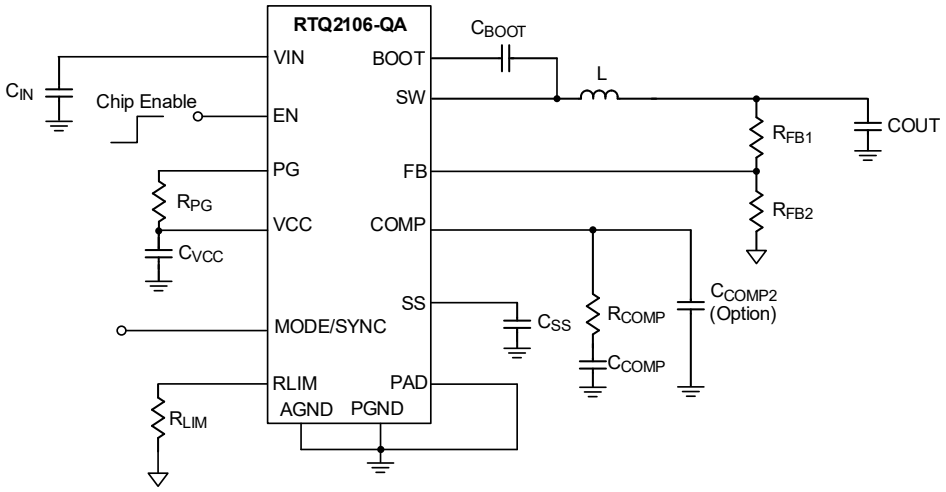
2 Features

- **AEC-Q100 Grade 1 Qualified**
- **Wide Input Voltage Range: 4V to 36V**
- **Wide Output Voltage Range: 0.8V to V_{IN}**
- **Maximum Output Current: 3A**
- **Peak Current Mode Control**
- **Integrated 90mΩ Switch and 90mΩ Synchronous Rectifier**
- **Low Quiescent Current: 40μA**
- **Fast 60ns Minimum Switch On-Time**
- **Ultra-Short 65ns Minimum Switch Off-Time**
- **Synchronizable Switching Frequency: 300kHz to 2.2MHz**
- **Selectable PSM/FPWM at Light Load**
- **Built-In Spread Spectrum Frequency Modulation for Low EMI**
- **Externally Adjustable Soft-Start**
- **Power-Good Indication**
- **Enable Control**
- **0.8V ±1.5% Reference Accuracy**
- **Adjustable Current Limit**
- **Adjacent Pin-Short Protection**
- **Built-In UVLO, UVP, OTP**

3 Applications

- Automotive Systems
- Car Camera Modules and Car Cockpit Systems
- Connected Car Systems
- Point of Load Regulator in Distributed Power Systems
- Digital Set-Top Boxes
- Broadband Communications

4 Simplified Application Circuit



5 Ordering Information

RTQ2106 □□-QA

Grade
QA: AEC-Q100 Qualified and Screened by High Temperature

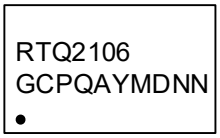
Package Type(1)
CP: TSSOP-14 (Exposed Pad)
(Exposed Pad-Option 2)

Lead Plating System
G: Richtek Green Policy Compliant(2)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

6 Marking Information



RTQ2106GCPQA: Product Code
YMDNN: Date Code

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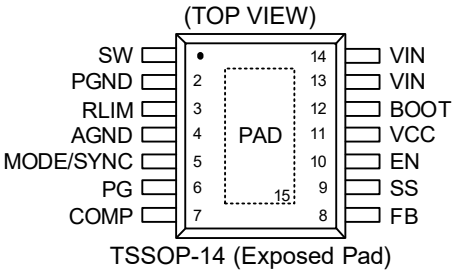
7 Pin Configuration

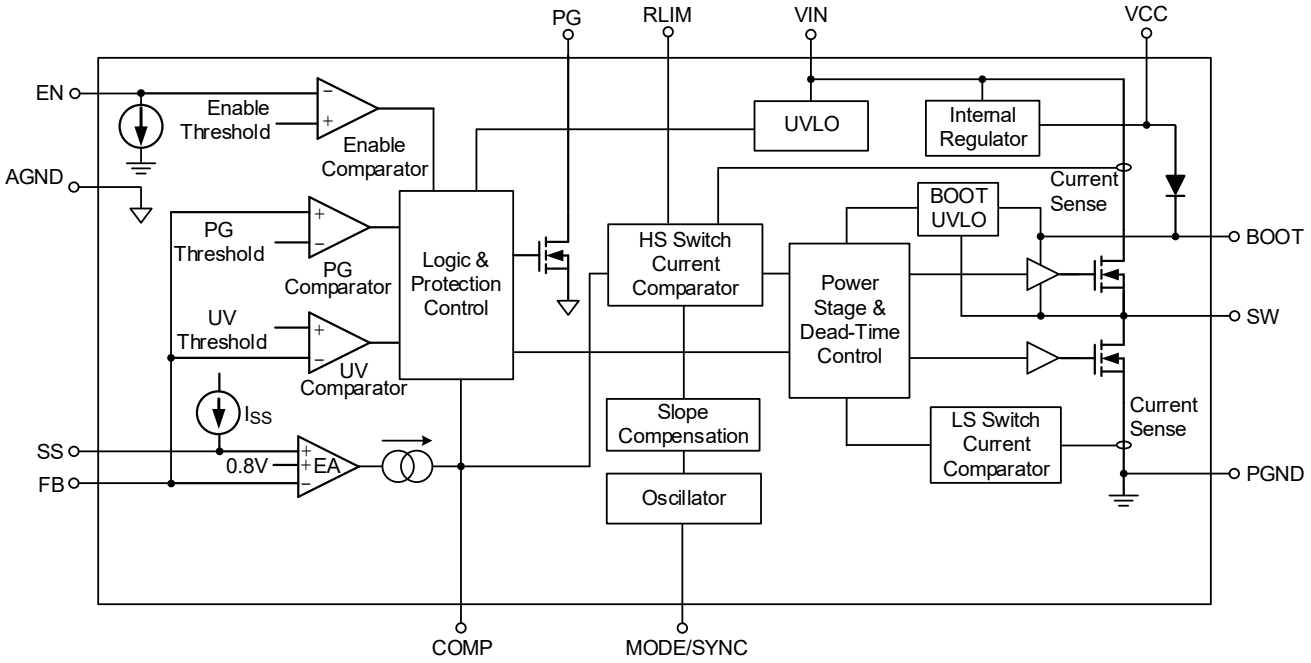


TSSOP-14 (Exposed Pad)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	SW	Switch node. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
2	PGND	Power ground. Connect this pin to the negative terminals of the input capacitor and output capacitor.
3	RLIM	Current limit setup pin. Connect a resistor from this pin to ground to set the current limit value. The recommended resistor value ranges from 33kΩ (for typically 5.5A) to 91kΩ (for typically 2.2A).
4	AGND	Analog ground.
5	MODE/SYNC	Mode selection and external synchronous signal input. Ground this pin or leave this pin floating enables the power saving mode operation at light load. Apply a DC voltage of 2V or higher or tie to VCC for FPWM mode operation. Tie to a clock source for synchronization to an external frequency.
6	PG	Open-drain power-good indication output. Once soft-start is finished, PG will be pulled low to ground if any internal protection is triggered.
7	COMP	Compensation node. Connect external compensation elements to this pin to stabilize the control loop.
8	FB	Feedback voltage input. Connect this pin to the midpoint of the external feedback resistive divider to set the output voltage of the converter to the desired regulation level. The device regulates the FB voltage at a feedback reference voltage, typically 0.8V.
9	SS	Soft-start capacitor connection node. Connect an external capacitor between this pin and ground to set the soft-start time. Note that, for proper device operation, it is essential that the minimum soft-start time (t_{SS_min}) exceeds 500μs.
10	EN	Enable control input. A logic-high enables the converter; a logic-low forces the device into shutdown mode.
11	VCC	Linear regulator output. VCC is the output of the internal 5V linear regulator powered by VIN. Decouple with a 1μF, X7R ceramic capacitor from VCC to ground for normal operation.
12	BOOT	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.1μF, X7R ceramic capacitor between this pin and SW pin.
13, 14	VIN	Power input. The input voltage range is from 4V to 36V after soft-start is finished. Connect input capacitors between this pin and PGND. It is recommended to use a 4.7μF, X7R and a 0.1μF, X7R capacitors.
15 (Exposed pad)	PAD	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large PGND plane. Connect this PGND plane to other layers with thermal vias to help dissipate heat from the device.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VIN Voltage, VIN ---------- –0.3V to 42V
- SW Voltage, V_{SW} ---------- –0.3V to 42V

  < 50ns ---------- –5V to 46.3V
- BOOT Voltage, V_{BOOT} ---------- –0.3V to 48V
- BOOT to SW Voltage, $V_{BOOT-SW}$ ---------- –0.3V to 6V
- EN and SS Voltage, V_{EN} and V_{SS} ---------- –0.3V to 42V
- Other Pins ---------- –0.3V to 6V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –40°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Susceptibility

(Note 3)

- HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage ---------- 4V to 36V
- Output Voltage ---------- 0.8V to VIN*

VIN*: $0.99 \times (V_{IN} - I_{OUT}(max) \times R_{DSON(max)})$

- Junction Temperature Range ---------- –40°C to 150°C
- Ambient Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		TSSOP-14	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	39.74	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	40.23	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	3.31	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	37.27	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	2.48	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	21.12	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(Top)}$, and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board, which is in size of 70mm x 100mm, four-layer PCB with 2 oz. Cu on the outer layers and 1 oz. Cu on the inner layers. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

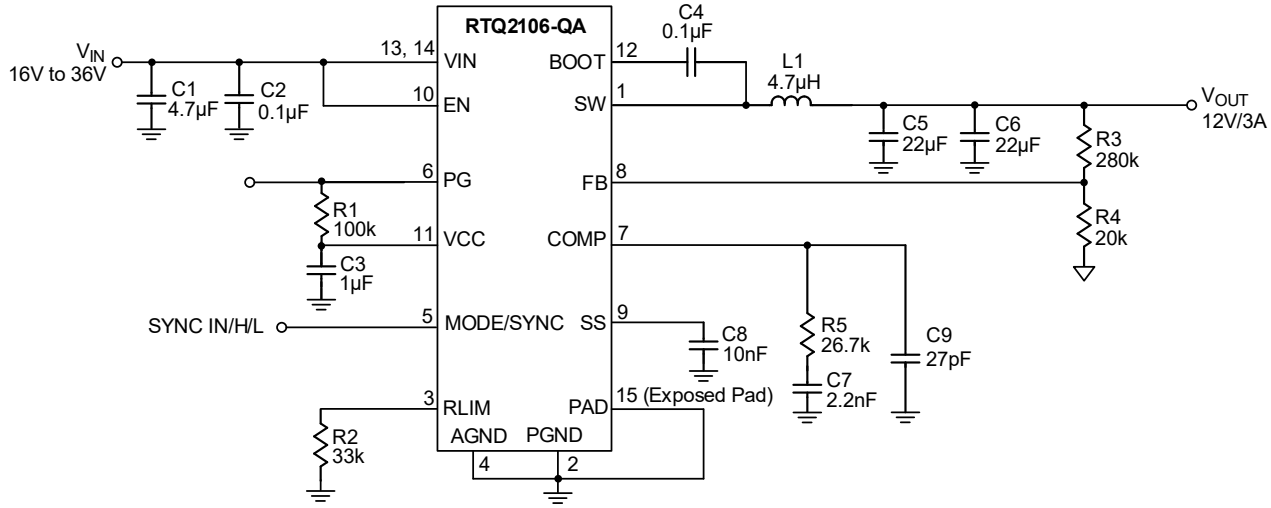
(V_{IN} = 12V, T_A = T_J = –40°C to 125°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VIN Supply Input Voltage	V_{IN}		4	--	36	V
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}	V_{IN} rising	3.6	3.8	4	V
Undervoltage-Lockout Falling Threshold	V_{UVLO_F}	V_{IN} falling	2.7	2.85	3	
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	5	μA
Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = 0.82V, not switching	--	40	50	μA
Constant Voltage Regulation						
Reference Voltage	V_{REF}	4V < V_{IN} < 36V, PWM, T_A = T_J = 25°C	0.792	0.8	0.808	V
		4V < V_{IN} < 36V, PWM, T_A = T_J = –40°C to 125°C	0.788	0.8	0.812	
Enable Voltage						
EN Input Voltage Rising Threshold	V_{EN_R}	VEN rising	1.15	1.25	1.35	V
EN Input Voltage Falling Threshold	V_{EN_F}	VEN falling	0.9	1.05	1.15	
Current Limit						
High-Side Switch Current Limit 1	I_{LIM_H1}	R_{LIM} = 91kΩ	1.87	2.2	2.53	A
High-Side Switch Current Limit 2	I_{LIM_H2}	R_{LIM} = 47kΩ	3.52	4	4.48	A
High-Side Switch Current Limit 3	I_{LIM_H3}	R_{LIM} = 33kΩ	4.84	5.5	6.16	A
Negative Inductor Peak Current Limit	$I_{LIM\_PEAK\_NEG}$	From drain to source	--	2	--	A
Switching						
Switching Frequency	f_{SW}		1.89	2.1	2.31	MHz
SYNC Frequency Range		MODE/SYNC Pin = External Clock	0.3	--	2.2	MHz
SYNC Switching High Threshold	V_{IH_SYNC}	MODE/SYNC Pin = External Clock	--	--	2	V
SYNC Switching Low Threshold	V_{IL_SYNC}	MODE/SYNC Pin = External Clock	0.4	--	--	V
SYNC Switching Clock Duty Cycle	D_{SYNC}	MODE/SYNC Pin = External Clock	20	--	80	%
Minimum On-Time	t_{ON_MIN}		--	60	80	ns
Minimum Off-Time	t_{OFF_MIN}		--	65	80	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Internal MOSFET						
On-Resistance of High-Side MOSFET	R_{DSON_H}		--	90	170	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}		--	90	170	mΩ
High-Side Switch Leakage Current	I_{LK_H}	V_{EN} = 0V, V_{SW} = 0V	--	--	1	μA
Soft-Start						
Soft-Start Current	I_{SS}		4.8	6	7.2	μA
Power-Good						
Power-Good Voltage Threshold	V_{TH_PGLH1}	V_{FB} rising, % of V_{REF}, PG from low to high	85	90	95	%
	V_{TH_PGHL1}	V_{FB} rising, % of V_{REF}, PG from high to low	--	120	--	
	V_{TH_PGHL2}	V_{FB} falling, % of V_{REF}, PG from high to low	80	85	90	%
	V_{TH_PGLH2}	V_{FB} falling, % of V_{REF}, PG from low to high	--	117	--	
Power-Good Leakage Current	I_{LK_PG}	PG signal good, V_{FB} = V_{REF}, V_{PG} = 5.5V	--	--	0.5	μA
Power-Good Sink Current Capability	I_{SK_PG}	PG signal fault, I_{PG} sinks 2mA	--	--	0.3	V
Error Amplifier						
Error Amplifier Transconductance	gm	$-10\mu A < I_{COMP} < 10\mu A$	665	950	1280	μA/V
COMP to Current Sense Transconductance	gm_{CS}		4.5	5.6	6.7	A/V
Spread Spectrum						
Spread Spectrum Range	f_{SS}		--	+6	--	%
Over-Temperature Protection						
Over-Temperature Protection Threshold	T_{OTP}		--	175	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	15	--	°C
Output Undervoltage Protection						
Output Undervoltage Protection Threshold	V_{UVP}	UVP detect	0.35	0.4	0.45	V

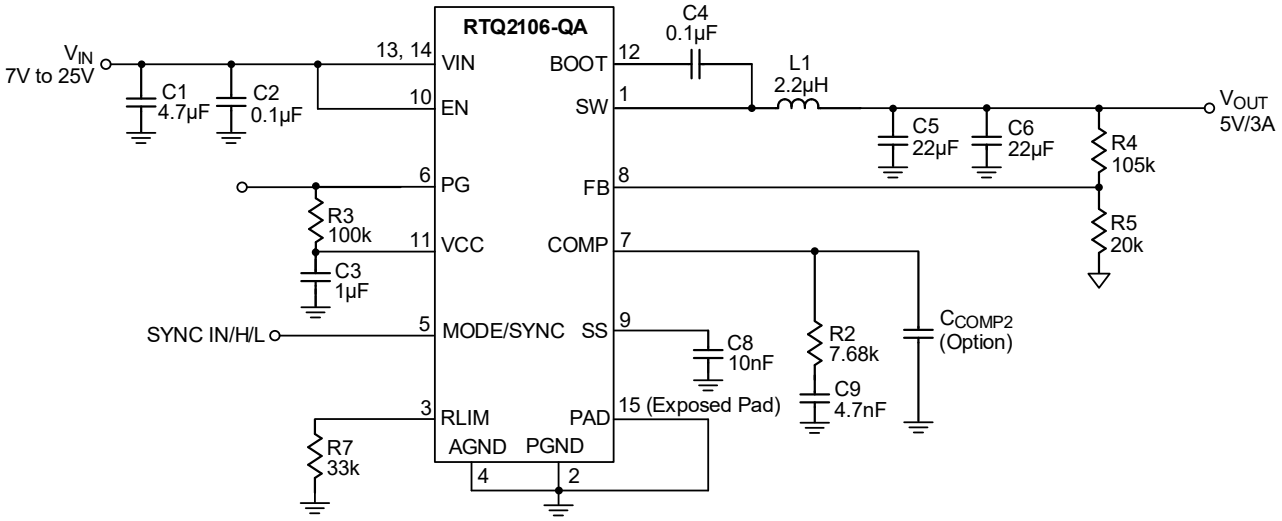
15 Typical Application Circuit

15.1 12V, 3A Buck Converter



L1 = WE-78439346047 / Cyntec-VCHA075D-4R7MS6
C5/C6 = GCM32EC71E226KE36L
C1 = GRM31CR71H475KA12L

15.2 5V, 3A Buck Converter

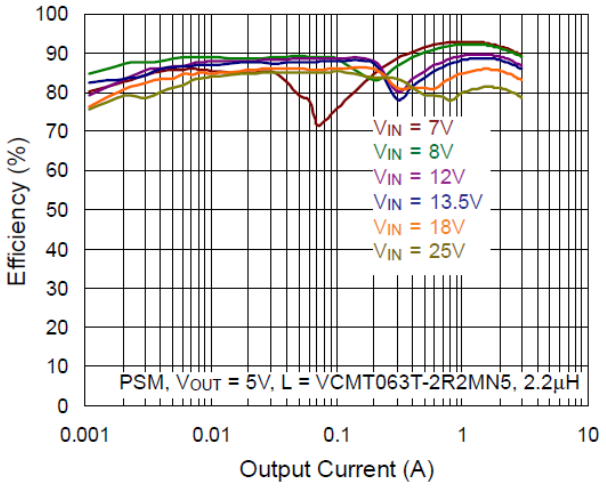


L1 = WE-78439344022 / Cyntec-VCMT063T-2R2MN5
C5/C6 = GRM31CR71A226KE15L
C1 = GRM31CR71H475KA12L

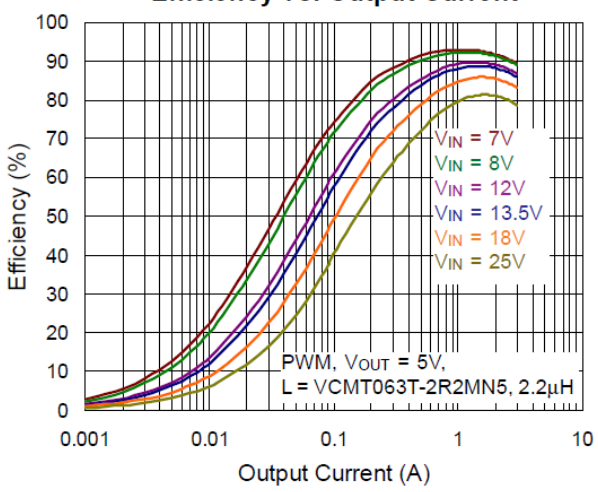
16 Typical Operating Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 12V, T_A = 25°C. Specified temperatures are ambient.

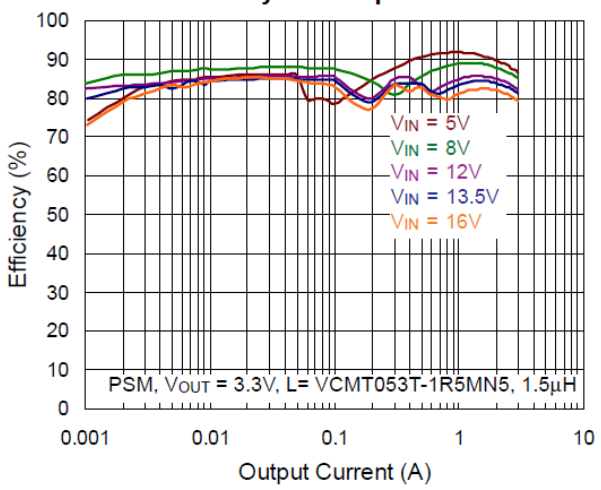
Efficiency vs. Output Current



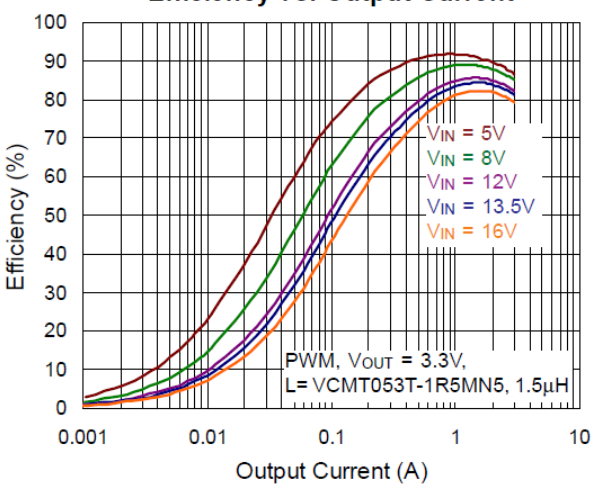
Efficiency vs. Output Current



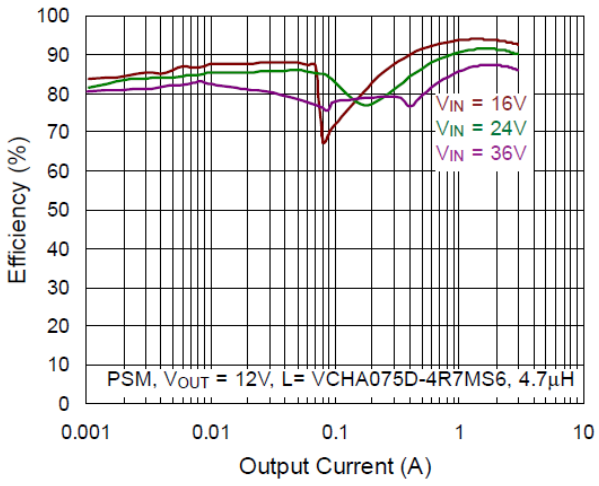
Efficiency vs. Output Current



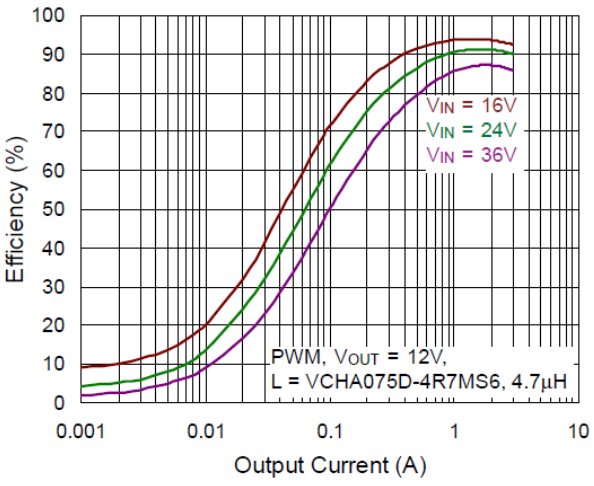
Efficiency vs. Output Current



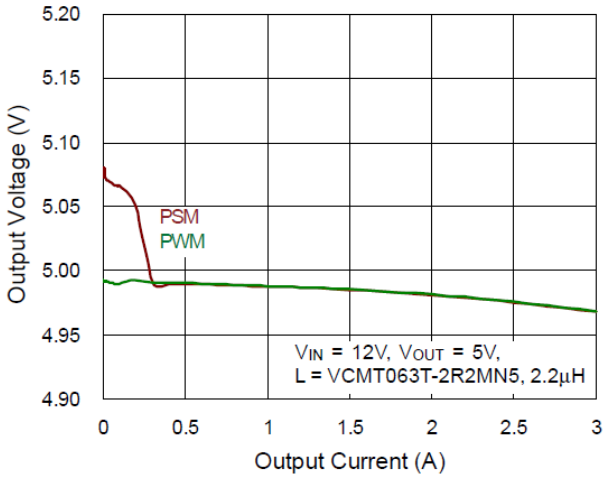
Efficiency vs. Output Current



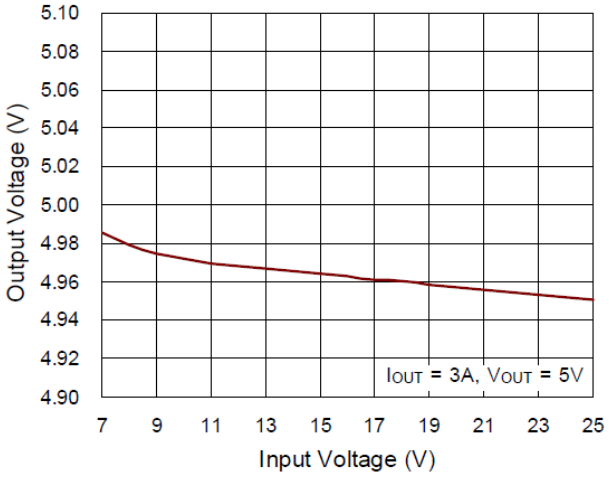
Efficiency vs. Output Current



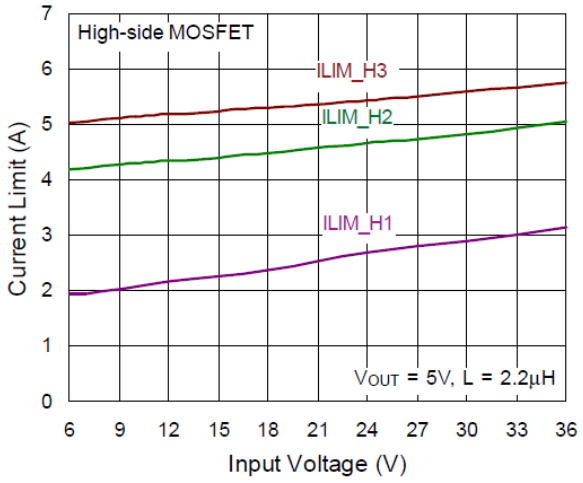
Output Voltage vs. Output Current



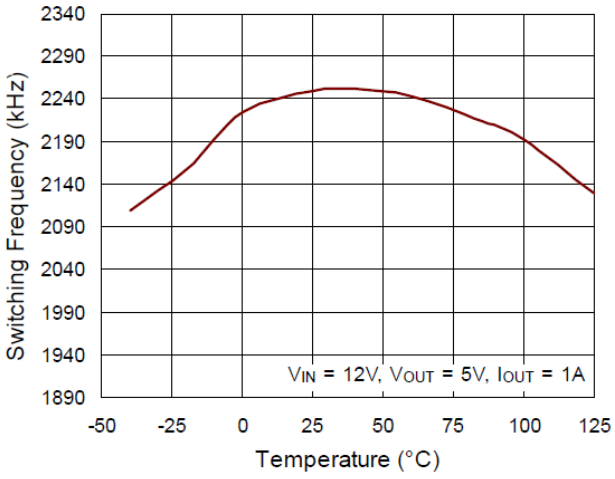
Output Voltage vs. Input Voltage



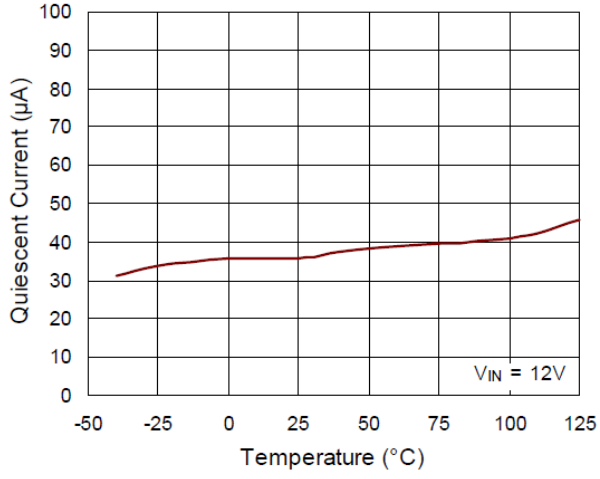
Current Limit vs. Input Voltage



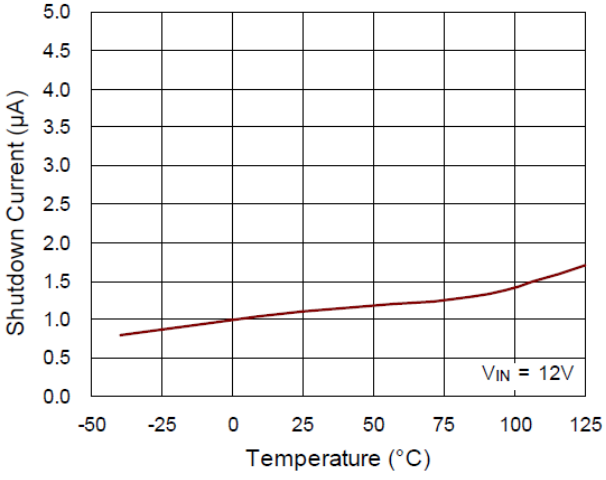
Switching Frequency vs. Temperature



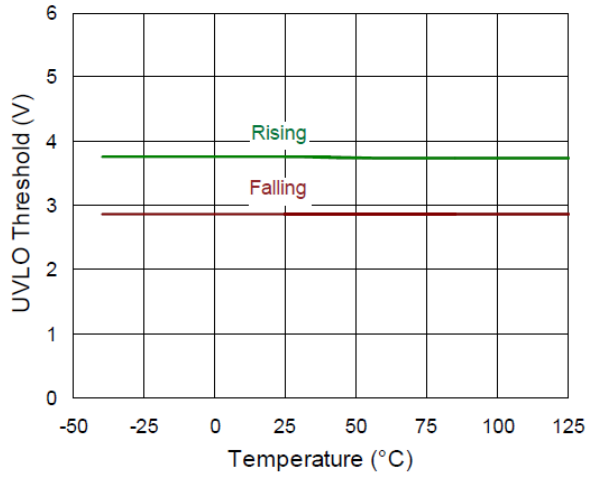
Quiescent Current vs. Temperature



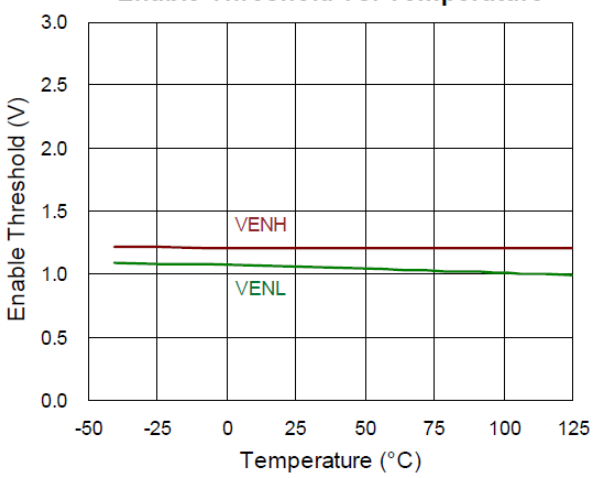
Shutdown Current vs. Temperature



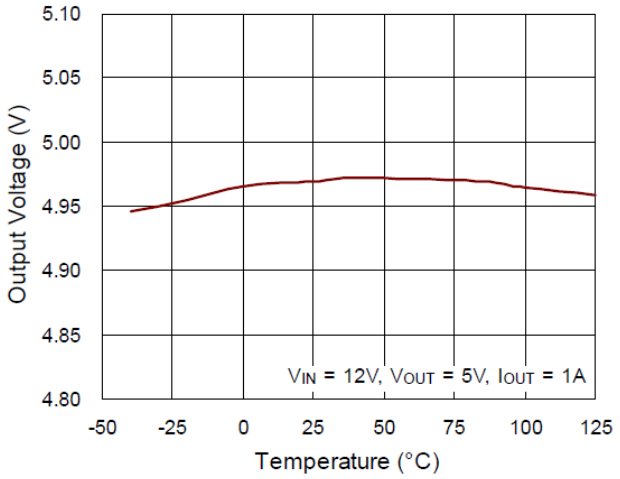
UVLO Threshold vs. Temperature



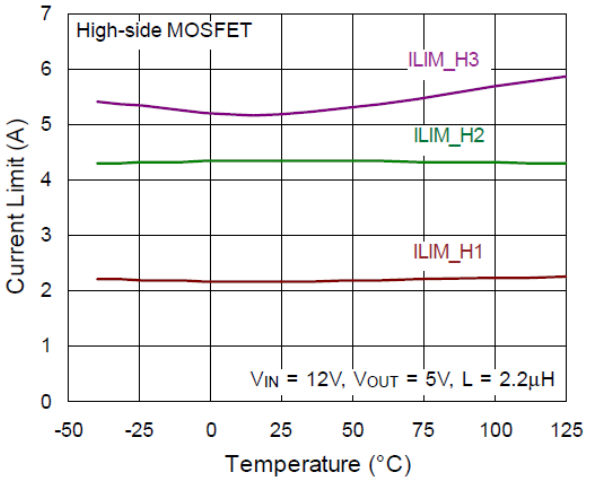
Enable Threshold vs. Temperature



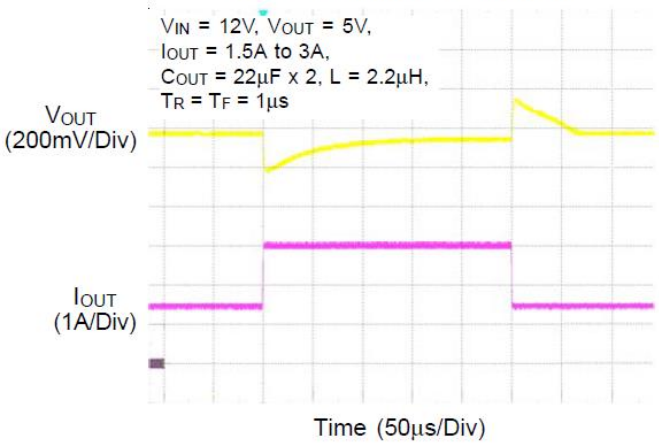
Output Voltage vs. Temperature



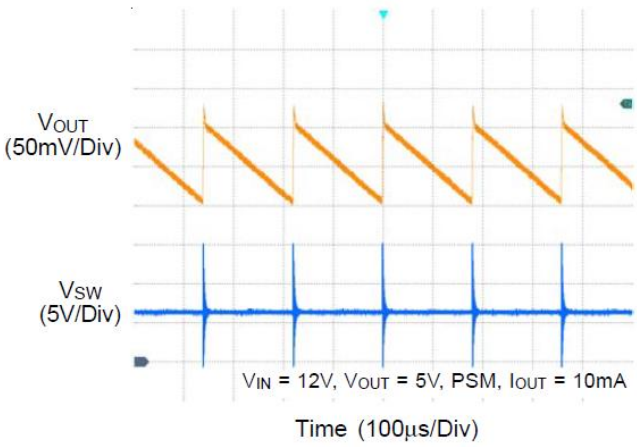
Current Limit vs. Temperature



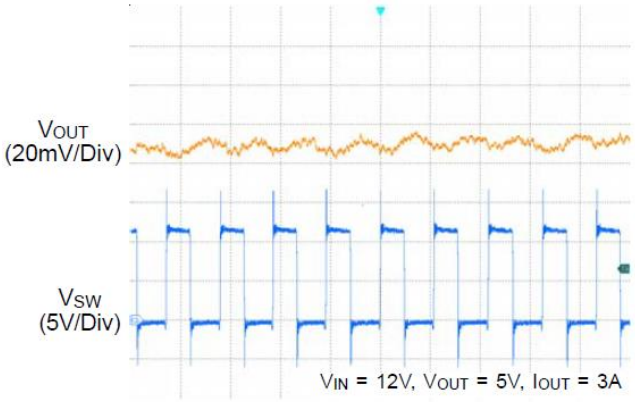
Load Transient Response



Output Ripple Voltage

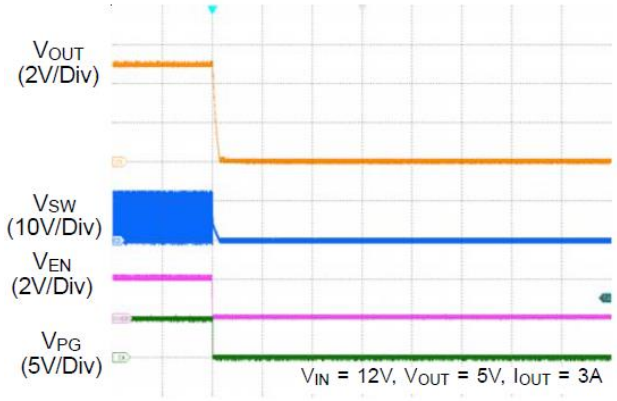


Output Ripple Voltage

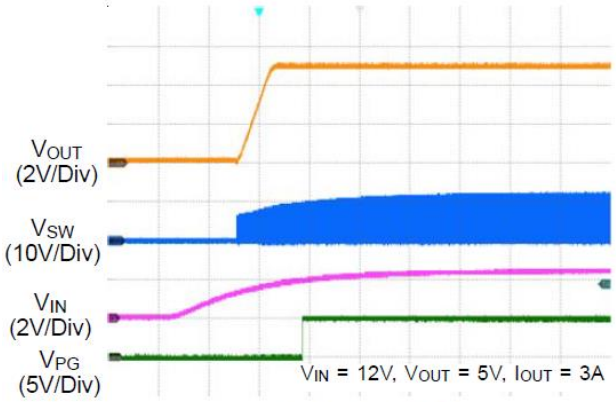


Power On from EN

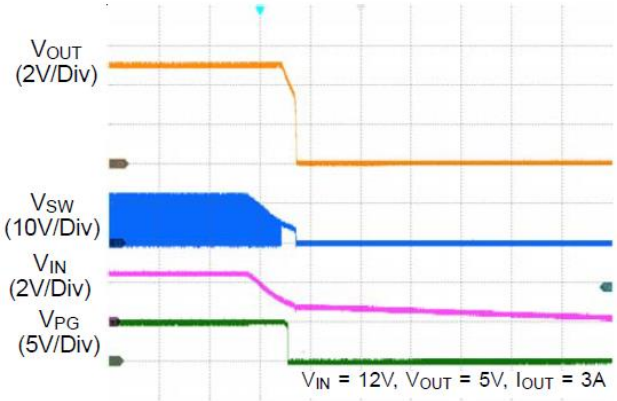
Power Off from EN



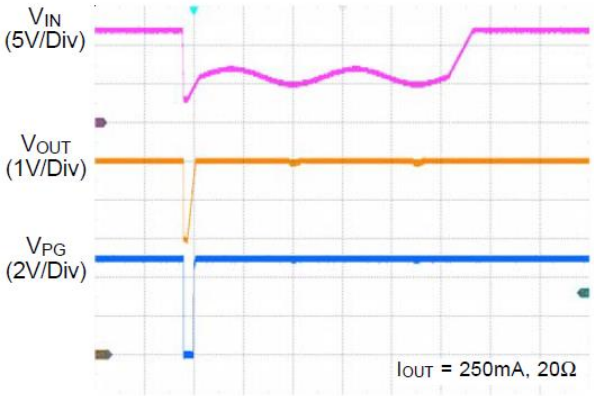
Power On from VIN



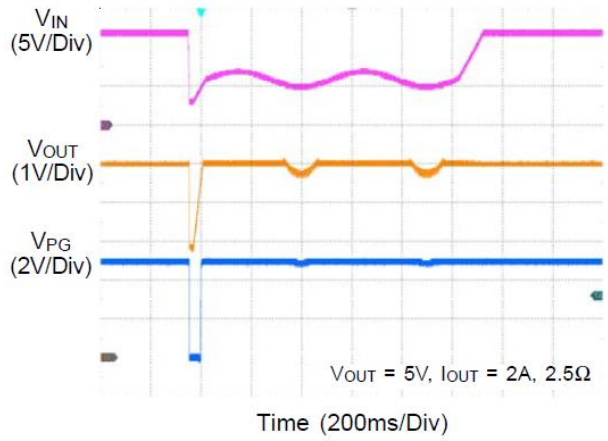
Power Off from VIN



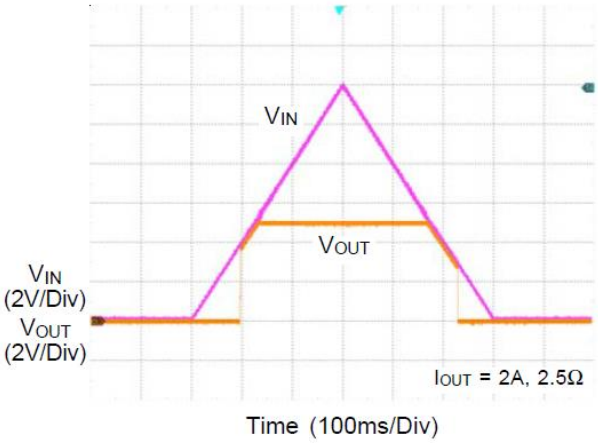
Level III of Starting Profile (ISO16750-2)



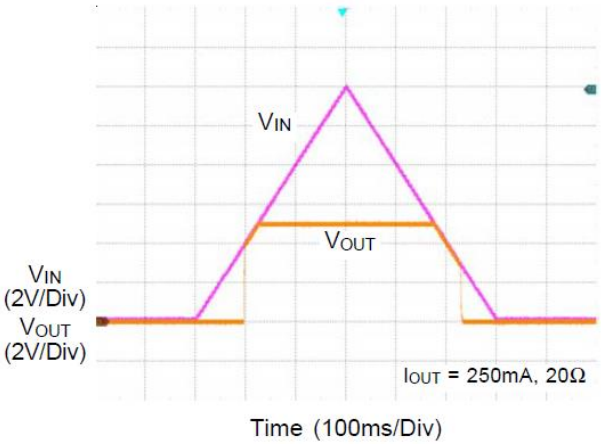
Level III of Starting Profile (ISO16750-2)



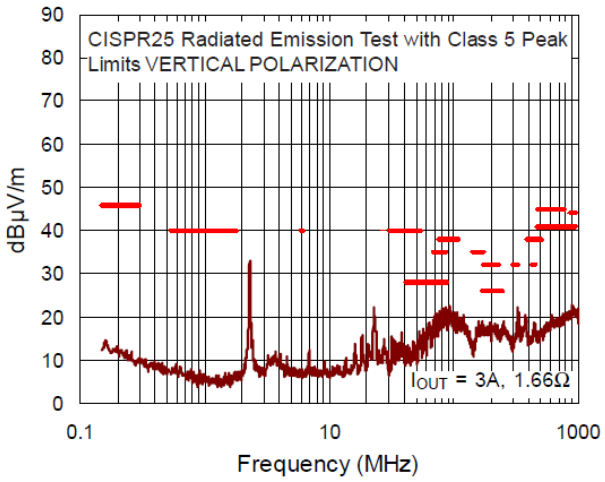
Start-Up Dropout Performance



Start-Up Dropout Performance



Radiated EMI Performance



17 Operation

17.1 Control Loop

The RTQ2106-QA is a high-efficiency buck converter utilizes the peak current mode control. An internal oscillator initiates turn-on of the high-side MOSFET switch. At the beginning of each clock cycle, the internal high-side MOSFET switch turns on, allowing current to ramp-up in the inductor. The inductor current is internally monitored during each switching cycle. The output voltage is sensed on the FB pin via the resistor divider, R1 and R2, and compared with the internal reference voltage (V_{REF}) to generate a compensation signal (V_{COMP}) on the COMP pin. A control signal derived from the inductor current is compared to the voltage at the COMP pin, derived from the feedback voltage. When the inductor current reaches its threshold, the high-side MOSFET switch is turned off and inductor current ramps-down. While the high-side MOSFET switch is off, inductor current is supplied through the low-side MOSFET switch. This cycle repeats at the next clock cycle. In this way, duty-cycle and output voltage are controlled by regulating inductor current.

17.2 MODE Selection and Synchronization

The RTQ2106-QA provides a MODE/SYNC pin for Forced-PWM Mode (FPWM) and Power Saving Mode (PSM) operation selection at light load. If $V_{MODE/SYNC}$ rises above a logic-high threshold voltage (V_{IH_SYNC}) of the MODE/SYNC input, the device is locked in FPWM. If $V_{MODE/SYNC}$ is held below a logic-low threshold voltage (V_{IL_SYNC}) of the MODE/SYNC input, the device operates in PSM at light load to improve efficiency. The RTQ2106-QA can also be synchronized with an external clock ranging from 300kHz to 2.2MHz by the MODE/SYNC pin.

17.3 Forced-PWM Mode

Forced-PWM operation provides constant frequency operation at all loads and is useful in applications sensitive to switching frequency. This mode trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, and constant switching frequency. In this mode, a negative current limit of I_{SK_L} is imposed to prevent damage to the low-side MOSFET switch of the regulator. The converter synchronizes to any valid clock signal on the SYNC input when in FPWM. When constant frequency operation is more important than light load efficiency, pull the MODE/SYNC input high or provide a valid synchronization input. Once activated, this feature ensures that the switching frequency stays away from the AM frequency band, while operating between the minimum and maximum duty cycle limits.

17.4 Power Saving Mode

With the MODE/SYNC pin floating or pulling low, that is, with a logic low on the MODE/SYNC input, the RTQ2106-QA operates in power saving mode (PSM) at light load to improve light load efficiency. In PSM, IC starts to switch when VFB is lower than the PSM threshold (V_{REF} x 1.005, typically) and stops switching when VFB is high enough. IC detects the peak inductor current (I_{L_PEAK}) and keeps high-side MOSFET switch on until the IL reaches its minimum peak current level (1A at V_{IN} = 12V, typically) to ensure that IC can provide sufficiency output current with each switching pulse. Zero-current detection is also activated to prevent IL from becoming negative and to ensure that no external discharging current from the output capacitor. During non-switching period, most of the internal circuit is shut down, and the supply current drops to quiescent current (typically, 40μA) to reduce the quiescent power consumption. With lower output loading, the non-switching period is longer, so the effective switching frequency becomes lower to reduce the switching loss and switch driving loss.

17.5 Minimum On-Time and Minimum Off-Time

The minimum on-time, t_{ON_MIN}, is the smallest duration of time in which the high-side MOSFET switch can be in its “on” state. The minimum on-time is 60ns (typically). In continuous mode operation, the minimum on-time limit imposes a maximum operating input voltage, V_{IN_MAX}, of:

$$V_{IN\_MAX} = \frac{V_{OUT}}{t_{ON\_MIN} \times f_{SW\_MAX}}$$

where f_{SW_MAX} is the maximum operating frequency. The minimum off-time, t_{OFF_MIN}, is the smallest amount of time that the RTQ2106-QA is capable of turning on the low-side MOSFET switch, tripping the current comparator and turning the MOSFET switch back off. The minimum off time is 65ns (typically). If the switching frequency should be constant, the required off time needs to be larger than the minimum off time. Below shows minimum off time calculation with loss terms consideration,

$$t_{OFF\_MIN} \leq \frac{1 - \left[\frac{V_{OUT} + I_{OUT\_MAX} \times \left(R_{DS(ON)\_L} + DCR \right)}{V_{IN\_MIN} - I_{OUT\_MAX} \times \left(R_{DS(ON)\_H} - R_{DS(ON)\_L} \right)} \right]}{f_{SW}}$$

where RDS(ON)_H is the on-resistance of the high-side MOSFET switch; RDS(ON)_L is the on-resistance of the low-side MOSFET switch; DCR is the DC resistance of the inductor.

17.6 Maximum Duty Cycle Operation

The RTQ2106-QA is designed to operate in dropout at the high duty cycle approaching 100%. If the operational duty cycle is large and the required off time becomes smaller than the minimum off time, the RTQ2106-QA starts to enable skip off time function and keeps high-side MOSFET switch on continuously. The RTQ2106-QA implements the skip off time function to achieve high duty approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application. The input voltage at which the devices enter dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

Note that achieving an actual 100% output will only be possible under no-load conditions. In practical scenarios, the ideal maximum output voltage will be equal to the input voltage minus the product of the output current and the maximum high-side MOSFET turn-on resistance. Additionally, when considering low boot voltage conditions, the low-side MOSFET may be turned on for a certain duration. In this case, the actual VOUT can be expressed as V_{OUT} = 0.99 x (V_{IN} – $I_{OUT(max)}$ x $R_{DSON(max)}$). Therefore, it is advisable to allocate a sufficient design margin to ensure that the target output is maintained under all possible loading current scenarios during the system's operation.

17.7 BOOT UVLO

The BOOT UVLO circuit is implemented to ensure sufficient voltage of the bootstrap capacitor for turning on the high-side MOSFET switch at any condition. The BOOT UVLO usually actives at extremely high conversion ratio or the higher VOUT application operates at very light load. For extremely high conversion ratio condition after softstart is finished or higher VOUT application operates at very light load and PSM, the low-side MOSFET switch may not have sufficient turn-on time to charge the bootstrap capacitor. The device monitors the voltage of the bootstrap capacitor and forces the low-side MOSFET switch to turn on when the voltage of the bootstrap capacitor falls below VBOOT_UVLO_L (typically, 2.3V). Meanwhile, the minimum off-time is extended to 150ns (typically) hence prolong the bootstrap capacitor charging time. The BOOT UVLO is sustained until the VBOOT−SW is higher than VBOOT_UVLO_H (typically, 2.4V).

17.8 Internal Regulator

The device integrates a 5V linear regulator (V_{CC}) that is supplied by VIN and provides power to the internal circuitry. The internal regulator operates in low dropout mode when V_{IN} is below 5V. The V_{CC} can be used as the PG pull-up supply but it is "NOT" allowed to power other devices or circuitry. The VCC pin must be bypassed to ground with a 1μF, X7R capacitor and it needs to be placed as close as possible to the VCC pin. Be careful to account for the voltage coefficient of ceramic capacitors when choosing the value and case size. Many ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

17.9 Enable Control

The RTQ2106-QA provides an EN pin, as an external chip enable control, to enable or disable the device. If V_{EN} is held below a logic-low threshold voltage (V_{EN_F}), switching is inhibited even if the VIN voltage is above VIN undervoltage-lockout threshold (V_{UVLO_R}). If V_{EN} is held below 0.4V, the converter will enter into shutdown mode, that is, the converter is disabled. During shutdown mode, the supply current can be reduced to I_{SHDN} (5μA or below). If the V_{EN} rises above the logic-high threshold voltage (V_{EN_R}) while the VIN voltage is higher than V_{UVLO_R}, the device will be turned on, that is, switching being enabled and soft-start sequence being initiated. The current source of EN typically sinks 1.2μA.

17.10 Soft-Start

The soft-start function is used to prevent large inrush currents while the converter is being powered up. The RTQ2106-QA provides an SS pin so that the soft-start time can be programmed by selecting the value of the external soft-start capacitor CSS connected from the SS pin to ground. During the start-up sequence, the soft-start capacitor is charged by an internal current source ISS (typically, 6μA) to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. If the output is for some reasons pre-biased to a certain voltage during start-up, the device will not turn on the high-side MOSFET switch until the voltage difference between the SS pin and the FB pin is larger than 400mV (i.e., VSS − VFB > 400mV, typically). And only when this ramp voltage is higher than the feedback voltage VFB, the switching will be resumed. The output voltage can then ramp up smoothly to its target regulation voltage, and the converter can have a monotonic smooth start-up. For soft-start control, the SS pin should never be left unconnected. After the VSS rises above 2V (typically), the PG pin will be in high impedance and V_{PG} will be held high. The typical startup waveform shown in Figure 1 indicates the sequence and timing between the output voltage and related voltage.

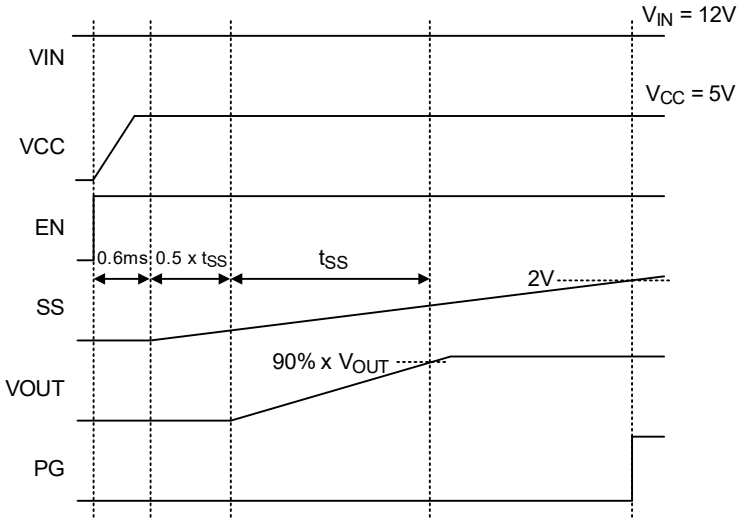


Figure 1. Start-Up Sequence

17.11 Power-Good Indication

The RTQ2106-QA features an open-drain power-good output (PG) to monitor the output voltage status. The output delay of the comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Pull-up PG with a resistor to VCC or an external voltage below 5.5V. The power-good function is activated after soft-start is finished and is controlled by a comparator connected to the feedback signal VFB. If VFB rises above a power-good high threshold (VTH_PGLH1) (typically 90% of the reference voltage), the PG pin will be in high impedance and V_{PG} will be held high after a certain delay elapsed. When VFB exceeds VTH_PGHL1 (typically 120% of the reference voltage), the PG pin will be pulled low, moreover, IC turns off the

high-side MOSFET switch and turns on low-side MOSFET switch until the inductor current reaches ISK_L if the MODE pin is set high. If the VFB is still higher than VTH_PGHL1, the high-side MOSFET switch remains prohibited and the low-side MOSFET switch will turn-on again at next cycle. If the MODE pin is set low, IC turns off low-side MOSFET switch once the inductor current reaches zero current unless VBOOT−SW is too low. For VFB higher than VTH_PGHL1, V_{PG} can be pulled high again if VFB drops back by a power-good high threshold (VTH_PGLH2) (typically 117% of the reference voltage). When VFB falls below the power-good low threshold (VTH_PGHL2) (typically 85% of the reference voltage), the PG pin will be pulled low. Once being started-up, if any internal protection is triggered, PG will be pulled low to ground. The internal open-drain pulldown device (10Ω, typically) will pull the PG pin low. The power-good indication profile is shown in Figure 2.

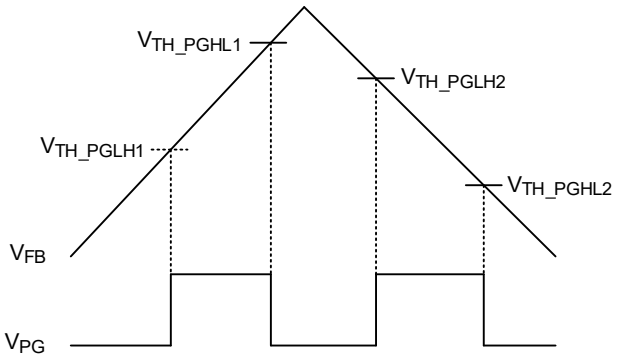


Figure 2. The Logic of PG

17.12 Spread Spectrum Operation

Due to the periodicity of the switching signals, energy is concentrated at a particular frequency and also in its harmonics. These energy levels are radiated and therefore this is where a potential EMI issue arises. The RTQ2106-QA built-in spread spectrum frequency modulation further helping systems designers with better EMC management. The spread spectrum can be active when soft-start is finished and zero-current is not detected. The spread spectrum is implemented by a pseudo random sequence and uses +6% spread of the switching frequency, that is, the frequency will vary from 2.1MHz to 2.226MHz. Therefore, the RTQ2106-QA still guarantees that the 2.1MHz switching frequency does not drop into the AM band limit of 1.8MHz. However, the spread spectrum cannot be active when the device is synchronized with an external clock by the MODE/ SYNC pin.

17.13 Input Undervoltage-Lockout

In addition to the EN pin, the RTQ2106-QA also provides enable control through the VIN pin. If VEN rises above V_{EN_R} first, switching will still be inhibited until the VIN voltage rises above V_{UVLO_R}. It is to ensure that the internal regulator is ready so that operation with not-fully-enhanced internal MOSFET switches can be prevented. After the device is powered up, if the VIN voltage goes below the UVLO falling threshold voltage (V_{UVLO_F}), this switching will be inhibited; if VIN voltage rises above the UVLO rising threshold (V_{UVLO_R}), the device will resume switching. Note that VIN = 3V is only designed for cold crank requirements; the normal input voltage should be larger than V_{UVLO_R}.

17.14 High-Side Switch Current-Limit Protection

The RTQ2106-QA includes a cycle-by-cycle high-side switch peak current-limit protection against the condition that the inductor current increases abnormally, even over the inductor saturation current rating. The high-side MOSFET switch peak current limit of the RTQ2106-QA is adjustable by placing a resistor on the RLIM pin. The recommended resistor value ranges from 33kΩ (for typically 5.5A) to 91kΩ (for typically 2.2A) and it is recommended to use resistors with 1% tolerance or better and temperature coefficient of 100 ppm or less. The

inductor current through the high-side MOSFET switch will be measured after a certain amount of delay when the high-side MOSFET switch being turned on. If an overcurrent condition occurs, the converter will immediately turn off the high-side MOSFET switch and turn on the low-side MOSFET switch to prevent the inductor current exceeding the high-side MOSFET switch peak current limit (I_{LIM_H}).

17.15 Low-Side Switch Current-Limit Protection

The RTQ2106-QA not only implements the high-side switch peak current limit but also provides the sourcing current limit and sinking current limit for low-side MOSFET switch. With these current protections, the IC can easily control inductor current at both side switches and avoid current runaway for short-circuit conditions. For the low-side MOSFET switch sourcing current limit, there is a specific comparator in internal circuitry to compare the low-side MOSFET switch sourcing current to the low-side MOSFET switch sourcing current limit at the end of every clock cycle. When the low-side MOSFET switch sourcing current is higher than the low-side MOSFET switch sourcing current limit which is high-side MOSFET switch current limit (I_{LIM_H}) multiplied by 0.95, the new switching cycle is not initiated until inductor current drops below the low-side MOSFET switch sourcing current limit. For the low-side MOSFET switch sinking current-limit protection, it is implemented by detecting the voltage across the low-side MOSFET switch. If the low-side MOSFET switch sinking current exceeds the low-side MOSFET switch sinking current limit (I_{SK_L}) (typically, 2A), the converter will immediately turn off the low-side MOSFET switch and turn on the high-side MOSFET switch.

17.16 Output Undervoltage Protection

The RTQ2106-QA includes output undervoltage protection (UVP) against overload or short-circuit conditions by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the undervoltage protection trip threshold (typically 50% of the internal reference voltage), the UV comparator will go high to turn off the high-side MOSFET and then turn off the low-side MOSFET when the inductor current drops to zero. If the output undervoltage condition continues for a period of time, the RTQ2106-QA enters output undervoltage protection with hiccup mode and discharges the C_{SS} by an internal discharging current source I_{SS_DIS} (typically, 2μA). During hiccup mode, the device remains shut down. After the V_{SS} is discharged to less than 150mV (typically), the RTQ2106-QA attempts to re-start up again, the internal charging current source ISS gradually increases the voltage on C_{SS}. The high-side MOSFET switch will start switching when the voltage difference between the SS pin and the FB pin is larger than 400mV (i.e., $V_{SS} - V_{FB} > 400mV$, typically). If the output undervoltage condition is not removed, the high-side MOSFET switch stops switching when the voltage difference between the SS pin and the FB pin is 700mV (i.e., $V_{SS} - V_{FB} = 700mV$, typically) and then the ISS_DIS discharging current source begins to discharge C_{SS}. Upon completion of the soft-start sequence, if the output undervoltage condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the output undervoltage condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and normal operation resumes as soon as the overload or short-circuit condition is removed. A short-circuit protection and recovery profile is shown in Figure 3.

Since the C_{SS} will be discharged to 150mV when the RTQ2106-QA enters output undervoltage protection, the first discharging time (t_{SS_DIS1}) can be calculated as follows:

$$t_{SS\_DIS1} = C_{SS} \times \frac{V_{SS} - 0.15}{I_{SS\_DIS}}$$

The equation below assumes that the V_{FB} will be 0 at short-circuit condition and it can be used to calculate the C_{SS} discharging time (t_{SS_DIS2}) and charging time (t_{SS_CH}) during hiccup mode.

$$t_{SS\_DIS2} = C_{SS} \times \frac{0.55}{I_{SS\_DIS}}$$

$$t_{SS\_CH} = C_{SS} \times \frac{0.55}{I_{SS\_CH}}$$

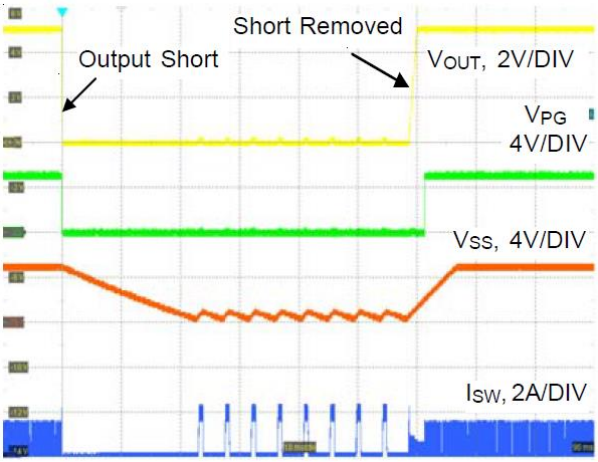


Figure 3. Short Circuit Protection and Recovery

17.17 Over-Temperature Protection

The RTQ2106-QA includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds a thermal shutdown threshold T_{OTP}. Once the junction temperature cools down by the over-temperature hysteresis (T_{OTP_HYS}), the IC will resume normal operation with a complete soft-start.

17.18 Pin-Short Protection

The RTQ2106-QA provides pin-short protection for adjacent pins. The internal protection fuse will be burned out to prevent IC smoke, fire, and spark when the BOOT pin is shorted to the VIN pin. The hiccup mode protection will be triggered to avoid IC burn-out when the SW pin is shorted to ground during the internal high-side MOSFET turns on.

18 Application Information

(Note 8)

A general RTQ2106-QA application circuit is shown in Typical Application Circuit. External component selection is largely driven by the load requirement and begins with the selection of operating mode by setting VMODE/SYNC. Next, the inductor L, the input capacitor C_{IN}, and the output capacitor C_{OUT} are chosen. Next, feedback resistors and compensation circuit are selected to set the desired output voltage and crossover frequency. Next, the internal regulator capacitor C_{VCC} and the bootstrap capacitor C_{BOOT} can be selected. Finally, the remaining optional external components can be selected for functions such as the EN, external soft-start, PG, inductor peak current limit, and synchronization.

18.1 FPWM/PSM Selection

The RTQ2106-QA provides a MODE/SYNC pin for Forced-PWM Mode (FPWM) and Power Saving Mode (PSM) operation selection at light load. To optimize efficiency at light loads, the RTQ2106-QA can be set in PSM. The VMODE/SYNC is held below a logic-low threshold voltage (V_{IL_SYNC}) of the MODE/SYNC input, that is, with the MODE/SYNC pin floating or pull low, the device operates in PSM at light load to improve light load efficiency. If it is necessary to keep switching harmonics out of the signal and, the RTQ2106-QA can operate in FPWM. The device is locked in PWM mode when VMODE/SYNC rises above a logic-high threshold voltage (V_{IH_SYNC}) of the MODE/SYNC input. The FPWM trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, fast transient response, and constant switching frequency.

18.2 Inductor Selection

The inductor selection makes trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR). A good compromise between size and loss is a 30% peak-to-peak ripple current to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. This results in additional phase lag in the loop and reduces the crossover frequency. As the ratio of the slope-compensation ramp to the sensed-current ramp increases, the current-mode system tilts towards voltage-mode control. Lower inductance values allow for smaller case size, but the increased ripple lowers the effective current-limit threshold, increases the AC losses in the inductor and may trigger low-side switch sinking current limit at FPWM. It also causes insufficient slope compensation and ultimately loop instability as the duty cycle approaches or exceeds 50%. When the duty cycle exceeds 50%, the following condition needs to be satisfied:

$$2.1 \times f_{SW} > \frac{V_{OUT}}{L}$$

A good compromise among size, efficiency, and transient response can be achieved by setting an inductor current ripple (ΔI_L) to about 10% to 50% of the maximum rated output current (3A). To enhance efficiency, choose a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The inductor value determines not only the ripple current but also the load-current value at which DCM/CCM switchover occurs. The inductor selected should have a saturation current rating greater than the peak current limit of the device. The core must be large enough not to saturate at the peak inductor current (I_{L_PEAK}):

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2} \Delta I_L$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power-up, faults, or transient load conditions, the inductor current can increase above the peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the high-side switch peak current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the high-side switch peak current limit, rather than the peak inductor current. It is recommended to use shielded inductors for good EMI performance.

18.3 Input Capacitor Selection

Input capacitor, C_{IN}, is needed to filter the pulsating current at the drain of the high-side MOSFET switch. C_{IN} should be sized to do this without causing a large variation in input voltage. The peak-to-peak voltage ripple on the input capacitor can be estimated using the following equation:

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + ESR \times I_{OUT}$$

where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

Figure 4 shows the C_{IN} ripple current flowing through the input capacitors and the resulting voltage ripple across the capacitors. For ceramic capacitors, the equivalent series resistance (ESR) is very low, the ripple caused by ESR can be ignored, and the minimum value of effective input capacitance can be estimated using the following equation:

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

Where $\Delta V_{CIN\_MAX} \leq 200mV$

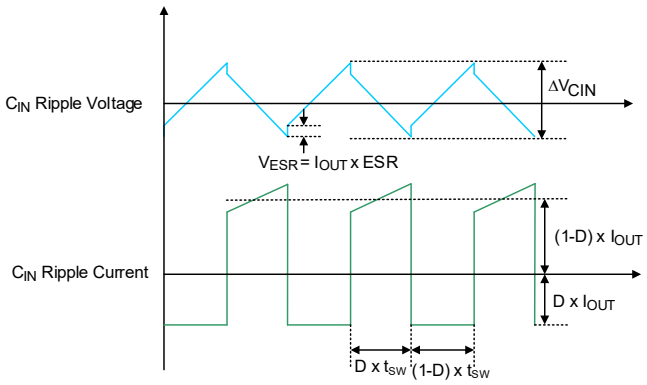


Figure 4. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current. The RMS ripple current (I_{RMS}) of the regulator can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) as the following equation:

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

From the above, the maximum RMS input ripple current occurs at maximum output load, which will be used as the

requirements to consider the current capabilities of the input capacitors. The maximum ripple voltage usually occurs at 50% duty cycle, that is, V_{IN} = 2 x V_{OUT}. It is common to use the worse-case I_{RMS} ≅ 0.5 x I_{OUT_MAX} at V_{IN} = 2 x V_{OUT} for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life. It is advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size, height, and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes. Ceramic capacitors are ideal for switching regulator applications due to their small size, robustness, and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high-quality (underdamped) tank circuit. If the RTQ2106-QA circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing. The input capacitor should be placed as close as possible to the VIN pin, with a low inductance connection to the PGND of the IC. It is recommended to connect a 4.7μF, X7R capacitor between the VIN pin to the PGND pin. For filtering high-frequency noise, additional small capacitor 0.1μF should be placed close to the device; the capacitor should be in a 0402 or 0603 package size. X7R capacitors are recommended for best performance across temperature and input voltage variations.

18.4 Output Capacitor Selection

The selection of C_{OUT} is determined by considering to satisfy the voltage ripple and the transient loads. The peak-to-peak output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right)$$

where the ΔI_L is the peak-to-peak inductor ripple current. The output ripple is highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Regarding to the transient loads, the V_{SAG} and V_{SOAR} requirements should be taken into consideration for choosing the effective output capacitance value. The amount of output sag/soar is a function of the crossover frequency factor at PWM, which can be calculated as follows:

$$V_{SAG} = V_{SOAR} = \frac{\Delta I_{OUT}}{2 \times \pi \times C_{OUT} \times f_C}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. The recommended dielectric type of the capacitor is X7R, which offers the best performance across temperature and input voltage variations. The variation of the capacitance value with temperature, DC bias voltage, and switching frequency must be considered. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage. Transient performance can be improved by using a higher output capacitance. Increasing the output capacitance will also decrease the output voltage ripple.

18.5 Output Voltage Programming

The output voltage can be programmed using a resistive divider connected from the output to ground, with the midpoint connected to the FB pin. The resistive divider allows the FB pin to sense a fraction of the output voltage, as shown in Figure 5. The output voltage is set according to the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2} \right)$$

where the reference voltage V_{REF}, is 0.8V (typically).

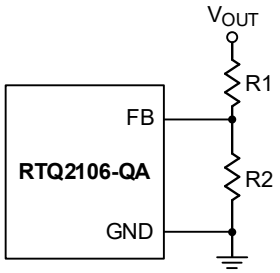


Figure 5. Output Voltage Setting

The placement of the resistive divider should be within 5mm of the FB pin. The resistance of R2 is not larger than 170kΩ for noise immunity consideration. The resistance of R1 can then be obtained as follows:

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

For better output voltage accuracy, the divider resistors (R1 and R2) with ±1% tolerance or better should be used.

18.6 Compensation Network Design

The purpose of loop compensation is to ensure stable operation while maximizing the dynamic performance. An undercompensated system may result in unstable operations. Typical symptoms of an unstable power supply include: audible noise from the magnetic components or ceramic capacitors, jittering in the switching waveforms, output voltage oscillation, overheating of power MOSFETs, and so on. In most cases, the peak current mode control architecture used in the RTQ2106-QA requires only two external components to achieve a stable design, as shown in Figure 6. The compensation can be selected to accommodate any capacitor type or value. The external compensation also allows the user to set the crossover frequency and optimize the transient performance of the device. Around the crossover frequency, the peak current mode control (PCMC) equivalent circuit of the buck converter can be simplified, as shown in Figure 7. The method presented here is easy to calculate and ignores the effects of the slope compensation, which is implemented internally in the device. Since the slope compensation is ignored, the actual crossover frequency will usually be lower than the crossover frequency used in the calculations. It is always necessary to verify the design through measurement before releasing the design for final production. Although the models of power supplies are theoretically correct, they cannot take full account for circuit parasitic and component nonlinearity, such as the ESR variations in output capacitors, then on linearity of inductors and capacitors. Also, PCB noise and limited measurement accuracy may also cause measurement errors. A Bode plot is ideally measured using a network analyzer while Richtek application note AN038 provides an alternative way to check the stability quickly and easily. Generally, follow the following steps to calculate the compensation components:

1. Set up the crossover frequency, f_C. For stability purposes, the target is to have a loop gain slope that is −20dB/decade from a very low frequency to beyond the crossover frequency. Do “NOT” design the crossover frequency over 80kHz with the RTQ2106-QA. For dynamic purposes, the higher bandwidth results in a faster load transient response. The downside of high bandwidth is that it increases the regulators susceptibility to board noise, which ultimately leads to excessive falling-edge jitter at the switch node voltage.

2. RCOMP can be determined by:

$$R_{COMP} = \frac{2\pi \times f_C \times V_{OUT} \times C_{OUT}}{gm \times V_{REF} \times gm\_CS} = \frac{2\pi \times f_C \times C_{OUT}}{gm \times gm\_CS} \times \frac{R1 + R2}{R2}$$

where gm is the error amplifier gain of transconductance (950μA/V) gm_cs is COMP to current sense (5.6A/V)

3. A compensation zero can be placed at or before the dominant pole of the buck converter, which is provided by the output capacitor and the maximum output loading (R_L). Calculate C_{COMP} as follows:

$$C_{COMP} = \frac{R_L \times C_{OUT}}{R_{COMP}}$$

4.The compensation pole is set to the frequency at the ESR zero or 1/2 of the operating frequency. Output capacitor and its ESR provide a zero and optional C_{COMP2} can be used to cancel this zero.

$$C_{COMP2} = \frac{R_{ESR} \times C_{OUT}}{R_{COMP}}$$

If 1/2 of the operating frequency is lower than the ESR zero, the compensation pole set at 1/2 of the operating frequency.

$$C_{COMP2} = \frac{1}{2\pi \times f_P \times R_{COMP}}$$

Note 7. Generally, C_{COMP2} is an optional component to be used to enhance noise immunity.

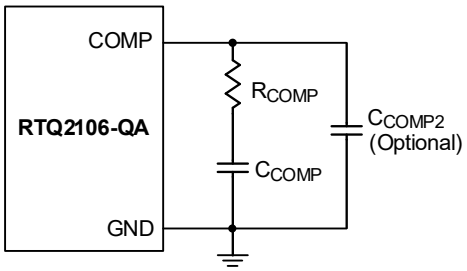


Figure 6. External Compensation Components

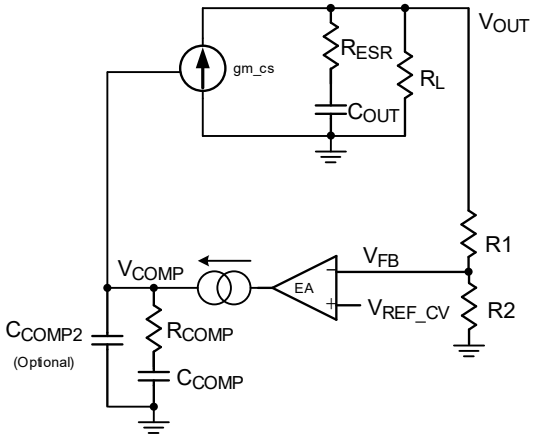


Figure 7. Simplified Equivalent Circuit of Buck with PCMC

18.7 Internal Regulator

The device integrates a 5V linear regulator (VCC) that is supplied by VIN and provides power to the internal circuitry. The internal regulator operates in low dropout mode when the VIN voltage is below 5V. V_{CC} can be used as the PG pull-up supply, but it is "NOT" allowed to power other devices or circuitry. The VCC pin must be bypassed to ground with a 1μF X7R capacitor, and it needs to be placed as close as possible to the VCC pin. Be careful to account for the voltage coefficient of ceramic capacitors when choosing the value and case size. Many ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

18.8 Bootstrap Driver Supply

The bootstrap capacitor (C_{BOOT}) between the BOOT pin and the SW pin is used to create a voltage rail above the applied input voltage, V_{IN}. Specifically, the bootstrap capacitor is charged through an internal diode to a voltage equal to approximately VCC each time the low-side switch is turned on. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle. For most applications a 0.1μF, 0603 ceramic capacitor with X7R is recommended and the capacitor should have a 6.3V or higher voltage rating.

18.9 External Bootstrap Diode (Option)

It is recommended to add an external bootstrap diode between an external 5V voltage supply and the BOOT pin to improve enhancement of the high-side MOSFET switch and improve efficiency when the input voltage is below 5.5V, the recommended application circuit is shown in Figure 8. The bootstrap diode can be a low-cost one, such as 1N4148 or BAT54. The external 5V can be a fixed 5V voltage supply from the system, or a 5V output voltage generated by the RTQ2106-QA. Note that the $V_{BOOT-SW}$ must be lower than 5.5V. Figure 9 shows efficiency comparison with and without Bootstrap Diode.

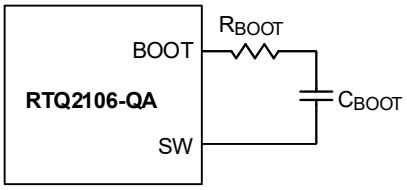


Figure 8. External Bootstrap Diode

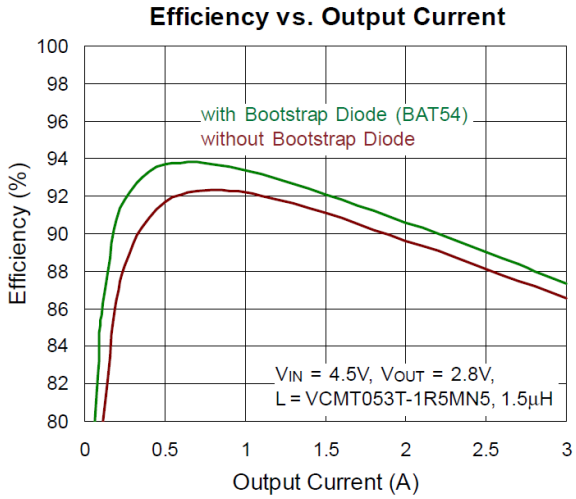


Figure 9. Efficiency Comparison with and without Bootstrap Diode

18.10 External Bootstrap Resistor (Option)

The gate driver of an internal power MOSFET, utilized as a high-side MOSFET switch, is optimized for turning on the switch not only fast enough for reducing switching power loss, but also slow enough for minimizing EMI. The EMI issue becomes more severe when the switch is turned on rapidly, due to the high di/dt noises induced. When the high-side MOSFET switch is turned off, the SW node will be discharged relatively slowly by the inductor current due to the presence of the dead time, when both the high-side and low-side MOSFET switches are turned off. In some cases, it is desirable to reduce EMI further, even at the expense of some additional power dissipation. The turn-on rate of the high-side MOSFET switch can be slowed by placing a small bootstrap resistor R_{BOOT} between

the BOOT pin and the external bootstrap capacitor, as shown in Figure 10. The recommended value for the R_{BOOT} ranges from several ohms to 10 ohms and it can be 0402 or 0603 in size. This will slow down the turn-on rate of the high-side MOSFET switch and the rise time of V_{SW}. In order to improve EMI performance and enhance of the internal MOSFET switch, the recommended application circuit is shown in Figure 11, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} placed between the BOOT pin and the capacitor/diode connection.

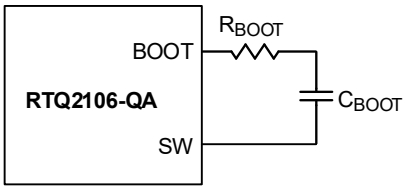


Figure 10. External Bootstrap Resistor at the BOOT Pin

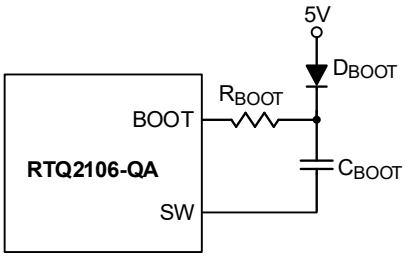


Figure 11. External Bootstrap Diode and Resistor at the BOOT Pin

18.11 EN Pin for Start-Up and Shutdown Operation

For automatic start-up, the EN pin, with high-voltage rating, can be connected to the input supply V_{IN} directly. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to VIN by adding a resistor R_{EN} and a capacitor C_{EN}, as shown in Figure 12, to have an additional delay. The time delay can be calculated with the EN's internal threshold, at which switching operation begins (typically 1.25V). An external MOSFET can be added for the EN pin to be logic-controlled, as shown in Figure 13. In this case, a pull-up resistor, R_{EN}, is connected between VIN and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin. To prevent the device being enabled when VIN is smaller than the V_{OUT} target level or some other desired voltage level, a resistive divider (R_{EN1} and R_{EN2}) can be used to externally set the input undervoltage-lockout threshold, as shown in Figure 14.

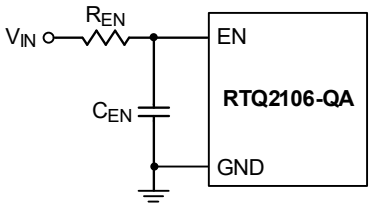


Figure 12. Enable Timing Control

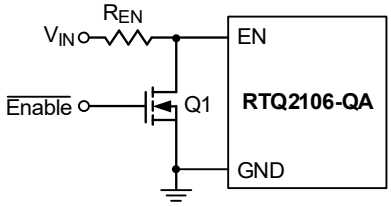


Figure 13. Logic Control for the EN Pin

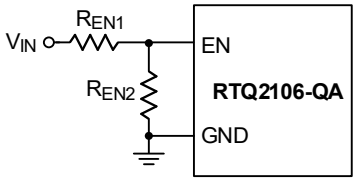


Figure 14. Resistive Divider for Undervoltage-Lockout Threshold Setting

18.12 Soft-Start

The RTQ2106-QA provides an adjustable soft-start function. The soft-start function is used to prevent large inrush current while the converter is being powered-up. For the RTQ2106-QA, the soft-start timing can be programmed by the external capacitor C_{SS} between the SS pin and ground. An internal current source I_{SS} (6μA) charges an external capacitor to build a soft-start ramp voltage. The V_{FB} will track the internal ramp voltage during soft-start interval. The typical soft-start time (t_{SS}), defined as the time V_{OUT} rise from zero to 90% of setting value, is calculated as follows:

$$t_{SS} = C_{SS} \times \frac{0.8}{I_{SS}}$$

Be aware that the system design should allocate a margin for the minimum capacitance of CSS to avoid the possibility of a failure to boot up within the soft-start period, which can occur due to a design with a slow compensation bandwidth. Additionally, for proper device operation, it is essential that the minimum soft-start time (t_{SS_min}) exceeds 500μs.

If a heavy load is added to the output with large capacitance, the output voltage will never enter regulation because of UVP. Thus, the device remains in hiccup operation. The C_{SS} should be large enough to ensure soft-start period ends after C_{OUT} is fully charged.

$$C_{SS} \geq C_{OUT} \times \frac{I_{SS} \times V_{OUT}}{0.8 \times I_{COUT\_CHG}}$$

where I_{COUT_CHG} is the C_{OUT} charge current, which is related to the switching frequency, inductance, high-side MOSFET switch peak current limit, and load current.

18.13 Power-Good Output

The PG pin is an open-drain power-good indication output and should be connected to an external voltage source through a pull-up resistor. The external voltage source can be an external voltage supply below 5.5V, V_{CC}, or the output of the RTQ2106-QA if the output voltage is regulated under 5.5V. It is recommended to connect a 100kΩ between the external voltage source to the PG pin.

18.14 Inductor Peak Current Limit Setting

The current limit of the high-side MOSFET switch is adjustable by an external resistor connected to the RLIM pin. The recommended resistor value ranges from 33kΩ (for typical 5.5A) to 91kΩ (for typical 2.2A). It is recommended to use resistors with 1% tolerance or better, and temperature coefficient of 100 ppm or less. When the inductor current reaches the current-limit threshold, the VCOMP will be clamped to limit the inductor current. The inductor current ripple current also should be considered into current limit setting.

It is recommended to set the minimum current limit to at least 1.2 times the peak inductor current. The minimum current limit can be calculated as follows:

Minimum current limit = ($I_{OUT(MAX)}$ + 1/2 inductor current ripple) x 1.2

The current limit value is set by connecting an external resistor R_{LIM} to the R_{LIM} pin.

The following formula provides an approximate calculation for the current limit value:

$$R_{LIM}(k\Omega) = \frac{178.8}{I_{SET} - 0.2531} - 1$$

where I_{SET} is the desired current limit value (A)

The failure modes and effects analysis (FMEA) should also be considered when setting the RLIM pin to avoid abnormal current limit operation under failure conditions. The following failure scenarios should be considered: short-circuit to ground and the pin is left open.

- The inductor peak current limit will be 6.2A (typical) if the RLIM pin is shorted to ground.
- The inductor peak current limit will be 1.4A (typical) if the RLIM pin is left open.

Note that the inductor peak current limit variation increases as the tolerance of R_{LIM} increases. If the R_{LIM} value is small, the inductor peak current limit will probably be operated as if the RLIM pin is shorted to ground, and vice versa. The RLIM variation range is limited from 30kΩ to 100kΩ to eliminate the undesired inductor peak current limit. If a value outside the recommended range is selected, make sure proper operation by evaluating it with real machine.

18.15 Synchronization

The RTQ2106-QA can be synchronized to an external clock ranging from 300kHz to 2.2MHz, which is applied to the MODE/SYNC pin. The external clock must have a duty cycle between 20% and 80%, and the amplitude should have valleys that are below V_{IL_SYNC} and peaks above V_{IH_SYNC} (up to 6V). The RTQ2106-QA will not enter PSM operation at light load while synchronized to an external clock. Instead, it will operate in FPWM to maintain regulation.

18.16 Thermal Consideration

In many applications, the RTQ2106-QA does not generate much heat due to its high efficiency and low thermal resistance of its TSSOP-14 (Exposed Pad) package.

However, in applications in which the RTQ2106-QA is running at a high ambient temperature and high input voltage or high switching frequency, the generated heat may exceed the maximum junction temperature of the part. The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. If the junction temperature reaches approximately 175°C, the RTQ2106-QA stop switching the power MOSFETs until the temperature drops about 15 °C cooler. The maximum power dissipation can be calculated by the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 150°C. T_A is the ambient operating temperature. θ_{JA} is the system-level junction to ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system. The device thermal resistance depends strongly on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance.

Experiments in the Richtek thermal lab show that simply set $\theta_{JA(EFFECTIVE)}$ as 110% to 120% of the $\theta_{JA(EVB)}$ is reasonable to obtain the allowed $P_{D(MAX)}$. As an example, consider the case when the RTQ2106-QA is used in applications where V_{IN} = 12V, I_{OUT} = 3A, V_{OUT} = 5V. The efficiency at 5V, 3A is 87.7% by using Cyntec-VCMT063T-2R2MN5 (2.2μH, 15mΩ DCR) as the inductor and measured at room temperature. The core loss can be obtained from its website of 37.1mW in this case. In this case, the power dissipation of RTQ2106-QA is

$$P_{D,\,RT} = \frac{1-\eta}{\eta} \times P_{OUT} - \left(I_O^2 \times DCR + P_{CORE}\right) = 1.932W$$

Considering the $\theta_{JA(EFFECTIVE)}$ is 41°C/W by using the RTQ2106-QA evaluation board with 4 layers with 2 OZ. copper thickness on the outer layers and 1 OZ. copper thickness on the inner layers copper thickness, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

T_J = 1.932W × 41°C/W + 25°C = 104.2°C

Figure 15 shows the RTQ2106-QA RDS(ON) versus different junction temperature. If the application calls for a higher ambient temperature, we might recalculate the device power dissipation and the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. Using 60°C ambient temperature as an example, the change of the equivalent $R_{DS(ON)}$ can be obtained from Figure 15 and yields a new power dissipation of 2.066W.

Therefore, the estimated new junction temperature is:

T_J' = 2.066W × 41°C/W + 60°C = 144.7°C

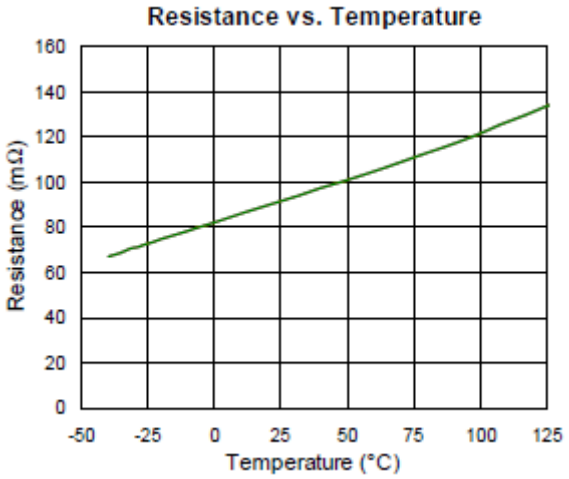


Figure 15. $R_{DS(ON)}$ vs. Temperature

If the application calls for a higher ambient temperature and/or higher switching frequency, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow. Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

18.17 Layout Guideline

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RTQ2106-QA:

- Four-layer or six-layer PCB with a maximum ground plane is strongly recommended for good thermal performance.
- Keep the traces of the main current paths wide and short.
- Place high frequency decoupling capacitor C_{IN2} as close as possible to the IC to reduce the loop impedance and minimize switch node ringing.
- Place the C_{VCC} as close to the VCC pin as possible.
- Place the bootstrap capacitor, C_{BOOT}, as close to the IC as possible. Routing the trace with a width of 20mil or wider.
- Place multiple vias under the device near VIN and PGND and near the input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the RTQ2106-QA to additional ground planes within the circuit board and on the bottom side.
- The high frequency switching nodes, SW and BOOT, should be as small as possible. Keep analog components away from the SW and BOOT nodes.
- Reducing the area size of the SW exposed copper to reduce the electrically coupling from this voltage.
- Connect the feedback sense network behind the via of the output capacitor.
- Place the feedback components R_{FB1}/R_{FB2}/C_{FF} near the IC.
- Place the compensation components R_{CP1}/C_{CP1}/C_{CP2} near the IC.
- Connect all analog grounds to a common node and then connect the common node to the power ground with a single point.

Figure 16 to Figure 19 are the layout examples using a 70mm x 100mm, four-layer PCB with 2 OZ. Cu on the outer layers and 1 OZ. Cu on the inner layers.

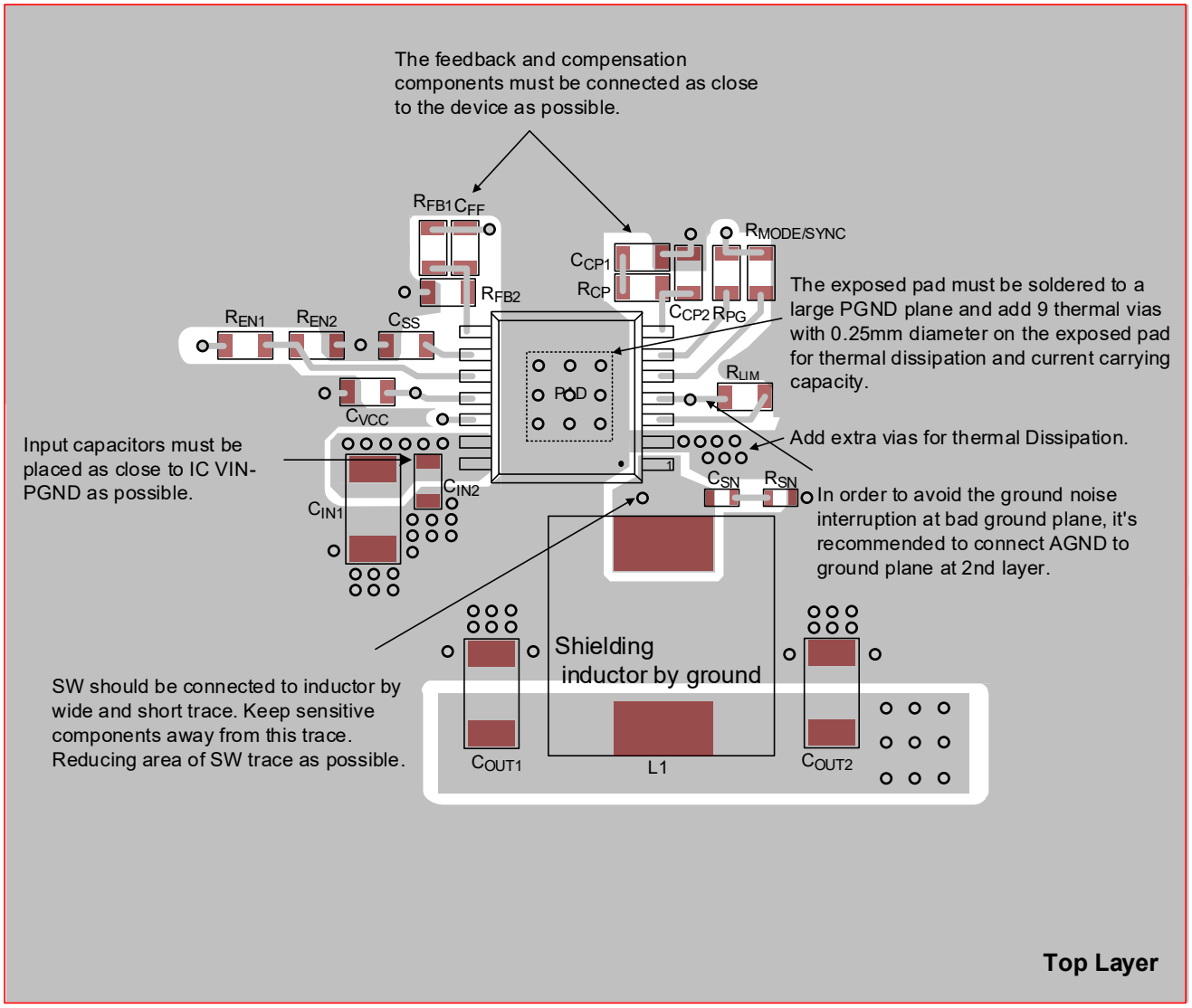


Figure 16. Layout Guide (Top Layer)

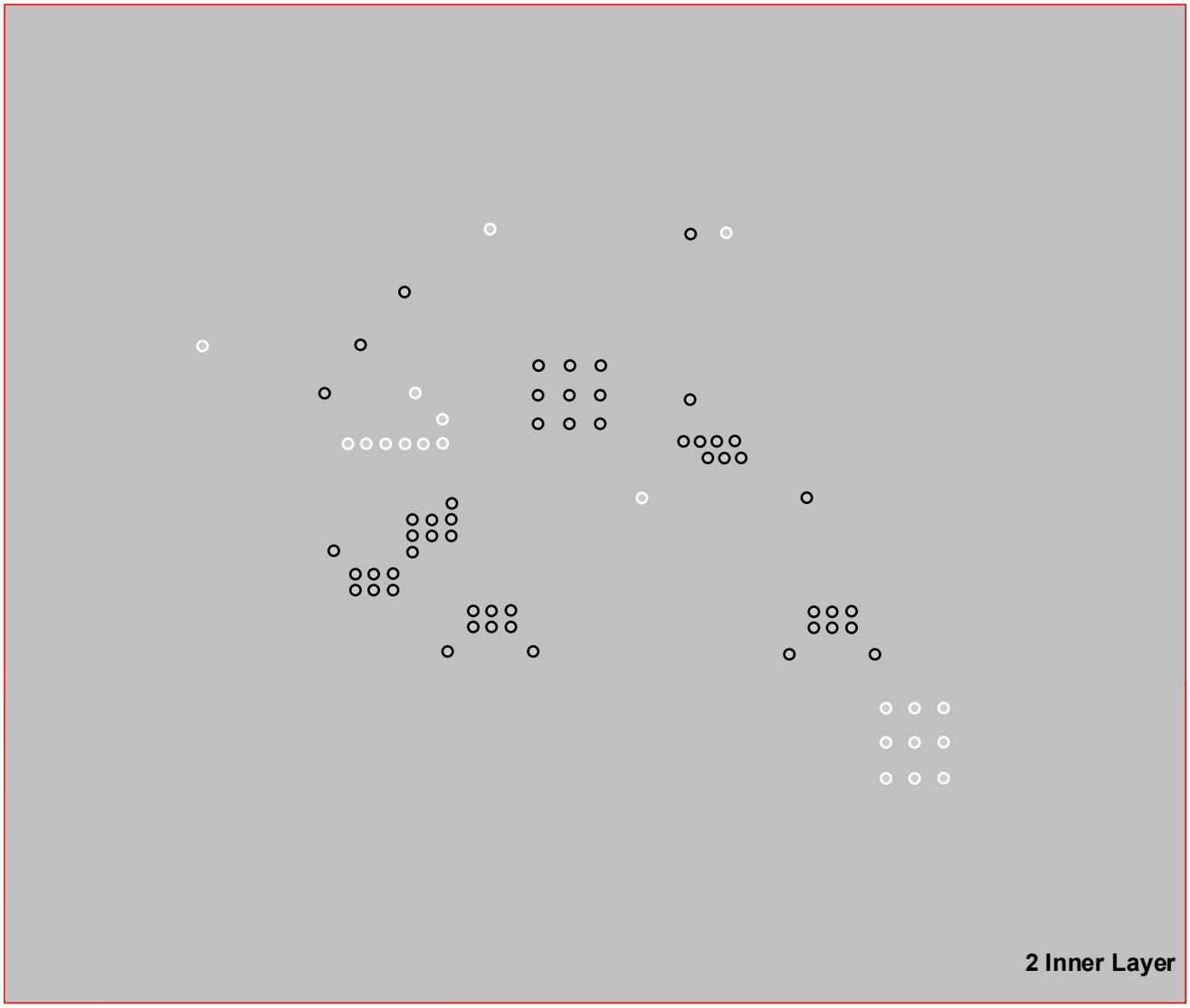


Figure 17. Layout Guide (2 Inner Layer)

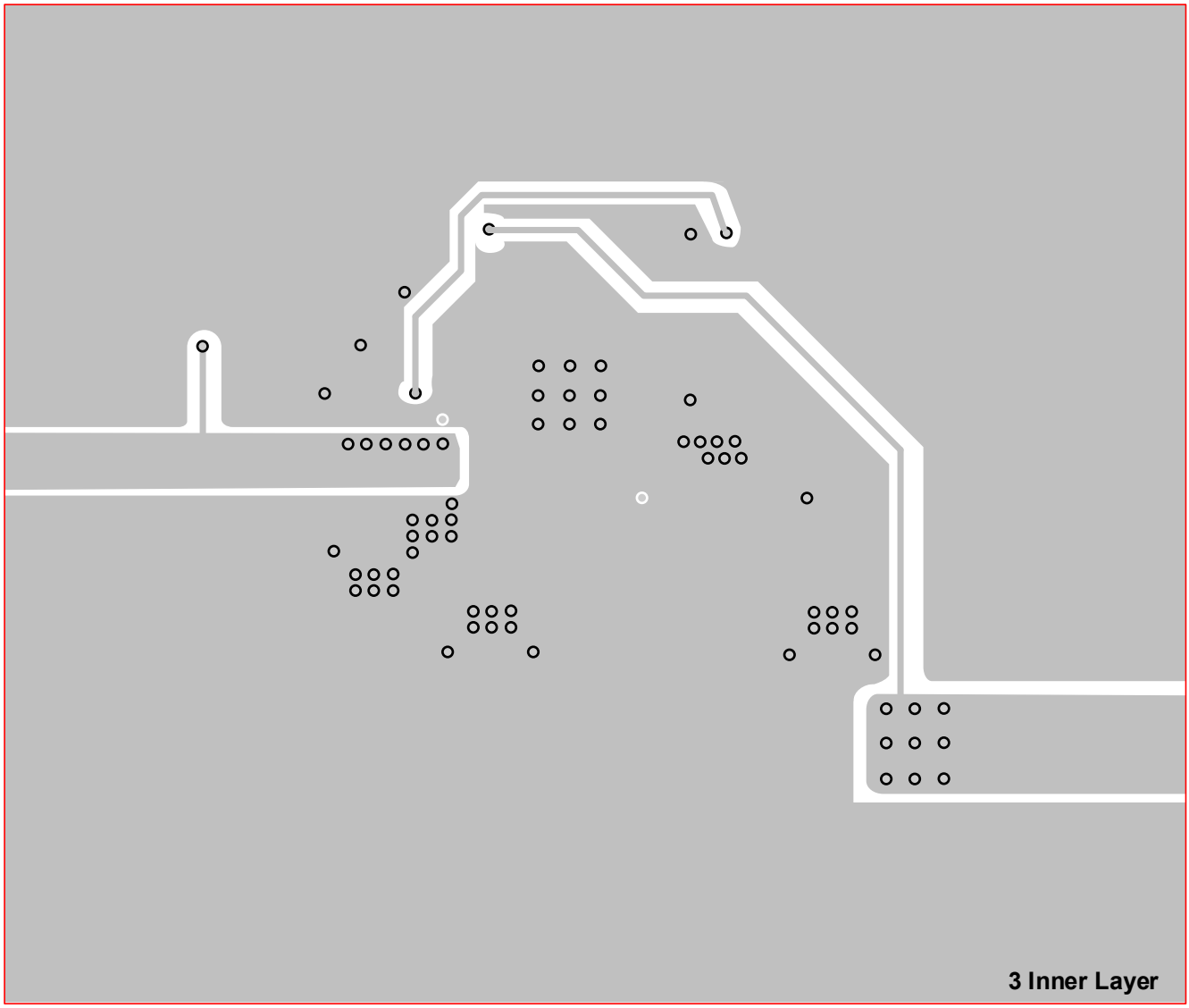


Figure 18. Layout Guide (3 Inner Layer)

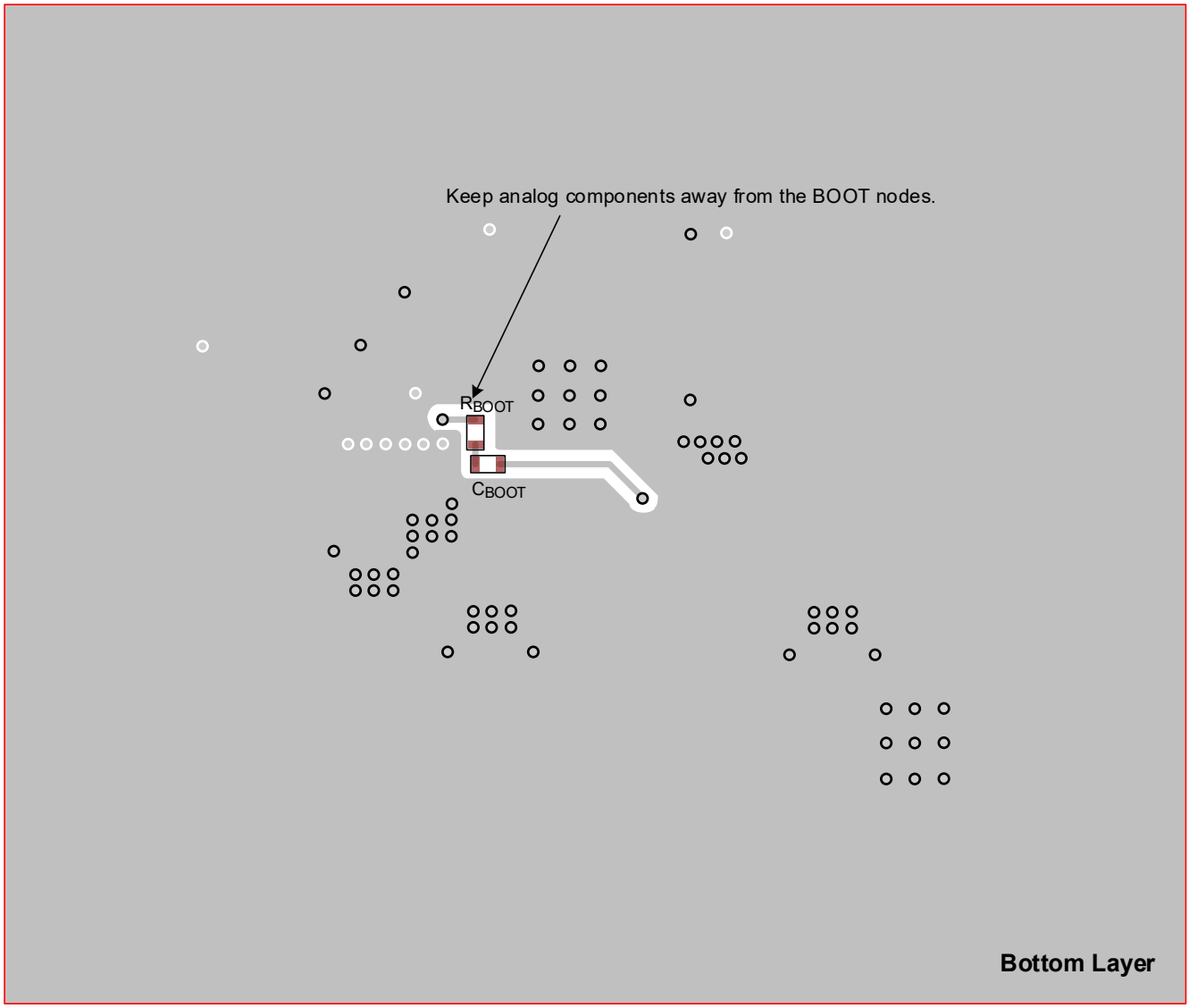
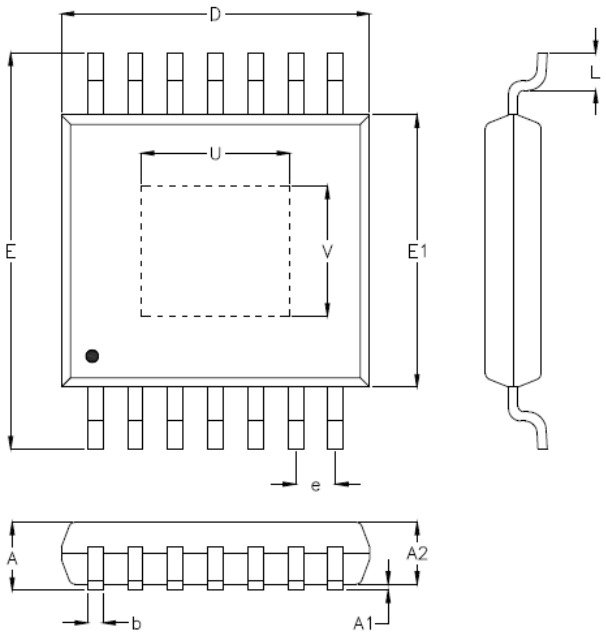


Figure 19. Layout Guide (Bottom Layer)

Note 8. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

19 Outline Dimension

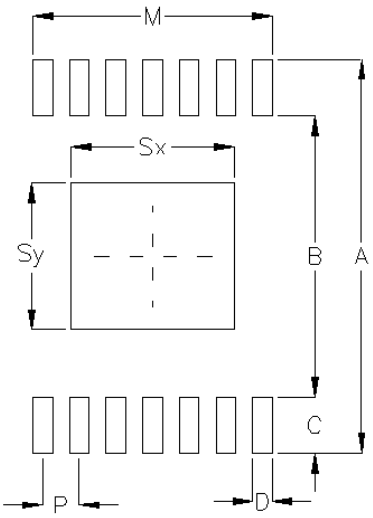


Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		1.000	1.200	0.039	0.047
A1		0.000	0.150	0.000	0.006
A2		0.800	1.050	0.031	0.041
b		0.190	0.300	0.007	0.012
D		4.900	5.100	0.193	0.201
e		0.650		0.026	
E		6.300	6.500	0.248	0.256
E1		4.300	4.500	0.169	0.177
L		0.450	0.750	0.018	0.030
U	Option1	1.900	2.900	0.075	0.114
	Option2	2.350	2.850	0.093	0.112
	Option3	2.640	3.100	0.104	0.122
V	Option1	1.600	2.600	0.063	0.102
	Option2	2.250	2.750	0.089	0.108
	Option3	2.550	3.000	0.100	0.118

14-Lead TSSOP (Exposed Pad) Plastic Package

Note 9. The package of the RTQ2106-QA uses Option 2.

20 Footprint Information



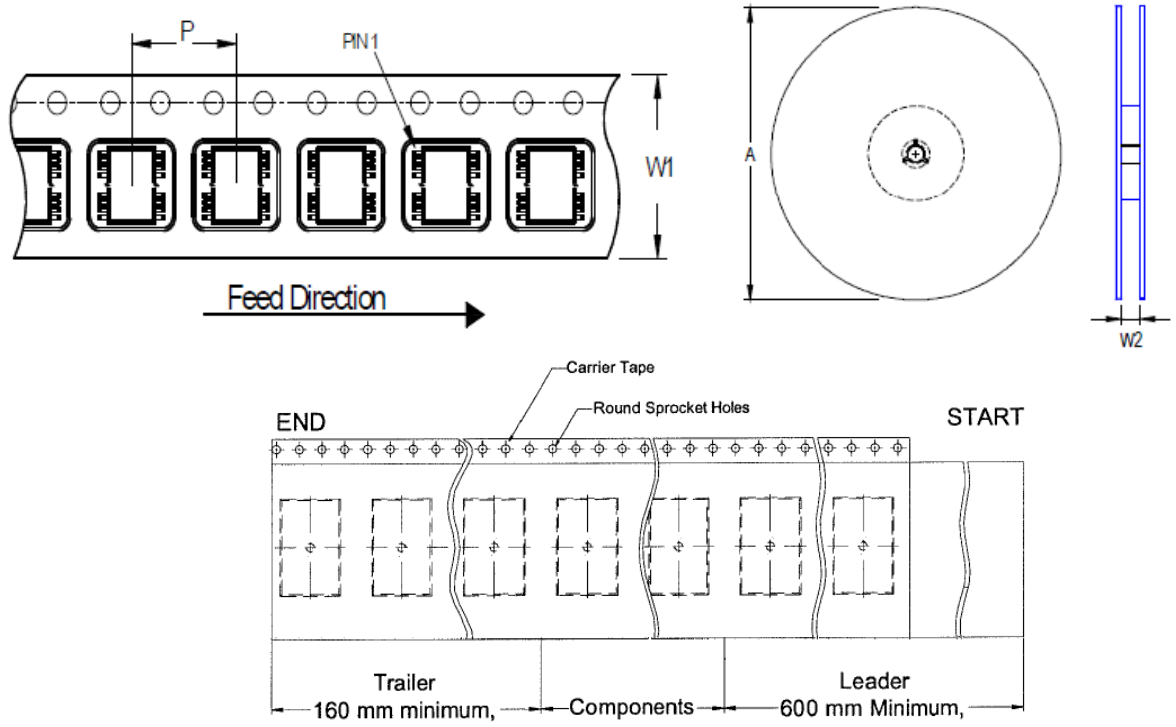
Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
TSSOP-14(PP)	Option1	14	0.65	7.00	5.00	1.00	0.35	2.90	2.60	4.25	±0.10
	Option2							2.85	2.75		
	Option3							3.10	3.00		

Note 10. The package of the RTQ2106-QA uses Option 2.

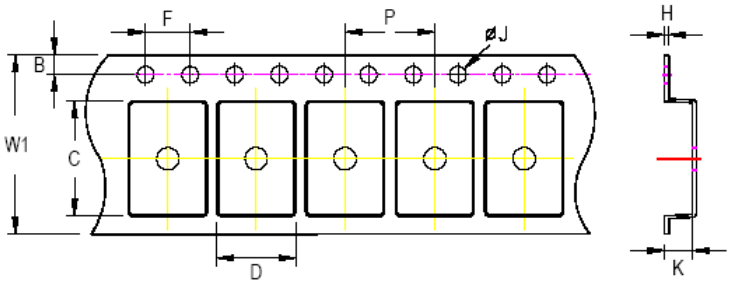
21 Packing Information

21.1 Tape and Reel Data

21.1.1 Units per Reel: 2500



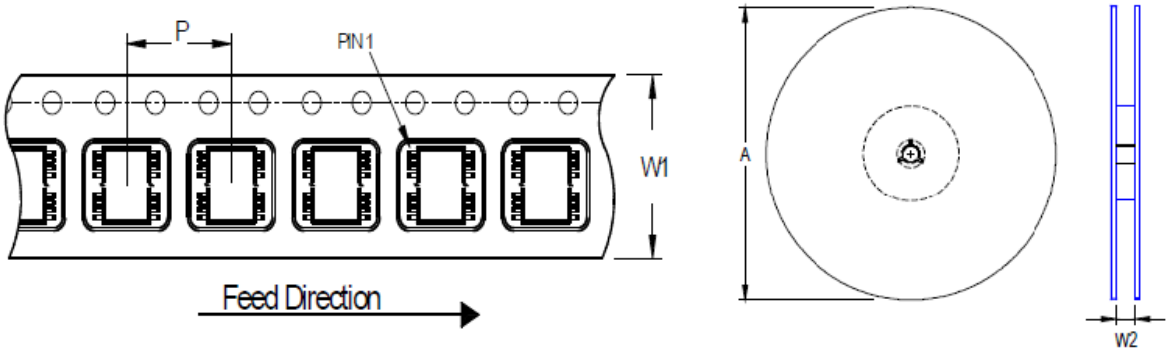
Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer(mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
TSSOP-14	12	8	330	13	2,500	160	600	12.4/14.4

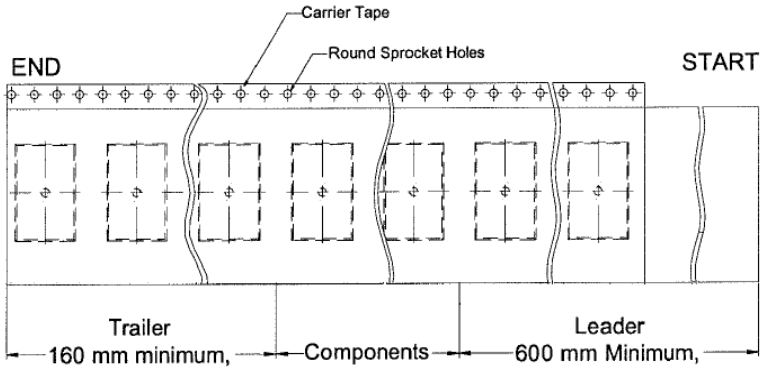


C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm maximum

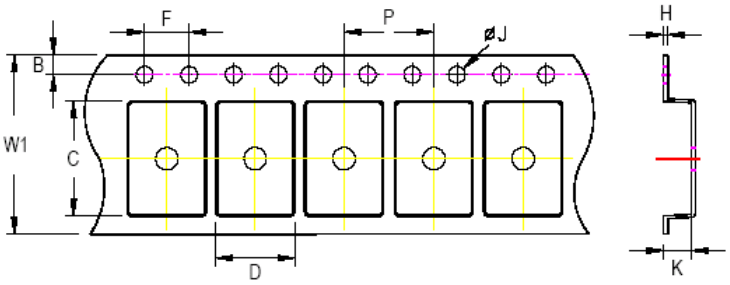
Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.5mm	1.7mm	0.6mm

21.1.2 Units per Reel: 3500





Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer(mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
TSSOP-14	12	8	330	13	3,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.5mm	1.7mm	0.6mm

21.2 Tape and Reel Packing

21.2.1 Units per Reel: 2500

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Package \ Container	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
TSSOP-14	13”	2,500	Box G	1	2,500	Carton A	6	15,000

21.2.1 Units per Reel: 3500

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
TSSOP-14	13”	3,500	Box G	1	3,500	Carton A	6	21,000

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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22 Datasheet Revision History

Version	Date	Description
03	2026/11/4	Changed the names PGOOD to PG General Description Features Simplified Application Circuit - Simplified Application Circuit Functional Pin Description Recommended Operating Conditions Thermal Information Electrical Characteristics Typical Application Circuit Operation Application Information Packing Information - Added packing information