RICHTEK®

RTQ2116A-QA

Charging Port Controller and Integrated 36V 3A Synchronous Buck Converter

1 General Description

The RTQ2116A-QA combines a charging port controller and a 3A synchronous buck converter.

The RTQ2116A-QA provides the electrical signatures on D+/D- to support charging schemes compatible with the USB 2.0 Battery Charging Specification BC1.2 and Chinese Telecommunication Industry Standard YD/T 1591-2009. Auto-detect mode is also integrated which supports USB 2.0 Battery Charging Specification BC1.2 Dedicated Charging Port (DCP), Divider 3 mode and 1.2V shorted mode to comply with the legacy fast charging mode of mobile devices.

The RTQ2116A-QA integrates a high efficiency, monolithic synchronous buck converter that can deliver up to 3A output current from a 4V to 36V wide range input supply and is protected from load-dump transients up to 42V.

The RTQ2116A-QA has constant current control to achieve adjustable USB current limit and implement the current sense signal for adjustable USB power output voltage with load line compensation. The converter includes optional spread spectrum frequency modulation to overcome EMI issue and complete protection for safe and smooth operation in all applied conditions. Protection features include cycle-by-cycle current limit for protection against shorted outputs, soft-start control to eliminate input current surge during start-up, input undervoltage-lockout, output undervoltage protection, output overvoltage protection and over-temperature protection. The RTQ2116A-QA can be used to support Type-A connectors.

The RTQ2116A-QA is fully specified over the temperature range of T_J = –40°C to 125°C and available in WET-WQFN-32L 5x5.

2 Features

- **USB Charging Port Controller**
  - **Support D+/D- DCP Modes per USB BC1.2**
  - **Support D+/D- Shorted Mode per Chinese Telecommunication Industry Standard YD/T 1591-2009**
  - **Support Automatic Selection Mode for D+/D- Shorted/Divider 3/1.2V Mode**
- **36V 3A Synchronous Buck Converter**
  - **4V to 36V Input Voltage Range**
  - **3A Continuous Output Current**
  - **CC/CV Mode Control**
  - **Adjustable and Synchronizable Switching Frequency: 300kHz to 2.2MHz**
  - **Selectable PSM/PWM at Light Load**
  - **Adjustable Soft-Start**
  - **Adjustable USB Power Output Voltage between 5V and 6V with Load Line Compensation**
  - **Optional Spread Spectrum Frequency Modulation for EMI Reductions**
- **Power-Good Indicator**
- **Enable Control**
- **±8kV HBM on DS+/DS-**
- **Over-Temperature Protection**
- **AEC-Q100 Grade 1 Qualified**
- **Cycle-by-Cycle Overcurrent-Limit Protection**
- **Input Undervoltage Protection**
- **Adjacent Pin-Short Protection**
- **–40°C to 125°C Operating Ambient Temperature**
- **DS+/DS- OVP**

3 Applications

- Automotive Car Chargers
- USB Power Chargers

4 Ordering Information

RTQ2116A □□-QA

Grade
QA : AEC-Q100 Qualified and Screened by High Temperature

Package Type(1)
QWT : WET-WQFN-32L 5x5 (W-Type)

Lead Plating System
G: Richtek Green Policy Compliant(2)

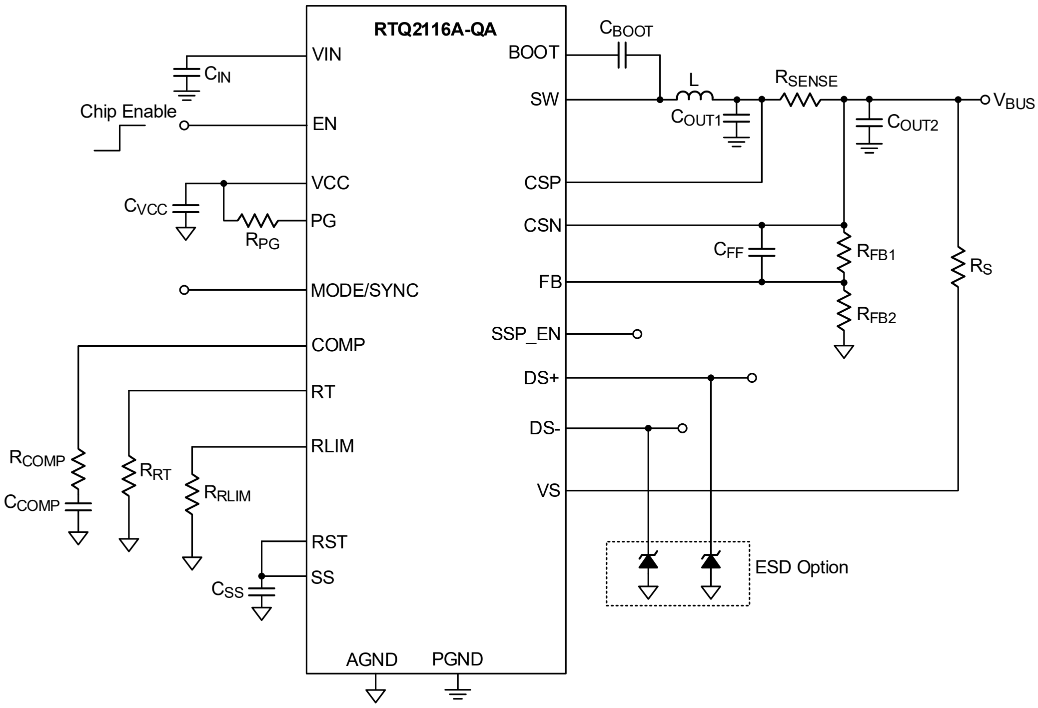
Note 1.

- Marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicates that Richtek products are Richtek Green Policy compliant.

5 Marking Information

RTQ2116AGQWT-QA : Product Number
YMDNN : Date Code

6 Simplified Application Circuit



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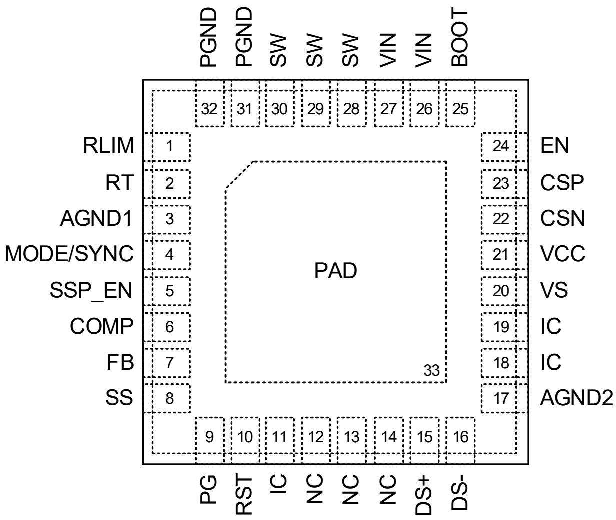
7 Pin Configuration

(TOP VIEW)



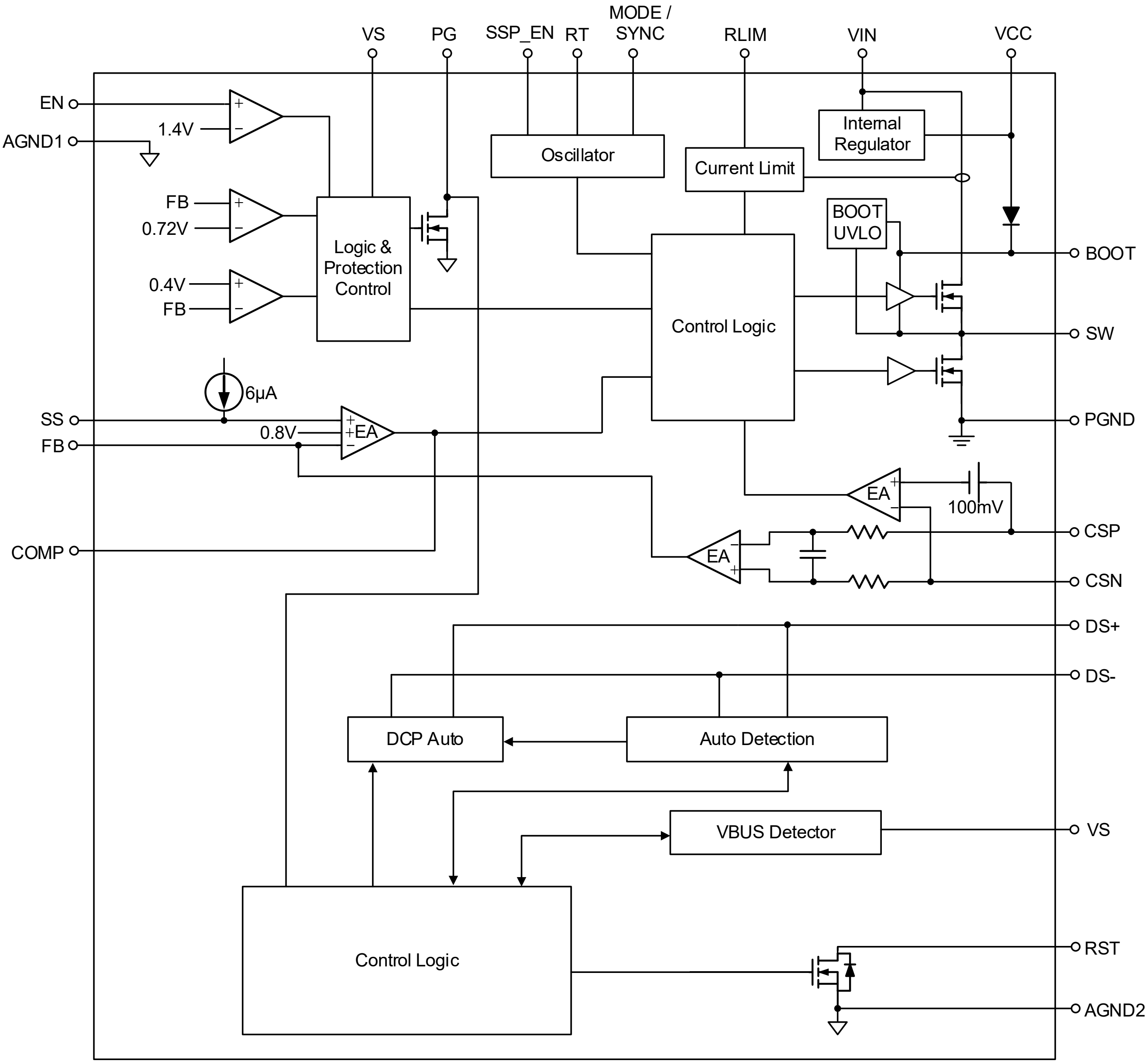
WET-WQFN-32L 5x5

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	RLIM	Current limit setup pin. Connect a resistor from this pin to ground to set the current limit value. The recommended resistor value ranges from 33kΩ (for typical 5.5A) to 91kΩ (for typical 2.3A).
2	RT	Oscillator frequency setup pin. Connect a resistor from this pin to ground to set the switching frequency. The recommended resistor value ranges from 174kΩ (for typical 300kHz) to 21kΩ (for typical 2.2MHz).
3	AGND1	Analog ground1.
4	MODE/SYNC	Mode selection and external synchronous signal input. Ground this pin or leave this pin floating enables the power saving mode operation at light load. Apply a DC voltage of 2V or higher, or tie to VCC for FPWM mode operation. Tie to a clock source for synchronization to an external frequency.
5	SSP_EN	Spread spectrum enable input. Connect this pin to VCC to enable spread spectrum. Float this pin or connect it to Ground to disable spread spectrum.
6	COMP	Compensation node. Connect external compensation elements to this pin to stabilize the control loop.
7	FB	Feedback voltage input. Connect this pin to the midpoint of the external feedback resistive divider to set the output voltage of the converter to the desired regulation level. The RTQ2116A-QA regulates the FB voltage at a feedback reference voltage, typically 0.8V.
8	SS	Soft-start capacitor connection node. Connect an external capacitor between this pin and analog ground to set the soft-start time.

Pin No.	Pin Name	Pin Function
9	PG	Open-drain power-good indication output. The power-good function is activated after soft-start is finished. "Do Not" leave this pin floating and must be connected this pin to VCC or external voltage supply above 1.2V through a resistor. PG is pulled high when both V_{OUT} > 90% and V_{SS} > 2V (typical). PG is pulled low when V_{OUT} < 85%, V_{OUT} > 120% and OTP is triggered.
10	RST	Open drain logic output for battery charging mode change output discharge. This pin must be directly connected to the SS pin.
11,18,19	IC	Internal connection.
12, 13, 14	NC	No internal connection.
15	DS+	D+ data line to upstream connector.
16	DS-	D- data line to upstream connector.
17	AGND2	Analog ground2.
20	VS	VBUS sensing, connected to VBUS through 200Ω external resistor.
21	VCC	Linear regulator output. VCC is the output of the internal 5V linear regulator powered by VIN. Decouple with a 1μF, X7R ceramic capacitor from VCC to ground for normal operation.
22	CSN	Current sense negative input. Do not leave this pin floating.
23	CSP	Current sense positive input. Do not leave this pin floating.
24	EN	Enable control input. A logic-high enables the converter; a logic-low forces the RTQ2116A-QA into shutdown mode.
25	BOOT	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.1μF ceramic capacitor between this pin and the SW pin.
26, 27	VIN	Power input. The input voltage range is from 4V to 36V after soft-start is finished. Connect input capacitors between this pin and PGND. It is recommended to use a 4.7μF, X7R and a 0.1μF, X7R capacitors.
28, 29, 30	SW	Switch node between the internal switch and the synchronous rectifier. Connect this pin to the inductor and bootstrap capacitor.
31, 32	PGND	Power ground.
33 (Exposed pad)	PAD	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large PGND plane. Connect this PGND plane to other layers with thermal vias to help dissipate heat from the RTQ2116A-QA.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VIN Voltage, VIN ---------- –0.3V to 42V
- SW Voltage, SW ---------- –0.3V to 42V
  <50ns ---------- –5V to 46.3V
- BOOT Voltage, V_{BOOT} ---------- –0.3V to 48V
- BOOT to SW Voltage, $V_{BOOT-SW}$ ---------- –0.3V to 6V
- EN, CSP, CSN, SS Voltage ---------- –0.3V to 42V
- DS+, DS- Voltage (T_R > 40ns, Note 3) ---------- –0.3V to 20V
- VS Voltage ---------- –0.3V to 24V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WET-WQFN-32L 5x5 ---------- 4.54W
- Package Thermal Resistance (Note 4)
  WET-WQFN-32L 5x5, θ_{JA} ---------- 27.5°C/W
  WET-WQFN-32L 5x5, θ_{JC} ---------- 6°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 5)
  HBM (Human Body Model)
  DS+, DS-, VS Pins to AGND2 ---------- 8kV
  Other Pins ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. The 20V absolute maximum rating of DS+ and DS- applies when the voltage rise time is more than 40ns. The absolute maximum rating of DS+ and DS- may occur down to 9.5V when the voltage rise time is under 40ns.

Note 4. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. The first layer is filled with copper. θ_{JC} is measured at the exposed pad of the package.

Note 5. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 6)

- Supply Input Voltage -- 4V to 36V
- Output Voltage -- 0.8V to 6V
- Ambient Temperature Range -- –40°C to 125°C
- Junction Temperature Range -- –40°C to 150°C

Note 6. The RTQ2116A-QA is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

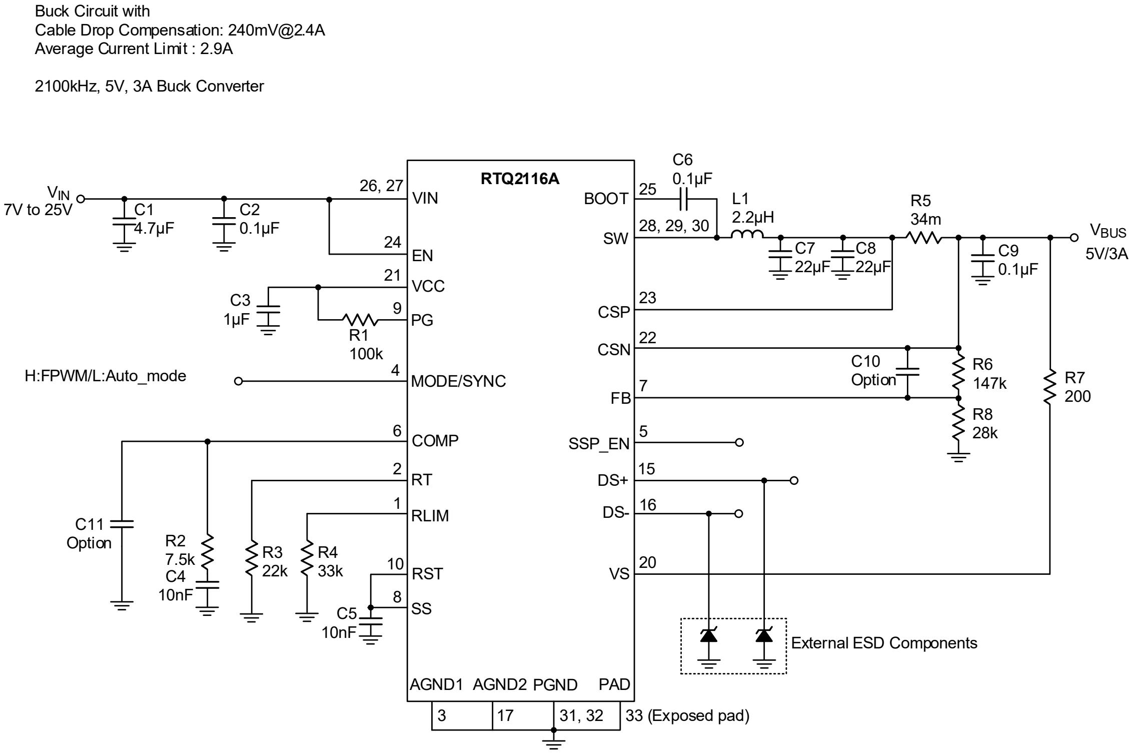
(V_{IN} = 12V, T_J = –40°C to 125°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
Input Operating Voltage	V_{IN}		4	--	36	V
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}	V_{IN} rising	3.6	3.8	4	V
Undervoltage-Lockout Falling Threshold	V_{UVLO_F}	V_{IN} falling	2.7	2.85	3	V
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	5	μA
Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = 0.82V, not switching, V_{CC} = 5V, Type C unattached	--	150	200	μA
Constant Voltage Regulation						
Reference Voltage for Constant Voltage Regulation	V_{REF_CV}	4V < V_{IN} < 36V, PWM, T_A = T_J = 25°C	0.792	0.8	0.808	V
		4V < V_{IN} < 36V, PWM, T_A = T_J = –40°C to 125°C	0.788	0.8	0.812	V
Enable Voltage						
EN Input Voltage Rising Threshold	V_{EN_R}	V_{EN} rising	1.15	1.25	1.35	V
EN Input Voltage Falling Threshold	V_{EN_F}	V_{EN} falling	0.9	1.05	1.15	V
Current Limit						
High-Side Switch Current Limit 1	I_{LIM_H1}	R_{LIM} = 91kΩ	1.87	2.2	2.53	A
High-Side Switch Current Limit 2	I_{LIM_H2}	R_{LIM} = 47kΩ	3.52	4.00	4.48	A
High-Side Switch Current Limit 3	I_{LIM_H3}	R_{LIM} = 33kΩ	4.84	5.5	6.16	A
Low-Side Switch Sinking Current Limit	I_{SK_L}	From drain to source	--	2	--	A
Switching						
Switching Frequency 1	f_{SW1}	R_{RT} = 174kΩ	264	300	336	kHz
Switching Frequency 2	f_{SW2}	R_{RT} = 51kΩ	0.88	0.98	1.08	MHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Frequency 3	f_{SW3}	R_{RT} = 21kΩ	1.98	2.2	2.42	MHz
SYNC Frequency Range			0.3	--	2.1	MHz
SYNC Switching High Threshold	V_{IH_SYNC}		--	--	2	V
SYNC Switching Low Threshold	V_{IL_SYNC}		0.4	--	--	V
SYNC Switching Clock Duty Cycle	D_{SYNC}		20	--	80	%
Minimum On-Time	t_{ON_MIN}		--	60	80	ns
Minimum Off-Time	t_{OFF_MIN}		--	65	80	ns
Internal MOSFET						
On-Resistance of High-Side MOSFET	R_{DSON_H}		--	70	130	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}		--	70	130	mΩ
High-Side Switch Leakage Current	I_{LEAK_H}	V_{EN} = 0V, V_{SW} = 0V	--	--	1	μA
Soft-Start						
Soft-Start Internal Charging Current	I_{SS}		4.5	6	7.2	μA
Power-Good						
Power-Good High Threshold 1	V_{TH_PGLH1}	V_{FB} rising, % of V_{REF_CV}, PG from low to high	85	90	95	%
Power-Good Low Threshold 1	V_{TH_PGHL1}	V_{FB} rising, % of V_{REF_CV}, PG from high to low	115	120	125	%
Power-Good Low Threshold 2	V_{TH_PGHL2}	V_{FB} falling, % of V_{REF_CV}, PG from high to low	80	85	90	%
Power-Good High Threshold 2	V_{TH_PGLH2}	V_{FB} falling, % of V_{REF_CV}, PG from low to high	112	117	122	%
Power-Good Leakage Current	I_{LK_PG}	PG signal good, V_{FB} = V_{REF}, V_{PG} = 5.5V	--	--	0.5	μA
Power-Good Sink Current Capability	I_{SK_PG}	PG signal fault, I_{PG} sinks 2mA	--	--	0.3	V
Error Amplifier						
Error Amplifier Trans-Conductance	gm	$-10\mu A < I_{COMP} < 10\mu A$	665	950	1280	μA/V
COMP to Current Sense Trans-Conductance	gm_{CS}		4.5	5.6	6.7	A/V
Load Line Compensation						
Load Line Compensation Current	I_{LC}	$V_{CSP} - V_{CSN}$ = 100mV, 5V < V_{CSP} and V_{CSN} < 6V	--	2	--	μA
		$V_{CSP} - V_{CSN}$ = 50mV, 5V < V_{CSP} and V_{CSN} < 6V	--	0.95	--	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Constant Current Regulation						
Reference Voltage for Constant Current Regulation	V_{REF_CC}	$V_{CSP} - V_{CSN}$, 3.3V < V_{CSP} and V_{CSN} < 6V	--	100	--	mV
Spread Spectrum						
Spread-Spectrum Range	SSP	Spread-spectrum option only	--	+6	--	%
Over-Temperature Protection						
Over-Temperature Protection Threshold	T_{OTP}		--	175	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	15	--	°C
Switching Pin Discharge Resistance		Force 1V	--	100	160	Ω
Output Undervoltage Protection						
Output Undervoltage Protection Threshold	V_{UVP}	UVP detect	0.35	0.4	0.45	V
DCP Shorted Mode						
DS+/DS- Shorting Resistance	R_{DCP_SHORT}	DS+ = 0.8V, I_{DS-} = 1mA	--	--	200	Ω
Resistance Between DS+/DS- and Ground	R_{DCHG_SHORT}	DS+ = 0.8V	300	--	--	kΩ
1.2V Shorted Mode						
DS+ Output Voltage	$V_{DP\_1.2V}$		1.12	1.2	1.28	V
DS+ Output Impedance	$R_{DP\_1.2V}$		80	102	130	kΩ
Divider 3 Mode						
DS+ Output Voltage	$V_{DP\_2.7V}$		2.57	2.7	2.84	V
DS- Output Voltage	$V_{DM\_2.7V}$		2.57	2.7	2.84	V
DS+ Output Impedance	$R_{DP\_2.7V}$		24	30	36	kΩ
DS- Output Impedance	$R_{DM\_2.7V}$		24	30	36	kΩ

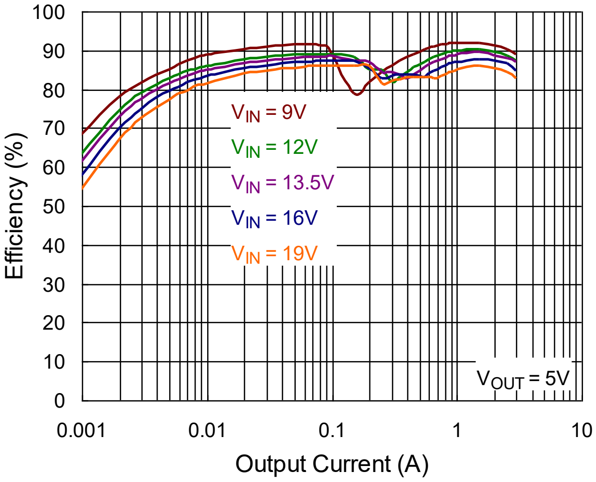
13 Typical Application Circuit



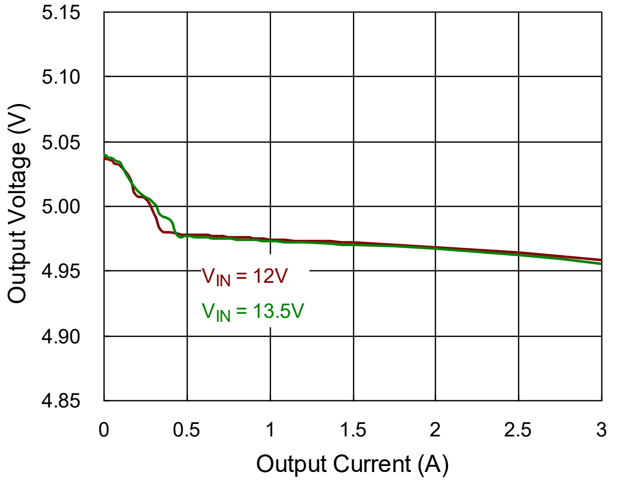
L1 = Cyntec-VCHA075D-2R2MS6
C7/C8 = GRM31CR71A226KE15L
C1 = GRM31CR71H475KA12L

14 Typical Operating Characteristics

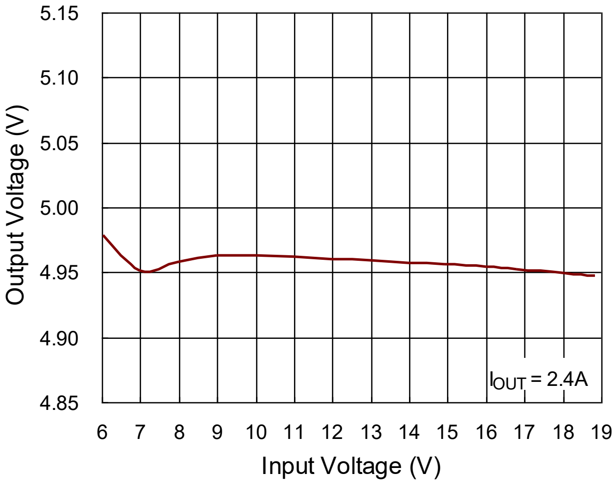
Efficiency vs. Output Current



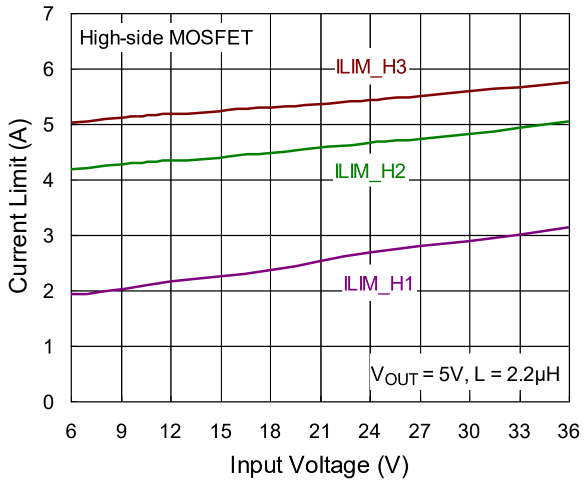
Output Voltage vs. Output Current



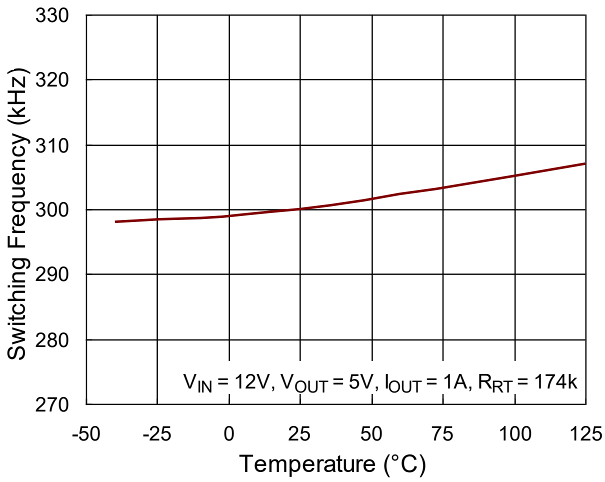
Output Voltage vs. Input Voltage



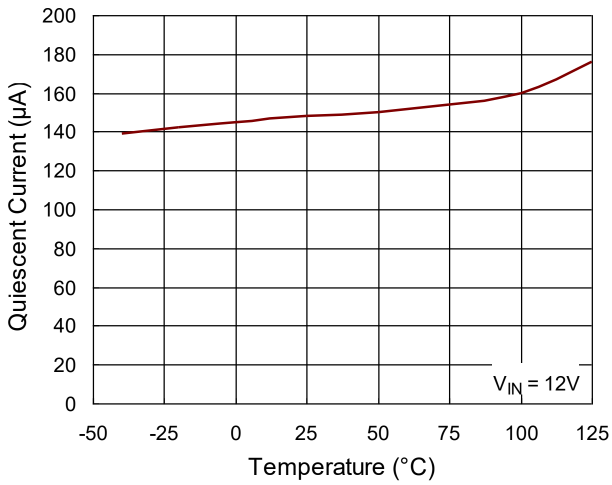
Current Limit vs. Input Voltage

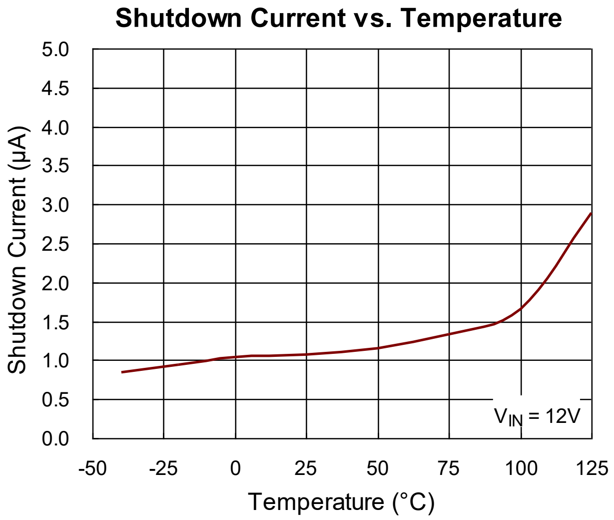


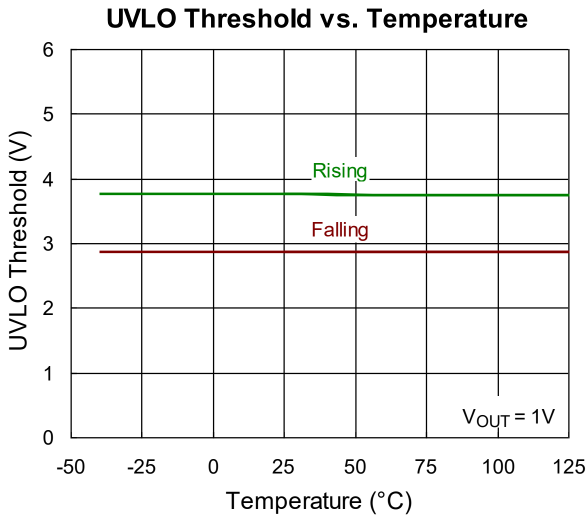
Switching Frequency vs. Temperature

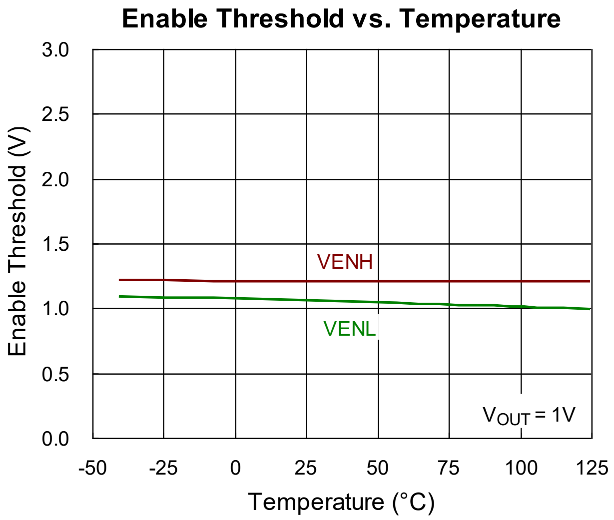


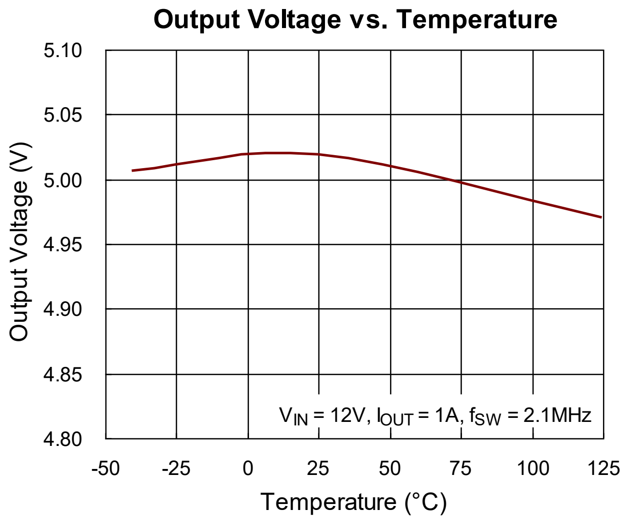
Quiescent Current vs. Temperature

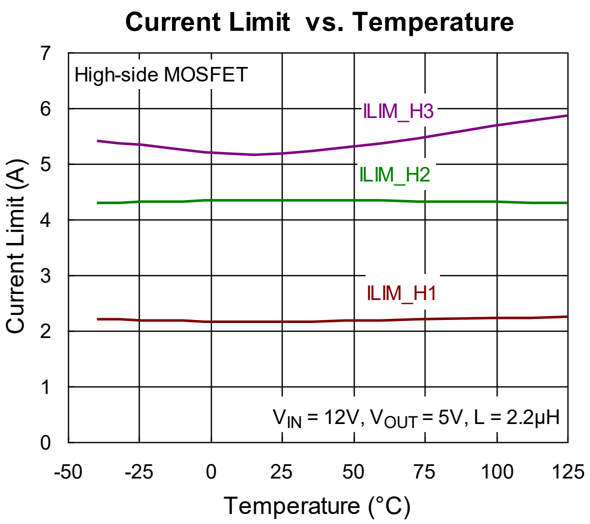


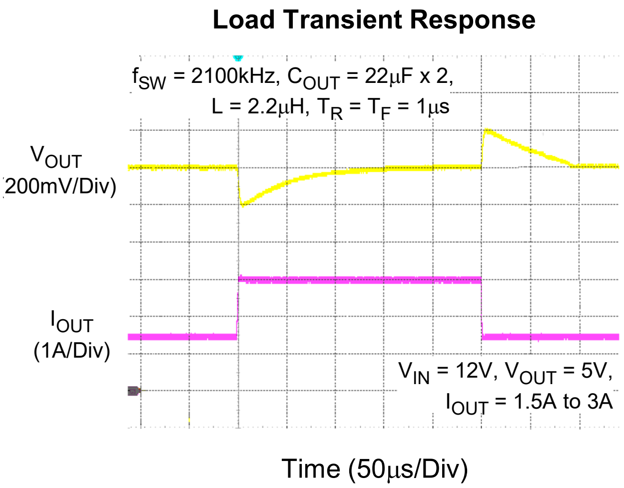

Shutdown Current vs. Temperature
Shutdown Current (μA)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-50
-25
0
25
50
75
100
125
Temperature (°C)
VIN = 12V


UVLO Threshold vs. Temperature
UVLO Threshold (V)
6
5
4
3
2
1
0
Rising
Falling
-50
-25
0
25
50
75
100
125
Temperature (°C)
VOUT = 1V

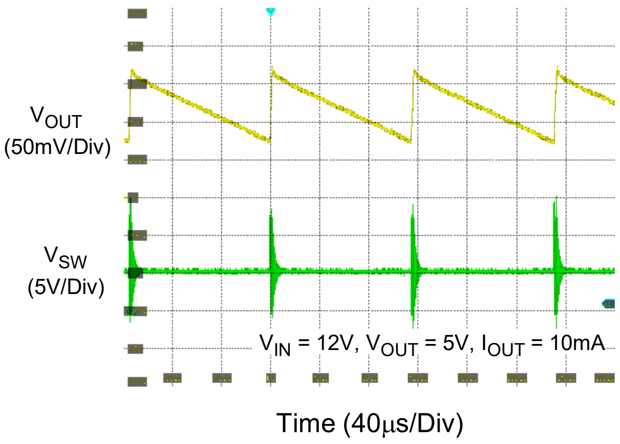

Enable Threshold vs. Temperature
Enable Threshold (V)
3.0
2.5
2.0
1.5
1.0
0.5
0.0
VENH
VENL
-50
-25
0
25
50
75
100
125
Temperature (°C)
VOUT = 1V


Output Voltage vs. Temperature
Output Voltage (V)
5.10
5.05
5.00
4.95
4.90
4.85
4.80
-50
-25
0
25
50
75
100
125
Temperature (°C)
VIN = 12V, IOUT = 1A, fSW = 2.1MHz

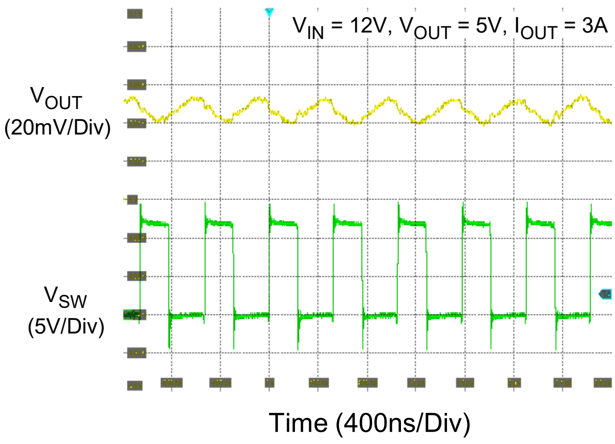

Current Limit vs. Temperature
Current Limit (A)
7
6
5
4
3
2
1
0
High-side MOSFET
ILIM_H3
ILIM_H2
ILIM_H1
-50
-25
0
25
50
75
100
125
Temperature (°C)
VIN = 12V, VOUT = 5V, L = 2.2μH


Load Transient Response
fSW = 2100kHz, COUT = 22μF x 2,
L = 2.2μH, TR = TF = 1μs
VOUT
(200mV/Div)
IOUT
(1A/Div)
VIN = 12V, VOUT = 5V,
IOUT = 1.5A to 3A
Time (50μs/Div)

Output Ripple Voltage



Output Ripple Voltage



15 Operation

The RTQ2116A-QA combines charging port controller and a 3A synchronous buck converter.

The RTQ2116A-QA integrates 70mΩ high-side and 70mΩ low-side MOSFETs to achieve high-efficiency conversion. The current mode control architecture supports fast transient response with simple compensation.

The RTQ2116A-QA supports the common USB charging schemes: USB Battery Charging Specification BC1.2, Chinese Telecommunications Industry Standard YD/T 1591-2009, Divider 3 Mode and 1.2V Short Mode. Pass through operation for USB Hi-Speed (480Mbps) and USB Full-Speed (12Mbps) is also supported.

15.1 Main Control Loop (CV Regulation)

The RTQ2116A-QA includes a high efficiency buck converter that utilizes the peak current mode control. An internal oscillator initiates the turn-on of the high-side MOSFET switch. At the beginning of each clock cycle, the internal high-side MOSFET switch turns on, allowing current to ramp up in the inductor. The inductor current is internally monitored during each switching cycle. The output voltage is sensed at the FB pin via the resistor divider, R1 and R2, and compared with the internal reference voltage for constant voltage control (V_{REF_CV}) to generate a CV compensation signal (V_{COMP}) at the COMP pin. A control signal derived from the inductor current is compared to the voltage at the COMP pin, derived from the feedback voltage. When the inductor current reaches its threshold, the high-side MOSFET switch is turned off and the inductor current ramps-down. While the high-side switch is off, the inductor current is supplied through the low-side MOSFET switch. This cycle repeats at the next clock cycle. In this way, the duty-cycle and output voltage are controlled by regulating inductor current.

15.2 MODE Selection and Synchronization

The RTQ2116A-QA provides a MODE/SYNC pin for Forced-PWM Mode (FPWM) and Power Saving Mode (PSM) operation selection at light load. If $V_{MODE/SYNC}$ at the MODE/SYNC input rises above the logic-high threshold voltage (V_{IH_SYNC}), the RTQ2116A-QA is locked in FPWM. If $V_{MODE/SYNC}$ at the MODE/SYNC input is held below the logic-low threshold voltage (V_{IL_SYNC}) of, the RTQ2116A-QA operates in PSM at light load to improve efficiency. The RTQ2116A-QA can also be synchronized with an external clock ranging from 300kHz to 2.2MHz via the MODE/SYNC pin.

15.3 Forced-PWM Mode

Forced-PWM operation provides constant frequency operation at all loads and is useful in applications sensitive to switching frequency. This mode trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, and constant switching frequency. In this mode, a negative current limit of I_{SK_L} is imposed to prevent damage to the low-side MOSFET switch of the regulator. "Do Not" connect external voltage source to the output terminal in FPWM, which may boost VIN. The converter synchronizes to any valid clock signal on the SYNC input when in FPWM.

When constant frequency operation is more important than light load efficiency, pull the MODE/SYNC input high or provide a valid synchronization input. Once activated, this feature ensures that the switching frequency stays away from the AM frequency band, while operating between the minimum and maximum duty cycle limits.

15.4 Maximum Duty Cycle Operation

The RTQ2116A-QA is designed to operate in dropout at the high duty cycle approaching 100%. If the operational duty cycle is large and the required off time becomes smaller than the minimum off time, the RTQ2116A-QA starts to enable the skip off time function and keeps the high-side MOSFET switch on continuously. The RTQ2116A-QA implements the skip off time function to achieve high duty approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application. The input voltage at which the RTQ2116A-QA enters dropout changes depends on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

15.5 BOOT UVLO

The BOOT UVLO circuit is implemented to ensure that a sufficient voltage of bootstrap capacitor for turning on the high-side MOSFET switch at any condition. The BOOT UVLO usually actives at extremely high conversion ratio or the higher VOUT application operates at very light load. With such conditions, the low-side MOSFET switch may not have sufficient turn-on time to charge the bootstrap capacitor. The RTQ2116A-QA monitors the voltage of the bootstrap capacitor and forces the low-side MOSFET switch on when the voltage of the bootstrap capacitor falls below $V_{BOOT\_UVLO\_L}$ (typically, 2.3V). Meanwhile, the minimum off time is extended to 150ns (typical) hence prolong the bootstrap capacitor charging time. The BOOT UVLO is sustained until the $V_{BOOT-SW}$ is higher than $V_{BOOT\_UVLO\_H}$ (typically, 2.4V).

15.6 Internal Regulator

The RTQ2116A-QA integrates a 5V linear regulator (V_{CC}) that is supplied by VIN and provides power to the internal circuitry. The internal regulator operates in low dropout mode when V_{IN} is below 5V. V_{CC} can be used as the PG pull-up supply, but it must “NOT” be used to power other devices or circuitry. The VCC pin must be bypassed to ground with a 1μF X7R capacitor and it needs to be placed as close as possible to the VCC pin. Be careful to account for the voltage coefficient of ceramic capacitors when choosing the value and case size. Many ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

15.7 Enable Control

The RTQ2116A-QA provides an EN pin, as an external chip enable control, to enable or disable the RTQ2116A-QA . If V_{EN} is held below a logic-low threshold voltage (V_{EN_F}) of the enable input (EN), switching is inhibited even if the VIN voltage is above VIN Undervoltage-Lockout Threshold (V_{UVLO_R}). If V_{EN} is held below 0.4V, the converter will enter shutdown mode, that is, the converter is disabled. During shutdown mode, the supply current can be reduced to I_{SHDN} (5μA or below). If the EN voltage rises above the logic-high threshold voltage (V_{EN_R}) while the VIN voltage is higher than V_{UVLO}, the RTQ2116A-QA will be turned on, that is, switching being enabled and soft-start sequence being initiated. The current source of EN typically sinks 1.2μA.

15.8 Soft-Start

The soft-start function is used to prevent large inrush currents while the converter is being powered up. The RTQ2116A-QA provides the SS pin so that the soft-start time can be programmed by selecting the value of the external soft-start capacitor C_{SS} connected from the SS pin to ground. During the start-up sequence, the soft-start capacitor is charged by an internal current source I_{SS} (typically, 6μA) to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. If the output is for some reasons pre-biased to a certain voltage during start-up, the RTQ2116A-QA will not turn on the high-side MOSFET switch until the voltage difference between the SS pin and the FB pin is larger than 400mV (typical). And only when this ramp voltage is higher than the feedback voltage V_{FB}, switching will be resumed. The output voltage can then ramp up smoothly to its target regulation voltage, and the converter can have a monotonic smooth start-up. For soft-start control, the SS pin should never be left unconnected. After the SS pin voltage rises above 2V (typical), the PG pin will be in high impedance and V_{PG} will be held high. The typical start-up waveform shown in Figure 1 indicate the sequence and timing between the output voltage and related voltage.

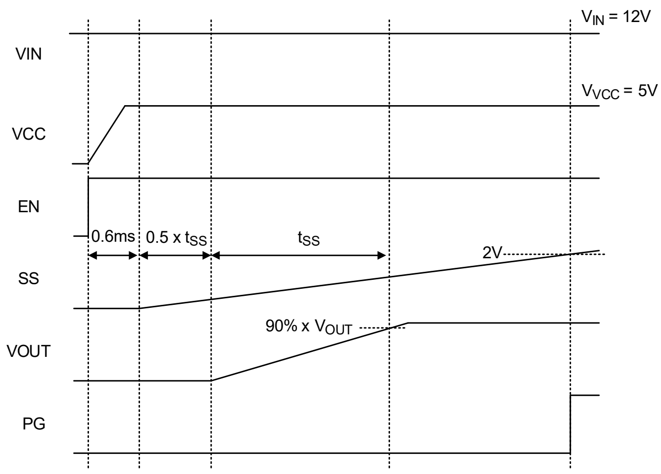


Figure 1. Start-Up Sequence

15.9 Power-Good Indication

The RTQ2116A-QA features an open-drain power-good output (PG) to monitor the output voltage status. The output delay of comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Pull-up PG with a resistor to V_{CC} or an external voltage below 5.5V. The power-good function is activated after soft-start is finished and is controlled by a comparator connected to the feedback signal V_{FB}. If V_{FB} rises above the power-good high threshold (V_{TH_PGLH1}) (typically 90% of the reference voltage), the PG pin will be in high-impedance and V_{PG} will be held high after a certain delay elapsed. When V_{FB} exceeds V_{TH_PGHL1} (typically 120% of the reference voltage), the PG pin will be pulled low, moreover, the IC turns off the high-side MOSFET switch and turns on the low-side MOSFET switch until the inductor current reaches I_{SK_L} if the MODE pin is set high. If the V_{FB} is still higher than V_{TH_PGHL1}, the converter enters low-side MOSFET switch sinking current limit operation. If the MODE pin is set low, the IC turns off the low-side MOSFET switch once the inductor current reaches zero current unless $V_{BOOT-SW}$ is too low. For V_{FB} higher than V_{TH_PGHL1}, V_{PG} can be pulled high again if V_{FB} drops back by a power-good high threshold (V_{TH_PGLH2}) (typically 117% of the reference voltage). When V_{FB} falls below the power-good low threshold (V_{TH_PGHL2}) (typically 85% of the reference voltage), the PG pin will be pulled low. Once being started-up, if any internal protection is triggered, PG will be pulled low to GND. The internal open-drain goes low impedance (10Ω, typical) and will pull the PG pin low.

The power-good indication profile is shown in Figure 2.

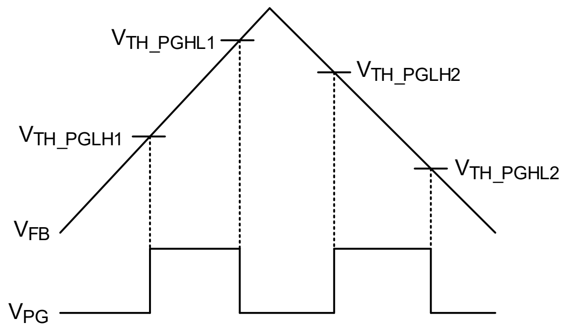


Figure 2. The Logic of PG

15.10 Spread-Spectrum Operation

Due to the periodicity of the switching signals, the energy concentrates in one particular frequency and also in its harmonics. These energy levels are radiated and therefore this is where a potential EMI issue arises. The

RTQ2116A-QA have optional spread-spectrum function and the SSP_EN pin can be programmed to turn on/off the spread spectrum, further simplifying compliance with the CISPR and automotive EMI requirements. The spread spectrum can be active when soft-start is finished and zero-current is not detected. If V_{SSP_EN} rises above a logic-high threshold voltage (2V, typical) of the SSP_EN input, the RTQ2116A-QA enables spread spectrum operation. The spread-spectrum is implemented by a pseudo random sequence and uses +6% spread of the switching frequency. For example, when the RTQ2116A-QA is programmed to 2.1MHz, the frequency will vary from 2.1MHz to 2.226MHz. Therefore, the RTQ2116A-QA still ensures that the 2.1MHz switching frequency setting does not drop into the AM band limit of 1.8MHz. However, the spread spectrum cannot be active when the RTQ2116A-QA is synchronized with an external clock by the MODE/SYNC pin.

15.11 Input Undervoltage-Lockout

In addition to the EN pin, the RTQ2116A-QA also provides enable control through the VIN pin. If V_{EN} rises above V_{EN_R} first, switching will still be inhibited until the VIN voltage rises above V_{UVLO}. It is to ensure that the internal regulator is ready so that operation with not-fully-enhanced internal MOSFET switches can be prevented. After the RTQ2116A-QA is powered up, if the input voltage V_{IN} goes below the UVLO falling threshold voltage (V_{UVLO_F}), this switching will be inhibited; if V_{IN} rises above the UVLO rising threshold (V_{UVLO_R}), the RTQ2116A-QA will resume switching. Note that V_{IN} = 3V is only design for cold crank requirements and the input voltage should be larger than the UVLO threshold to turn on the device.

15.12 High-Side Switch Current-Limit Protection

The RTQ2116A-QA includes a cycle-by-cycle high-side switch current-limit protection against the condition that the inductor current increasing abnormally, even over the inductor saturation current rating. The high-side MOSFET switch current limit of the RTQ2116A-QA is adjustable by placing a resistor on the RLIM pin. The recommended resistor value ranges from 33kΩ (for typically 5.5A) to 91kΩ (for typically 2.2A) and it is recommended to use resistors with 1% tolerance or better and temperature coefficient of 100 ppm or less. The inductor current through the high-side MOSFET switch will be measured after a certain amount of delay when the high-side MOSFET switch being turned on. If an overcurrent condition occurs, the converter will immediately turn off the high-side MOSFET switch and turn on the low-side MOSFET switch to prevent the inductor current exceeding the high-side MOSFET switch current limit (I_{LIM_H}).

15.13 Low-Side Switch Current-Limit Protection

The RTQ2116A-QA not only implements the high-side switch current limit but also provides the sourcing current limit and sinking current limit for the low-side MOSFET switch. With these current protections, the IC can easily control inductor current at both side switches and avoid current runaway for short-circuit conditions.

For the low-side MOSFET switch sourcing current limit, there is a specific comparator in the internal circuitry to compare the low-side MOSFET switch sourcing current to the low-side MOSFET switch sourcing current limit at the end of every clock cycle. When the low-side MOSFET switch sourcing current is higher than the low-side MOSFET switch sourcing current limit, which is the high-side MOSFET switch current limit (I_{LIM_H}) multiplied by 0.95, the new switching cycle is not initiated until the inductor current drops below the low-side MOSFET switch sourcing current limit.

For the low-side MOSFET switch sinking current-limit protection, it is implemented by detecting the voltage across the low-side MOSFET switch. If the low-side switch sinking current exceeds the low-side MOSFET switch sinking current limit (I_{SK_L}) (typically, 2A), the converter will immediately turn off the low-side MOSFET switch and turn on the high-side MOSFET switch. ”Do Not” choose an inductance that is too small, as this may trigger the low-side MOSFET switch sinking current-limit protection.

15.14 Output Undervoltage Protection

The RTQ2116A-QA includes output undervoltage protection (UVP) against overload or short-circuited conditions by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the undervoltage protection trip threshold (typically 50% of the internal reference voltage), the UV comparator will go high to turn off the high-side MOSFET and then turn off the low-side MOSFET when the inductor current drops to zero. If the output undervoltage condition continues for a period of time, the RTQ2116A-QA enters output undervoltage protection with hiccup mode and discharges the C_{SS} by an internal discharging current source I_{SS_DIS} (typically, 80nA). During hiccup mode, the RTQ2116A-QA remains shut down. When V_{SS} discharges below 150mV (typical), the RTQ2116A-QA attempts to restart, the internal charging current source I_{SS} gradually increases the voltage on C_{SS}. The high-side MOSFET switch will start switching when the voltage difference between the SS pin and the FB pin is larger than 400mV ($V_{SS} - V_{FB} > 400mV$, typical). If the output undervoltage condition remains, the high-side MOSFET switch stops switching when the voltage difference between the SS pin and the FB pin is 700mV ($V_{SS} - V_{FB} = 700mV$, typical) and then the I_{SS_DIS} discharging current source begins to discharge C_{SS}.

Upon completion of the soft-start sequence, if the output undervoltage condition is removed, the converter will resume normal operation. Otherwise, the auto-recovery cycle will be repeated until the output undervoltage condition is cleared.

Hiccup mode allows the circuit to operate safely with low input current and power dissipation, resuming normal operation as soon as the overload or short-circuit condition is removed. A short circuit protection and recovery profile is shown in Figure 3.

The C_{SS} will be discharged to 150mV when the RTQ2116A-QA enters output undervoltage protection. The first discharge time (t_{SS_DIS1}) can be calculated as follows:

$$t_{SS\_DIS1} = C_{SS} \times \frac{V_{SS} - 0.15}{I_{SS\_DIS}}$$

The equation below assumes that the V_{FB} will be 0 under short-circuit conditions and it can be used to calculate the C_{SS} discharge time (t_{SS_DIS2}) and charging time (t_{SS_CH}) during hiccup mode.

$$t_{SS\_DIS2} = C_{SS} \times \frac{0.55}{I_{SS\_DIS}}$$

$$t_{SS\_CH} = C_{SS} \times \frac{0.55}{I_{SS\_CH}}$$

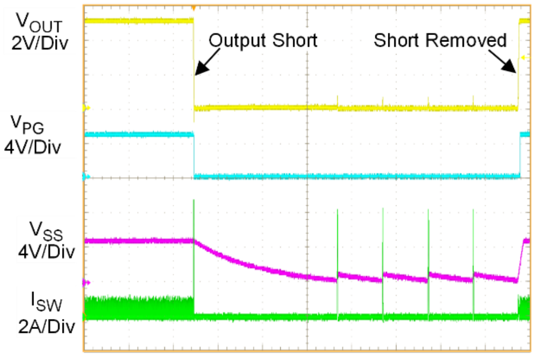


Figure 3. Short Circuit Protection and Recovery

15.15 Over-Temperature Protection

The RTQ2116A-QA includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds the Over-Temperature Protection threshold T_{OTP}. Once the junction temperature cools down by the Over-Temperature Protection hysteresis (ΔT_{OTP_HYS}), the IC will resume normal operation with a complete soft-start.

15.16 Pin-Short Protection

The RTQ2116A-QA provides pin-short protection for neighbor pins. The internal protection fuse will be burned out to prevent IC smoke, fire and spark when the BOOT pin is shorted to the VIN pin.

15.17 DS+ DS- Overvoltage Protection

The RTQ2116A-QA includes a data overvoltage protection function against the condition that DS+ or DS- suffers high voltage. When the voltage at DS+ or DS- is over protection trip threshold, 3.85V (typical), the PG will be pulled low after 100μs. It is maintained until the voltage is lower than the threshold. Then, the PG is released after 100μs. When the RTQ2116A-QA detects the rising edge of V_{PG}, the VOUT/VBUS will be reset for 400ms. This behavior will let charged devices re-attach and start the charging detection operation again. The sequence is shown in Figure 4.

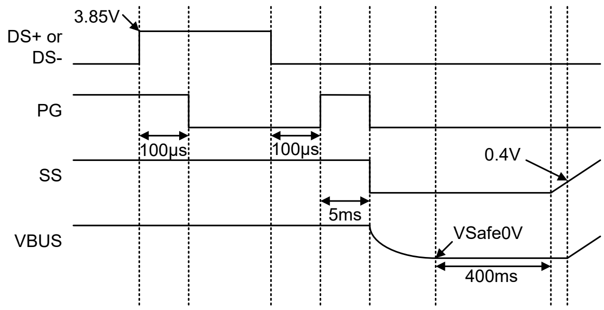


Figure 4. Data Overvoltage Protection Sequence

16 Application Information

(Note 8)

A general RTQ2116A-QA application circuit is shown in the Typical Application Circuit section. External component selection is primarily determined by the load requirements and begins with the selection of the operating mode by setting the MODE/SYNC pin voltage and the operating frequency using the external resistor RT. Next, choose the inductor L, input capacitor C_{IN}, and output capacitor C_{OUT}. Then, select the feedback resistors and compensation circuit to set the desired output voltage and crossover frequency. The internal regulator capacitor C_{VCC}, and the bootstrap capacitor C_{BOOT} can be selected. Finally, the remaining optional external components can be selected for functions such as the EN, external soft-start, PG, inductor peak current limit, synchronization, spread spectrum, average current limit, and adjustable output voltage with cable drop compensation.

16.1 FPWM/PSM Selection

The RTQ2116A-QA provides a MODE/SYNC pin for Forced-PWM Mode (FPWM) and Power Saving Mode (PSM) operation selection at light load. To optimize efficiency at light loads, the RTQ2116A-QA can be set in PSM. The $V_{MODE/SYNC}$ is held below a logic-low threshold voltage (V_{IL_SYNC}) of the MODE/SYNC input, that is, with the MODE/SYNC pin floating or pull low, the RTQ2116A-QA operates in PSM at light load to improve light load efficiency. If it is necessary to keep switching harmonics out of the signal band, the RTQ2116A-QA can operate in FPWM. The RTQ2116A-QA is locked in PWM mode when $V_{MODE/SYNC}$ rises above a logic-high threshold voltage (V_{IH_SYNC}) of the MODE/SYNC input. The FPWM trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, fast transient response, and constant switching frequency.

16.2 Switching Frequency Setting

The RTQ2116A-QA offers adjustable switching frequency setting and the switching frequency can be set by using external resistor RT. The switching frequency range is from 300kHz to 2.2MHz. Selecting the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge and transition losses, but requires larger inductance values and/or capacitance to maintain low output ripple voltage. An additional constraint on operating frequency is the minimum on-time and minimum off-time. The minimum on-time, t_{ON_MIN}, is the smallest duration of time in which the high-side switch can be in its “on” state. This time is 60ns (typical). In continuous mode operation, the minimum on-time limit imposes a maximum operating frequency, f_{SW_MAX}, of:

$$f_{SW\_MAX} = \frac{V_{OUT}}{t_{ON\_MIN} \times V_{IN\_MAX}}$$

where V_{IN_MAX} is the maximum operating input voltage. The minimum off-time, t_{OFF_MIN}, is the shortest period that the RTQ2116A-QA is capable of turning on the low-side MOSFET switch, tripping the current comparator and turning the MOSFET switch back off. The minimum off time is 65ns (typical). If the switching frequency should be constant, the required off time needs to be larger than the minimum off time. The minimum off time, considering loss terms, can be calculated as follows:

$$t_{OFF\_MIN} \le \frac{1 - \left[\dfrac{V_{OUT} + I_{OUT\_MAX} \times \left(R_{DS(ON)\_L} + R_L\right)}{V_{IN\_MIN} - I_{OUT\_MAX} \times \left(R_{DS(ON)\_H} - R_{DS(ON)\_L}\right)} \right]}{f_{SW}}$$

where $R_{DS(ON)\_H}$ is the on resistance of the high-side MOSFET switch; $R_{DS(ON)\_L}$ is the on resistance of the low-side MOSFET switch; R_L is the DC resistance of the inductor.

The switching frequency f_{SW} is set by connecting an external resistor R_{RT} between the RT pin and GND. The failure modes and effects analysis (FMEA) consideration is applied to the RT pin to avoid abnormal switching frequency operation under failure conditions. It includes failure scenarios of short-circuit to GND and the pin is left open. The switching frequency will be 2.35MHz (typical) when the RT pin is shorted to GND. The switching frequency will be 250kHz (typical) when the pin is left open. The equation below shows the relationship between the setting frequency and the R_{RT} value.

$$R_{RT(k\Omega)} = 74296 \times fsw^{-1.06}$$

where f_{SW} (kHz) is the desire setting frequency. It is recommended to use resistors with 1% tolerance or better and a temperature coefficient of 100 ppm or less. Figure 5 shows the relationship between switching frequency and the R_{RT} resistor.

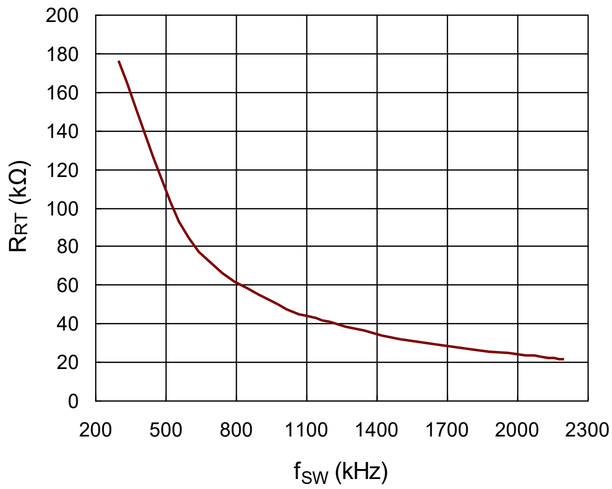


Figure 5. Switching Frequency vs. R_{RT} Resistor

16.3 Inductor Selection

The inductor selection makes trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the RTQ2116A-QA : inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determine the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. This results in additional phase lag in the loop and reduces the crossover frequency. As the ratio of the slope-compensation ramp to the sensed-current ramp increases, the current-mode system tilts towards voltage-mode control. Lower inductance values allow for smaller case size, but the increased ripple lowers the effective current-limit threshold, increases the AC losses in the inductor and may trigger the low-side switch sinking current limit in FPWM. It also causes insufficient slope compensation and ultimately loop instability as the duty cycle approaches or exceeds 50%. When the duty cycle exceeds 50%, the following condition needs to be satisfied:

$$2.1 \times f_{SW} > \frac{V_{OUT}}{L}$$

A good compromise among size, efficiency, and transient response can be achieved by setting an inductor current ripple (ΔI_L) with about 10% to 50% of the maximum rated output current (3A).

To enhance efficiency, choose a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The inductor value determines not only the ripple current but also the load-current value at which DCM/CCM switchover occurs. The inductor selected should have a saturation current rating greater than the peak current limit of the RTQ2116A-QA. The core must be large enough to avoid saturation at the peak inductor current (I_{L_PEAK}):

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2}\Delta I_L$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the RTQ2116A-QA. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current. It is recommended to use shielded inductors for good EMI performance.

16.4 Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to do this without causing a large variation in the input voltage. The peak-to-peak voltage ripple on the input capacitor can be estimated using the following equation:

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + ESR \times I_{OUT}$$

where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

For ceramic capacitors, the equivalent series resistance (ESR) is very low, the ripple caused by ESR can be ignored, and the minimum value of effective input capacitance can be estimated using the following equation:

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

Where $\Delta V_{CIN\_MAX} \leq 200mV$

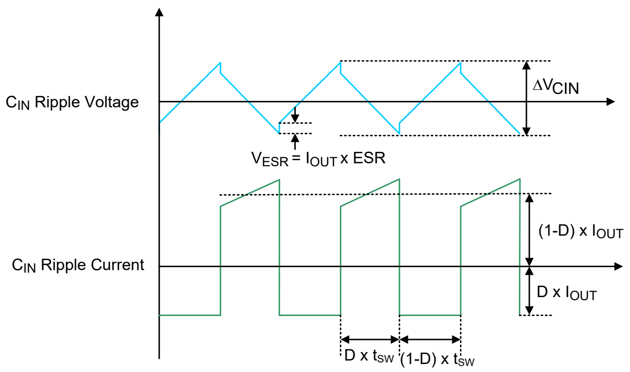


Figure 6. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current. The RMS ripple current (I_{RMS}) of the regulator can be determined using the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) as shown in the following equation:

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

From above, the maximum RMS input ripple current occurs at maximum output load, which will be used as the requirements to consider the current capabilities of the input capacitors. The maximum ripple voltage usually occurs at 50% duty cycle, that is, $V_{IN} = 2 \times V_{OUT}$. It is common to use the worse $I_{RMS} \cong 0.5 \times I_{OUT\_MAX}$ at $V_{IN} = 2 \times V_{OUT}$ for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications due to their small size, robustness, and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high-quality (underdamped) tank circuit. If the RTQ2116A-QA circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the RTQ2116A-QA's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pin, with a low inductance connection to the PGND of the IC. It is recommended to connect a 4.7μF, X7R capacitors between the VIN pin to the PGND pin for 2.1MHz switching frequency. A larger input capacitance is required when a lower switching frequency is used. For filtering high frequency noise, an additional small capacitor 0.1μF should be placed close to the part and the capacitor should be in 0402 or 0603 package size. X7R capacitors are recommended for best performance across temperature and input voltage variations.

16.5 Output Capacitor Selection

The selection of C_{OUT} is determined by considering to satisfy the voltage ripple and the transient loads. The peak-to-peak output voltage ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} = \Delta I_L \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right)$$

where the ΔI_L is the peak-to-peak inductor ripple current. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding transient loads, the V_{SAG} and V_{SOAR} requirements should be taken into consideration for choosing the effective output capacitance value. The amount of output sag/soar is a function of the crossover frequency factor at PWM, which can be calculated as follows:

$$V_{SAG} = V_{SOAR} = \frac{\Delta I_{OUT}}{2 \times \pi \times C_{OUT} \times f_C}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. The recommended dielectric type of the capacitor is X7R, as it provides the best performance across temperature and input voltage variations. The variation of the capacitance value with temperature, DC bias voltage, and switching frequency needs to be taken into consideration. For example, the capacitance of a capacitor decreases as the DC bias across the capacitor increases. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

Transient performance can be improved with a higher value output capacitor. Increasing the output capacitance will also decrease the output voltage ripple.

16.6 Output Voltage Programming

The output voltage can be programmed using a resistive divider from the output to ground, with the midpoint connected to the FB pin. The resistive divider allows the FB pin to sense a fraction of the output voltage, as shown in Figure 7. The output voltage is set according to the following equation:

$$V_{OUT} = V_{REF\_CV} \times \left(1 + \frac{R1}{R2}\right)$$

where the reference voltage of constant voltage control V_{REF_CV}, is 0.8V (typical).

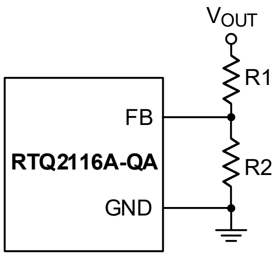


Figure 7. Output Voltage Setting

The placement of the resistive divider should be within 5mm of the FB pin. The resistance of R2 is not larger than 170kΩ for noise immunity consideration. The resistance of R1 can then be obtained as below:

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF\_CV})}{V_{REF\_CV}}$$

For better output voltage accuracy, the divider resistors (R1 and R2) with ±1% tolerance or better should be used. Note that the resistance of R1 relates to cable drop compensation setting. The resistance of R1 should be designed to match the needs of the voltage drop application, see the adjustable output voltage with cable drop compensation section.

16.7 Compensation Network Design

The purpose of loop compensation is to ensure stable operation while maximizing the dynamic performance. An undercompensated system may result in unstable operations. Typical symptoms of an unstable power supply include: audible noise from the magnetic components or ceramic capacitors, jittering in switching waveforms, oscillation of output voltage, and overheating of power MOSFETs.

In most cases, the peak current mode control architecture used in the RTQ2116A-QA only requires two external components to achieve a stable design as shown in Figure 8. The compensation can be selected to accommodate any capacitor type or value. The external compensation also allows the user to set the crossover frequency and optimize the transient performance of the RTQ2116A-QA . Around the crossover frequency, the peak current mode control (PCMC) equivalent circuit of buck converter can be simplified, as shown in Figure 9. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the RTQ2116A-QA . Since the slope compensation is ignored, the actual cross over frequency will usually be lower than the crossover frequency used in the calculations. It is always necessary to make a measurement before releasing the design for final production. Although the models of power supplies are theoretically correct, they cannot take full account of circuit parasitic and component nonlinearity, such as the ESR variations of output capacitors, then nonlinearity of inductors and capacitors. Also, circuit PCB noise and limited measurement accuracy may also cause measurement errors. A Bode plot is ideally measured with a network analyzer. Alternatively, the Richtek application note DC/DC Converter Testing with Fast Load Transient provides a quick and easy method to check stability. Generally, the compensation components can be calculated using the following steps:

1. Set the crossover frequency, fc. For stability , the target is to have a loop gain slope that is –20dB/decade from a very low frequency to beyond the crossover frequency. In general, one-twentieth to one- tenth of the switching frequency (5% to 10% of f_{SW}) is recommended to be the crossover frequency. Do “NOT” design the crossover frequency over 80kHz when the switching frequency is larger than 800kHz. For dynamic purposes, a higher bandwidth results in a faster load transient response. The downside of high bandwidth is that it increases the regulator’s susceptibility to board noise which ultimately leads to excessive falling edge jitter at the switch node voltage.
2. R_{COMP} can be determined by:

$$R_{COMP} = \frac{2\pi \times f_C \times V_{OUT} \times C_{OUT}}{gm \times V_{REF\_CV} \times gm\_cs} = \frac{2\pi \times f_C \times C_{OUT}}{gm \times gm\_cs} \times \frac{R1 + R2}{R2}$$

where

gm is the error amplifier gain of trans-conductance (950μA/V)

gm_cs is COMP to current sense (5.6A/V)

3. A compensation zero can be placed at or before the dominant pole of the buck converter, which is provided by the output capacitor and the maximum output loading (R_L). Calculate C_{COMP}:

$$C_{COMP} = \frac{R_L \times C_{OUT}}{R_{COMP}}$$

4. The compensation pole is set to the frequency at the ESR zero or 1/2 of the operating frequency. The output capacitor and its ESR provide a zero, and optional CCOMP2 can be used to cancel this zero

$$C_{COMP2} = \frac{R_{ESR} \times C_{OUT}}{R_{COMP}}$$

If 1/2 of the operating frequency is lower than the ESR zero, the compensation pole is set at 1/2 of the operating frequency.

$$C_{COMP2} = \frac{1}{2 \times \pi \times \frac{f_{SW}}{2} \times R_{COMP}}$$

Note 7. Generally, C_{COMP2} is an optional component to be used to enhance noise immunity.

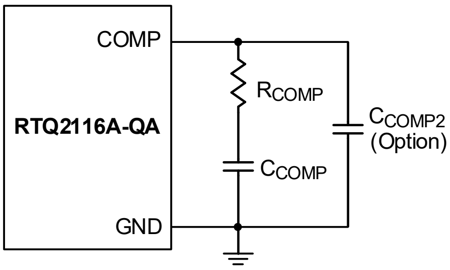


Figure 8. External Compensation Components

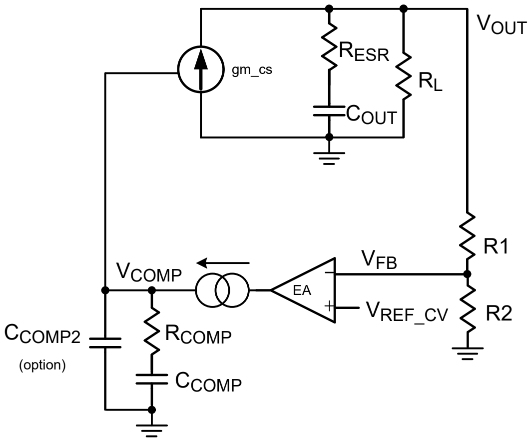


Figure 9. Simplified Equivalent Circuit of Buck with PCMC

16.8 Bootstrap Driver Supply

The bootstrap capacitor (C_{BOOT}) between the BOOT pin and the SW pin is used to create a voltage rail above the applied input voltage, VIN. Specifically, the bootstrap capacitor is charged through an internal diode to a voltage approximately equal to V_{CC} each time the low-side switch turns on. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle. For most applications a 0.1μF, 0603 ceramic capacitor with X7R is recommended and the capacitor should have a 6.3 V or higher voltage rating.

16.9 External Bootstrap Diode (Option)

It is recommended to add an external bootstrap diode between an external 5V voltage supply and the BOOT pin to improve enhancement of the high-side switch and improve efficiency when the input voltage is below 5.5V The recommended application circuit is shown in Figure 10. The bootstrap diode can be a low-cost one, such as 1N4148 or BAT54. The external 5V can be a fixed 5V voltage supply from the system, or a 5V output voltage generated by the RTQ2116A-QA . Note that the $V_{BOOT-SW}$ must be lower than 5.5V. Figure 11 shows efficiency comparison with and without Bootstrap Diode.

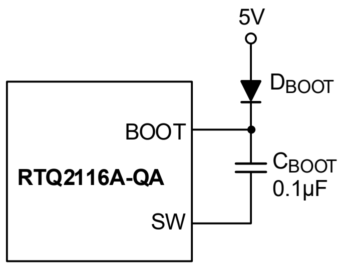


Figure 10. External Bootstrap Diode

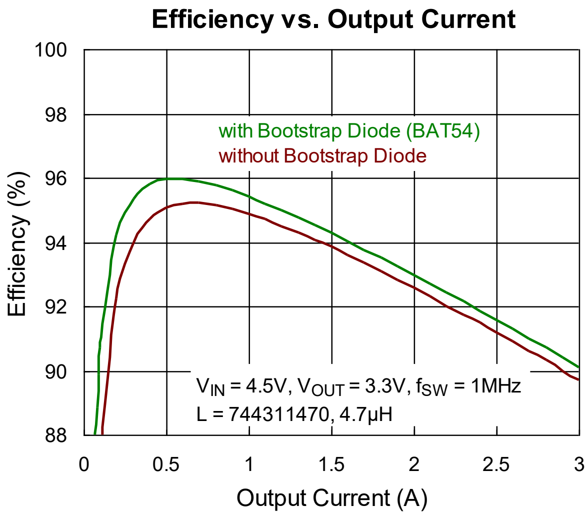


Figure 11. Efficiency Comparison with and without Bootstrap Diode

16.10 External Bootstrap Resistor (Option)

The gate driver of an internal power MOSFET, utilized as a high-side switch, is optimized for turning on the switch not only fast enough for reducing switching power loss, but also slow enough for minimizing EMI. The EMI issue is worse when the switch is turned on rapidly due to high di/dt noises induced. When the high-side switch is being turned off, the SW node will be discharged relatively slowly by the inductor current due to the presence of the dead time when both the high-side and low-side switches are turned off.

In some cases, it is desirable to reduce EMI further, even at the expense of some additional power dissipation. The turn-on rate of the high-side switch can be slowed by placing a small bootstrap resistor R_{BOOT} between the BOOT pin and the external bootstrap capacitor, as shown in Figure 12. The recommended range for the R_{BOOT} is several ohms to 10 ohms and it can be 0402 or 0603 in size.

This will slow down the rates of the high-side switch turn-on and the rise of V_{SW}. In order to improve EMI performance and enhancement of the internal MOSFET switch, the recommended application circuit is shown in Figure 13, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} being placed between the BOOT pin and the capacitor/diode connection.

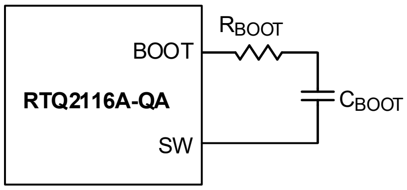


Figure 12. External Bootstrap Resistor at the BOOT Pin

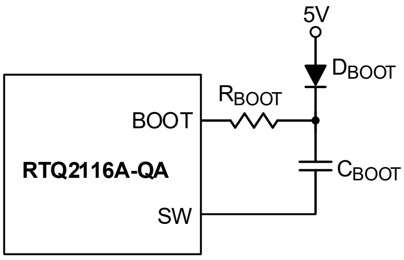


Figure 13. External Bootstrap Diode and Resistor at the BOOT Pin

16.11 EN Pin for Start-Up and Shutdown Operation

For automatic start-up, the EN pin, with high-voltage rating, can be connected to the input supply V_{IN} directly. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. To have an additional delay, the EN pin can be externally connected to V_{IN} by adding a resistor R_{EN} and a capacitor C_{EN}, as shown in Figure 14. The time delay can be calculated with the EN's internal threshold, at which switching operation begins (typically 1.25V).

An external MOSFET can be added for the EN pin to be logic-controlled, as shown in Figure 15. In this case, a pull-up resistor, R_{EN}, is connected between VIN and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin. To prevent the RTQ2116A-QA being enabled when V_{IN} is smaller than the V_{OUT} target level or some other desired voltage level, a resistive divider (R_{EN1} and R_{EN2}) can be used to externally set the input undervoltage-lockout threshold, as shown in Figure 16.

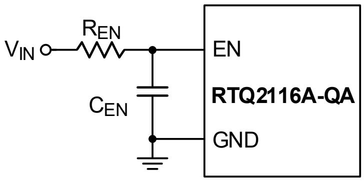


Figure 14. Enable Timing Control

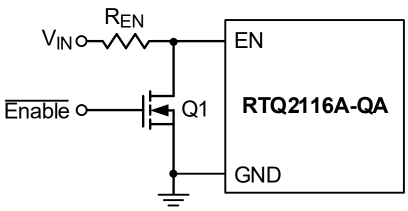


Figure 15. Logic Control for the EN Pin

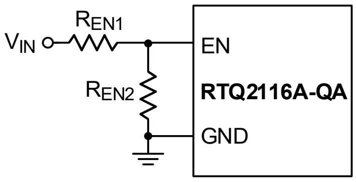


Figure 16. Resistive Divider for Undervoltage-lockout Threshold Setting

16.12 Soft-Start

The RTQ2116A-QA provides an adjustable soft-start function, which helps prevent large inrush current while the converter is powered-up. For the RTQ2116A-QA, the soft-start timing can be programmed by connecting the external capacitor C_{SS} between the SS pin and GND. An internal current source I_{SS} (6μA) charges an external capacitor to build a soft-start ramp voltage. The V_{FB} will track the internal ramp voltage during soft-start interval. The typical soft-start time (t_{SS}) for V_{OUT} to rise from zero to 90% of its set value, can be calculated as follows:

$$t_{SS} = C_{SS} \times \frac{0.8}{I_{SS}}$$

If a heavy load is added to the output with large capacitance, the output voltage will never enter regulation because of UVP. Thus, the RTQ2116A-QA remains in hiccup operation. The C_{SS} should be large enough to ensure soft-start period ends after C_{OUT} is fully charged.

$$C_{SS} \geq C_{OUT} \times \frac{I_{SS} \times V_{OUT}}{0.8 \times I_{COUT\_CHG}}$$

where I_{COUT_CHG} is the C_{OUT} charge current, which is related to the switching frequency, inductance, high-side MOSFET switch peak current limit, and load current.

16.13 Power-Good Output

The PG pin is an open-drain power-good indication output and is to be connected to an external voltage source through a pull-up resistor.

The external voltage source can be an external voltage supply below 5.5V, V_{CC} or the output of the RTQ2116A-QA if the output voltage is regulated under 5.5V. It is recommended to connect a 100kΩ between an external voltage source to PG pin.

16.14 Inductor Peak Current Limit Setting

The current limit of high-side MOSFET switch is adjustable by an external resistor connected to the RLIM pin. The recommended resistor value ranges from 33kΩ (for a typical 5.5A) to 91kΩ (for a typical 2.2A) and it is recommended to use 1% tolerance or better and temperature coefficient of 100 ppm or less resistors. When the inductor current reaches the current-limit threshold, the COMP voltage will be clamped to limit the inductor current. Inductor current ripple current also should be considered into the current limit setting. It recommends to set the current limit minimum to 1.2 times the peak inductor current. Current limit minimum value can be calculated as below:

Current limit minimum = ($I_{OUT(MAX)}$ + 1/2 inductor current ripple) x 1.2. Through external resistor R_{LIM} connects to the RLIM pin to set the current limit value.

The current limit value below offers the approximate formula equation:

$$R_{LIM}(k\Omega) = \frac{178.8}{I_{SET} - 0.2531} - 1$$

where I_{SET} is the desired current limit value (A)

The failure modes and effects analysis (FMEA) consideration is also applied to the RLIM pin setting to avoid abnormal current limit operation at failure condition. It includes failure scenarios of short-circuit to GND and the pin is left open. The inductor peak current limit will be 6.2A (typical) when the RLIM pin short to GND and 1.4A (typical) when the pin is left open. Note that the inductor peak current limit variation increases as the tolerance of R_{LIM} resistor increases. As the R_{LIM} resistor value is small, the inductor peak current limit will probably be operated as the RLIM pin short to GND, and vice versa. The R_{LIM} resistance variation range is limited from 30kΩ to 100kΩ to eliminate the undesired inductor peak current limit. When choosing an R_{LIM} outside the recommended range, make sure that there is no problem by evaluating it with real machine.

16.15 Synchronization

The RTQ2116A-QA can be synchronized with an external clock ranging from 300kHz to 2.2MHz which is applied to the MODE/SYNC pin. The external clock duty cycle must be from 20% to 80% and amplitude should have valleys that are below V_{IL_SYNC} and peaks above V_{IH_SYNC} (up to 6V). The RTQ2116A-QA will not enter PSM operation at light load while synchronized to an external clock, but instead will operate in FPWM to maintain regulation.

16.16 Average Current Limit

The RTQ2116A-QA implements Constant Current Control to achieve average current limit. The constant current of CC mode control is set by external sense resistance (R_{SENSE}).

The average current is set according to the following equation:

$$\text{Average Current Limit} = \frac{V_{REF\_CC}}{R_{SENSE}}$$

where the reference voltage of constant current regulation V_{REF_CC}, is 100mV (typical) and the V_{REF_CC} variation is around ±10%. The average current limit function is recommended to operate with CSP/CSN voltages range from 3.3 V to 6V.

16.17 Adjustable Output Voltage with Cable Drop Compensation

The RTQ2116A-QA provides cable drop compensation function at CV regulation. If the trace from the RTQ2116A-QA output terminator to the load is too long, there will be a voltage drop on the long trace which is variable with load current. The RTQ2116A-QA is capable of compensating the output voltage drop to keep a constant voltage at load, whatever the load current is.

The compensation voltage (V_{O_OFFSET}) is based on cable drop compensation current (I_{LC}) and divide upper side resistor R1, which can be calculated as following formula:

$$V_{O\_OFFSET} = I_{LC} \times R1$$

The cable drop compensation current variation is ±10%, and it is a function of current sense voltage (V_{CS}):

$$I_{LC}(\mu A) = 21 \times (V_{CS} - 0.00476)$$

where current sense voltage is the voltage difference between the CSP pin and the CSN pin, that is the voltage across a current sense resistor (R_{SENSE}). Figure 17 shows the relationship between cable drop compensation current (I_{LC}) and V_{CS}.

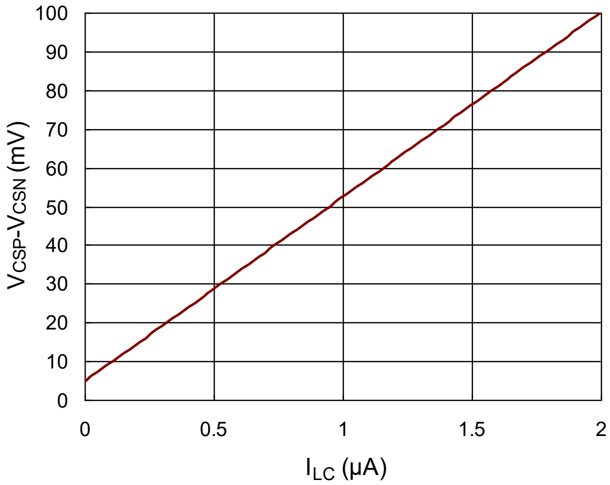


Figure 17. I_{LC} vs. $V_{CSP} - V_{CSN}$

According to the formula above, the desired compensation voltage which is set at rated output current can be calculated as below

$V_{O\_OFFSET} = 21 \times (R_{SENSE} \times I_{OUT} - 0.00476) \times 10^{-6} \times R1$ Where I_{OUT} is the rated output current.

Choose the R_{SENSE} with rated load current and reserve some de-rating margin for better thermal and life consideration. In order to avoid the undesired CC control loop interruption, the current sense voltage is selected should be the lower value of 100mV. If the system implements constant current control to achieve average current limit, the R_{SENSE} is set based on the average current limit equation.

Considering CV regulation with cable drop compensation situation, the desire cable drop compensation is 0.24V at rated 2.4A loading and R_{SENSE} is selected as 34mΩ, the R1 can be calculated as below:

$$R1 = \frac{V_{O\_SFFSET}}{21 \times (R_{SENSE} \times I_{OUT} - 0.00476) \times 10^{-6}} = 148.7k\Omega$$

Select 147kΩ for R1. The resistance of R2 can then be obtained as below:

$$R2 = \frac{R1 \times V_{REF\_CV}}{V_{OUT} - V_{REF\_CV}} = 28k\Omega$$

In this case, 147kΩ is available for resistance of R1 and 28kΩ is available for resistance of R2. The R1 and R2 values can be calculated based on above equation. If the R1 and R2 values are too high, the regulator will be more susceptible to noise and voltage errors from the FB input current will be noticeable. Make sure the current flowing through the FB resistive divider is larger than 5×10^{-6}. In addition, a feed-forward capacitor C_{FF} may be required to improve output voltage ripple at PSM.

The power dissipation on sensing resistor will be:

$$P_{RSENSE} = R_{SENSE} \times I_{OUT}^2 = 306mW$$

Choose current sense resistor power rated with 50% de-rating rule of thumb for better heat and life consideration, 1W size is well enough for this case. Hence, the 34mΩ, 1W size R_{SENSE} is determined and with aid of the cable drop compensation feature, the RTQ2116A-QA can compensate the 0.24V voltage drop to maintain excellent output voltage accuracy at rated 2.4A load current. Note that the R_{SENSE} should be connected as close to the

CSP/CSN with short, direct traces, creating Kelvin connection to ensure that noise and current sense voltage errors do not corrupt the differential current sense signals between the CS and VOUT pins. The cable drop compensation function is recommended to operate with CSP/CSN voltages range from 3.3 V to 6V.

16.18 DCP Auto Mode

The DCP Auto Mode only provides power but does not support data connection to an upstream port. The RTQ2116A-QA integrates an auto-detect state machine.

that supports all the DCP charging schemes listed below:

- Shorted
- Divider 3
- 1.2V shorted

Shorted mode complies with BC1.2 DCP and Chinese Telecommunications Industry Standard YD/T 1591-2009, defining that the D+/D- data lines should be shorted together with a maximum series impedance of 200Ω.

In Divider3 charging scheme, the device applies 2.7V/2.7V to D+/D- data lines.

1.2V shorted charging scheme applies 1.2V to the shorted D+/D- data lines.

The DCP auto mode starts in Divider 3 Mode, however if a BC1.2 or YD/T 1591-2009 compliant device is attached, it responds by operating in BC1.2 shorted mode briefly then moves to 1.2V shorted mode.

16.19 Thermal Considerations

In many applications, the RTQ2116A-QA does not generate much heat due to its high efficiency and low thermal resistance of its WET-WQFN-32L 5x5 package. However, in applications in which the RTQ2116A-QA is running at a high ambient temperature and high input voltage or high switching frequency, the generated heat may exceed the maximum junction temperature of the part.

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the RTQ2116A-QA. If the junction temperature reaches approximately 175°C, the RTQ2116A-QA stop switching the power MOSFETs until the temperature drops about 15°C cooler.

The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA(EFFECTIVE)}$$

where $T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 150°C. T_A is the ambient operating temperature, $\theta_{JA(EFFECTIVE)}$ is the system-level junction to ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system.

The RTQ2116A-QA thermal resistance depends strongly on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance.

Experiments in the Richtek thermal lab show that simply setting $\theta_{JA(EFFECTIVE)}$ as 110% to 120% of the θ_{JA} is reasonable to obtain the allowed $P_{D(MAX)}$.

As an example, consider the case when the RTQ2116A-QA is used in applications where V_{IN} = 12V, I_{OUT} = 2.4A, f_{SW} = 2100kHz, V_{OUT} = 5V. The efficiency at 5V, 2.4A is 89% by using Cyntec-VCHA075D-2R2MS6 (2.2μH, 9.5mΩ DCR) as the inductor and measured at room temperature. The core loss can be obtained from its website of 18.8mW in this case. In this case, the power dissipation of the RTQ2116A-QA is

$$P_{D,\,RT} = \frac{1-\eta}{\eta} \times P_{OUT} - \left(I_O^2 \times DCR + P_{CORE}\right) = 1.41W$$

Considering the $\theta_{JA(EFFECTIVE)}$ is 50.9°C/W by using the RTQ2116A-QA evaluation board with 4 layers PCB, 1OZ for all layers. the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

$$T_J = 1.41W \times 50.9°C/W + 25°C = 96.7°C$$

Figure 18 shows the RTQ2116A-QA R_{DSON} versus different junction temperature. If the application calls for a higher ambient temperature, we might recalculate the RTQ2116A-QA power dissipation and the junction temperature based on a higher R_{DSON} since it increases with temperature.

Using 50°C ambient temperature as an example, the change of the equivalent R_{DSON} can be obtained from Figure 18 and yields a new power dissipation of 1.467W. Therefore, the estimated new junction temperature is

$$T_J' = 1.467W \times 50.9°C/W + 50°C = 124.7°C$$

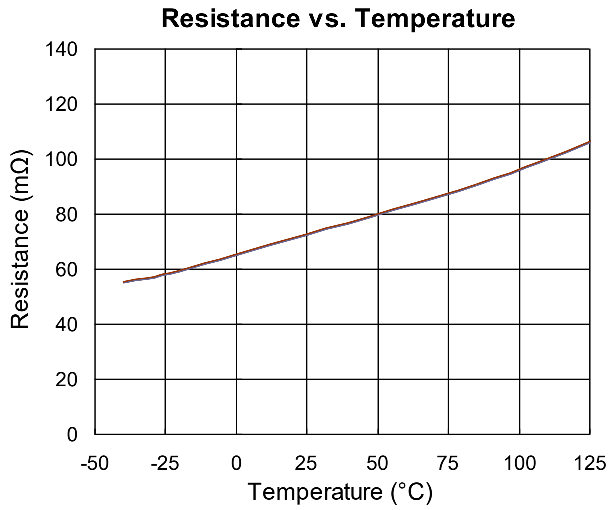


Figure 18. Resistance Variation Curve at Different Temperature

16.20 Layout Consideration

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RTQ2116A-QA :

- Four-layer or six-layer PCB with maximum ground plane is strongly recommended for good thermal performance.
- Keep the traces of the main current paths wide and short.
- Place high frequency decoupling capacitor C_{IN3} as close as possible to the IC to reduce the loop impedance and minimize switch node ringing.
- Place the C_{VCC} as close to VCC pin as possible.
- Place bootstrap capacitor, C_{BOOT}, as close to the IC as possible. Routing the trace with width of 20mil or wider.
- Place multiple vias under the RTQ2116A-QA near VIN and PGND and near input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the RTQ2116A-QA to additional ground planes within

the circuit board and on the bottom side.

- The high frequency switching nodes, SW and BOOT, should be as small as possible. Keep analog components away from the SW and BOOT nodes.
- Reducing the area size of the SW exposed copper to reduce the electrically coupling from this voltage.
- Connect the feedback sense network behind the via of the output capacitor.
- Place the feedback components near the IC.
- Place the compensation components near the IC.
- Connect all analog grounds to common node and then connect the common node to the power ground with a single point.
- Minimize current sense voltage errors by using Kelvin connection for PCB routing of the CSP pin, CSN pin and current sense resistor (R_{SENSE}).

Figure 19 to Figure 22 are the layout example.

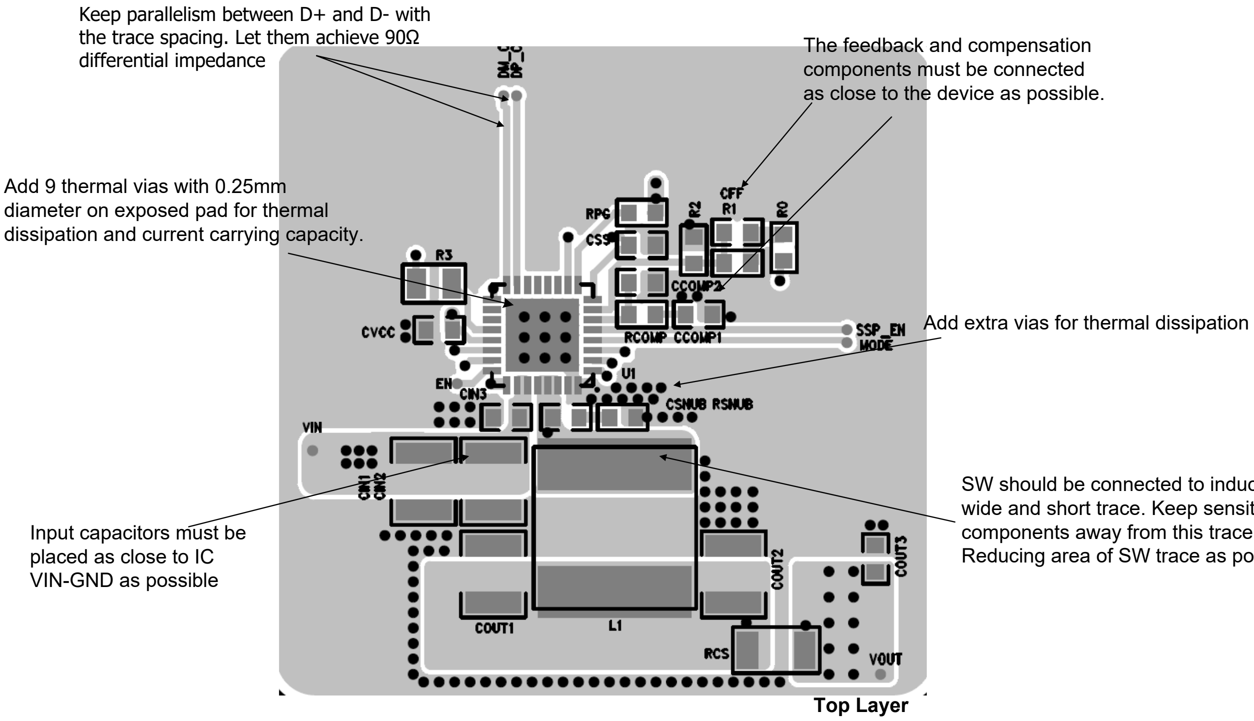


Figure 19. Layout Guide (Top Layer)

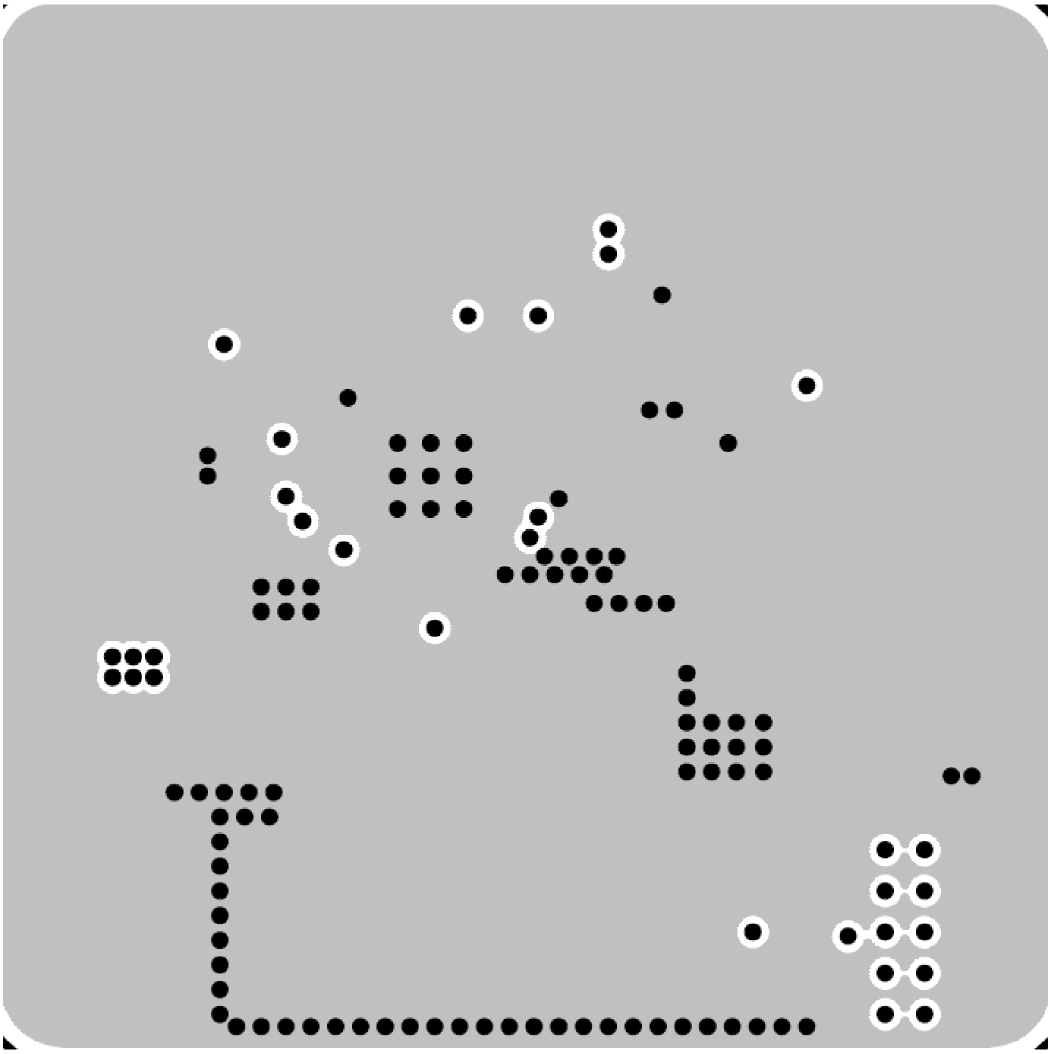


Figure 20. Layout Guide (2 Inner Layer)

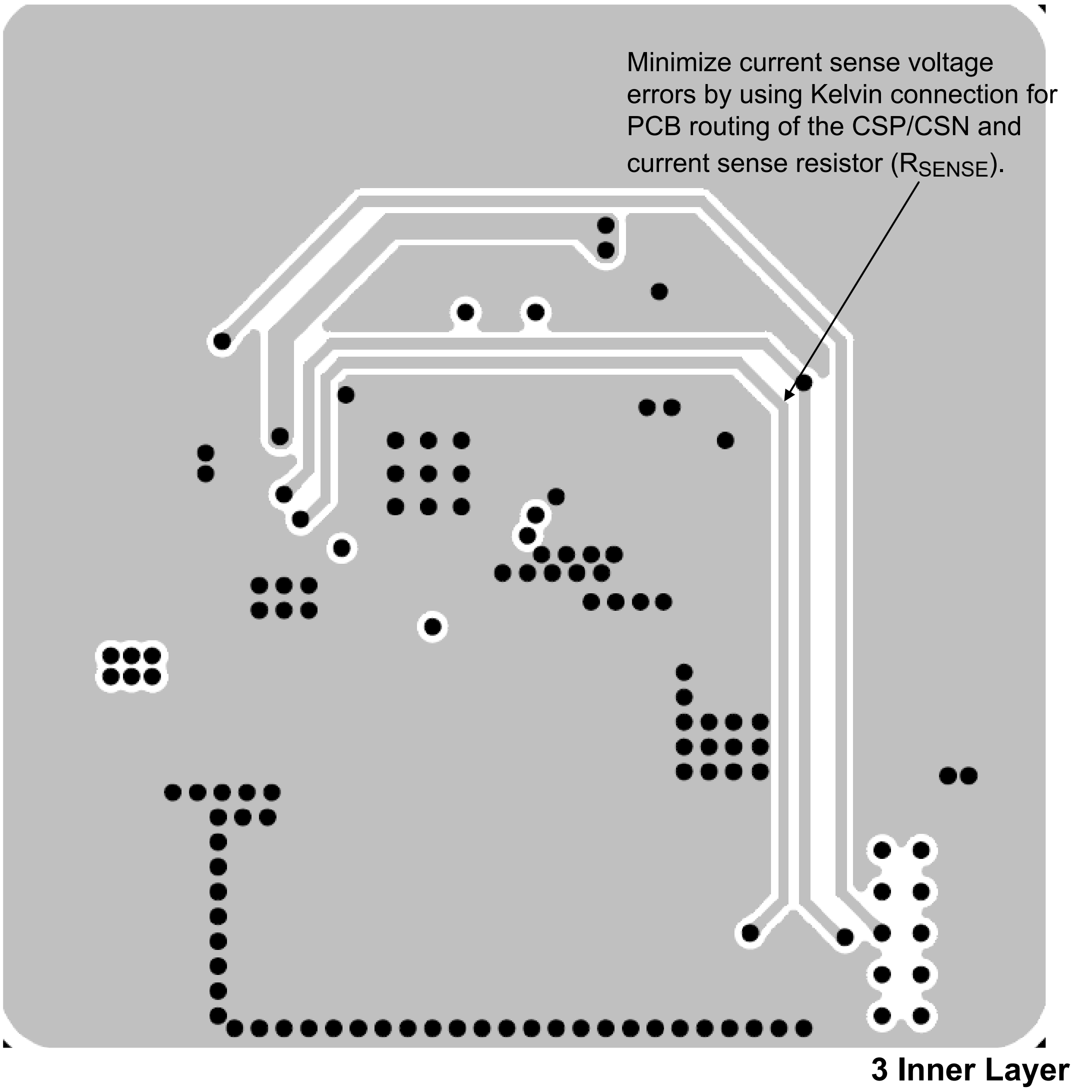


Figure 21. Layout Guide (3 Inner Layer)

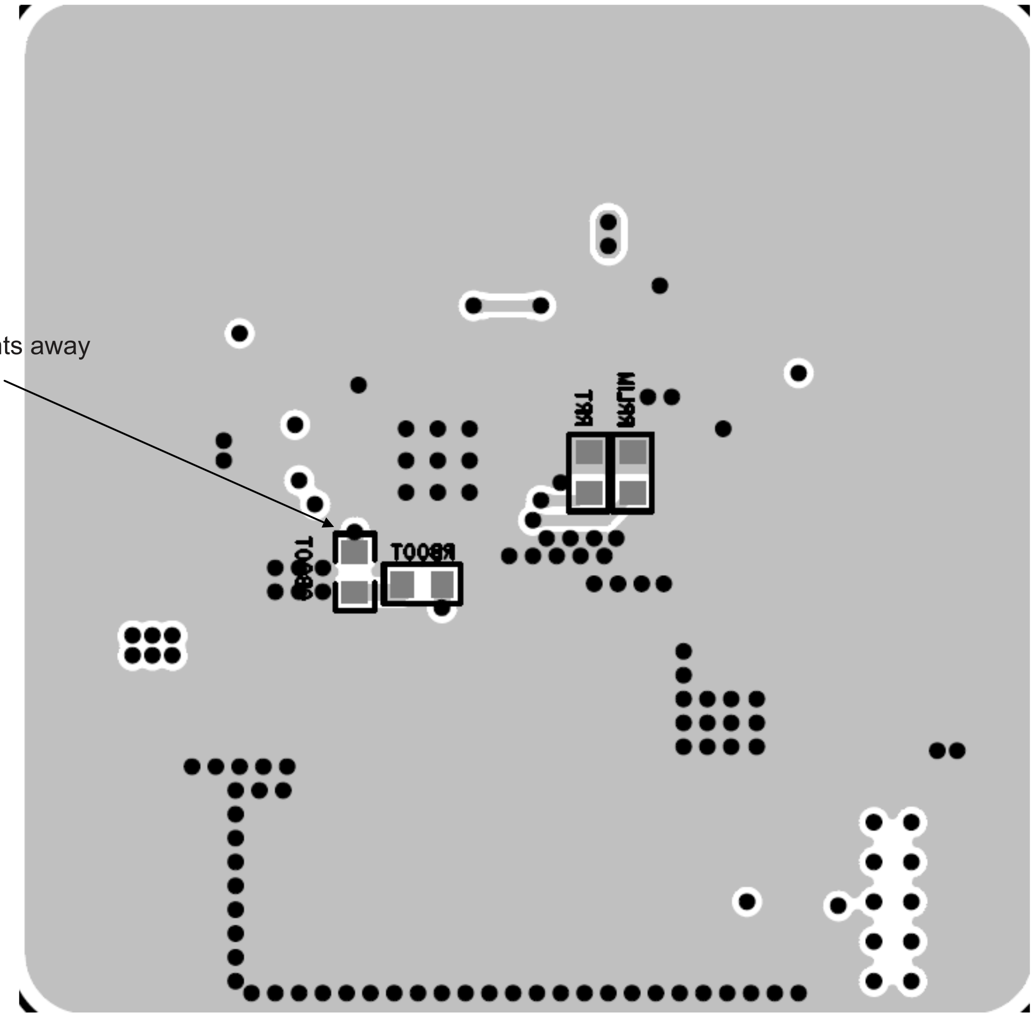
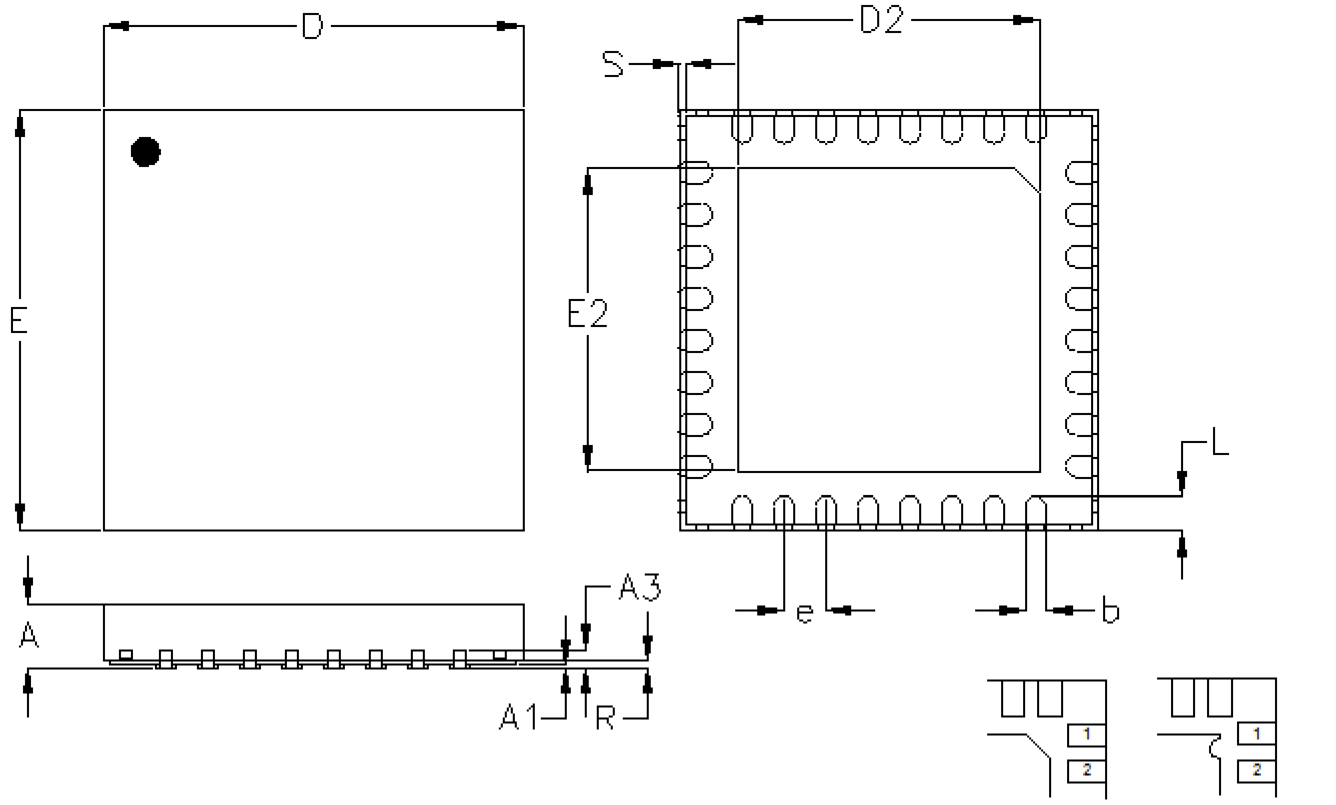


Figure 22. Layout Guide (Bottom Layer)

Note 8. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

17 Outline Dimension



DETAIL A

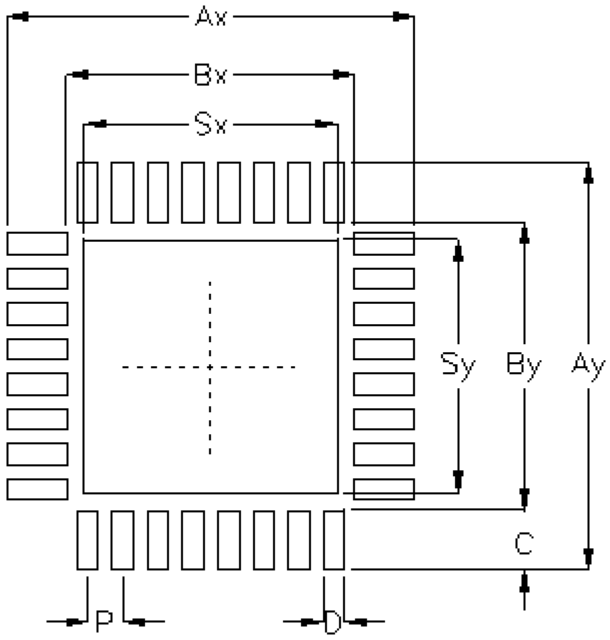
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	4.950	5.050	0.195	0.199
D2	3.550	3.650	0.140	0.144
E	4.950	5.050	0.195	0.199
E2	3.550	3.650	0.140	0.144
e	0.500		0.020	
L	0.350	0.450	0.014	0.018
R	0.050	0.150	0.002	0.006
S	0.001	0.090	0.000	0.004

WET W-Type 32L QFN 5x5 Package

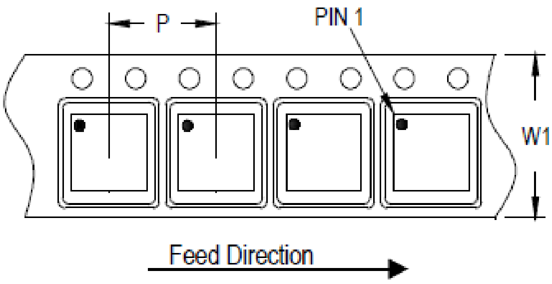
18 Footprint Information

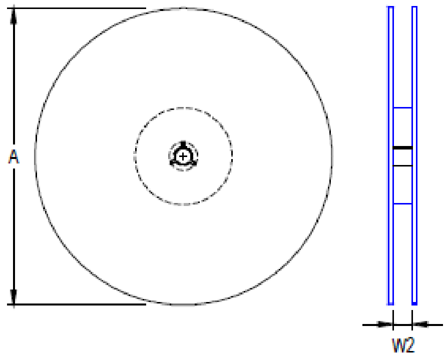


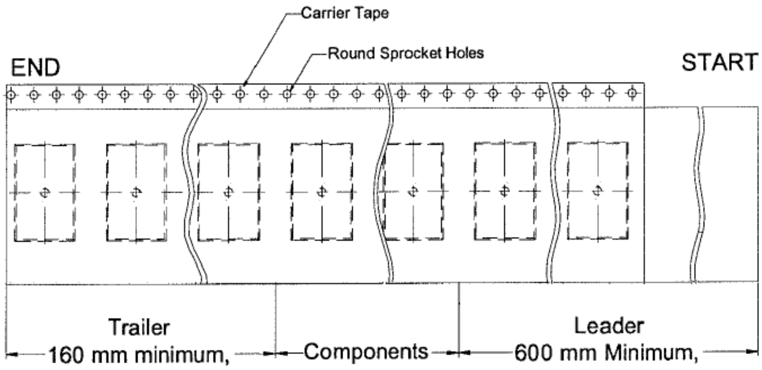
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
WET-V/W/U/XQFN5x5-32	32	0.50	5.80	5.80	4.10	4.10	0.85	0.30	3.60	3.60	±0.05

19 Packing Information

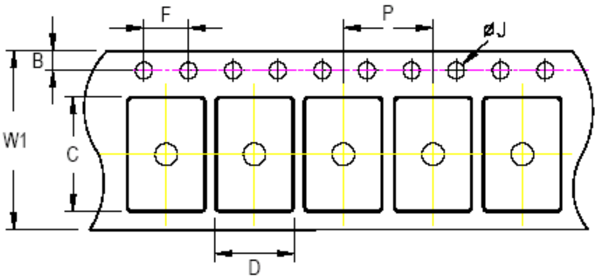
19.1 Tape and Reel Data

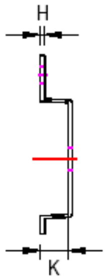






Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 5x5	12	8	180	7	1,500	160	600	12.4/14.4





C, D, and K are determined by component size.
The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN/DFN 5x5	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description
01	2026/3/16	Changed the names PGOOD to PG General Description Features Ordering Information Simplified Application Circuit - Added simplified application circuit Recommended Operating Conditions Electrical Characteristics Typical Application Circuit Operation Application Information Packing Information - Added packing information