1A, 36V, 2.1MHz Synchronous Step-Down Converter

General Description

The RTQ2131B is a 1A, high-efficiency, current mode synchronous step-down converter which is optimized for automotive applications. The device operates with input voltages from 3V to 36V and is protected from load dump transients up to 42V, eases input surge protection design. The device can program the output voltage between 0.8V to V_{IN}. The peak current mode control with simple external compensation allows the use of small inductors and results in fast transient response and good loop stability.

The RTQ2131B provides complete protection functions such as input under voltage lockout, output under voltage protection, over current protection, and thermal shutdown. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. The RTQ2131B is available in WDFN-10SL 3x3 (Exposed Pad) package.

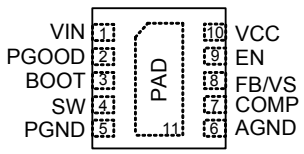
The recommended junction temperature range is –40°C to 150°C.

Applications

- Automotive Systems
- Car Camera Module and Car Cockpit Systems
- Connected Car Systems
- Point of Load Regulator in Distributed Power Systems
- Digital Set Top Boxes
- Broadband Communications

Pin Configuration

(TOP VIEW)



WDFN-10SL 3x3

Features

- **AEC-Q100 Grade 1 Qualified**
- **Wide Input Voltage Range**
  - **4V to 36V**
  - **3V to 36V (soft-start is finished)**
- **Tight Switching Frequency Variation 2.1MHz ±10% Over Operating Ambient Temperature**
- **5V Fixed Output Voltage (see Ordering Information for availability)**
- **Maximum Output Current : 1A**
- **Peak Current Mode Control**
- **Integrated 200mΩ Switch and 160mΩ Synchronous Rectifier**
- **Built-In Spread-Spectrum Frequency Modulation for Low EMI**
- **Power Good Indication**
- **Enable Control**
- **0.8V ±1.5% Reference Voltage Accuracy**
- **Adjacent Pin-Short Protection**
- **Built-In UVLO, UVP, OTP**
- **Junction Temperature Range : –40°C to 150°C**

Ordering Information

RTQ2131B(-□□)□□-QA

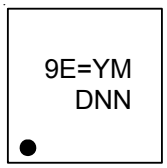
- Grade
  QA: AEC-Q100 Qualified and Screened by High Temperature
- Package Type
  QW: WDFN-10SL 3x3 (W-Type)
- Lead Plating System
  G: Richtek Green Policy Compliant
- Fixed Output Voltage
  50: 5V

Note :

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

Marking Information

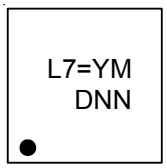
RTQ2131BGQW-QA



9E= : Product Code

YMDNN : Date Code

RTQ2131B-50GQW-QA



L7= : Product Code

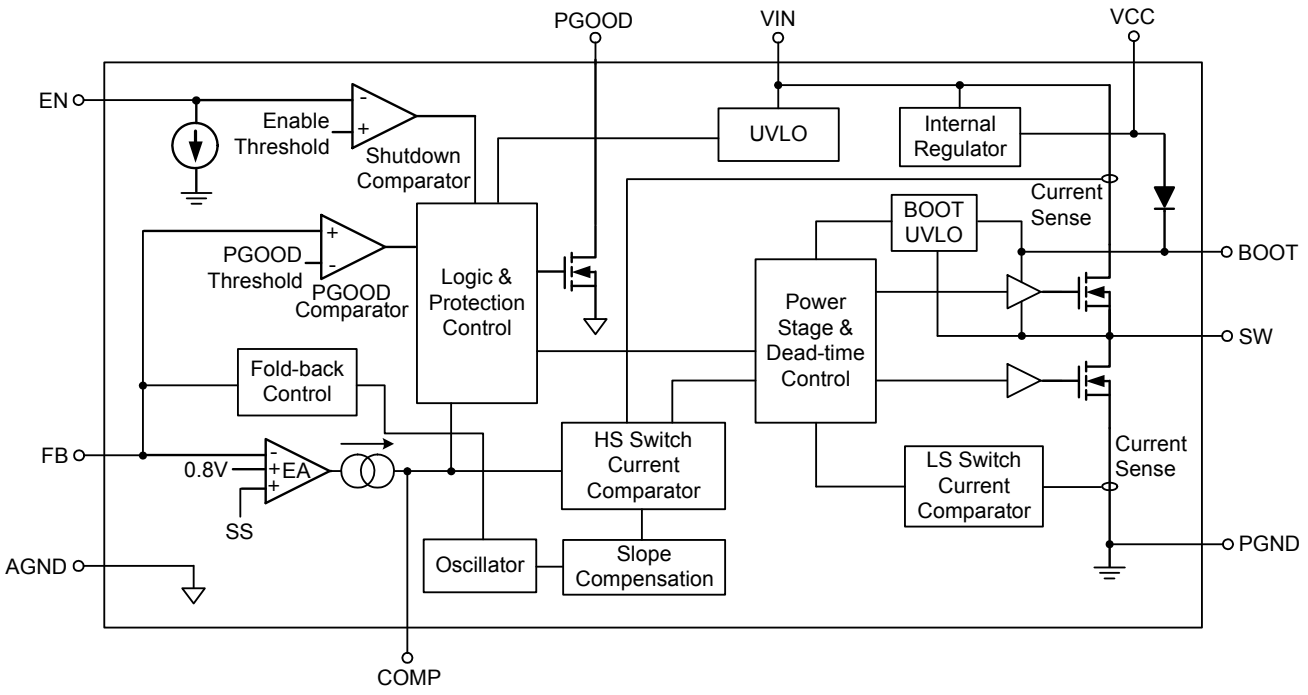
YMDNN : Date Code

Functional Pin Description

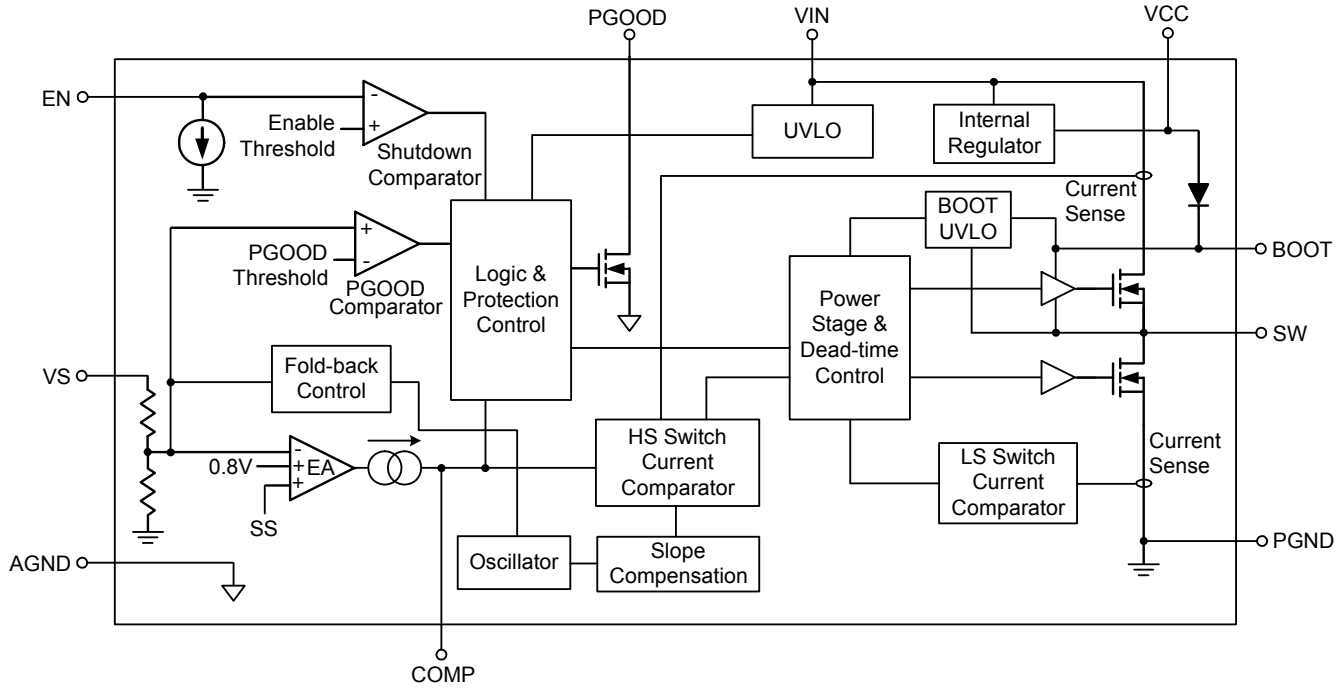
Pin No.	Pin Name	Pin Function
1	VIN	Power input. The input voltage range is from 3V to 36V after soft-start is finished. Connect input capacitors between this pin and PGND. It is recommended to use a 2.2μF, X7R and a 0.1μF, X7R capacitors.
2	PGOOD	Open-drain power-good indication output. Once soft-start is finished, PGOOD will be pulled low to ground if any internal protection is triggered.
3	BOOT	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.1μF, X7R ceramic capacitor between this pin and SW pin.
4	SW	Switch node. SW is the switching node that supplies power to the output and connect the output LC filter from SW to the output load.
5	PGND	Power ground.
6	AGND	Analog ground.
7	COMP	Compensation node. Connect external compensation elements to this pin to stabilize the control loop.
8	FB/VS	Output voltage sense. There are two output voltage setting options : one is that trimmed output voltage options for a fixed output voltage are available for the VS pin, and the other is through a resistive divider to sense the output voltage at the FB pin. The feedback reference voltage is 0.8V typically.
9	EN	Enable control input. Connecting this pin to logic high can enable the device and connecting this pin to GND can disable the device.
10	VCC	Linear regulator output. VCC is the output of the internal 5V linear regulator powered by VIN. Decouple with a 1μF, X7R ceramic capacitor from VCC to ground for normal operation.
11 (Exposed Pad)	PAD	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large PGND plane. Connect this PGND plane to other layers with thermal vias to help dissipate heat from the device.

Functional Block Diagram

Adjustable Output Voltage



Fixed 5V Output Voltage



Operation

Control Loop

The RTQ2131B is a high efficiency step down converter utilizes the peak current mode control. An internal oscillator initiates turn-on of the high-side MOSFET switch. At the beginning of each clock cycle, the internal high-side MOSFET switch turns on, allowing current to ramp-up in the inductor. The inductor current is internally monitored during each switching cycle. The output voltage is sensed on the FB pin via the resistor divider and compared with the internal reference voltage (V_{REF}) to generate a compensation signal (V_{COMP}) on the COMP pin. A control signal derived from the inductor current is compared to the voltage at the COMP pin, derived from the feedback voltage. When the inductor current reaches its threshold, the high-side MOSFET switch is turned off and inductor current ramps-down. While the high-side switch is off, inductor current is supplied through the low-side MOSFET switch. This cycle repeats at the next clock cycle. In this way, duty-cycle and output voltage are controlled by regulating inductor current.

Input Voltage Range

The minimum on-time, t_{ON_MIN}, is the smallest duration of time in which the high-side MOSFET switch can be in its "on" state. Considering the minimum on-time, the allowed maximum input voltage, V_{IN_MAX}, is calculated by :

$$V_{IN\_MAX} \leq \frac{V_{OUT}}{t_{ON\_MIN} \times f_{SW}}$$

where the minimum on-time of the RTQ2131B is 60ns (typically) ; f_{SW} is the maximum operating frequency. The maximum operating frequency of the RTQ2131B is 2.3MHz.

In contrast, the minimum off-time determines the allowed minimum operating input voltage, V_{IN_MIN}, to maintain the fixed frequency operation. The minimum off-time, t_{OFF_MIN}, is the smallest amount of time that the RTQ2131B is capable of turning on the low-side MOSFET switch, tripping the current comparator and turning the MOSFET switch back off. Below shows minimum off-time calculation that considers the loss terms,

$$V_{IN\_MIN} \geq \left[\frac{V_{OUT} + I_{OUT\_MAX} \times \left(R_{DS(ON)\_L} + DCR\right)}{1 - t_{OFF\_MIN} \times fsw} \right] + I_{OUT\_MAX} \times \left(R_{DS(ON)\_H} - R_{DS(ON)\_L}\right)$$

where the minimum off-time of the RTQ2131B is 65ns (typically) ; $R_{DS(ON)\_H}$ is the on resistance of the high-side MOSFET switch; $R_{DS(ON)\_L}$ is the on resistance of the low-side MOSFET switch; DCR is the DC resistance of inductor.

Maximum Duty Cycle Operation

The RTQ2131B is designed to operate in dropout at the high duty cycle approaching 100%. If the operational duty cycle is large and the required off time becomes smaller than minimum off time, the RTQ2131B starts to enable skip off time function and keeps high-side MOSFET switch on continuously. The RTQ2131B implements skip off time function to achieve high duty approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application. The input voltage at which the devices enter dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

Please take note that achieving an actual 100% output will only be possible under no-load conditions. In practical scenarios, the ideal maximum output voltage will be equal to the input voltage minus the product of the output current and the maximum high-side MOSFET turn-on resistance. Additionally, when considering a low boot voltage condition, the low-side MOSFET ay be turned on for a certain duration. In this case, the actual V_{OUT} can be expressed as $V_{OUT} = 0.99 \times (V_{IN} - I_{OUT(max)} \times R_{DSON(max)})$. Therefore, it is advisable to allocate a sufficient design margin to ensure that the target output is maintained under all possible loading current scenarios during the system's operation.

Frequency Foldback

The RTQ2131B implements a frequency foldback function to protect the device at over-load or short-circuited condition, especially higher switching frequencies and input voltages. The switching frequency is divided by 1, 4, and

8 as the FB pin voltage falls from 0.8 V to 0 V.

During short-circuit events, the inductor current may exceed the peak current limit because of the high input voltage and the minimum controllable on time. When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off time. The frequency foldback function increases the off time by increasing the switching cycle period and provides more time for the inductor current to ramp down.

The switching frequency is divided by 8, 4, and 1 as the FB pin voltage ramps from 0 to 0.8V. The device implements frequency foldback during normal start-up and fault conditions. The dropout mechanism is also enabled during soft start. The on time can be extended to be longer than one clock cycle, so RTQ2131B can power on at lower input voltage.

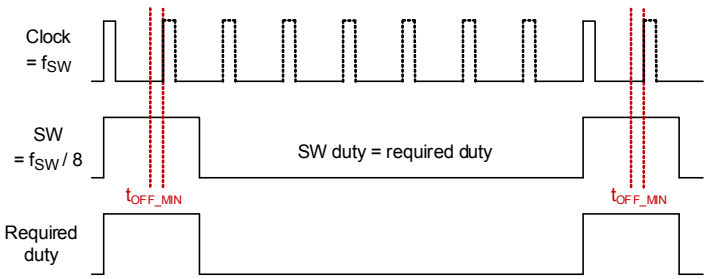


Figure 1. Frequency Foldback and Dropout Mechanism during Start-Up

BOOT UVLO

The BOOT UVLO circuit is implemented to ensure a sufficient voltage of BOOT capacitor for turning on the high-side MOSFET switch at any condition. The BOOT UVLO usually actives at extremely high conversion ratio. With such conditions, the low-side MOSFET switch may not have sufficient turn-on time to charge the BOOT capacitor. The device monitors BOOT pin capacitor voltage and force to turn on the low-side MOSFET switch when the BOOT to SW voltage falls below $V_{BOOT\_UVLO\_L}$ (typically, 2.3V). Meanwhile, the minimum off time is extended to 100ns (typically) hence prolong the BOOT capacitor charging time. The BOOT UVLO is sustained until the $V_{BOOT-SW}$ is higher than $V_{BOOT\_UVLO\_H}$ (typically, 2.4V).

Internal Regulator

The device integrates a 5V linear regulator (V_{CC}) that is supplied by VIN and provides power to the internal circuitry. The internal regulator operates in low dropout mode when V_{VIN} is below 5V. The V_{CC} can be used as the PGOOD pull-up supply but it is "NOT" allowed to power other device or circuitry. In many applications, a 1μF, X7R is recommended and it needs to be placed as close as possible to the VCC pin. Be careful to account for the voltage coefficient of ceramic capacitors when choosing the value and case size. Many ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

Enable Control

The RTQ2131B provides an EN pin, as an external chip enable control, to enable or disable the device. If V_{EN} is held below a logic-low threshold voltage (V_{IL}), switching is inhibited even if the VIN voltage is above VIN under-voltage lockout threshold (V_{UVLO}). If V_{EN} is held below 0.4V, the converter will enter into shutdown mode, that is, the converter is disabled. During shutdown mode, the supply current can be reduced to I_{SHDN} (1.2μA or below). If the EN voltage rises above the logic-high threshold voltage (V_{IH}) while the VIN voltage is higher than V_{UVLO}, the device will be turned on, that is, switching being enabled and soft-start sequence being initiated. When VCC exceeds 5V, the current source typically sinks 1.2μA for V_{EN} < 4V and up to 70μA for V_{EN} > 4V.

Internal Soft-Start Function

The RTQ2131B provides an internal soft-start function. The soft-start function is used to prevent large inrush current while the converter is being powered-up. The typical soft-start time (i.e. for the FB voltage to ramp from 0V to 0.8V) is 2ms.

When voltage of EN pin exceeds threshold voltage, VCC will start up first and after 0.8ms output voltage ramp up during soft-start time as shown in Figure 2.

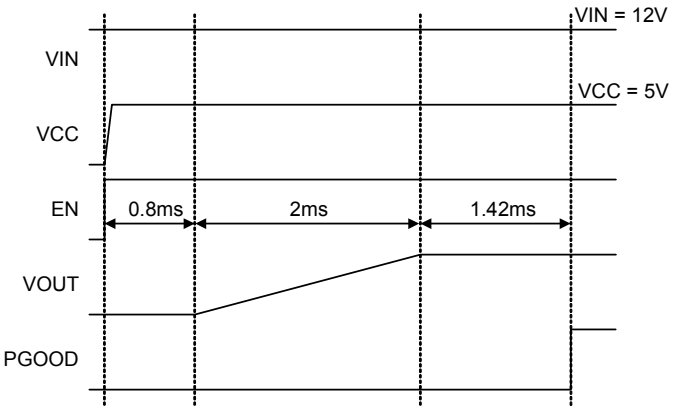


Figure 2. Soft-Start Sequence

Power Good Indication

The RTQ2131B features an open-drain power-good output (PGOOD) to monitor the output voltage status. The output delay of comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Pull-up PGOOD with a resistor to V_{CC} or an external voltage below 5.5V. The power-good function is activated after soft start is finished and is controlled by a comparator connected to the feedback signal V_{FB}. If V_{FB} rises above a power-good high threshold (V_{TH_PGLH1}) (typically 90% of the reference voltage), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapsed. When V_{FB} fall short of power-good low threshold (V_{TH_PGHL2}) (typically 85% of the reference voltage) or exceeds V_{TH_PGHL1} (typically 120% of the reference voltage), the PGOOD pin will be pulled low. For V_{FB} higher than V_{TH_PGHL1}, V_{PGOOD} can be pulled high again if V_{FB} drops back by a power-good high threshold (V_{TH_PGLH2}) (typically 117% of the reference voltage). Once being started-up, if any internal protection is triggered, PGOOD will be pulled low to GND. The internal open-drain pull-down device (1kΩ, typically) will pull the PGOOD pin low. The power good indication profile is shown in Figure 3.

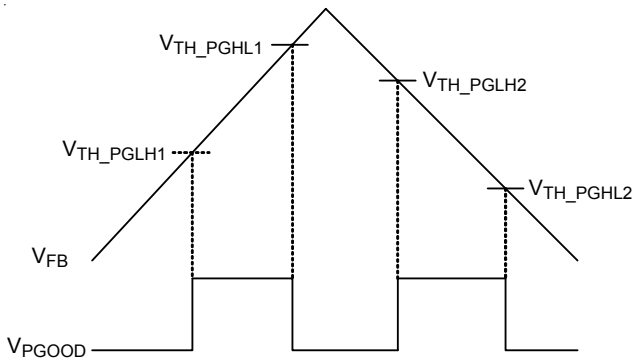


Figure 3. The Logic of PGOOD

Spread-Spectrum Operation

Due to the periodicity of the switching signals, the energy concentrates in one particular frequency and also in its harmonics. These levels or energy is radiated and therefore this is where a potential EMI issue arises. The RTQ2131B build-in spread-spectrum frequency modulation further helping systems designers with better EMC management. The spread spectrum can be active when soft-start is finished. The spread-spectrum is implemented by a pseudo random sequence and uses +6% spread of the switching frequency, that is, the frequency will vary from 2.1MHz to 2.226MHz. Therefore, the RTQ2131B still guarantees that the 2.1MHz switching frequency does not drop into the AM band limit of 1.8MHz.

Input Under-Voltage Lockout

In addition to the EN pin, the RTQ2131B also provides enable control through the VIN pin. If V_{EN} rises above V_{IH} first, switching will still be inhibited until the VIN voltage rises above V_{UVLO}. It is to ensure that the internal regulator is ready so that operation with not-fully-enhanced internal MOSFET switches can be prevented. After the device is powered up, if the VIN voltage goes below the UVLO falling threshold voltage ($V_{UVLO} - \Delta V_{UVLO}$), this switching will be inhibited; if VIN voltage rises above the UVLO rising threshold (V_{UVLO}), the device will resume switching. Note that V_{VIN} = 3V is only designed for cold crank requirement, normal input voltage should be larger than UVLO threshold.

High-Side Switch Peak Current-Limit Protection

The RTQ2131B includes a cycle-by-cycle high-side switch peak current-limit protection against the condition that

the inductor current increasing abnormally, even over the inductor saturation current rating. The inductor current through the high-side MOSFET switch will be measured after a certain amount of delay when the high-side MOSFET switch being turned on. If an over-current condition occurs, the converter will immediately turn off the high-side MOSFET switch and turn on the low-side MOSFET switch to prevent the inductor current exceeding the high-side MOSFET switch peak current limit (I_{LIM_H}).

Low-Side Switch Current-Limit Protection

The RTQ2131B not only implements the high-side switch peak current limit but also provides the sourcing current limit and sinking current limit for low-side MOSFET switch. With these current protections, the IC can easily control inductor current at both side switch and avoid current runaway for short-circuit condition.

For the low-side MOSFET switch sourcing current limit, there is a specific comparator in internal circuitry to compare the low-side MOSFET switch sourcing current to the low-side MOSFET switch sourcing current limit at the end of every clock cycle. When the low-side MOSFET switch sourcing current is higher than the low-side MOSFET switch sourcing current limit (typically, 1.35A), the new switching cycle is not initiated until inductor current drops below the low-side MOSFET switch sourcing current limit.

For the low-side MOSFET switch sinking current limit protection, it is implemented by detecting the voltage across the low-side MOSFET switch. If the low-side MOSFET switch sinking current exceeds the low-side MOSFET switch sinking current limit (typically, 0.8A), both switches are off immediately, and it is held to stop switching until the beginning of next cycle.

Output Under-Voltage Protection

The RTQ2131B includes output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the under-voltage protection trip threshold, 50% (typ.) of the internal reference voltage, the UV comparator will go high to turn off the internal high-side MOSFET switches. If the output under-voltage condition continues for a period of time, the RTQ2131B will enter output under-voltage protection with hiccup mode. During hiccup mode, the device remains shut down. After a period of time, a soft-start sequence for auto-recovery will be initiated. Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed. A short circuit protection and recovery profile is shown in Figure 4.

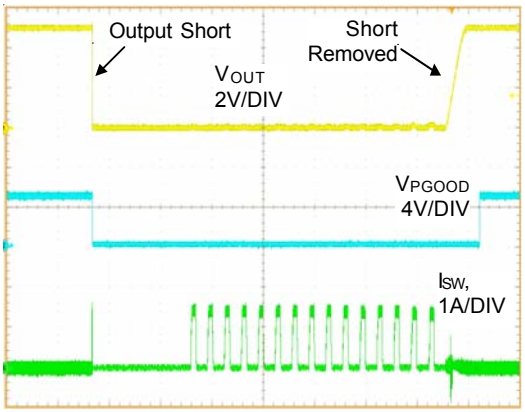


Figure 4. Short Circuit Protection and Recovery

Over-Temperature Protection

The RTQ2131B includes an over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold T_{SD} (175°C). Once the junction temperature cools down by a thermal shutdown hysteresis ΔT_{SD} (15°C), the IC will resume normal operation with a complete soft-start.

Pin-Short Protection

The RTQ2131B provides pin-short protection for neighbor pins. The internal protection fuse will be burned out to prevent IC smoke, fire and spark when BOOT pin is shorted to VIN pin. The hiccup mode protection will be triggered to avoid IC burn-out when SW pin is shorted to ground during internal high-side MOSFET turns on.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 42V
- Switch Voltage, SW ---------- –0.3V to 42V
  <100ns ---------- –5V to 46.3V
- BOOT to SW, V_{BOOT} – V_{SW} ---------- –0.3V to 6V
- EN, PGOOD Voltage ---------- –0.3V to 42V
- Other Pins ---------- –0.3V to 6V
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C

ESD Ratings (Note 2)

- ESD Susceptibility
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 3)

- Supply Voltage ---------- 4V to 36V
- Output Voltage ---------- 0.8V to 0.99 x (V_{IN} – I_{OUT}(max) x $R_{DSON(max)}$)
- Junction Temperature Range ---------- –40°C to 150°C
- Ambient Temperature Range ---------- –40°C to 125°C

Thermal Information (Note 4 and Note 5)

Thermal Parameter		WDFN-10SL 3x3	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	35.5	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	34	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	3.9	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	41.9	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	3.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	22	°C/W

Electrical Characteristics

(V_{IN} = 12V, T_A = T_J = –40°C to 125°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
Input Operating Voltage	V_{IN}	Soft start is finished	3	--	36	V
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising	3.6	3.8	4	V
Under-Voltage Lockout Threshold Hysteresis	ΔV_{UVLO}		--	900	--	mV
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	10	μA
Quiescent Current	I_Q	V_{EN} = 2V, not switching	--	1.1	1.3	mA
Enable Voltage						
Enable Threshold Voltage	V_{IH}	V_{EN} rising	1.3	1.45	1.6	V
	V_{IL}	V_{EN} falling	1.1	1.25	1.4	
Output Voltage						
Output Voltage Sense (Note 6)	V_S	V_S = 5V	4.9	5	5.1	V
Reference Voltage	V_{REF}	3V ≤ V_{IN} ≤ 36V	0.788	0.8	0.812	V
Current Limit						
High-Side Switch Current Limit	I_{LIM_H}	V_{BOOT} – V_{SW} = 4.8V, minimum duty cycle	1.36	1.6	1.84	A
Low-Side Switch Sourcing Current Limit	I_{sr_L}	From source to drain	1.08	1.35	1.62	A
Low-Side Switch Sinking Current Limit	I_{sk_L}	From drain to source	--	0.8	--	A
Switching						
Switching Frequency	f_{SW}		1890	2100	2310	kHz
Minimum On-Time	t_{ON_MIN}		--	60	80	ns
Internal MOSFET						
High-Side On-Resistance	$R_{DS(ON)\_H}$		--	200	360	mΩ
Low-Side On-Resistance	$R_{DS(ON)\_L}$		--	160	288	
Soft-Start						
Soft-Start Time	t_{SS}		1.3	2	2.7	ms
Error Amplifier						
Error Amplifier Trans-Conductance	gm	–10μA < I_{COMP} < 10μA	665	950	1235	μA/V
COMP to Current Sense Trans-Conductance	gm_{CS}		0.9	1.2	1.5	A/V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Over-Temperature Protection						
Thermal Shutdown	T_{SD}		--	175	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	15	--	
Power-Good						
Power-Good Rising Threshold	V_{TH_PGLH1}	V_{FB} rising, PGOOD from low to high	85	90	95	%V_{REF}
	V_{TH_PGHL1}	V_{FB} rising, PGOOD from high to low	--	120	--	
Power-Good Falling Threshold	V_{TH_PGHL2}	V_{FB} falling, PGOOD from high to low	80	85	90	%V_{REF}
	V_{TH_PGLH2}	V_{FB} falling, PGOOD from low to high	--	117	--	
Power-Good Leakage Current		PGOOD signal good, V_{FB} = V_{REF}, V_{PGOOD} = 5.5V	--	--	0.5	μA
Power-Good Sink Current Capability		PGOOD signal fault, I_{PGOOD} sinks 0.2mA	--	---	0.3	V
Spread Spectrum						
Spread-Spectrum Rang	SS		--	+6	--	%

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. Devices are ESD sensitive. Handling precautions are recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

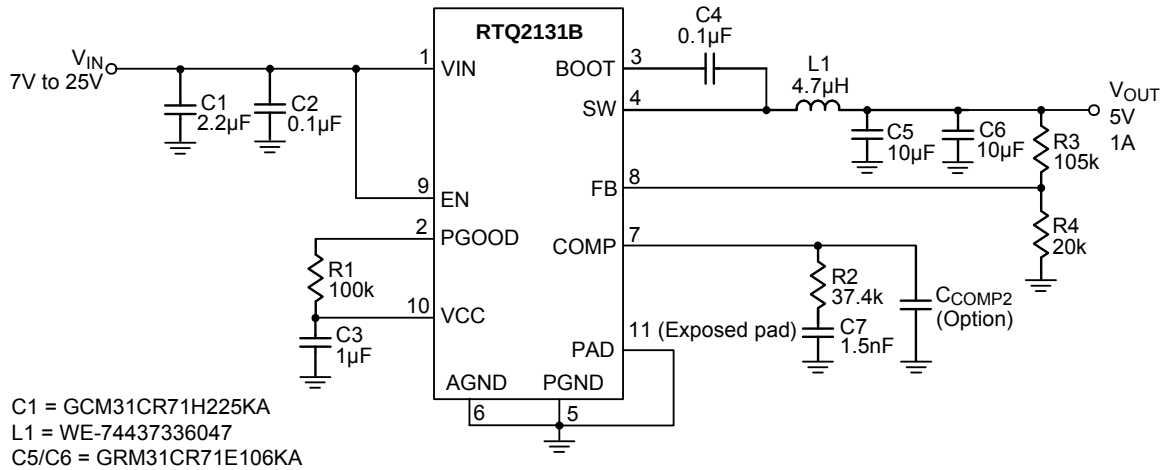
Note 4. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

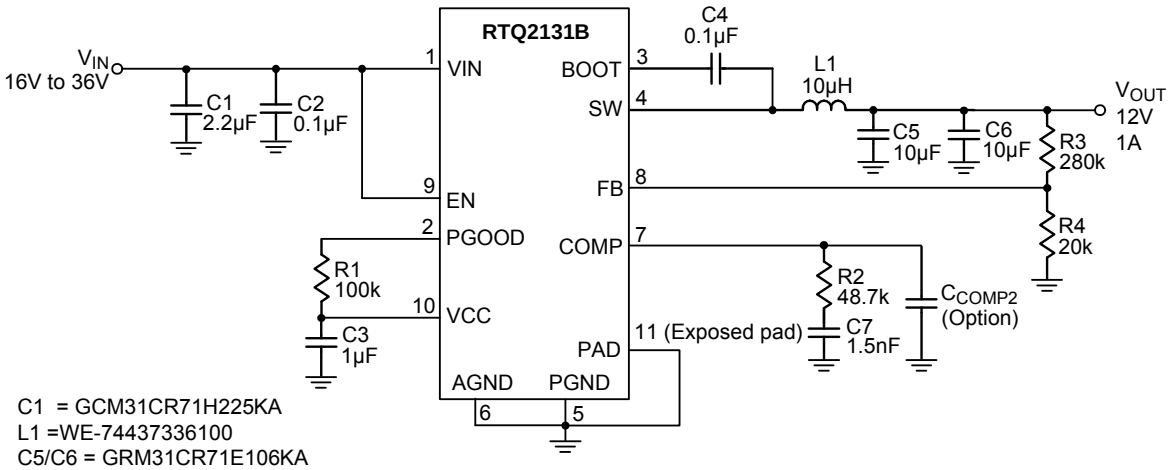
Note 5. $\theta_{JA(EVB)}$, $\Psi_{JC(Top)}$ and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 110mm x 80mm, furthermore, all layers with 1 oz.Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

Note 6. There are two output voltage setting options : one is that trimmed output voltage options for a fixed output voltage are available for the VS pin, and the other is through a resistive divider to sense the output voltage at the FB pin.

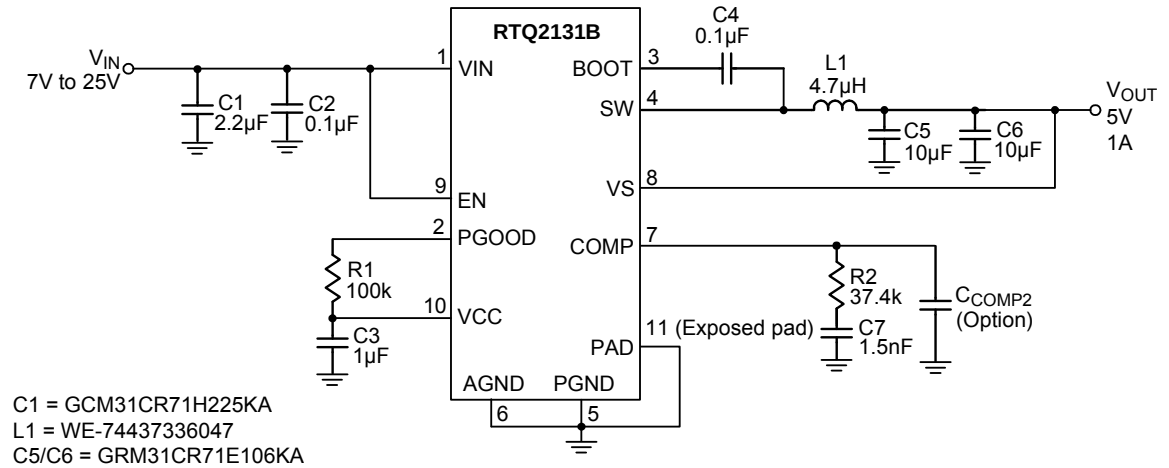
Typical Application Circuit

Adjustable Output Voltage

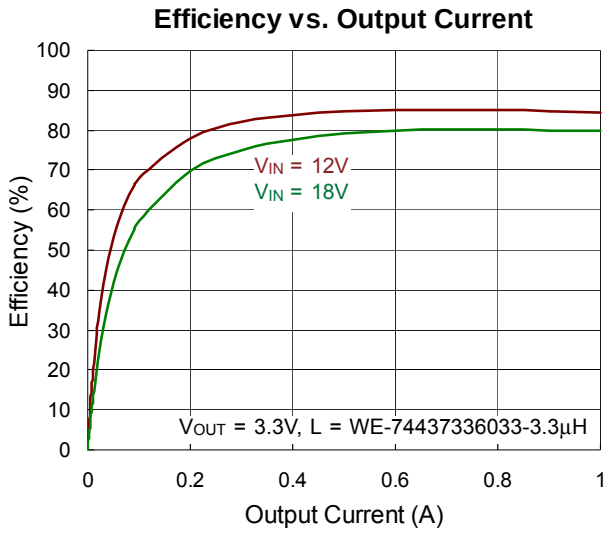


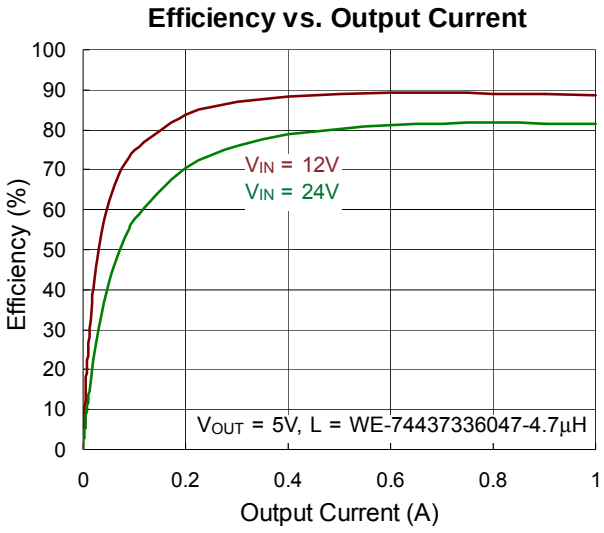


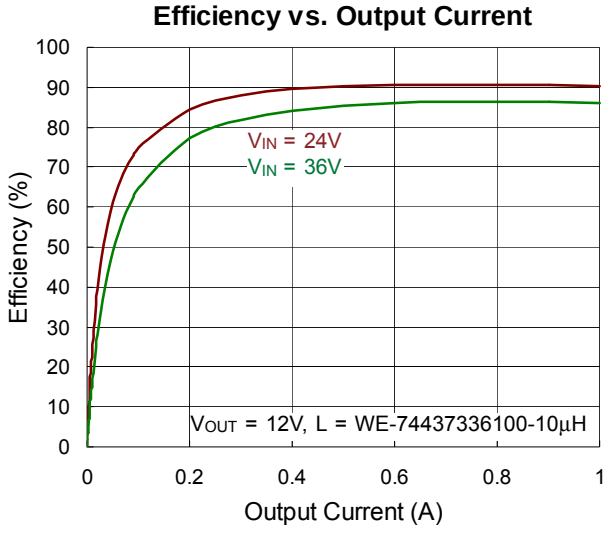
Fixed 5V Output Voltage

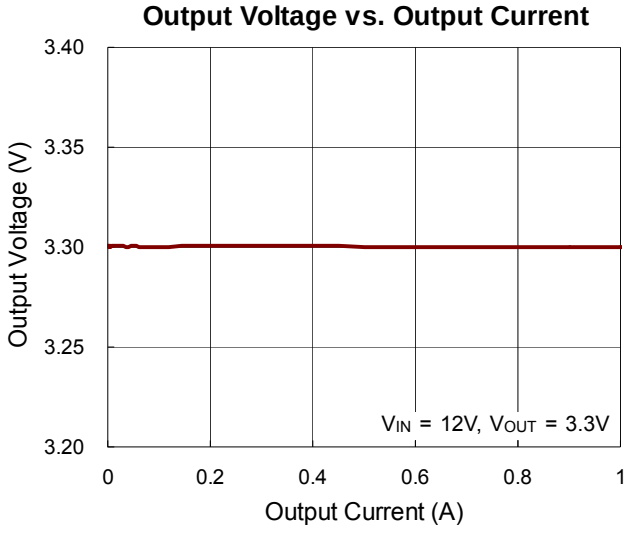


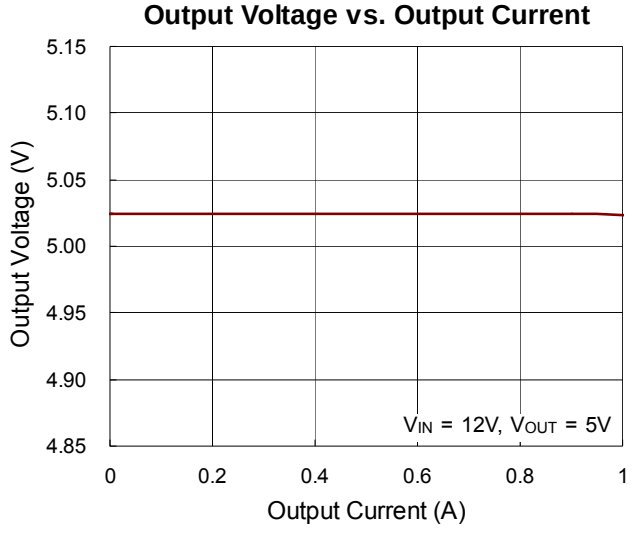
Typical Operating Characteristics

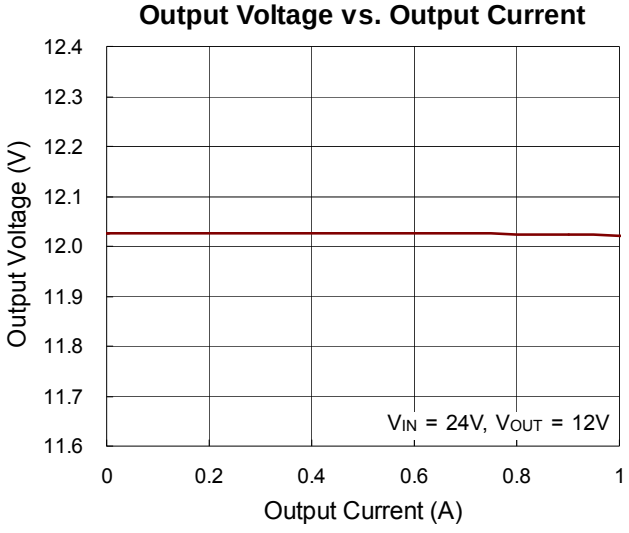




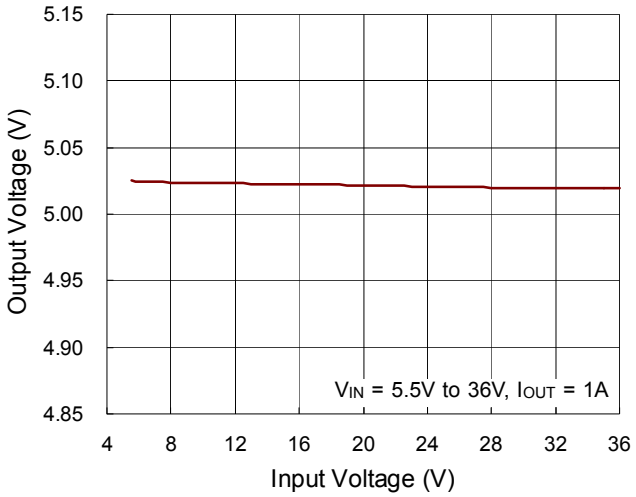




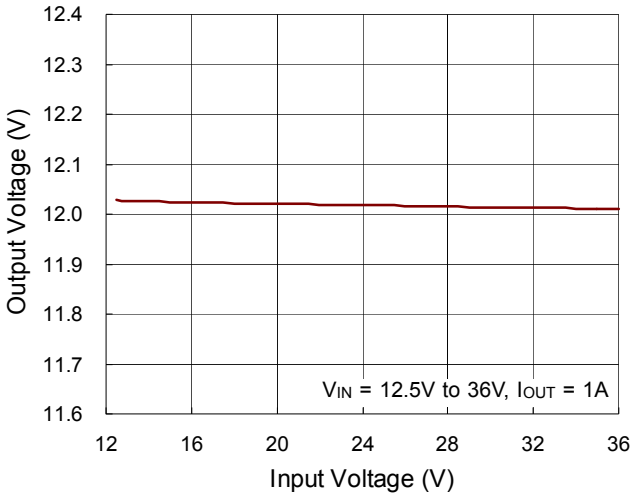




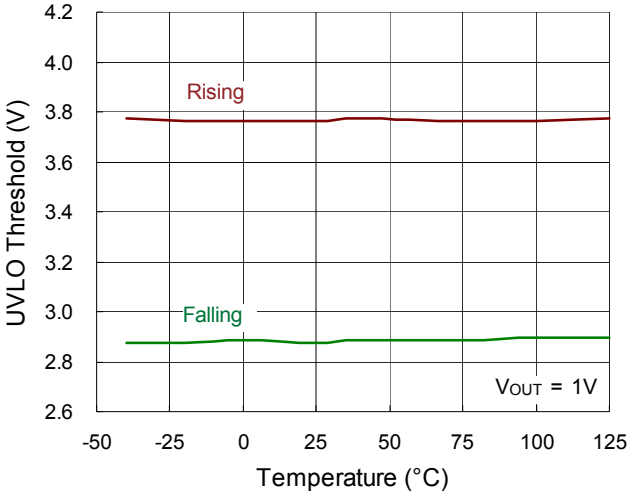
Output Voltage vs. Input Voltage



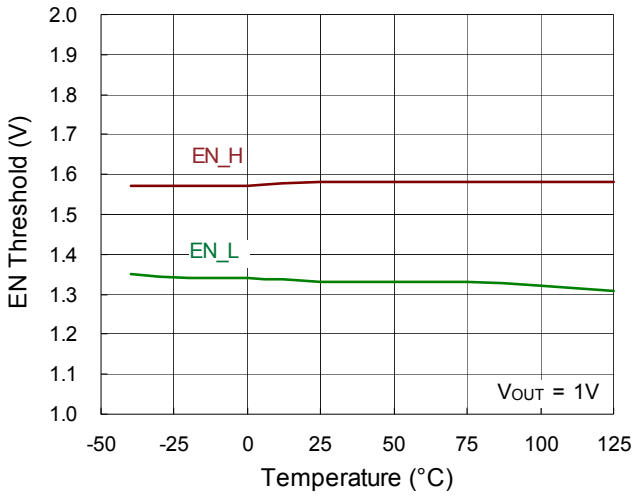
Output Voltage vs. Input Voltage



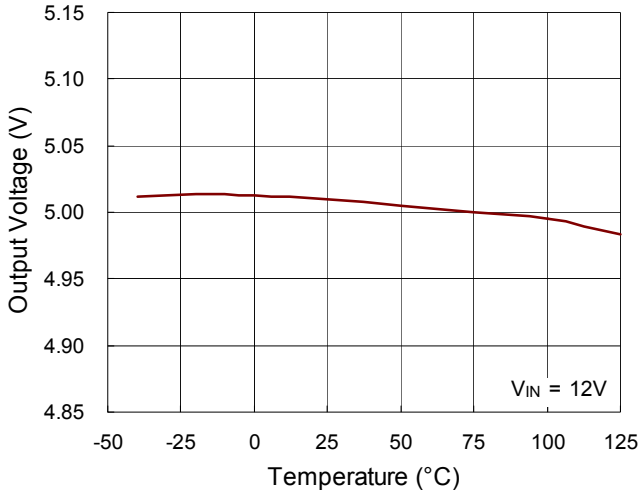
UVLO Threshold vs. Temperature



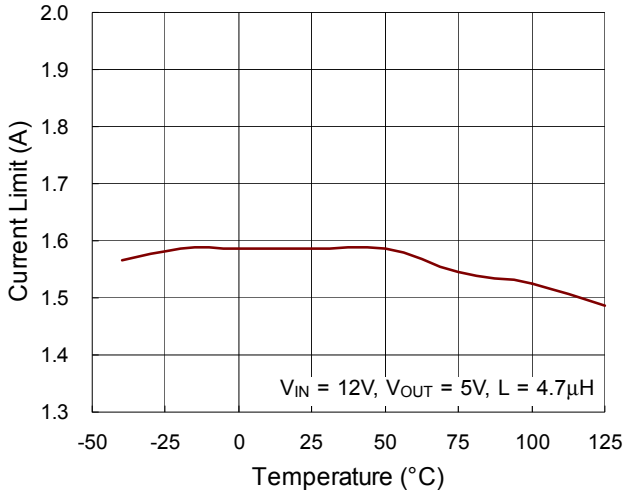
EN Threshold vs. Temperature



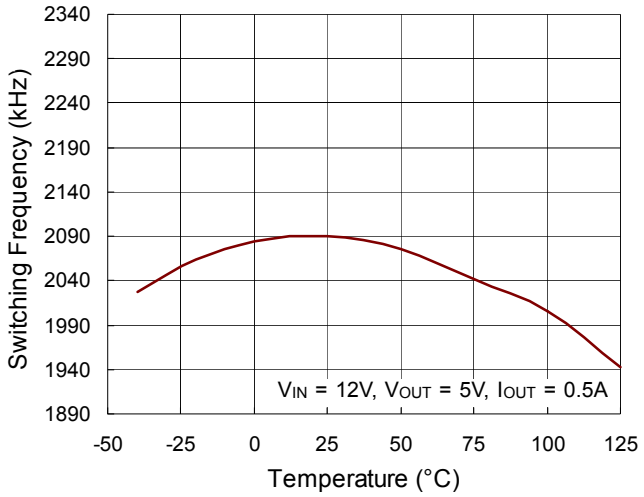
Output Voltage vs. Temperature



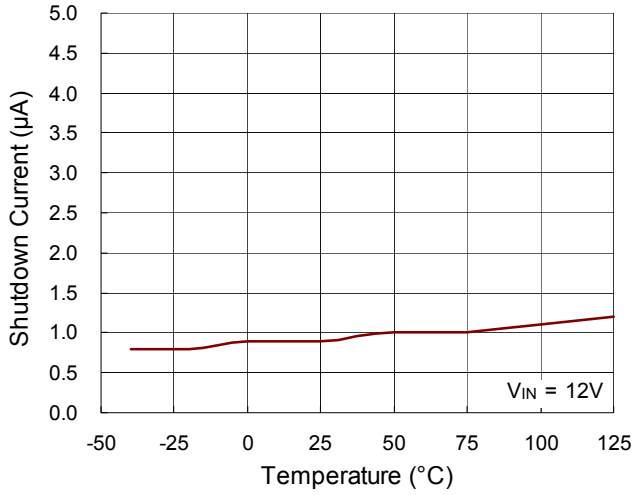
Current Limit vs. Temperature



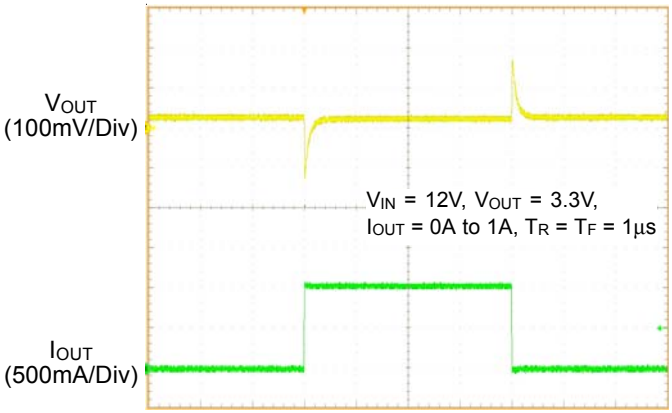
Switching Frequency vs. Temperature



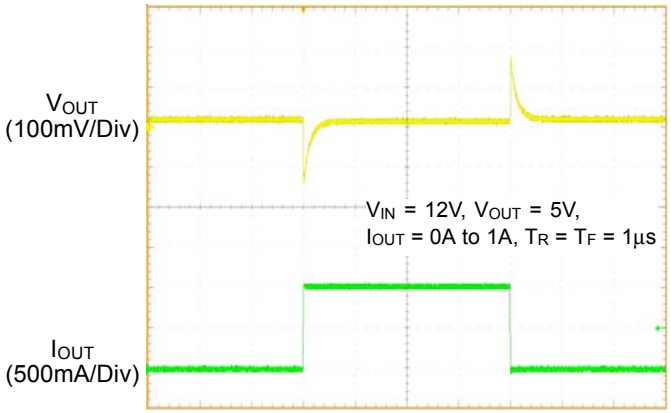
Shutdown Current vs. Temperature



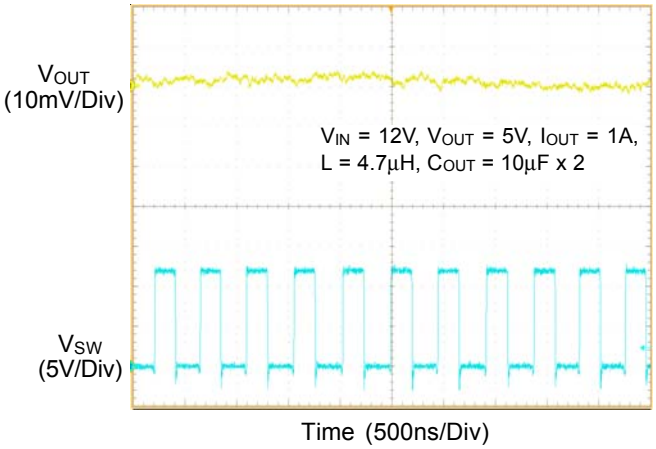
Load Transient Response



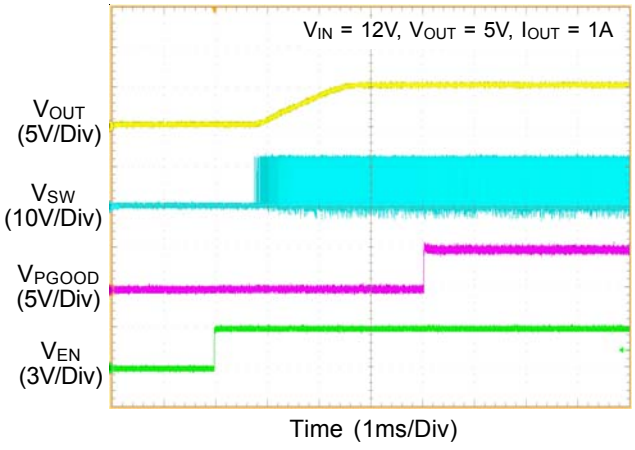
Load Transient Response



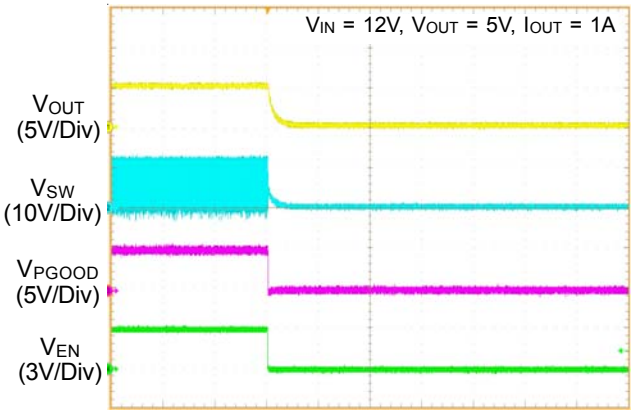
Output Ripple Voltage



Power On from EN

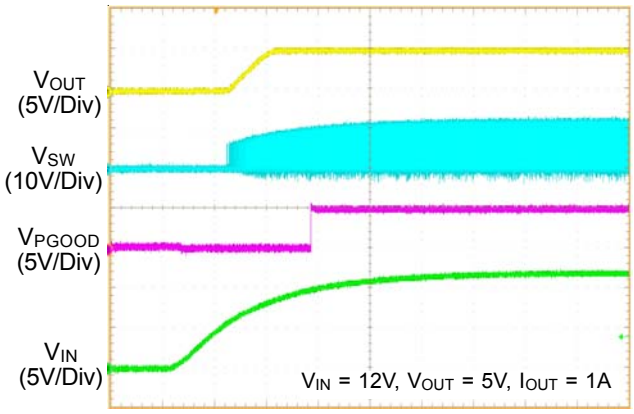


Power Off from EN



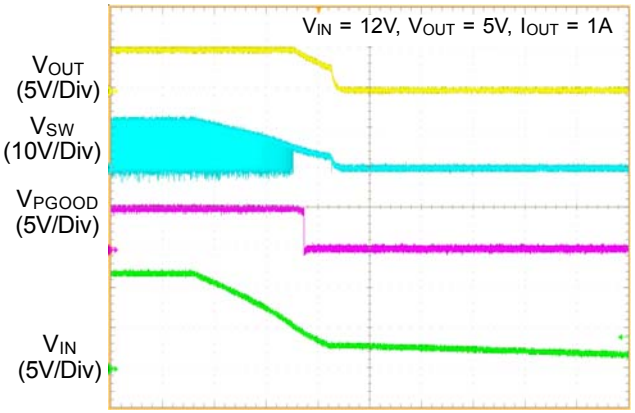
Time (1ms/Div)

Power On from VIN



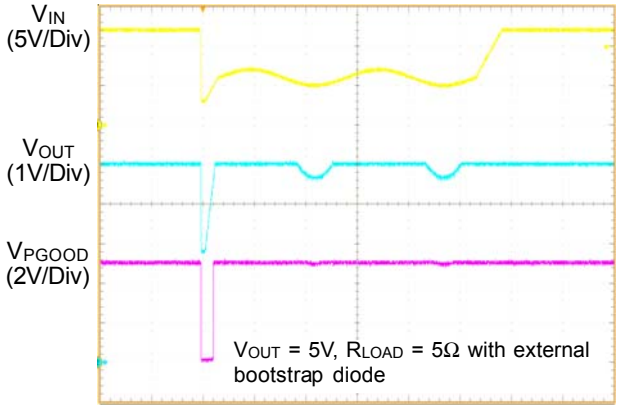
Time (2ms/Div)

Power Off from VIN



Time (2ms/Div)

Starting Profile III (Cold cranking)



Time (200ms/Div)

Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

A general the RTQ2131B application circuit is shown in typical application circuit section. External component selection is largely driven by the load requirement. First of all, the inductor L is chosen. Then the input capacitor C_{IN} and the output capacitor C_{OUT} can be decided. Next, feedback resistors and compensation circuit are selected to set the desired output voltage and crossover frequency. After that, the internal regulator capacitor C_{VCC}, and the bootstrap capacitor C_{BOOT} can be selected. Finally, the remaining external components can be selected for functions such as the EN and PGOOD.

Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. This result in additional phase lag in the loop and reduce the crossover frequency. As the ratio of the slope-compensation ramp to the sensed-current ramp increases, the current-mode system tilts towards voltage-mode control. Lower inductance values allow for smaller case size, but the increased ripple lowers the effective current limit threshold, increases the AC losses in the inductor and may trigger low-side switch sinking current limit at FPWM. It also causes insufficient slope compensation and ultimately loop instability as duty cycle approaches or exceeds 50%.

When duty cycle exceeds 50%, below condition needs to be satisfied :

$$0.54 \times f_{SW} > \frac{V_{OUT}}{L}$$

A good compromise among size, efficiency, and transient response can be achieved by setting an inductor current ripple (ΔI_L) with about 10% to 50% of the maximum rated output current (1A).

To enhance the efficiency, choose a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The inductor selected should have a saturation current rating greater than the peak current limit of the device. The core must be large enough not to saturate at the peak inductor current (I_{L_PEAK}) :

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2} \Delta I_L$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the high-side switch peak current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the high-side switch peak current limit rather than the peak inductor current. It is recommended to use shielded inductors for good EMI performance.

Input Capacitor Selection

Input capacitor, C_{IN}, is needed to filter the pulsating current at the drain of the high-side MOSFET switch. C_{IN} should be sized to do this without causing a large variation in input voltage. The peak-to-peak voltage ripple on input capacitor can be estimated as equation below :

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + ESR \times I_{OUT}$$

Where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

Figure 5 shows the C_{IN} ripple current flowing through the input capacitors and the resulting voltage ripple across the capacitors. For ceramic capacitors, the equivalent series resistance (ESR) is very low, the ripple which is caused by ESR can be ignored, and the minimum value of effective input capacitance can be estimated as equation below :

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

Where $\Delta V_{CIN\_MAX} \leq 200mV$

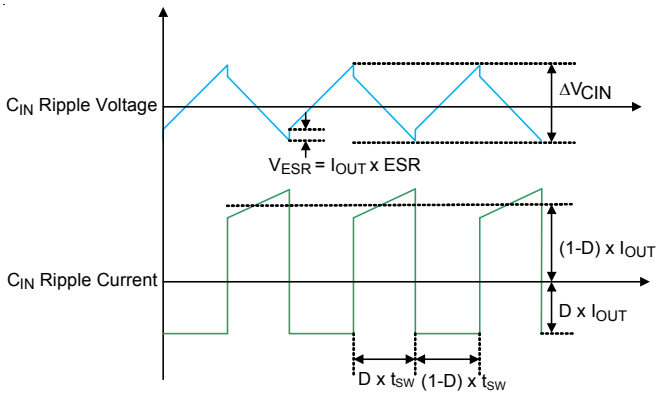


Figure 5. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current. The RMS ripple current (I_{RMS}) of the regulator can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) as the following equation :

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

From the above, the maximum RMS input ripple current occurs at maximum output load, which will be used as the requirements to consider the current capabilities of the input capacitors. The maximum ripple voltage usually occurs at 50% duty cycle, that is, V_{IN} = 2 x V_{OUT}. It is commonly to use the worse $I_{RMS} \cong 0.5 \times I_{OUT\_MAX}$ at V_{IN} = 2 x V_{OUT} for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes. Ceramic capacitors are ideal for witching regulator applications due to its small, robust and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the RTQ2131B circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pin, with a low inductance connection to the PGND of the IC. It is recommended to connect a 2.2µF, X7R capacitor between VIN pin to PGND pin. For filtering high frequency noise, additional small capacitor 0.1µF should be placed close to the part and the capacitor should be 0402 or 0603 in size. X7R capacitors are recommended for best performance across temperature and input voltage variations.

Output Capacitor Selection

The selection of C_{OUT} is determined by considering to satisfy the voltage ripple and the transient loads. The peak-to-peak output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}} + \Delta I_L \times ESR$$

Where the ΔI_L is the peak-to-peak inductor ripple current. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding to the transient loads, the V_{SAG} and V_{SOAR} requirement should be taken into consideration for choosing the effective output capacitance value. The amount of output sag/soar is a function of the crossover frequency factor at PWM, which can be calculated from below.

$$V_{SAG} = V_{SOAR} = \frac{\Delta I_{OUT}}{2 \times \pi \times C_{OUT} \times f_C}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. The recommended dielectric type of the capacitor is X7R best performance across temperature and input voltage variations. The variation of the capacitance value with temperature, DC bias voltage and switching frequency needs to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

Transient performance can be improved with a higher value of output capacitor. Increasing the output capacitance will also decrease the output voltage ripple.

Output Voltage Programming

The output voltage can be programmed by a resistive divider from the output to ground with the midpoint connected to the FB pin. The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 6. The output voltage is set according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where the reference voltage, V_{REF}, is 0.8V (typically).

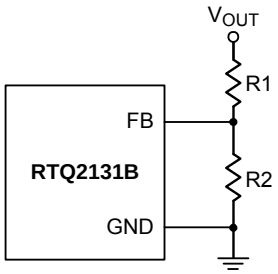


Figure 6. Output Voltage Setting

The placement of the resistive divider should be within 5mm of the FB pin. The resistance of R2 is not larger than 170kΩ for noise immunity consideration. The resistance of R1 can then be obtained as below :

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

For better output voltage accuracy, the divider resistors (R1 and R2) with ±1% tolerance or better should be used.

Compensation Network Design

The purpose of loop compensation is to ensure stable operation while maximizing the dynamic performance. An undercompensated system may result in unstable operations. Typical symptoms of an unstable power supply include: audible noise from the magnetic components or ceramic capacitors, jittering in the switching waveforms, oscillation of output voltage, overheating of power MOSFETs and so on.

In most cases, the peak current mode control architecture used in the RTQ2131B only requires two external components to achieve a stable design as shown in Figure 7. The compensation can be selected to accommodate any capacitor type or value. The external compensation also allows the user to set the crossover frequency and optimize the transient performance of the device. Around the crossover frequency the peak current mode control (PCMC) equivalent circuit of Buck converter can be simplified as shown in Figure 8. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the device. Since the slope compensation is ignored, the actual cross over frequency will usually be lower than the crossover frequency used in the calculations. It is always necessary to make a measurement before releasing the design for final production. Though the models of power supplies are theoretically correct, they cannot take full account of circuit parasitic and component nonlinearity, such as the ESR variations of output capacitors, then on linearity of inductors and capacitors, etc. Also, circuit PCB noise and limited measurement accuracy may also cause measurement errors. A Bode plot is ideally measured with a network analyzer while Richtek application note AN038 provides an alternative way to check the stability quickly and easily. Generally, follow the following steps to calculate the compensation components :

1. Set up the crossover frequency, f_C. For stability purposes, our target is to have a loop gain slope that is –20dB/decade from a very low frequency to beyond the crossover frequency. Do "NOT" design the crossover frequency over 90kHz with the RTQ2131B. For dynamic purposes, the higher the bandwidth, the faster the load transient response. The downside to

high bandwidth is that it increases the regulators susceptibility to board noise which ultimately leads to excessive falling edge jitter of the switch node voltage.

2. R_{COMP} can be determined by :

$$R_{COMP} = \frac{2\pi \times f_C \times V_{OUT} \times C_{OUT}}{gm \times V_{REF} \times gm\_CS} = \frac{2\pi \times f_C \times C_{OUT}}{gm \times gm\_CS} \times \frac{R1 + R2}{R2}$$

where

gm is the error amplifier gain of trans-conductance (950μA/V) gm_cs is COMP to current sense (1.2A/V)

3. A compensation zero can be placed at or before the dominant pole of buck which is provided by output capacitor and maximum output loading(R_L). Calculate C_{COMP}:

$$C_{COMP} = \frac{R_L \times C_{OUT}}{R_{COMP}}$$

4. The compensation pole is set to the frequency at the ESR zero or 1/2 of the operating frequency. Output capacitor and its ESR provide a zero and optional C_{COMP2} can be used to cancel this zero

$$C_{COMP2} = \frac{R_{ESR} \times C_{OUT}}{R_{COMP}}$$

If 1/2 of the operating frequency is lower than the ESR zero, the compensation pole is set at 1/2 of the operating frequency.

$$C_{COMP2} = \frac{1}{2 \times \pi \times \frac{fsw}{2} \times R_{COMP}}$$

Note : Generally, C_{COMP2} is an optional component to be used to enhance noise immunity.

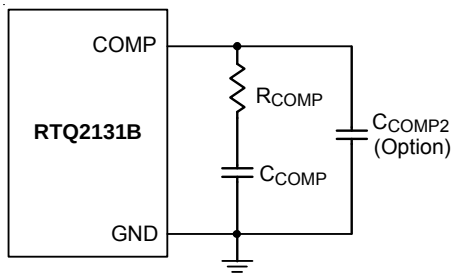


Figure 7. External Compensation Components

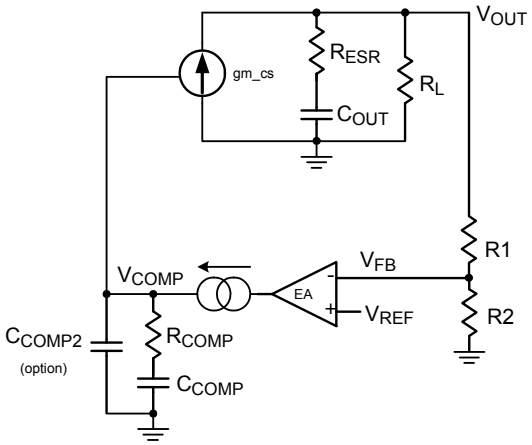


Figure 8. Simplified Equivalent Circuit of Buck with PCMC

Internal Regulator

The device integrates a 5V linear regulator (VCC) that is supplied by VIN and provides power to the internal circuitry. The internal regulator operates in low dropout mode when VIN voltage is below 5V. The VCC can be used as the PGOOD pull-up supply but it is "NOT" allowed to power other device or circuitry. In many applications, a 1μF, X7R is recommended and it needs to be placed as close as possible to the VCC pin. Be careful to account for the voltage coefficient of ceramic capacitors when choosing the value and case size. Many ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

Bootstrap Driver Supply

The bootstrap capacitor (C_{BOOT}) between BOOT pin and SW pin is used to create a voltage rail above the applied input voltage, VIN. Specifically, the bootstrap capacitor is charged through an internal diode to a voltage equal to approximately V_{VCC} each time the low-side switch is turned on. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle. For most applications a 0.1μF, 0603 ceramic capacitor with X7R is recommended and the capacitor should have a 6.3 V or higher voltage rating.

External Bootstrap Diode

It is recommended to add an external bootstrap diode between an external 5V voltage supply and the BOOT pin to improve enhancement of the high-side switch and

improve efficiency when the input voltage is below 5.5V, the recommended application circuit is shown in Figure 9. The bootstrap diode can be a low-cost one, such as 1N4148 or BAT54. The external 5V can be a fixed 5V voltage supply from the system, or a 5V output voltage generated by the RTQ2131B. Note that the $V_{BOOT-SW}$ must be lower than 5.5V.

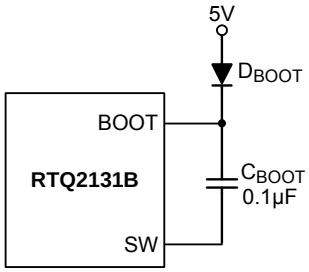


Figure 9. External Bootstrap Diode

External Bootstrap Resistor (Option)

The gate driver of an internal power MOSFET, utilized as a high-side switch, is optimized for turning on the switch not only fast enough for reducing switching power loss, but also slow enough for minimizing EMI. The EMI issue is worse when the switch is turned on rapidly due to high di/dt noises induced. When the high-side switch is being turned off, the SW node will be discharged relatively slowly by the inductor current due to the presence of the dead time when both the high-side and low-side switches are turned off.

In some cases, it is desirable to reduce EMI further, even at the expense of some additional power dissipation. The turn-on rate of the high-side switch can be slowed by placing a small bootstrap resistor R_{BOOT} between the BOOT pin and the external bootstrap capacitor as shown in Figure 10. The recommended range for the R_{BOOT} is several ohms to 10 ohms and it could be 0402 or 0603 in size.

This will slow down the rates of the high-side switch turn-on and the rise of V_{SW}. In order to improve EMI performance and enhancement of the internal MOSFET switch, the recommended application circuit is shown in Figure 11, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} being placed between the BOOT pin and the capacitor/diode connection.

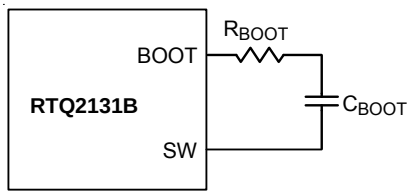


Figure 10. External Bootstrap Resistor at the BOOT Pin

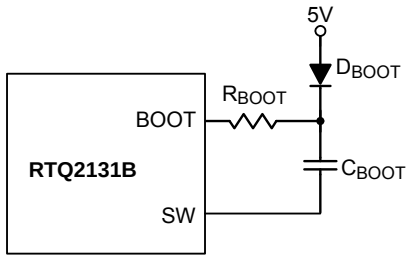


Figure 11. External Bootstrap Diode and Resistor at the BOOT Pin

EN Pin for Start-Up and Shutdown Operation

For automatic start-up, the EN pin, with high-voltage rating, can be connected to the input supply V_{IN} directly. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to V_{IN} by adding a resistor R_{EN} and a capacitor C_{EN}, as shown in Figure 12, to have an additional delay. The time delay can be calculated with the EN's internal threshold, at which switching operation begins (typically 1.25V).

An external MOSFET can be added for the EN pin to be logic-controlled, as shown in Figure 13. In this case, a pull-up resistor, R_{EN}, is connected between VIN and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin. To prevent the device being enabled when VIN is smaller than the V_{OUT} target level or some other desired voltage level, a resistive divider (R_{EN1} and R_{EN2}) can be used to externally set the input under-voltage lockout threshold, as shown in Figure 14.

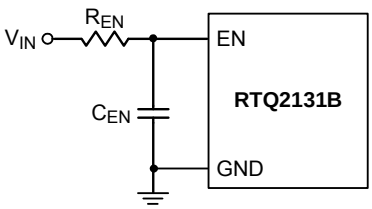


Figure 12. Enable Timing Control

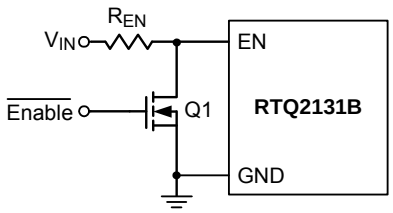


Figure 13. Logic Control for the EN Pin

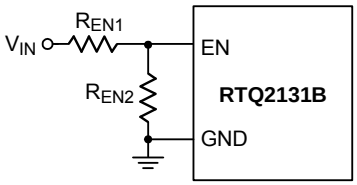


Figure 14. Resistive Divider for Under-Voltage Lockout Threshold Setting

Power-Good Output

The PGOOD pin is an open-drain power-good indication output and is to be connected to an external voltage source through a pull-up resistor.

The external voltage source can be an external voltage supply below 5.5V, VCC or the output of the RTQ2131B if the output voltage is regulated under 5.5V. It is recommended to connect a 100kΩ between external voltage source to PGOOD pin.

Thermal Consideration

In many applications, the RTQ2131B does not generate much heat due to its high efficiency and low thermal resistance of its WDFN-10SL 3x3 (Exposed Pad) package. However, in applications in which the RTQ2131B is running at a high ambient temperature and high input voltage or high switching frequency, the generated heat may exceed the maximum junction temperature of the part.

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. If the junction temperature reaches approximately 175°C, the RTQ2131B stop switching the power MOSFETs until the temperature drops about 15°C cooler.

The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = \left(T_{J(MAX)} - T_A\right) / \theta_{JA}$$

where

$T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 150°C. T_A is the ambient operating temperature, θ_{JA} is the system-level junction to ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system.

The device thermal resistance depends strongly on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance.

Experiments in the Richtek thermal lab show that simply set $\theta_{JA(EFFECTIVE)}$ as 110% to 120% of the $\theta_{JA(EVB)}$ is reasonable to obtain the allowed $P_{D(MAX)}$.

As an example, consider the case when the RTQ2131B is used in applications where V_{IN} = 12V, I_{OUT} = 1A, V_{OUT} = 5V. The efficiency at 5V, 1A is 88.6% by using WE-74437336047 (4.7μH, 50mΩ DCR) as the inductor and measured at room temperature. The core loss can be obtained from its website of 30.5mW in this case. In this case, the power dissipation of the RTQ2131B is

$$P_{D,\,RT} = \frac{1-\eta}{\eta} \times P_{OUT} - \left(I_O^2 \times DCR + P_{CORE}\right) = 0.563W$$

Considering the $\theta_{JA(EFFECTIVE)}$ is 50.3°C/W by using the RTQ2131B evaluation board with 4 layers with 1 oz. copper thickness on all layers, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately :

$$T_J = 0.563W \times 50.3°C/W + 25°C = 53.3°C$$

Figure 15 shows the RTQ2131B $R_{DS(ON)}$ versus different junction temperature. If the application calls for a higher ambient temperature, we might recalculate the device power dissipation and the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature.

Using 60°C ambient temperature as an example, the change of the equivalent $R_{DS(ON)}$ can be calculated as below

$$\Delta R_{DS(ON)} = \Delta R_{DS(ON),HS} \times \frac{V_{OUT}}{V_{IN}} + \Delta R_{DS(ON),LS} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$= 35m\Omega \times \frac{5}{12} + 25m\Omega \times \left(1 - \frac{5}{12}\right) = 29.2m\Omega$$

and yields a new power dissipation of 0.592W. Therefore, the estimated new junction temperature is

$T_J' = 0.592W \times 50.3°C/W + 60°C = 89.8°C$

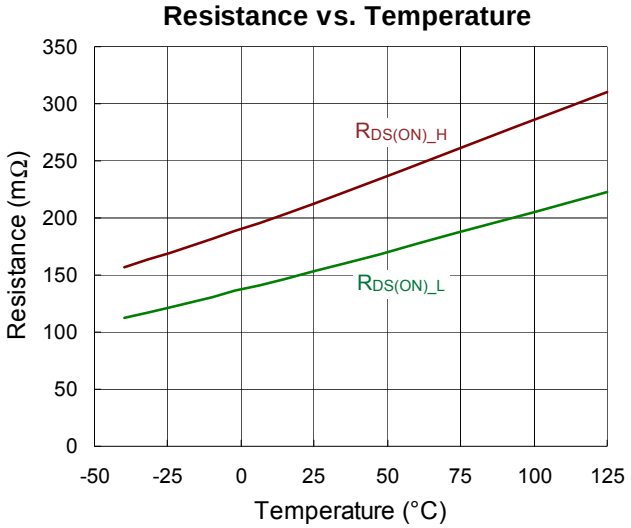


Figure 15. RTQ2131B $R_{DS(ON)}$ vs. Temperature

If the application calls for a higher ambient temperature, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow.

Layout Guideline

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RTQ2131B :

- Four-layer or six-layer PCB with maximum ground plane is strongly recommended for good thermal performance.
- Keep the traces of the main current paths wide and short.
- Place high frequency decoupling capacitor C_{IN2} as close as possible to the IC to reduce the loop impedance and minimize switch node ringing.
- Place the VCC decoupling capacitor, C_{VCC}, as close to VCC pin as possible.
- Place bootstrap capacitor, C_{BST}, as close to IC as possible. Routing the trace with width of 20mil or wider.
- Place multiple vias under the device near VIN and PGND and near input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the RTQ2131B to additional ground planes within the circuit board and on the bottom side.
- The high frequency switching nodes, SW and BOOT, should be as small as possible. Keep analog components away from the SW and BOOT nodes.
- Reducing the area size of the SW exposed copper to reduce the electrically coupling from this voltage.
- Connect the feedback sense network behind via of output capacitor.
- Place the feedback components R_{FB1} / R_{FB2} / C_{FF} near the IC.
- Place the compensation components R_{CP1} / C_{CP1} / C_{CP2} near the IC.
- Connect all analog grounds to common node and then connect the common node to the power ground with a single point.

Figure 16 to Figure 19 are the layout example which uses 110mm x 80mm, four-layer PCB with 1 oz. Cu on all layers.

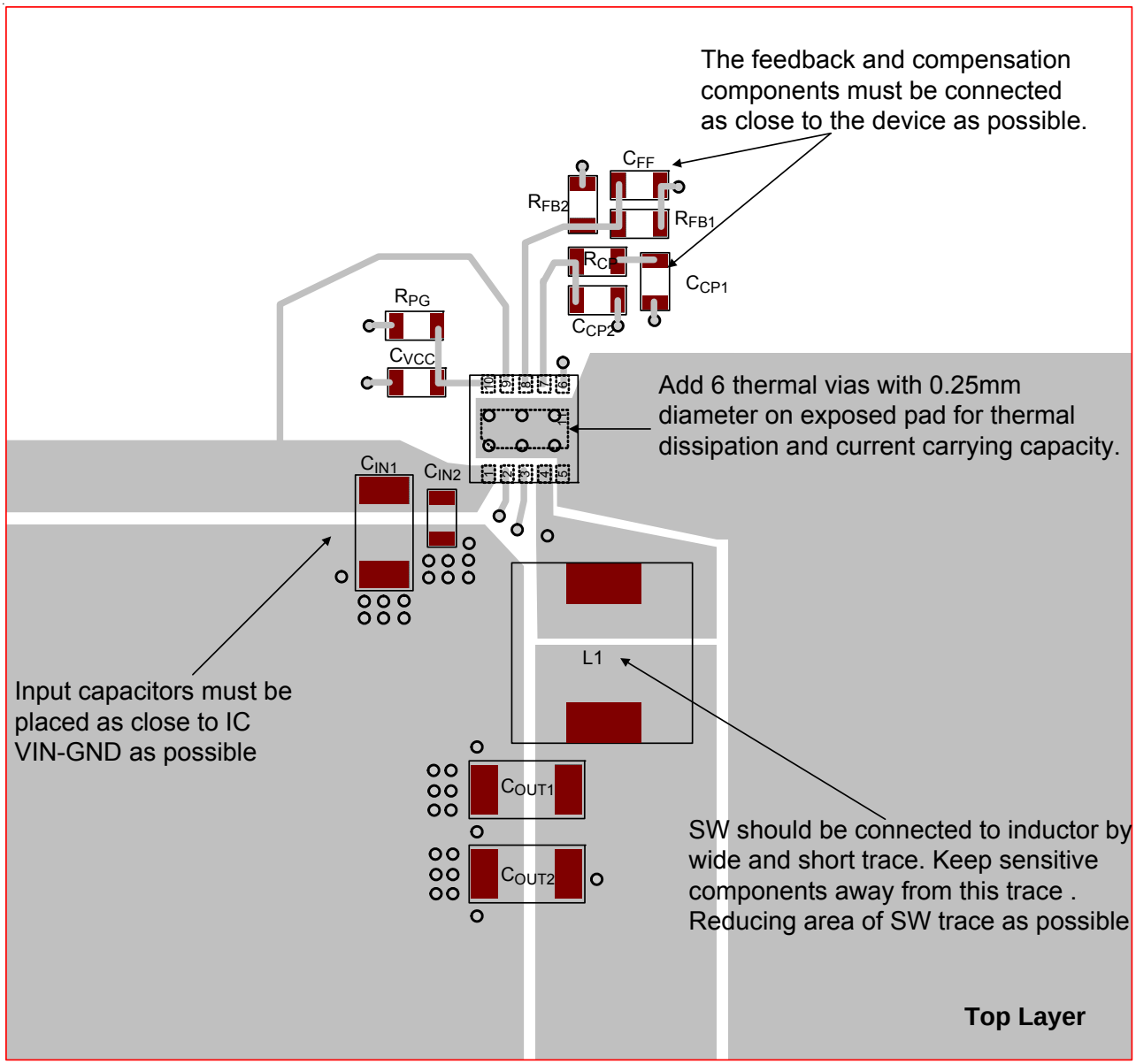


Figure 16. Layout Guide (Top Layer)

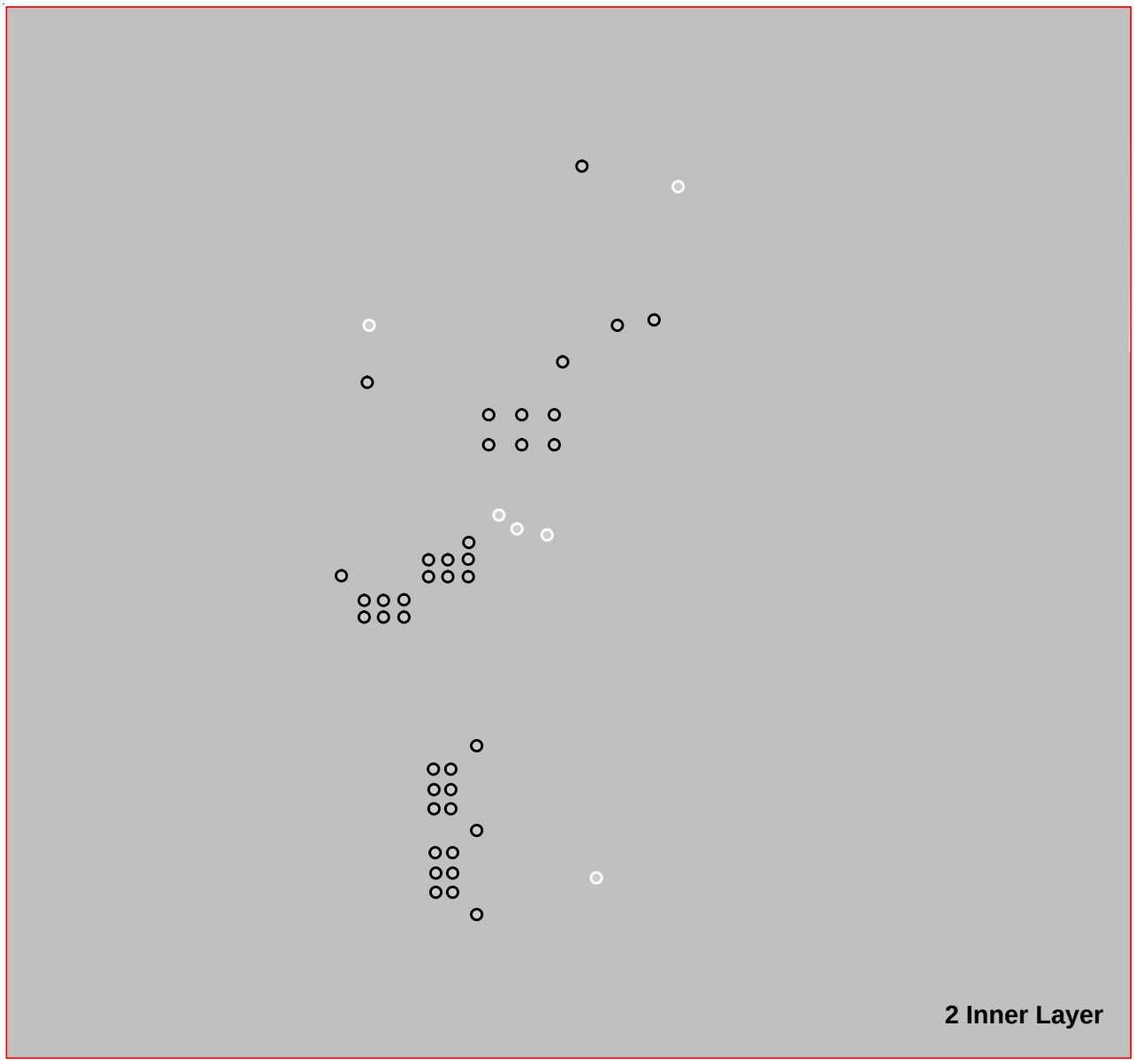


Figure 17. Layout Guide (2 Inner Layer)

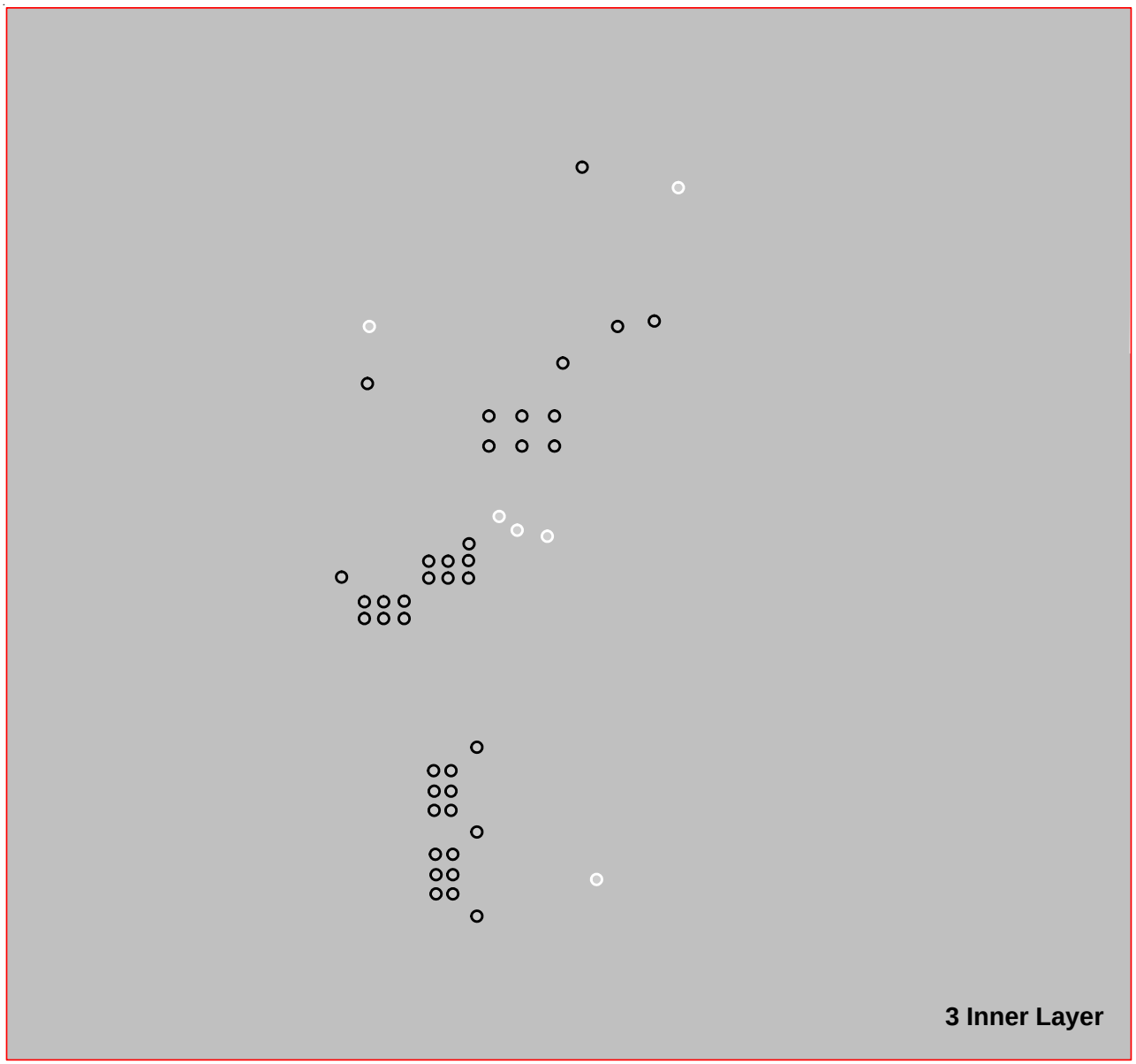


Figure 18. Layout Guide (3 Inner Layer)

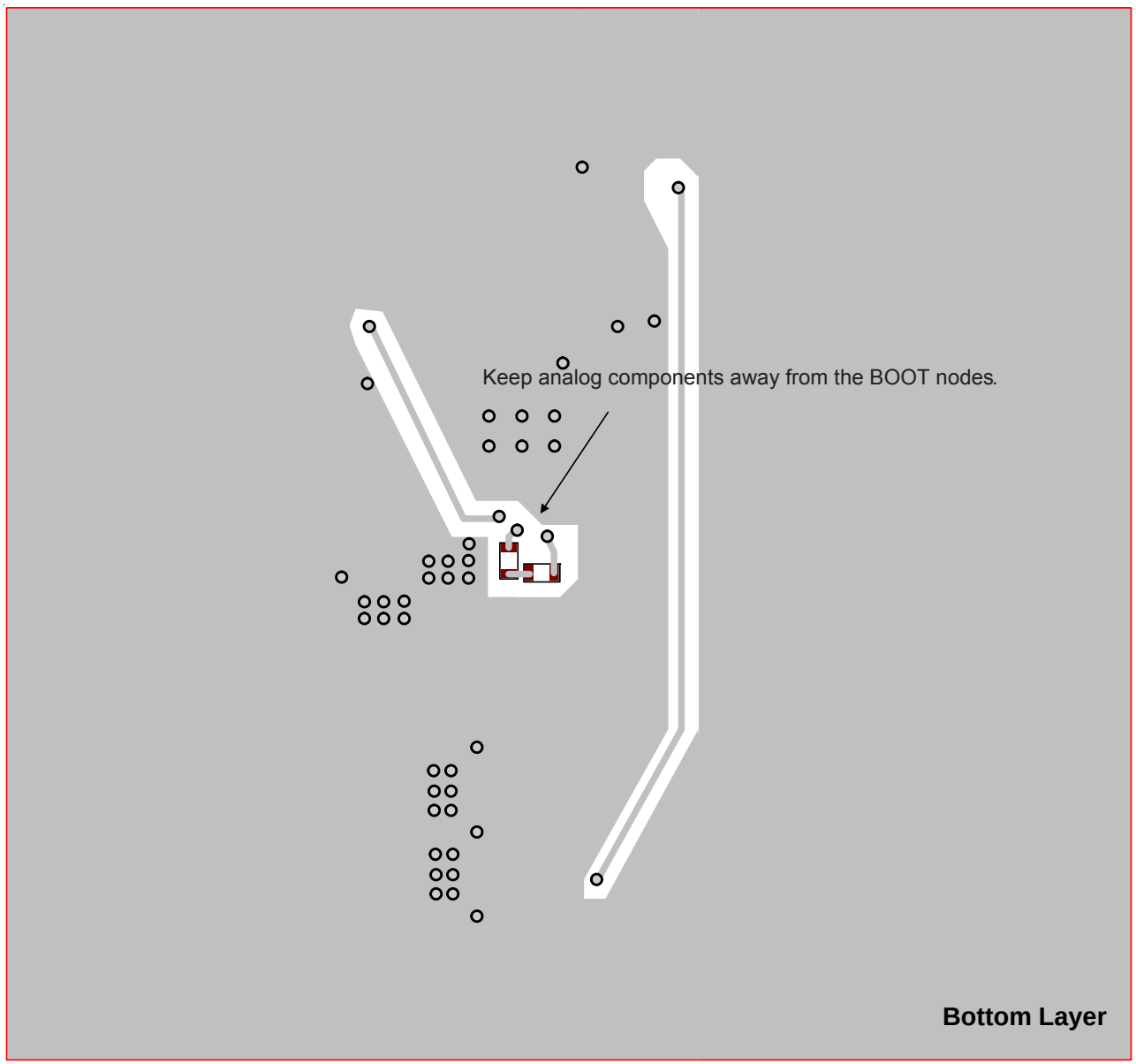
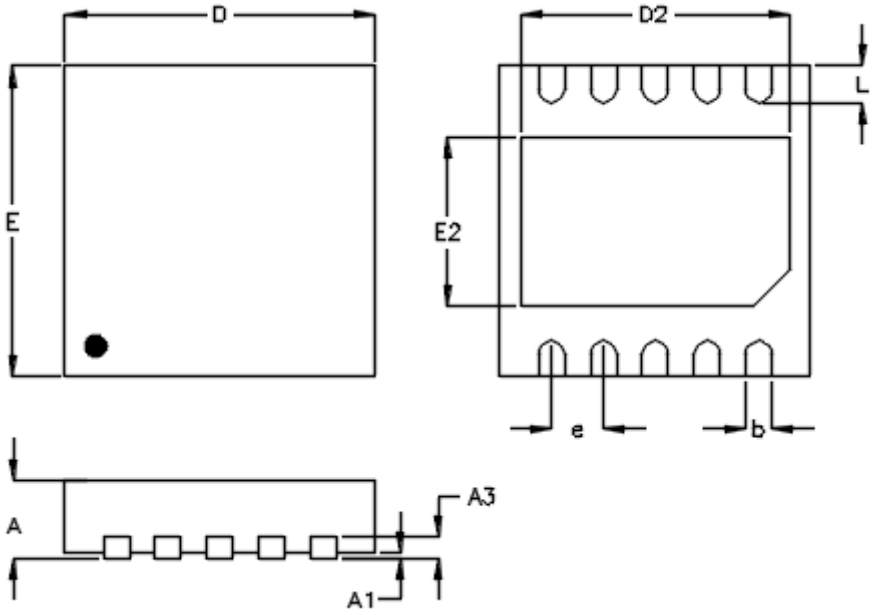
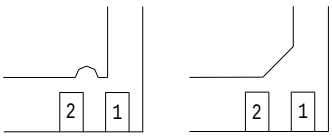


Figure 19. Layout Guide (Bottom Layer)

Outline Dimension





DETAIL A

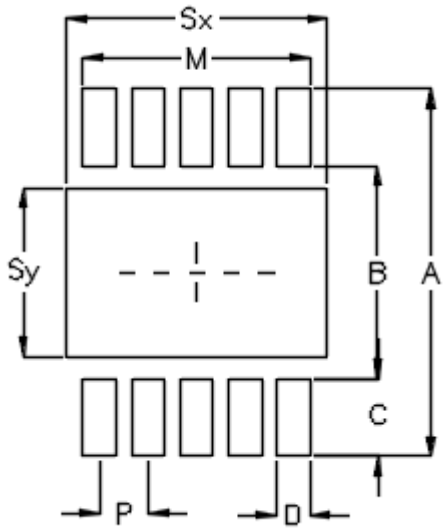
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	2.900	3.100	0.114	0.122
D2	2.550	2.650	0.100	0.104
E	2.900	3.100	0.114	0.122
E2	1.590	1.690	0.063	0.067
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 10SL DFN 3x3 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN3*3-10S	10	0.50	3.80	2.20	0.80	0.35	2.70	1.74	2.35	±0.05

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Datasheet Revision History

Version	Date	Description	Item
02	2023/10/12	Modify	Features on P1 Absolute Maximum Ratings on P8 Recommended Operating Conditions on P8 Thermal Information on P8 Operation on P4, 7 Electrical Characteristics on P9 Application Information on P16, 21, 22
03	2023/11/6	Modify	Features on P1 Operation on P4, 5, 6, 7 Recommended Operating Conditions on P8