RICHTEK®

RTQ2183-QA

5.5V, 3A, 2.4MHz, Automotive Synchronous Buck Converter

1 General Description

The RTQ2183-QA is a synchronous buck converter designed to operate within an input voltage range of 2.5V to 5.5V. It delivers up to 3A output current and supports an adjustable output voltage ranging from 0.6V to 3.3V.

Utilizing Advanced Constant On-Time (ACOT®) control architecture, the RTQ2183-QA achieves fast and stable output voltage regulation, making it ideal for applications with dynamic load requirements. By minimizing the number of external components, The ACOT® architecture minimizes the number of required external components, simplifying design and reducing system cost for efficient power management.

Key features include an independent enable control input and a power-good indicator for easy sequence control. A programmable soft-start function, implemented via an external capacitor on the SS pin, ensures controlled inrush current and smooth power-up.

The RTQ2183-QA provides comprehensive protection functions, including input undervoltage-lockout, output undervoltage protection, output overvoltage protection, overcurrent protection, and over-temperature protection. Cycle-by-cycle current-limit protection safeguards against shorted outputs. The RTQ2183-QA is available in a compact WET-VDFN-8J2L 2x1.5 (FC) package, providing flexibility and space-saving advantages for various system designs.

The recommended junction temperature range is –40°C to 150°C, and ambient temperature range is –40°C to 125°C.

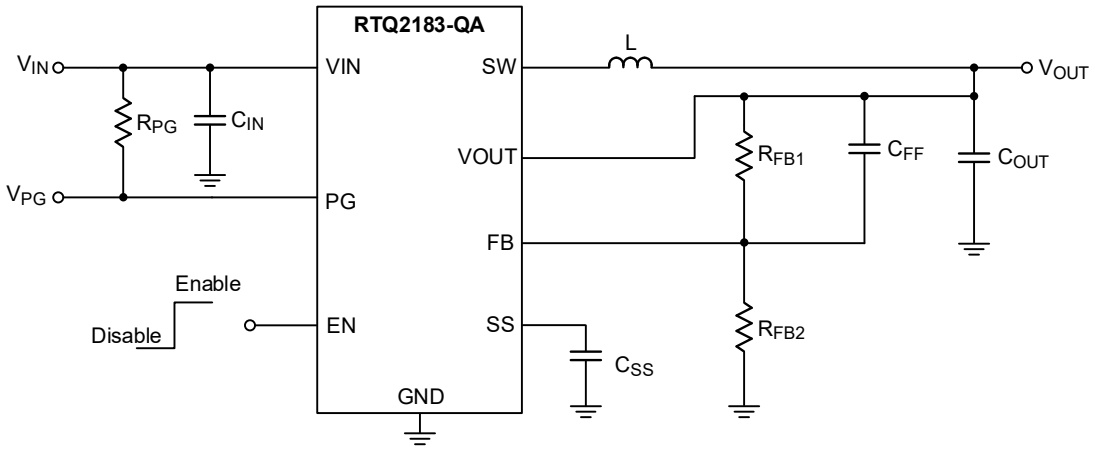
2 Features

- **AEC-Q100 Grade 1 Qualified**
- **±1.5% Output Accuracy from –40°C to 125°C Junction Temperature Range**
- **Soft-Start Control with External Css**
- **Forced PWM Mode**
- **Input Voltage Range: 2.5V to 5.5V**
- **Output Voltage Range: 0.6V to 3.3V**
- **65mΩ and 35mΩ Integrated Power MOSFETs**
- **Fixed 2.4MHz Switching Frequency**
- **Fast Load Transient Response with ACOT® Control Topology**
- **Enable Pin and Soft-Start Pin for Sequence Control**
- **Power-Good Indicator**
- **Operate Up to 100% Duty Cycle**
- **Input Undervoltage-Lockout Protection (UVLO)**
- **Input Overvoltage-Lockout Protection (OVLO)**
- **Output Overvoltage Protection (OVP)**
- **Output Undervoltage Protection (UVP)**
- **Short Circuit Protection with Hiccup Mode**
- **Over-Temperature Protection**
- **Small Form Factor**
  - **WET-VDFN-8J2L 2x1.5 (FC) Package with Compact BOM**
- **Ambient Temperature Range: –40°C to 125°C**
- **Junction Temperature Range: –40°C to 150°C**

3 Applications

- ADAS
- Automotive IVI
- Automotive Clusters

4 Simplified Application Circuit



5 Ordering Information

RTQ2183□-QA□

Packing
A: Standard

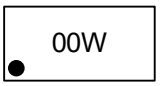
Grade
QA: AEC-Q100 Qualified and Screened by High Temperature

Package Type(1)
TN: WET-VDFN-8J2L 2x1.5 (FC) (V-Type)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information



00: Product Code
W: Date Code

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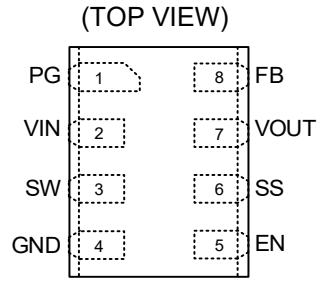
7 Pin Configuration

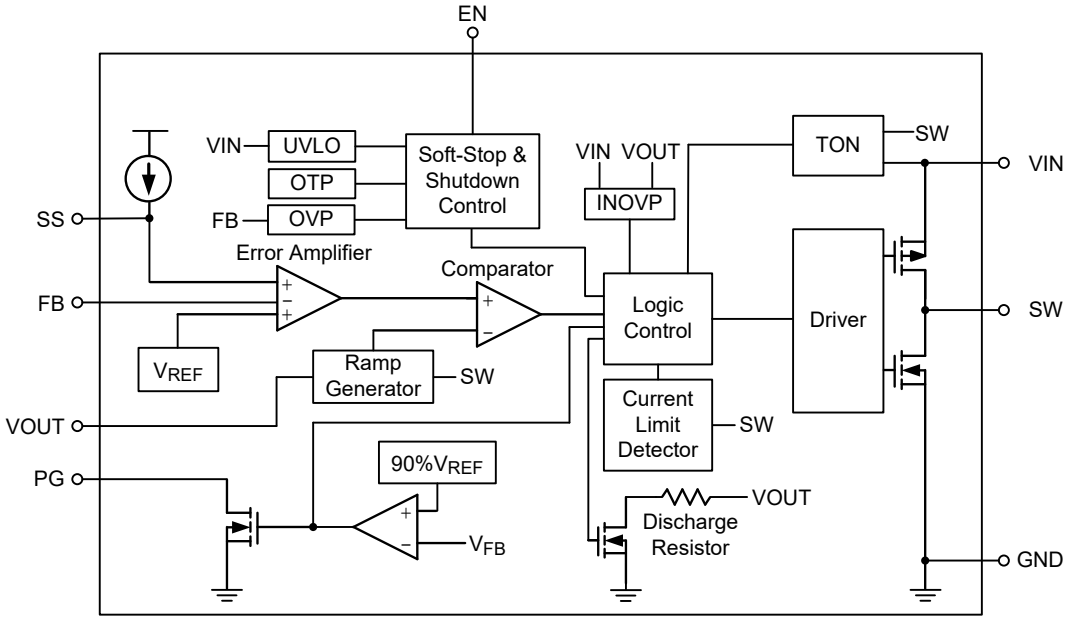


WET-VDFN-8J2L 2x1.5 (FC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PG	Open-drain, power-good indicator pin for device output status. Connect a 300kΩ pull-up resistor to the I/O reference power source. The PG output is logic-high when V_{FB} exceeds 90% of V_{REF}, and is pulled low to ground when V_{FB} falls below 85% of V_{REF}. If unused, leave this pin floating.
2	VIN	Power input. The input voltage range is from 2.5V to 5.5V. Connect at least a 10μF X7R or larger ceramic capacitor between this pin and GND.
3	SW	Switch node between the internal switch and the synchronous rectifier. Connect this pin to an inductor, with the other end connected to the output capacitor.
4	GND	Power ground. Connect this pin to the PCB ground plane with multiple vias to optimize thermal performance.
5	EN	Enable control input. Pulling this pin high enables the device; pulling it low disables the device.
6	SS	Soft-start capacitor connection. Connect an external capacitor between this pin and ground to set the soft-start time.
7	VOUT	Output voltage sense input. Connect this pin to the external output capacitors located near the critical load to maintain the desired output voltage.
8	FB	Feedback sense input pin. Connect this pin to the midpoint of the external feedback resistive divider between VOUT and GND to set the output voltage. The device regulates the FB voltage to a reference value, typically 0.6V.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VIN ---------- –0.3V to 6.5V
- Output Voltage, VOUT ---------- –0.3V to 4V
- VIN to SW ---------- –0.3V to 6.5V
- VIN to SW (t ≤ 10ns) ---------- –2.5V to 9V
- Switch Node Voltage, SW ---------- –0.3V to 6.5V

  <10ns ---------- –5V to 8V
- Other I/O Pins Voltages ---------- –0.3V to 6.5V
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility

  HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage, VIN ---------- 2.5V to 5.5V
- Output Voltage, VOUT ---------- 0.6V to 3.3V
- Junction Temperature Range ---------- –40°C to 150°C
- Ambient Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		WET-VDFN-8J2L 2x1.5 (FC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	99	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	121	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	8	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

14 Electrical Characteristics

(V_{IN} = 3.6V, T_J = –40 to 150°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VIN Supply Input Operating Voltage	V_{IN}	V_{EN} = 2V	2.5	--	5.5	V
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}	V_{IN} rising	2.15	2.3	2.45	V
Undervoltage-Lockout Falling Threshold	V_{UVLO_F}	V_{IN} falling	1.95	2.1	2.25	
Supply Current (Shutdown)	I_{SHDN}	V_{EN} = 0V, T_J = 25°C	--	0.01	1	µA
		V_{EN} = 0V, T_J = –40°C to 125°C	--	--	20	
Supply Current (Quiescent)	I_{Q_FPWM}	V_{FB} = 0.63V	--	460	650	µA
Soft-Start						
Soft-Start Charge Current	I_{SS}	0%V_{FB} to 95%V_{FB}	--	0.75	0.9	µA
Enable Voltage						
EN Input Voltage Rising Threshold	V_{EN_R}	EN high-level input voltage	1.1	--	--	V
EN Input Voltage Falling Threshold	V_{EN_F}	EN low-level input voltage	--	--	0.4	V
Enable Input Current	I_{EN}	EN = 2V	--	1.2	--	µA
Enable Turn-On Delay Time	$t_{DLY\_EN\_ON}$	Time for EN on to start switching, SS pin = floating.	--	120	--	µs
Output Voltage						
Feedback Threshold Voltage	V_{FB}	T_J = 25°C	0.594	0.6	0.606	V
		T_J = –40°C to 125°C	0.591	0.6	0.609	
Feedback Current	I_{FB}	V_{FB} = 0.63V	--	50	100	nA
Internal MOSFET						
High-Side On-Resistance	R_{DSON_H}	V_{IN} = 5V	--	65	--	mΩ
Low-Side On-Resistance	R_{DSON_L}	V_{IN} = 5V	--	35	--	
Current Limit						
High-Side Switch Peak Current Limit	I_{LIM_H}		4	5	6	A
Low-Side Switch Valley Current Limit	I_{LIM_L}		--	3	--	
Low-Side Switch Negative Current Limit	I_{LIM_N}	Current flow from SW to GND	--	1.2	--	A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching						
Switching Frequency	f_{SW}	V_{IN} = 3.3V, V_{OUT} = 1.2V, FCCM	2	2.4	2.67	MHz
Minimum Off-Time	t_{OFF_MIN}	V_{IN} = 5V	--	80	--	ns
Maximum Duty Cycle	D_{MAX}		--	--	100	%
Switch Pin Leakage Current	I_{SW_LK}	EN = 0V, V_{IN} = 6V, V_{SW} = 0V or 6V, T_J = –40°C to 125°C	--	--	30	μA
Protection						
Input Overvoltage Protection Threshold	V_{IN_OVP}	After V_{OUT_OVP} enabled	--	6.1	--	V
Input Overvoltage Protection Hysteresis	$V_{IN\_OVP\_HYS}$		--	160	--	mV
Output Overvoltage Protection Threshold	V_{OUT_OVP}		110	115	120	%
Output Overvoltage Protection Hysteresis	$V_{OUT\_OVP\_HYS}$	Overvoltage protection release	--	10	--	%
Output Undervoltage Protection Threshold	V_{OUT_UVP}		--	40	--	%
Output Undervoltage Protection Hysteresis	$V_{OUT\_UVP\_HYS}$	Undervoltage protection release	--	10	--	%
Over-Temperature Protection						
Over-Temperature Protection Threshold	T_{OTP}		--	170	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	
Power-Good						
Power-Good High Threshold	V_{PG_H}	V_{OUT} rising, PG from low to high	87	90	93	%V_{FB}
Power-Good Low Threshold	V_{PG_L}	V_{OUT} falling, PG from high to low	82	85	88	
Power-Good Delay Time	t_{DLY_PG}		--	80	--	μs
Power-Good High-Level Voltage	V_{PG_HL}	V_{IN} = 5V, V_{FB} = 0.6V	4.6	--	--	V
Power-Good Low-Level Voltage	V_{PG_LL}	Sink current = 1mA	0	--	250	mV
Power-Good Leakage Current	I_{PG_LK}	Pull-up voltage is 5V	--	--	100	nA
Self-Bias PG		When VIN = 0 & EN =0, PG pull-up voltage = 3.6V, pull-up resistor = 300kΩ (Note 7)	--	--	0.7	V
Output Discharge Resistor						
Output Discharge Switch On-Resistance	R_{DISCHG}	V_{EN} = 0V, V_{OUT} = 1.2V	--	5	10	Ω

Note 7. Guaranteed by design.

15 Typical Application Circuit

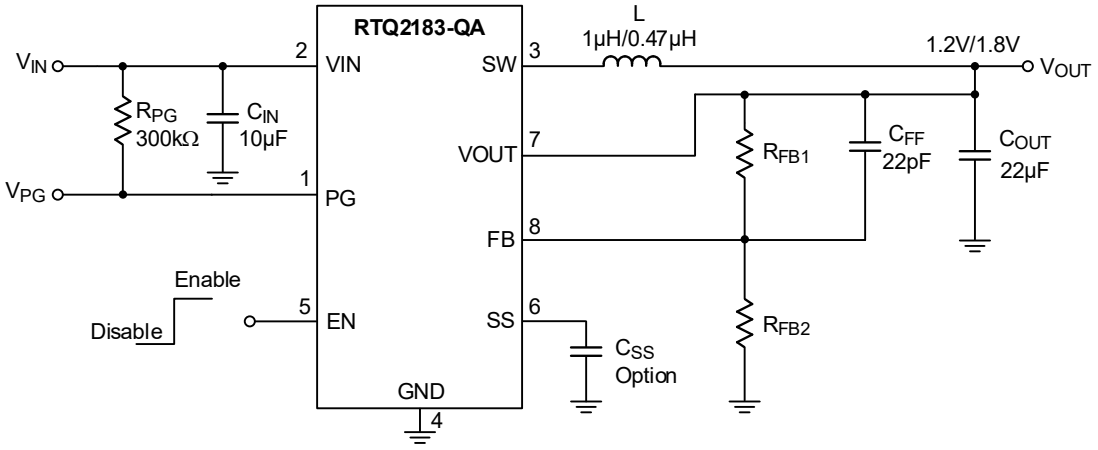
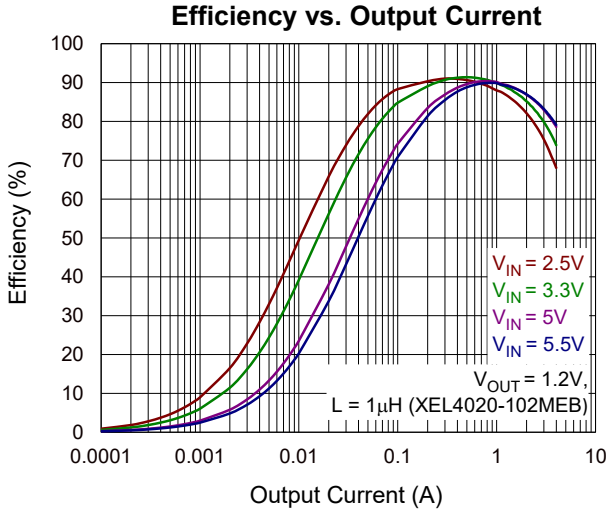


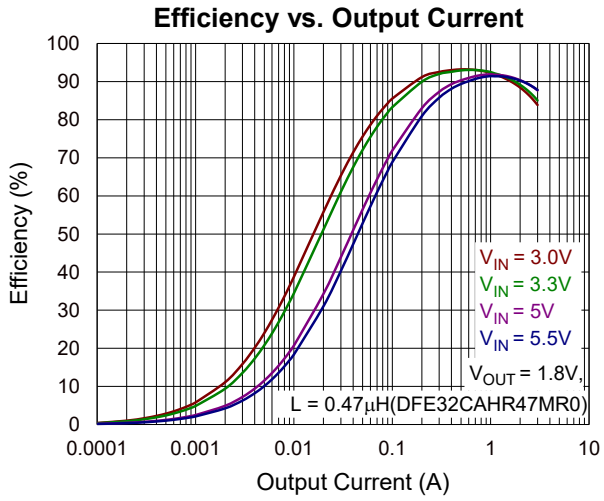
Table 1. Recommended External Components for 3A Maximum Load Current (Note 8)

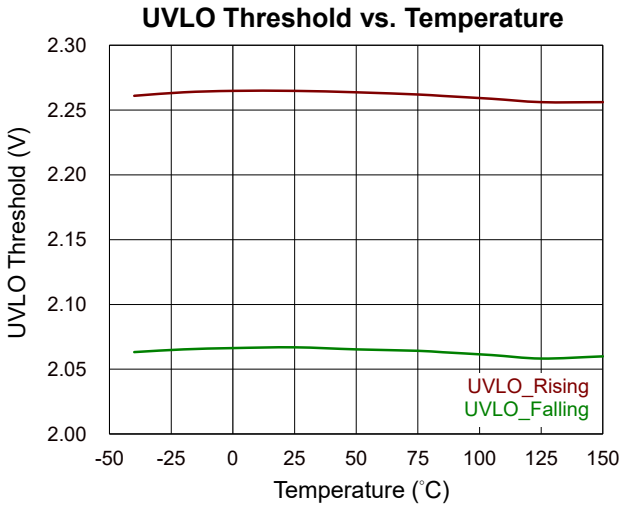
Component	Part Number	Description	Manufacturer
C_{IN}	GCM21BC71C106KE36	10μF/16V/X7S/0805	MURATA
C_{OUT}	GCM21BD70J226ME36	22μF/6.3V/X7T/0805	MURATA
L (For 1.8V)	DFE32CAHR47MR0	470nH/8.7A/14mΩ	MURATA
L (For 1.2V)	XEL4020-102MEC	1μH/9A/14.6mΩ	COILCRAFT
C_{FF}	GCM1555C1H220JA16	22pF/50V/C0G/0402	MURATA
R_{FB1} (For 1.8V)	MR04X1003FTL	100kΩ/1%/0402	WALSIN
R_{FB2} (For 1.8V)	MR04X4992FTL	49.9kΩ/1%/0402	WALSIN
R_{FB1} (For 1.2V)	MR04X1003FTL	100kΩ/1%/0402	WALSIN
R_{FB2} (For 1.2V)	MR04X1003FTL	100kΩ/1%/0402	WALSIN
R_{PG}	MR04X3003FTL	300kΩ/1%/0402	WALSIN

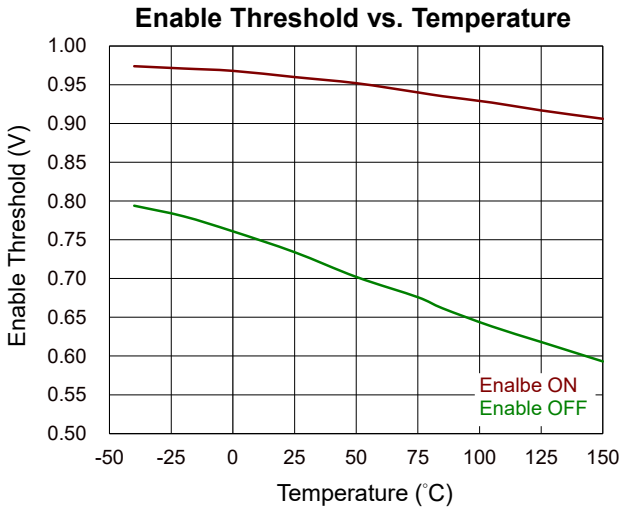
Note 8. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

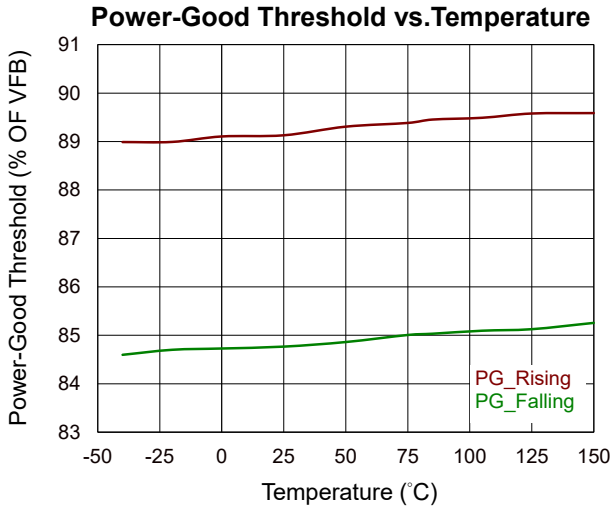
16 Typical Operating Characteristics

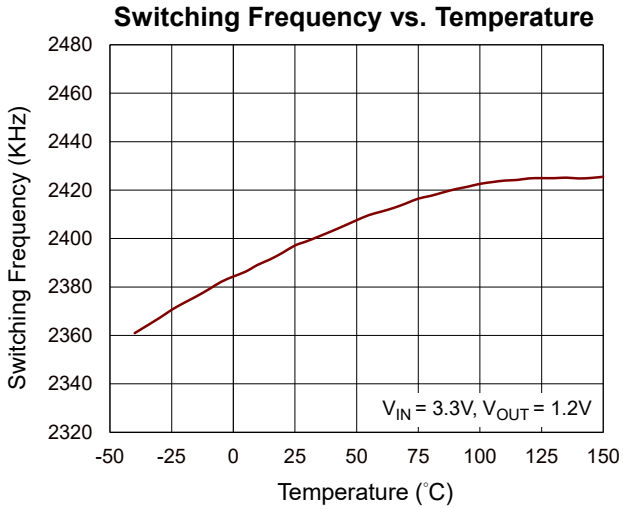




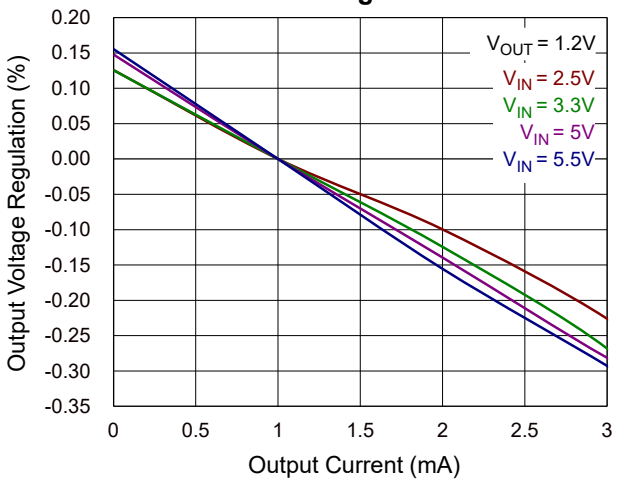




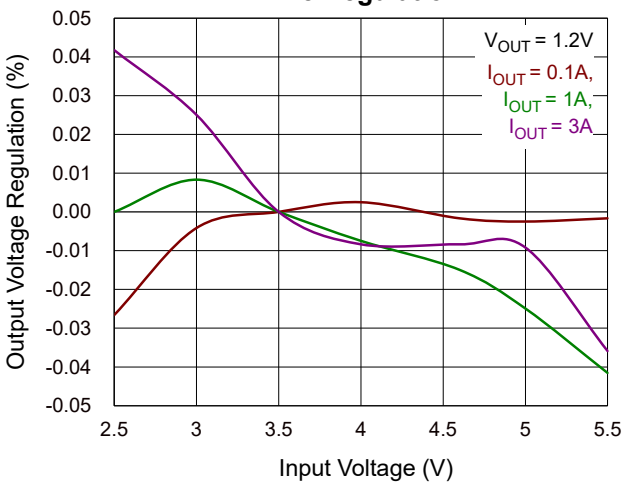




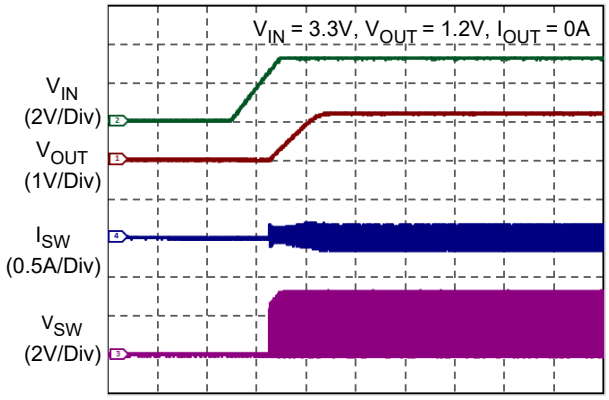
Load Regulation



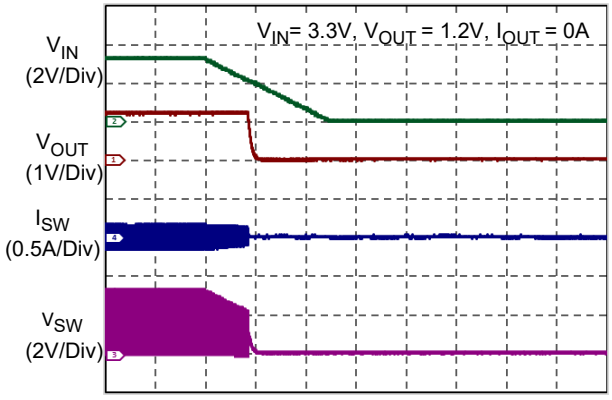
Line Regulation



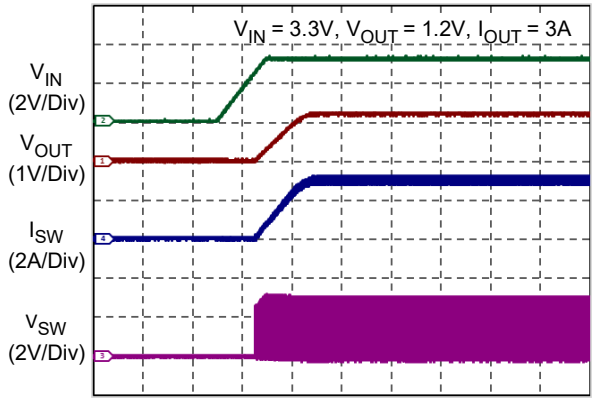
Power On from VIN



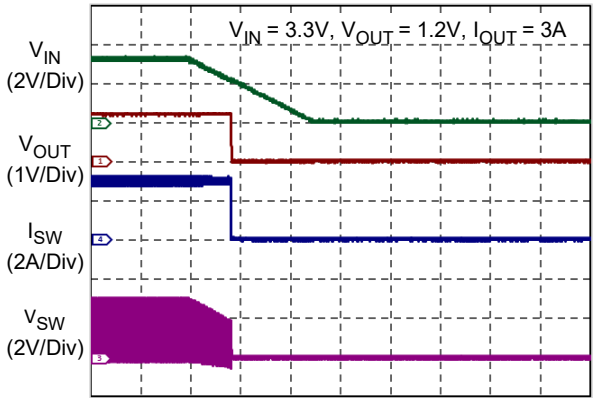
Power Off from VIN



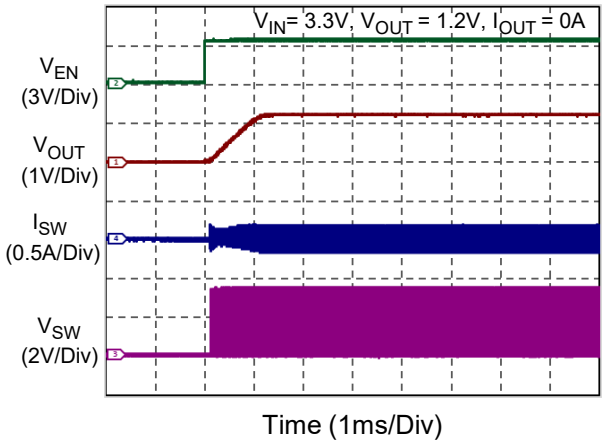
Power On from VIN



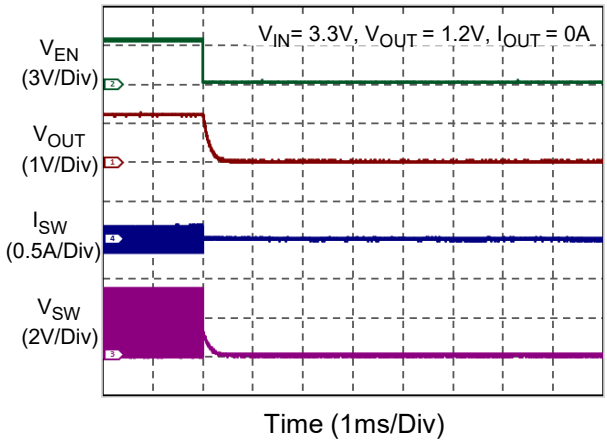
Power Off from VIN



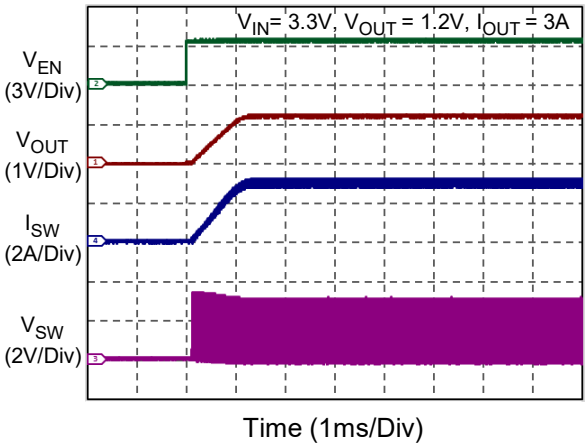
Power On from EN



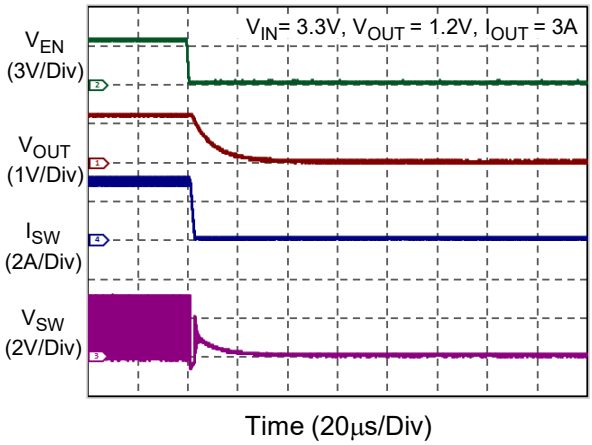
Power Off from EN



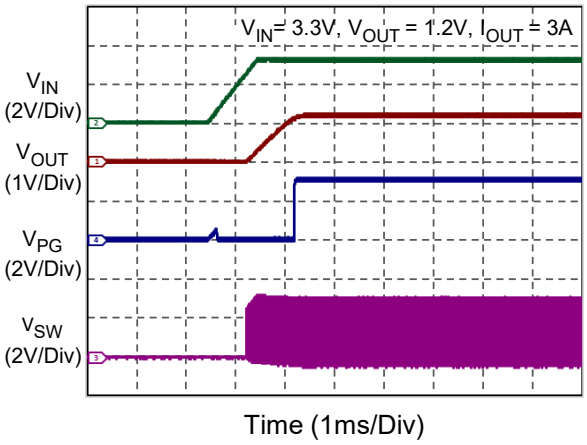
Power On from EN



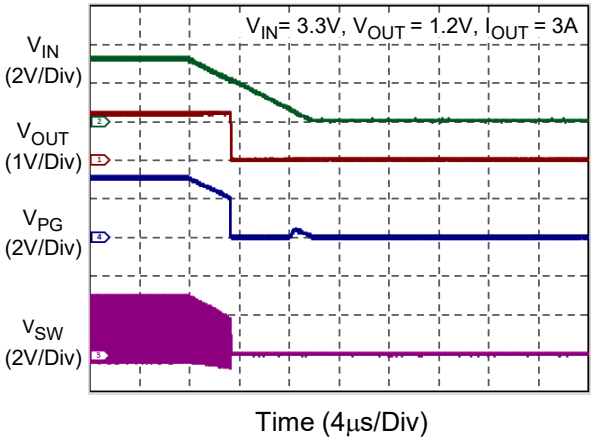
Power Off from EN



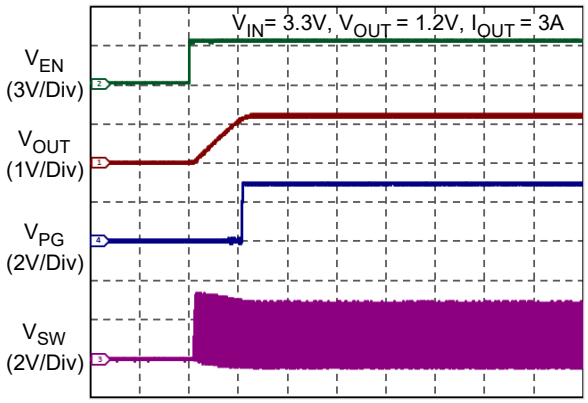
PG Output vs. VIN Rising



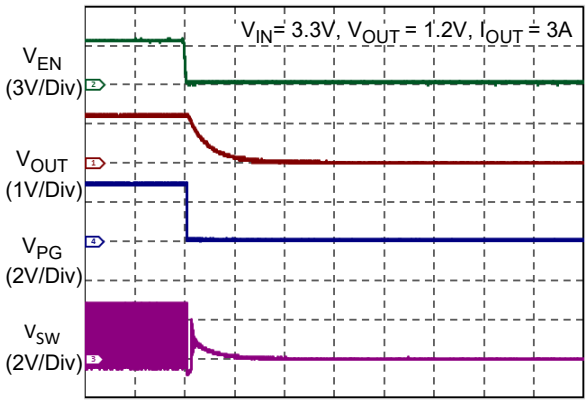
PG Output vs. VIN Falling



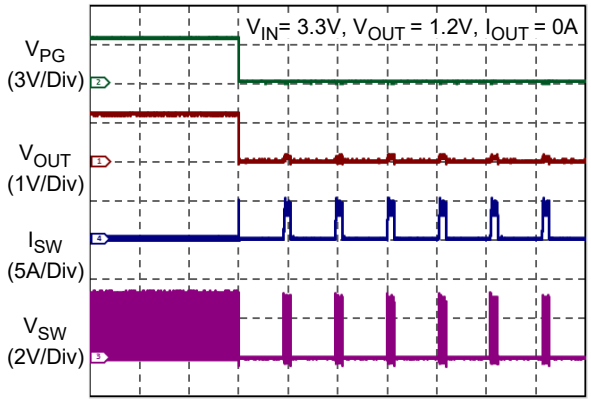
PG Output vs. EN Rising



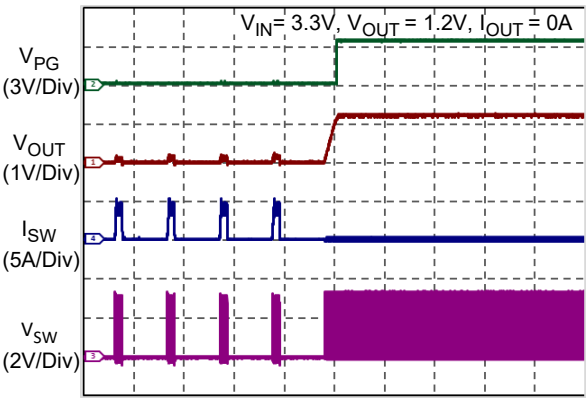
PG Output vs. EN Falling



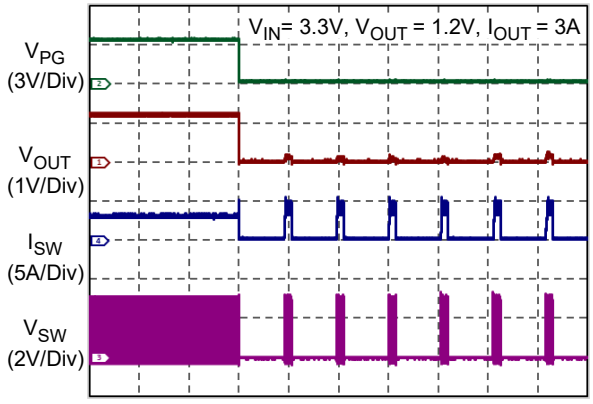
Hiccup Mode Entry



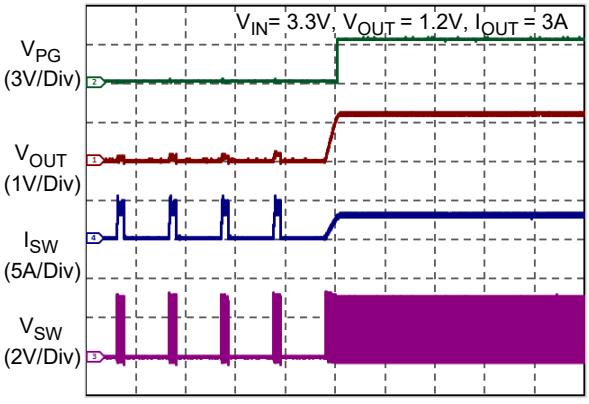
Hiccup Mode Recovery



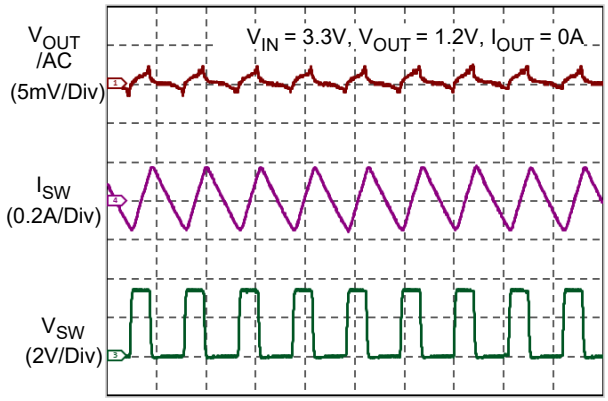
Hiccup Mode Entry



Hiccup Mode Recovery

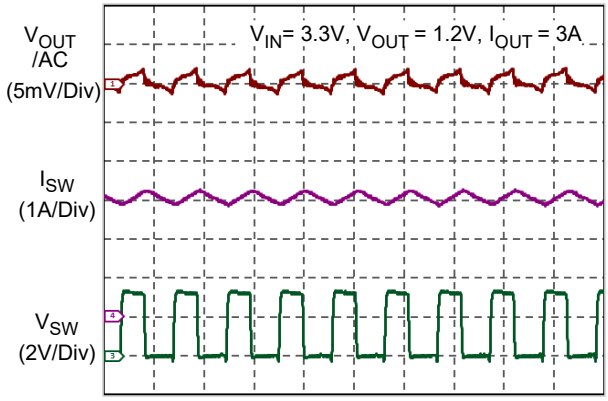


Output Ripple Voltage



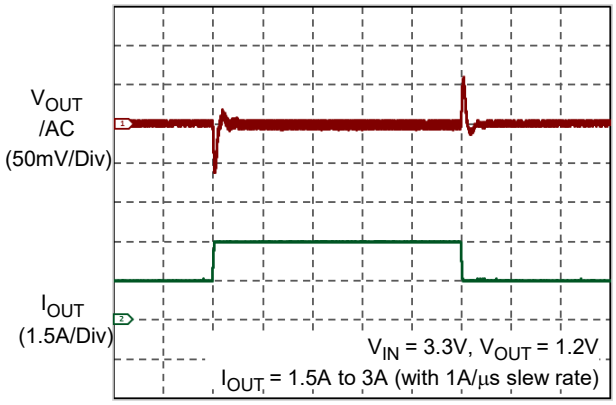
Time (400ns/Div)

Output Ripple Voltage



Time (400ns/Div)

Load Transient



Time (40ns/Div)

17 Operation

The RTQ2183-QA is a synchronous buck converter capable of delivering up to 3A output current from a 2.5V to 5.5V input supply.

17.1 Advanced Constant On-Time (ACOT®) Control and Switching Node Operation

The RTQ2183-QA utilizes ACOT® control to achieve ultrafast transient response, reduce external component count, and ensure stability with low ESR MLCC output capacitors. When the feedback voltage drops below the reference and the minimum off-time one-shot (80ns, typical) has expired with inductor current below the current-limit threshold, the internal on-time one-shot circuitry is triggered, turning on the high-side switch. The short minimum off-time enables ultrafast transient response and allows for smaller output capacitance.

The on-time duration is inversely proportional to the input voltage and directly proportional to the output voltage, maintaining a pseudo-fixed switching frequency across the input range. After the on-time period, the high-side switch turns off, and the low-side switch turns on until the next on-time trigger. In the steady state, the error amplifier compares the feedback voltage (V_{FB}) to the internal reference voltage. If the virtual inductor current ramp voltage is lower than the output of the error amplifier, a new fixed on-time is triggered.

17.2 Forced PWM Mode Operation

The RTQ2183-QA operates in forced PWM mode (FCCM) for applications requiring exclusion of switching harmonics from the signal band. While FCCM mode reduces light load efficiency, it provides low output voltage ripple, precise output voltage regulation, fast transient response, and stable switching frequency.

17.3 Enable Control

The RTQ2183-QA features an EN pin for external enable control. If the EN pin voltage (V_{EN}) is below the falling threshold (V_{EN_F}), the converter disables its output, regardless of V_{IN} voltage being above the input undervoltage-lockout rising threshold (V_{UVLO_R}). In shutdown mode, the supply current is reduced to I_{SHDN} (μA). If the EN voltage exceeds the rising threshold (V_{EN_R}) and the VIN voltage is above the UVLO rising threshold (V_{UVLO_R}), the device is enabled and the soft-start sequence is initiated.

17.4 Soft-Start (SS)

The RTQ2183-QA features an internal soft-start mechanism controlled by an external capacitor. Upon power-up, the external capacitor is charged by an internal current source, generating a soft-start ramp voltage as the reference for the PWM controller. The output voltage ramps smoothly to its target regulation voltage once this ramp voltage exceeds feedback voltage (V_{FB}), ensuring smooth start-up from a pre-biased output. The soft-start time (t_{SS}) is determined by the external soft-start capacitor (C_{SS}) and the internal charge current (I_{SS} ≈ 0.75μA):

$$tss(ms) = \frac{Css(nF)\times 0.6}{Iss(uA)}$$

The minimum soft-start time is approximately 1ms, even if no external C_{SS} is connected or the calculated t_{SS} is less than 1ms.

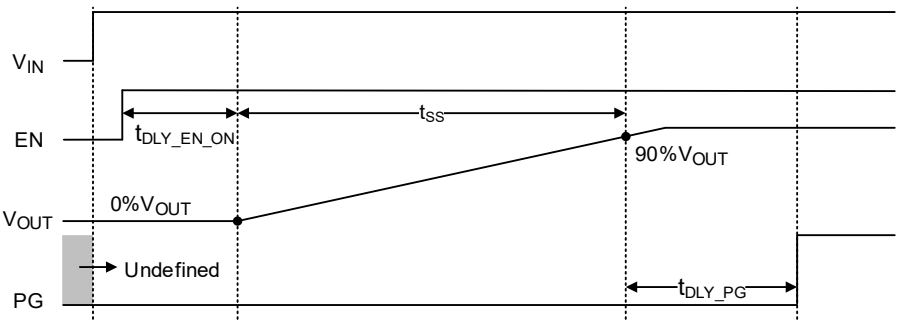


Figure 1. Start-Up Sequence

17.5 Maximum Duty Cycle Operation

The RTQ2183-QA is designed to operate in dropout mode when the duty cycle approaches 100%. If the required off-time becomes less than the minimum off-time, the RTQ2183-QA activates the skip off-time function, allowing the high-side MOSFET to remain continuously on. This enables the converter to achieve a duty cycle close to 100%, so the maximum output voltage is nearly equal to the input supply voltage. The actual dropout voltage depends on several factors, including the input voltage, output voltage, switching frequency, load current, and overall efficiency.

17.6 Power-Good Indication (PG)

The RTQ2183-QA features an open-drain power-good output (PG) that indicates the status of the output voltage. The PG pin should be connected to VIN or an external voltage source (not exceeding 5.5V) through a pull-up a resistor.

The power-good function is enabled after the soft-start process and is monitored by a comparator connected to the feedback signal (V_{FB}). When V_{FB} rises above the power-good high threshold (V_{PG_H}, typically 90% of the reference voltage), the PG pin enters a high-impedance state and the V_{PG} remains high after a short delay. If V_{FB} falls below the power-good low threshold (V_{PG_L}, typically 85% of the reference voltage), the PG pin is pulled low. Figure 2 illustrates the power-good indication profile.

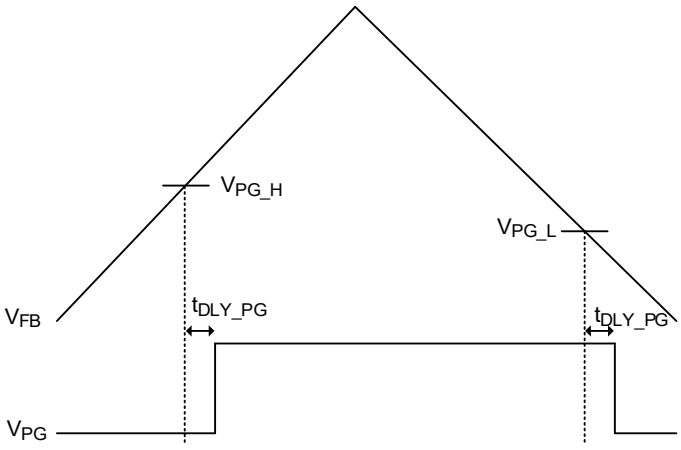


Figure 2. The Logic of Power-Good Function

17.7 Input Voltage Protection

The RTQ2183-QA is equipped with both input undervoltage-lockout protection (UVLO) and input overvoltage protection overvoltage-lockout protection (OVLO) (V_{IN_OVP}) to ensure proper operation. The device continuously monitors V_{IN} and initiates soft-start to the regulated output voltage when the V_{IN} voltage rises above the UVLO

high threshold (typically 2.3V). If V_{IN} drops below the UVLO low threshold (typically 2.1V), the device shuts down immediately.

Additionally, during output OVP (and only then), if the voltage on the VIN pin exceeds the OVLO threshold (typically 6.1V), the device will immediately shut down to prevent potential damage.

17.8 Overcurrent Protection (OCP)

The RTQ2183-QA features cycle-by-cycle current-limit protection on both the high-side and low-side MOSFETs to prevent catastrophic damage during output short circuits, overcurrent conditions, or inductor saturation.

Overcurrent protection is implemented using an internal current comparator that monitors the current in the high-side MOSFET during each switching cycle. The switch current is compared to the high-side peak current limit (I_{LIM_H}) and the low-side valley current limit (I_{LIM_L}). If an overcurrent condition persists, the converter will shut down after a certain number of hiccup cycles.

Negative overcurrent protection is also provided in forced PWM (FPWM) mode by measuring the inductor current through the low-side switch during its on-time. If the current exceeds the low-side negative current limit (I_{LIM_N}), the low-side switch is turned off immediately.

17.9 Output Active Discharge

When the RTQ2183-QA is disabled due to the EN pin being inactive, an undervoltage-lockout (UVLO), or an over-temperature protection (OTP) event, the device actively discharges the output capacitors through an internal 5Ω resistor connected to ground via the SW pins. This built-in discharge function prevents reverse current flow from the output to the input capacitors in the event of an input voltage drop. No external active discharge circuit is required. This discharge function ceases once the fault condition is cleared.

17.10 Output Undervoltage Protection (UVP)

The RTQ2183-QA features output undervoltage protection (UVP) with hiccup mode to safeguard against overloads or short circuits. The IC consistently monitors the feedback voltage (V_{FB}). If V_{FB} drops below the UVP threshold, typically 40% of the reference voltage, the UV comparator is triggered. The IC responds by disabling the low-side and enabling the high-side MOSFET, causing the inductor current to ramp up to the peak current limit (POC) and then down to the valley current limit (VOC). If this condition is detected 7 consecutive cycles, the device enters hiccup mode, shutting down for a predetermined off-time (t_{HICCUP_OFF}), typically 5 times of (2/3 x t_{SS} + 76μs), and then attempts recovery for a predetermined on-time (t_{HICCUP_ON}), typically 1 time (2/3 x t_{SS} + 76μs). If the fault is resolved before the soft-start completes, normal operation resumes. Otherwise, the device continues cycling through hiccup mode until the fault is cleared. This mechanism reduces input current and power dissipation, ensuring safe operation and smooth recovery.

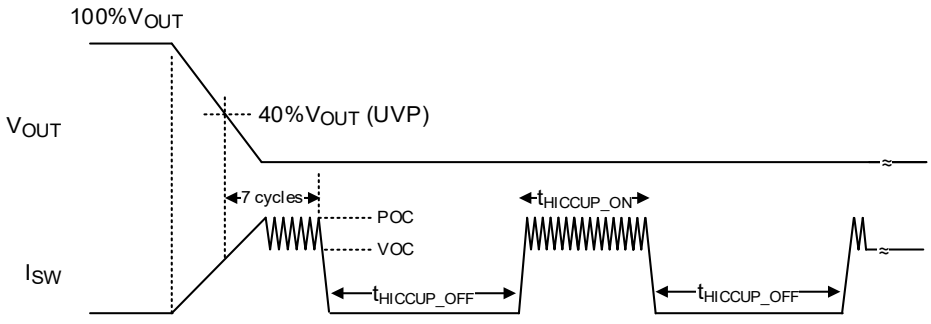


Figure 3. Hiccup Mode Behavior

17.11 Output Overvoltage Protection (OVP)

The RTQ2183-QA includes output overvoltage protection (OVP) to limit output voltage overshoot. If the V_{FB} exceeds 115% of the reference voltage, the PG pin remains high. If the overvoltage condition persists, the low-side MOSFET remains on until the low-side MOSFET valley current reaches the negative current limit −1.2A (typical). If dynamic regulation cannot limit the increase in VOUT, and the input reaches the input OVP threshold (6.1V, typical), the RTQ2183-QA stops switching until the input voltage drops below 6V (typical). The RTQ2183-QA then resumes operation.

17.12 Over-Temperature Protection (OTP)

The RTQ2183-QA features over-temperature protection to prevent damage from excessive power dissipation. When the junction temperature exceeds the over-temperature threshold (T_{OTP} = 170ºC), The converter shuts down switching operation. Normal operation resumes with a complete soft-start sequence once the junction temperature drops below the threshold by the hysteresis value (T_{OTP_HYS} = 20ºC).

Note that the over-temperature protection is designed as a secondary fail-safe for transient overload conditions. It is not intended for continuous operation outside the specified absolute maximum operating junction temperature range. Prolonged operation above the maximum rated temperature may impair device reliability or cause permanent damage.

18 Application Information

(Note 9)

The basic application circuit for the RTQ2183-QA is shown in Typical Application Circuit. The selection of external components is determined by the maximum load current. The process begins with selecting the appropriate inductor value and the operating frequency, followed by C_{IN} and C_{OUT}.

18.1 Inductor Selection

Inductor selection involves trade-offs among size, cost, efficiency, and transient response. Three key parameters should be considered: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A common design guideline is to select an inductor that results in a peak-to-peak ripple current of approximately 30% of the IC's rated current, balancing size and power loss. However, the optimal value may vary depending on application constraints. The inductor value is determined by the switching frequency, input voltage, output voltage, and the desired inductor ripple current, using the following equation:

$$L(\mu H) = \frac{V_{OUT}(V) \times [V_{IN}(V) - V_{OUT}(V)]}{V_{IN}(V) \times f_{SW}(MHz) \times \Delta I_L(A)}$$

To maximize efficiency, choose a low-loss inductor with the lowest possible DC resistance that fits within the available space. The inductor's saturation current rating should exceed the device's peak current limit. The core must be large enough to avoid saturation at the peak inductor current (I_{L_PEAK}):

$$\Delta L(A) = \frac{V_{OUT}(V) \times [V_{IN}(V) - V_{OUT}(V)]}{V_{IN}(V) \times f_{SW}(MHz) \times L(\mu H)}$$

$$I_{L\_PEAK}(A) = I_{OUT\_MAX}(A) + \frac{1}{2} \Delta I_L(A)$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power-up, faults, or transient load conditions, the inductor current may exceed the calculated peak inductor current value. For robust design, select an inductor with a saturation current rating equal to or greater than the device's switch current limit.

18.2 Input Capacitor Selection

The Input capacitance, C_{IN}, filters the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to minimize input voltage variation. The waveform of C_{IN} ripple voltage and current is shown in Figure 4. The peak-to-peak voltage ripple on the input capacitor can be estimated using the following equation:

$$\Delta V_{CIN\_PP}(V) = D \times I_{OUT}(A) \times \frac{1-D}{C_{IN}(\mu F) \times f_{SW}(MHz)} + 2 \times [I_{OUT}(A) \times ESR(\Omega)]$$

$D = \frac{V_{OUT}(V)}{V_{IN}(V) \times \eta(\%)}$, where η: Estimated efficiency at maximum load.

For ceramic capacitors, the ESR-induced ripple is negligible due to their very low ESR. The minimum input capacitance can be estimated using the following equation:

$$C_{IN\_MIN}(\mu F) = I_{OUT\_MAX}(A) \times \frac{D \times (1-D)}{\Delta V_{IN\_PP\_MAX}(V) \times f_{SW}(MHz)}$$

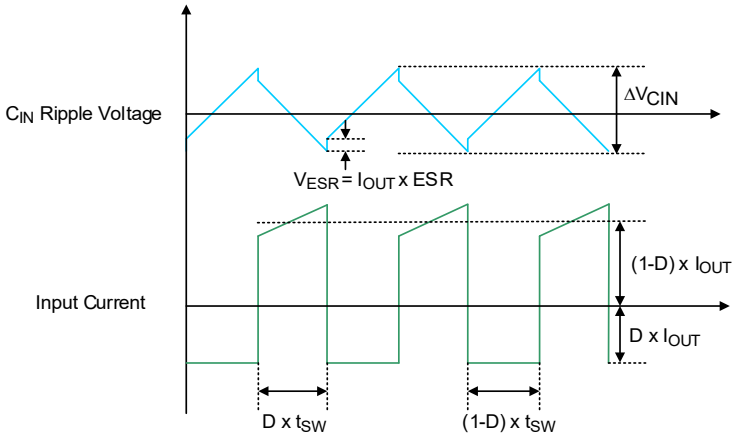


Figure 4. C_{IN} Ripple Voltage and Input Current

In addition, the input capacitor must have a very low ESR and be rated to handle the worst-case RMS input current, calculated as:

$$I_{RMS}(A) \cong I_{OUT\_MAX}(A) \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

For design purposes, it is common to use the worse-case I_{RMS} value, approximately $I_{RMS} \cong I_{OUT} / 2$ at $V_{IN} = 2\ V_{OUT}$. Note that capacitor manufacturers often specify ripple current ratings based on a lifespan of only 2000 hours. It is advisable to further de-rate the capacitor, or select a capacitor rated for a higher temperature than required.

Multiple capacitors may be paralleled to meet size, height and thermal requirements. For low input voltage applications, sufficient bulk input capacitance is necessary to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications because of their small size, robustness, and very low ESR. However, care must be taken when using ceramic capacitors at the input.

The input capacitor should be placed as close as possible to the VIN pin, with a low-inductance connection to the PGND of the IC. It is recommended to use a 10μF, X7R capacitors between the VIN pin to the PGND pin.

18.3 Output Capacitor Selection

The selection of C_{OUT} is determined by the required ESR to minimize output voltage ripple. Additionally, the amount of bulk capacitance is critical to ensure loop stability. Loop stability can be verified by analyzing the load transient response.

The output voltage ripple, ΔV_{OUT}, can be estimated using the following equation:

$$\Delta V_{OUT\_PP}(V) = \Delta I_L(A) \times \left(ESR(\Omega) + \frac{1}{8 \times C_{OUT}(\mu F) \times f_{SW}(MHz)} \right)$$

where f_{SW} is the switching frequency and ΔIL is the inductor ripple current. The output voltage ripple will be the highest at the maximum input voltage, as the ΔIL increases with the input voltage. Multiple capacitors may be placed in parallel to meet the ESR and RMS current handling requirements. Ceramic capacitors are recommended due to their outstanding low ESR characteristics.

18.4 Output Ripple

The output voltage ripple at the switching frequency is determined by the inductor current ripple passing through the output capacitor's impedance. To derive the output voltage ripple, the output capacitor with capacitance, C_{OUT}, and its equivalent series resistance, ESR, must be taken into consideration. The total peak-to-peak output voltage ripple (V_{RIPPLE}) consists of two components: the ESR-induced ripple ($V_{RIPPLE(ESR)}$) and the capacitive ripple ($V_{RIPPLE(C)}$), and can be expressed as follows:

$$V_{RIPPLE}(V) = V_{RIPPLE(ESR)}(V) + V_{RIPPLE(C)}(V)$$

$$V_{RIPPLE(ESR)}(V) = \Delta I_L(A) \times R_{ESR}(\Omega)$$

$$V_{RIPPLE(C)}(V) = \frac{\Delta I_L(A)}{8 \times C_{OUT}(\mu F) \times f_{SW}(MHz)}$$

If ceramic capacitors are used for output capacitors, both the components should be considered due to the extremely low ESR and relatively small capacitance.

18.5 Feedback Voltage Setting

Set the output voltage using a resistive divider from the output to ground, with the midpoint connected to FB, as shown in Figure 5. The output voltage is set according to the following equation:

$V_{OUT} = 0.6V \times (1 + R_{FB1} / R_{FB2})$

For optimal output voltage accuracy, use resistors with 1% or better tolerance And place the divider as close as possible to the FB pin.

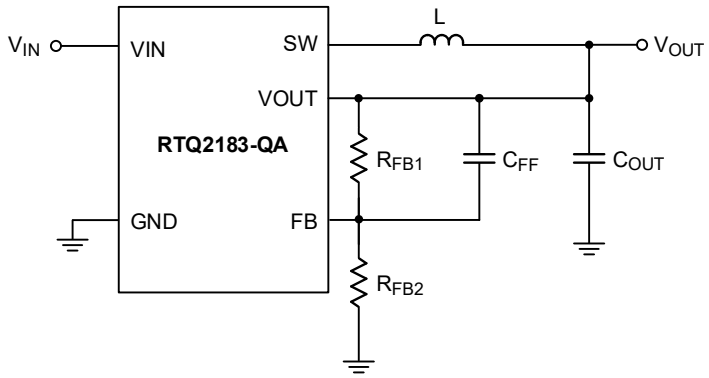


Figure 5. Output Voltage Setting

18.6 EN Pin for Start-Up and Shutdown Operations

For automatic start-up, the EN pin can be connected to the input supply V_{IN} directly. The large built-in hysteresis band makes the EN pin suitable for implementing simple delay and timing circuits. To introduce a start-up delay, connect the EN pin to V_{IN} through a resistor R_{EN} and a capacitor C_{EN}, as shown in Figure 6. The delay time can be calculated based on the EN's internal threshold voltage, which determines when switching operation begins.

For logic-controlled enable, an external MOSFET can be used, as shown in Figure 7. In this case, a pull-up resistor, R_{EN}, connects VIN to the EN pin, while the MOSFET (Q1) pulls the EN pin low under logic control. To prevent the device from being enabled when V_{IN} is below the desired voltage (e.g., less than the V_{OUT} target), a resistive

divider (R_{EN1} and R_{EN2}) can be used to externally set a custom input undervoltage-lockout threshold, as shown in Figure 8.

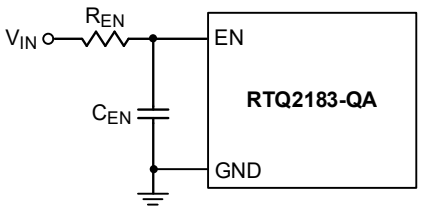


Figure 6. Enable Timing Control

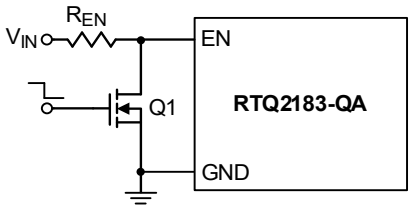


Figure 7. Logic Control for the EN Pin

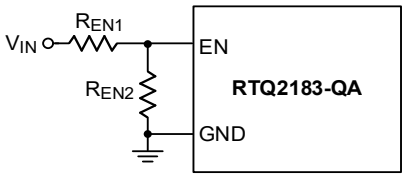


Figure 8. Resistive Divider for Undervoltage-Lockout Threshold Setting

18.7 Power-Good (PG)

The PG pin is an open-drain power-good indication output and should be connected to an external voltage source through a pull-up resistor.

The external voltage source can be either an independent supply below 5.5V or the input of the RTQ2183-QA, provided the input voltage is regulated below 5.5V. For reliable operation, it is recommended to keep the PG pull-up voltage ≤ VIN. A 300kΩ pull-up resistor is recommended between the external voltage source and the PG pin.

18.8 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature TJ(MAX), listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation is influenced by the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WET-VDFN-8J2L 2x1.5 (FC) package, the thermal resistance, θ_{JA}, is 99°C/W on a

standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (150°C – 25°C) / (99°C/W) = 1.26W for a WET-VDFN-8J2L 2x1.5 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 9 allows the designer to estimate the effect of rising ambient temperature on the maximum power dissipation.

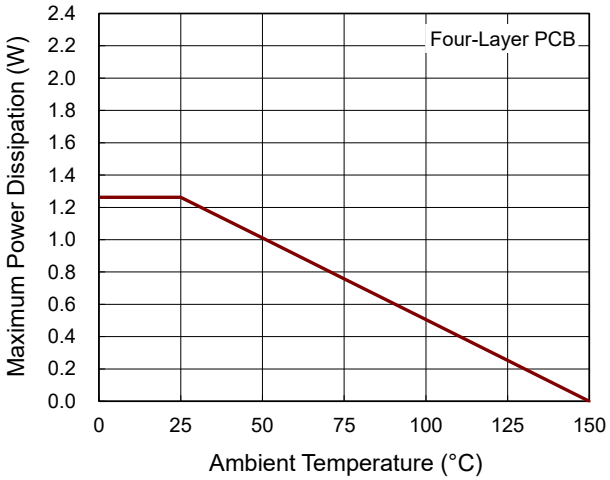


Figure 9. Derating Curve of Maximum Power Dissipation

18.9 Layout Considerations

For optimal performance of the RTQ2183-QA, the following layout guidelines must be strictly followed.

- The input capacitor must be placed as close as possible to the IC to minimize the power loop area. A typical 10μF decoupling capacitor is recommended to reduce high-frequency noise on VIN.
- The SW node experiences high-frequency voltage swings Keep the area around the SW node as small as possible, and ensure analog components are placed away from the SW node to prevent stray capacitive noise pickup.
- Ensure all power trace connections as wide as possible to improve thermal dissipation.
- Keep the feedback line as short as possible and route it away from the power inductor and other noisy areas.

An example PCB layout is shown in Figure 10.

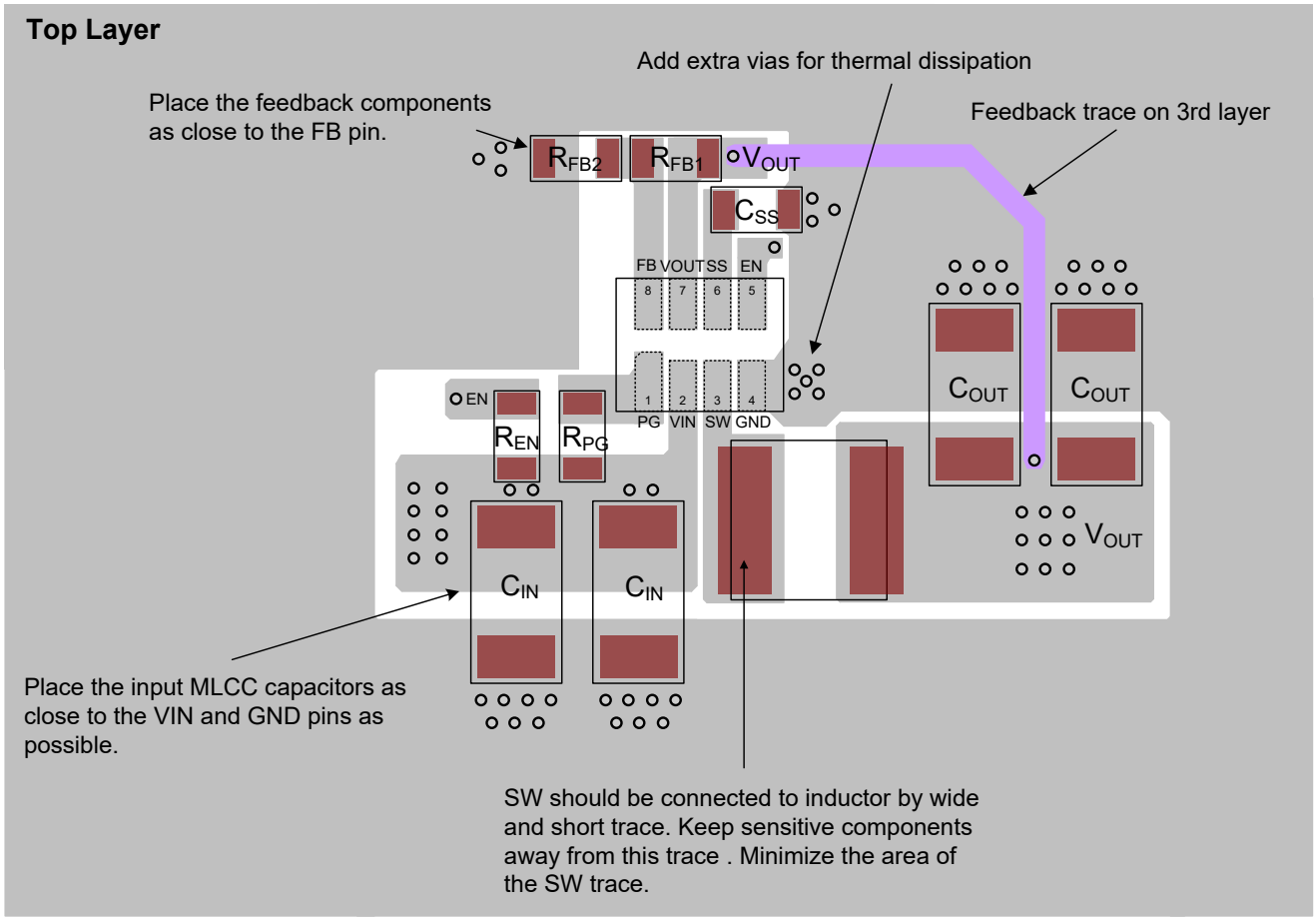
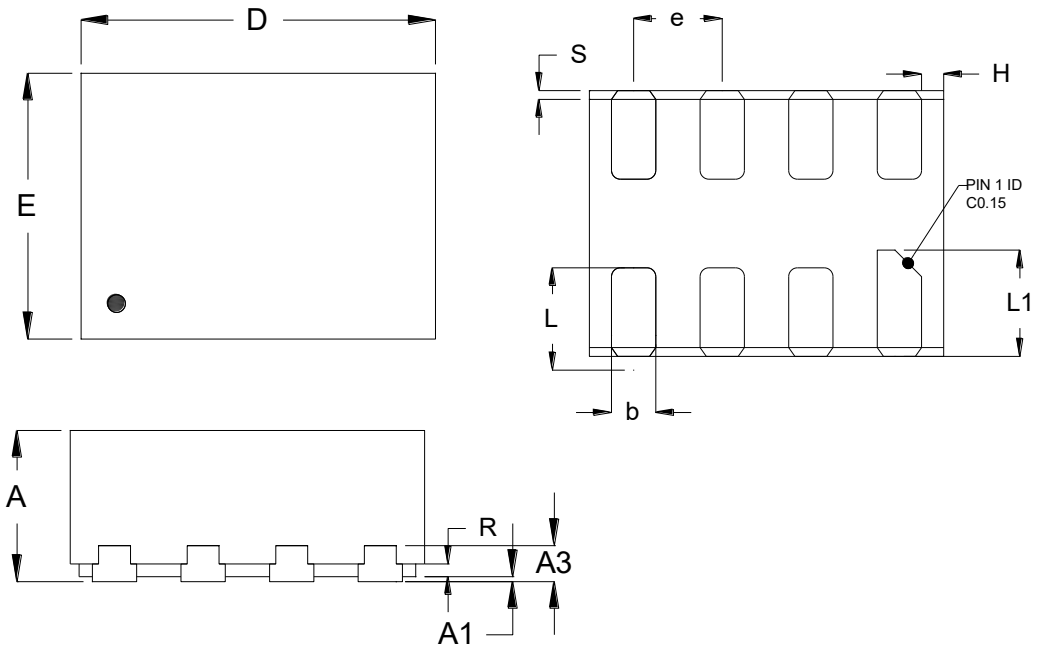


Figure 10. PCB Layout Guide

Note 9. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

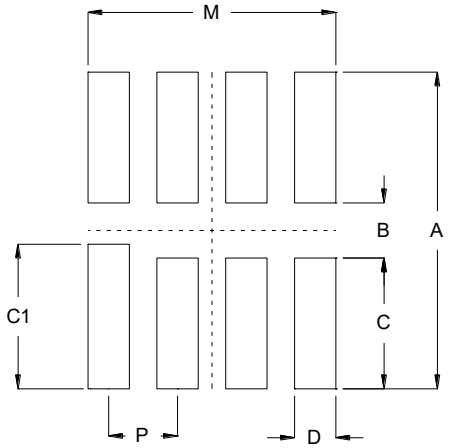
19 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
E	1.450	1.550	0.057	0.061
e	0.500		0.020	
L	0.450	0.550	0.018	0.022
L1	0.550	0.650	0.022	0.026
R	0.050	0.150	0.002	0.006
S	0.001	0.090	0.000	0.004
H	0.125		0.005	

WET V-Type 8J2L DFN 2x1.5 Package (FC)

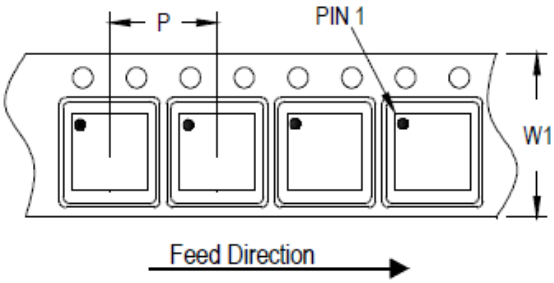
20 Footprint Information

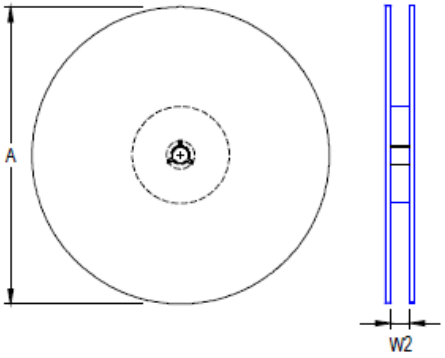


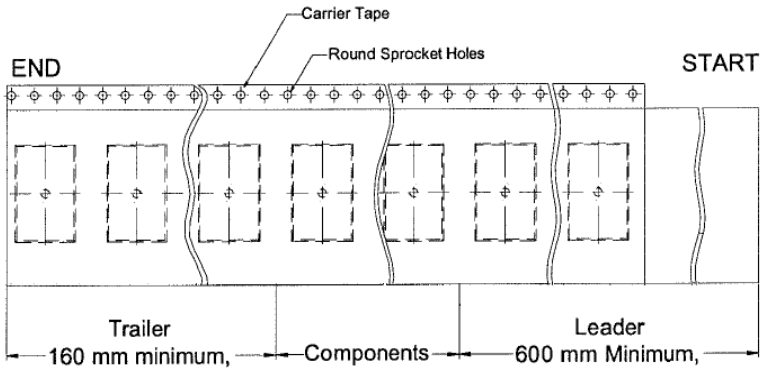
Package	Number of Pins	Footprint Dimension (mm)							Tolerance
		P	A	B	C	C1	D	M	
WET-VDFN2X1.5-8J2(FC)	8	0.50	2.30	0.40	0.95	1.05	0.30	1.80	±0.05

21 Packing Information

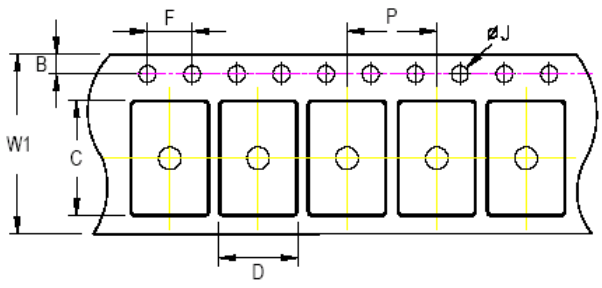
21.1 Tape and Reel Data

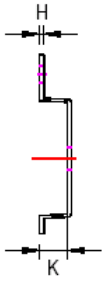






Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 2x1.5	8	4	180	7	2,500	160	600	8.4/9.9





C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 2x1.5	7”	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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22 Datasheet Revision History

Version	Date	Description
00	2025/11/12	First Edition